(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
06 August 2020 (06.08.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/159882 A1

(51) International Patent Classification:
C23C 16/455 (2006.01) *C23C 16/34* (2006.01)
C23C 16/56 (2006.01) *H01L 21/02* (2006.01)
C23C 16/30 (2006.01)

(21) International Application Number:
PCT/US2020/015241

(22) International Filing Date:
27 January 2020 (27.01.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/797,860 28 January 2019 (28.01.2019) US

(71) Applicant: **LAM RESEARCH CORPORATION** [US/US]; 4650 Cushing Parkway, Fremont, California 94538 (US).

(72) Inventors: **COLLINS, Joshua**; 4650 Cushing Parkway, Fremont, California 94538 (US). **KENNEDY, Griffin John**; 4650 Cushing Parkway, Fremont, California 94538 (US). **BAMNOLKER, Hanna**; 4650 Cushing Parkway, Fremont, California 94538 (US). **VAN CLEEMPUT, Patrick**; 4650 Cushing Parkway, Fremont, California 94538 (US). **VARADARAJAN, Seshasayee**; 4650 Cushing Parkway, Fremont, California 94538 (US).

(74) Agent: **BERGIN, Denise S.** et al.; WEAVER AUSTIN VILLENEUVE & SAMPSON LLP, P.O. Box 70250, Oakland, California 94612-0250 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

(54) Title: DEPOSITION OF METAL FILMS

(57) Abstract: Provided herein are low resistance metallization stack structures for logic and memory applications and related methods of fabrication. In some embodiments, thin metal oxynitride or metal nitride nucleation layers are deposited followed by deposition of a pure metal conductor. The nucleation layer is amorphous, which templates large pure metal film grain growth and reduced resistivity. Further, certain embodiments of the methods described below convert most or all of the metal oxynitride nucleation layer to a pure metal layer, further lowering the resistivity.

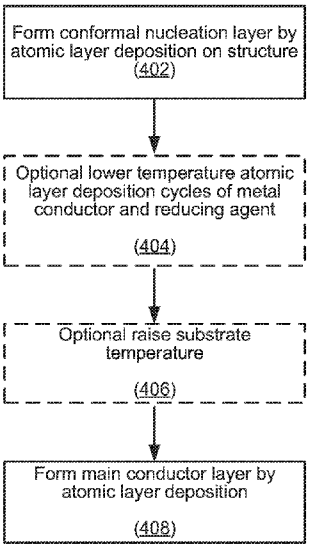

FIG. 4

WO 2020/159882 A1

[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

DEPOSITION OF METAL FILMS

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

BACKGROUND

[0002] Tungsten (W) film deposition using chemical vapor deposition (CVD) techniques is an integral part of semiconductor fabrication processes. For example, tungsten films may be used as low resistivity electrical connections in the form of horizontal interconnects, vias between adjacent metal layers, and contacts between a first metal layer and the devices on a silicon substrate. Tungsten films may also be used in various memory applications, including in formation of buried wordline (bWL) architectures for dynamic random access memory (DRAM), word lines for 3D NAND, and logic applications. However, the continued decrease in feature size and film thickness brings various challenges including high resistivity for thinner films. Other metals such as molybdenum (Mo) are being evaluated as low resistivity replacements for W.

[0003] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

SUMMARY

[0004] One aspect of the disclosure relates to method of depositing metal. It includes depositing a first layer from a metal oxychloride precursor and ammonia using a first atomic layer deposition (ALD) process. It also includes depositing an elemental metal layer on the first layer from a metal oxychloride precursor and hydrogen using a second ALD process.

[0005] Implementations may include one or more of the following features. The method where the first layer is a metal oxynitride or metal nitride layer. The method where the first layer is converted to an elemental metal layer during or prior to the second ALD process. The method where the converted elemental metal later contains less than 1 (atomic) % impurities. The method where the first layer is an amorphous layer. The method where the elemental layer is crystalline. The method where the first and second ALD processes are performed in the same chamber and without exposure to air. The method where the first layer is a template for metal grain growth in the second layer. The method where the elemental layer contains less than 1 (atomic) % impurities. The method where the elemental metal layer is elemental tungsten. The method where the elemental metal layer is elemental molybdenum. The method where the first layer is one of molybdenum oxynitride and molybdenum nitride. The method where the first ALD process is performed at a temperature less than 400°C.

The method where the second ALD process is performed at a temperature greater than 400°C. The method where deposition of the first layer and deposition of the elemental layer are performed in the same chamber. The method where deposition of the first layer and deposition of the elemental layer are performed in different stations of the same chamber. The method where deposition of the first layer is performed in a first chamber and deposition of the elemental layer is performed in a second chamber. The method further including exposing the first layer to a prior to deposition of the elemental layer.

[0006] Another aspect of the disclosure includes relates to an apparatus including: first and second process chambers each configured to house a substrate, a substrate support in each of the process chambers, gas inlets configured to direct gas into each of the process chambers, a heater configured to heat the substrate support in each process chamber, and a controller including program instructions for:. The apparatus also includes sequentially inletting a metal oxychloride precursor and ammonia into the first process chamber while a substrate is housed in the first process chamber. The apparatus also includes after (a), transfer the substrate to the second process chamber. The apparatus also includes after (b), sequentially inletting a metal oxychloride precursor and hydrogen into the second process chamber while the substrate is housed in the second process chamber.

[0007] Another aspect of the disclosure relates to an apparatus including: a process chamber having one or more stations, each configured to house a substrate; a substrate support in each of the one or more stations; gas inlets configured to direct gas into each of the one or more stations; a heater configured to heat the substrate support in each station; and a controller including program instructions for: sequentially inletting a metal oxychloride precursor and ammonia into one of the one or stations; and sequentially inletting a metal oxychloride precursor and hydrogen into one of the one or stations.

[0008] These and other aspects are described more fully below with reference to the drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0009] Figures 1A and 1B are schematic examples of material stacks that include a nucleation layer as a template for metal growth.

[0010] Figures 2, 3A, and 3B provide examples of structures in which the material stacks may be employed according to various embodiments.

[0011] Figure 4 is a process flow diagram illustrating operations in a method of depositing a conductive material according to various embodiments,

[0012] Figure 5 shows atomic layer deposition growth rate on a dielectric surface of a molybdenum-containing layer using ammonia reducing agent and a molybdenum oxychloride precursor.

[0013] Figure 6 shows molybdenum growth from hydrogen and a molybdenum oxychloride on a nucleation layer deposited on a dielectric surface as described compared to molybdenum growth from hydrogen and a molybdenum oxychloride directly on a dielectric surface.

[0014] Figure 7 is a plot showing resistivity of molybdenum films deposited as described herein compared to a molybdenum film deposited on titanium nitride.

[0015] Figure 8 is a block diagram of a processing system suitable for conducting deposition processes

in accordance with embodiments described herein.

DETAILED DESCRIPTION

[0016] In the following description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

[0017] Provided herein are low resistance metallization stack structures for logic and memory applications and related methods of fabrication. In some embodiments, thin metal oxynitride or metal nitride nucleation layers are deposited followed by deposition of a pure metal conductor. The nucleation layer is amorphous, which templates large pure metal film grain growth and reduced resistivity. Further, certain embodiments of the methods described below convert most or all of the metal oxynitride nucleation layer to a pure metal layer, further lowering the resistivity.

[0018] According to various embodiments, one or more advantages may be realized. In some embodiments, deposition of metals such as Mo directly on aluminum oxide and other dielectrics may be performed. In some embodiments, these depositions may be performed at temperatures less than 500°C or even lower than 400°C without significant nucleation delay. Deposition at low temperatures can result in better step coverage. In various embodiments, lower resistivity films may be obtained from large grain size of the films and/or because the films may be deposited directly on dielectrics without high resistivity films such as titanium nitride (TiN). Addition of a low-temperature metal-nitride nucleation layer can enable subsequent pure metal deposition at temperatures less than 600°C or even less than 500°C. This can make the metal (nitride) + pure-metal nucleation stack suitable for semiconductor applications that have thermal budgets of less than 600°C or 500°C for wafer processing. This enables deposition of metals without a high resistivity layer such as TiN and at temperatures inaccessible for pure films; for example, temperatures for pure Mo ALD can exceed 600°C when deposited directly on dielectrics.

[0019] Figures 1A and 1B are schematic examples of material stacks that include a nucleation layer as a template for metal growth. Figures 1A and 1B illustrate the order of materials in a particular stack and may be used with any appropriate architecture and application, as described further below with respect to Figures 2, 3A, and 3B. In the example of Figure 1A, a substrate 102 has a nucleation layer 108 deposited thereon. The substrate 102 may be a silicon or other semiconductor wafer, e.g., a 200-mm wafer, a 300-mm wafer, or a 450-mm wafer, including wafers having one or more layers of material, such as dielectric, conducting, or semi-conducting material deposited thereon. The methods may also be applied to form metallization stack structures on other substrates, such as glass, plastic, and the like.

[0020] In Figure 1A, a dielectric layer 104 is on the substrate 102. The dielectric layer 104 may be deposited directly on a semiconductor (e.g., Si) surface of the substrate 102, or there may be any number of intervening layers. Examples of dielectric layers include doped and undoped silicon oxide, silicon

nitride, and aluminum oxide layers, with specific examples including doped or undoped layers SiO_2 and Al_2O_3. Also, in Figure 1A, a diffusion barrier layer 106 is disposed between the nucleation layer 108 and the dielectric layer 104. Examples of diffusion barrier layers including titanium nitride (TiN), titanium/titanium nitride (Ti/TiN), tungsten nitride (WN), and tungsten carbon nitride (WCN). A metal layer 110 is deposited on the nucleation layer 108 and is the main conductor (also referred to as a bulk conductor or bulk layer) of the structure with the nucleation layer 108 providing a template for metal growth.

[0021] As described further below, the nucleation layer 108 is deposited as an amorphous film. By using an amorphous film, which has large grains, as a template for metal growth, metal having large grains and low resistivity can be formed. Examples of metal layers include tungsten (W) and molybdenum (Mo) layers.

[0022] Figure 1B shows another example of a material stack. In this example, the stack includes the substrate 102, dielectric layer 104, with the nucleation layer 108 deposited directly on the dielectric layer 104, without an intervening diffusion barrier layer. As in the example of Figure 1A, a metal layer 110 is deposited on the nucleation layer 108 and is the main conductor of the structure.

[0023] In the examples of Figures 1A and 1B, the nucleation layer 108 may be deposited a metal oxynitride layer, e.g., a tungsten oxynitride or molybdenum oxynitride layer. However, during subsequent processing, in certain embodiments, all or most of the nucleation layer 108 may be converted to a pure metal. Accordingly, according to various embodiments, the nucleation layer 108 may or may not be the same composition as the pure metal layer 110. The nucleation layer 108 may be characterized by its amorphous character, with the pure metal layer 110 characterized by its large grain size.

[0024] In some embodiments, the metal of the metal oxynitride layer is the same as that of the pure metal conductor, e.g., a molybdenum oxynitride layer may be deposited as a nucleation layer prior to deposition of a molybdenum layer or a tungsten oxynitride layer may be deposited as a nucleation layer prior to deposition of a tungsten layer. In other embodiments, the metal oxynitride layer may have a different metal than that of the pure conductor, e.g., a tungsten layer may be deposited on a molybdenum-containing nucleation layer or a molybdenum layer may be deposited on a tungsten-containing nucleation layer.

[0025] While Figures 1A and 1B show examples of metallization stacks, the methods and resulting stacks are not so limited. For example, in some embodiments, the nucleation layer may be deposited directly on a Si or other semiconductor substrate as a template for metal growth. Further, while tungsten (W) or molybdenum (Mo) growth on the nucleation layers is described above, the nucleation layers may be serve as a template for low resistivity growth of other metals cobalt (Co), ruthenium (Ru), nickel (Ni), and alloys including these metals such as MoW. Still further, the nucleation layer may be any appropriate metal oxynitride or metal nitride layer, including molybdenum oxynitride, molybdenum nitride, tungsten oxynitride, tungsten nitride, nickel nitride, etc.

[0026] The material stacks described above and further below may be implemented in a variety of structures. Figures 2, 3A, and 3B provide examples of structures in which the stacks may be employed.

Figure 2 depicts a schematic example of a DRAM architecture including a buried wordline (bWL) 210 in a silicon substrate 202. The bWL 210 is formed in a trench etched in the silicon substrate 202. Lining the trench is a conformal nucleation layer 208 and an insulating layer 204 that is disposed between the conformal nucleation layer 208 and the silicon substrate 202. In the example of Figure 2, the insulating layer 204 may be a gate oxide layer, formed from a high-k dielectric material such as a silicon oxide or silicon nitride material. In some embodiments, a conformal barrier layer such as TiN or a tungsten-containing layer may be interposed between the nucleation layer 208 and the insulating layer 204.

[0027] Figure 3A depicts a schematic example of wordlines 310 in a 3D NAND structure 323. The wordlines 310 are separated by oxide layers 311. In Figure 3B, a detail of the interface between a wordline 310 and oxide layer 311 is shown including a layer of aluminum oxide (Al_2O_3) 304 and a nucleation layer 308 is shown. In some embodiments, the nucleation layer 308 may be deposited directly on the oxide layer 311 or on a TiN or other barrier layer as described herein. The nucleation layers may be between about 10Å and 100Å, or 10Å and 50Å, for example, for deposition of a wordline 310 of between about 10 nm and 100 nm thick.

[0028] Figure 4 is a process flow diagram illustrating operations in a method of depositing a conductive material. In operation 402, a conformal nucleation layer is formed on a structure by an atomic layer deposition (ALD). In an ALD method, the substrate may be exposed in cycles such that the substrate is first exposed to a pulse of a suitable metal-containing precursor, then the precursor is optionally purged, then the substrate is exposed to a pulse of a reducing agent, and then the reducing agent is optionally purged, and such cycles may be repeated until a desired thickness of the nucleation layer is formed on the substrate. It will be appreciated that the order of precursor and reducing agent may be reversed such that the sequence may be initiated by a reducing agent dose followed by a metal containing precursor dose.

[0029] In some embodiments, the reducing agent is ammonia (NH_3) or other nitrogen-containing reducing agent such hydrazine (N_2H_4). NH_3 chemisorption on dielectrics is more favorable than that of hydrogen (H_2). In some embodiments, the reducing agent and precursor are selected such that they react without reducing agent dissociation. NH_3 reacts with metal oxychlorides and metal chlorides without dissociation. This is in contrast to, for example, ALD from metal oxychlorides that uses H_2 as a reducing agent; H_2 dissociates on the surface to form adsorbed atomic hydrogen, which results in very low concentrations of reactive species and low surface coverage during initial nucleation of metal on the dielectric surface. By using NH_3 and metal oxychloride or metal chloride precursors, nucleation delay is reduced or eliminated at deposition temperatures up to hundreds of degrees lower than used by H_2 reduction of the same metal precursors.

[0030] In some embodiments, the reducing agent may be a boron-containing or silicon-containing reducing agent such as diborane (B_2H_6) or (SiH_4). These reducing agents may be used with metal chloride precursors; with metal oxychlorides, however, the B_2H_6 and SiH_4 will react with water formed as a byproduct during the ALD process and form solid B_2O_3 and SiO_2, which are insulating and will remain in the film, increasing resistivity. Use of NH_3 also has improved adhesion over B_2H_6 and SiH_4 ALD processes

on certain surfaces including Al_2O_3.

[0031] Examples of metal oxychloride and metal chloride precursors include molybdenum pentachloride ($MoCl_5$), molybdenum oxychlorides such as molybdenum dichloride dioxide (MoO_2Cl_2) and molybdenum oxytetrachloride ($MoOCl_4$), tungsten pentachloride (WCl_5), tungsten hexachloride (WCl_6), tungsten tetrachloride (WCl_4), tungsten dichloride (WCl_2), and tungsten oxychlorides (WO_xCl_y) such as tungsten oxytetrachloride ($WOCl_4$).

[0032] The metal chloride and metal oxychloride may be useful in embodiments in which fluorine incorporation is a concern. However, in some embodiments, fluorine-containing precursors may be used. These include metal fluorides such as tungsten hexafluoride (WF_6), molybdenum hexafluoride (MoF_6), and molybdenum pentafluoride (MoF_5).

[0033] The resulting nucleation layer is generally not a pure elemental film but a metal nitride or metal oxynitride film. In some embodiments, there may be residual chlorine or fluorine from the deposition, particularly if the deposition is performed at low temperatures. In some embodiments, there no more than a trace amount of residual chlorine or fluorine. In some embodiments, the nucleation layer is an amorphous layer. Impurities in the film (e.g., oxygen, NH_3, chlorine or other halogen) facilitate growth of an amorphous microstructure. In some embodiments, the nucleation layer as deposited is an amorphous metal oxynitride layer or an amorphous metal nitride layer. The amorphous character templates large grain growth in the subsequently deposited conductor. The surface energy of nitride or oxynitride relative to an oxide surface is much more favorable than that of a metal on an oxide surface, facilitating formation of a continuous and smooth film on the dielectric. This allows formation of thin, continuous layers. Example thicknesses of the nucleation layer range from 5–30Å as deposited. Depending on the temperature, this may be about 5–50 ALD cycles for example.

[0034] As described below, during subsequent processing the nucleation layer may be converted to a pure (or less impure) elemental metal film with the thickness decreasing.

[0035] Substrate temperature for nucleation layer deposition may range, for example, from 300°C–600°C. In some embodiments, low temperatures may be used. Such temperatures may be less than 500°C, less than 550°C, less than 450°C, less than 400°C, or less than 350°C. Low temperatures may be used for improved step coverage. In addition, low temperatures may increase the amount of impurities in the nucleation layer, increasing the amorphous character, which in turn may increase grain size of the subsequently deposited conductor.

[0036] The surface on which the nucleation layer is deposited depends on the particular application. In some embodiments, the nucleation layer is deposited directly on a dielectric (e.g., silicon oxide, aluminum oxide, silicon nitride, etc.) surface. In some embodiments, the nucleation layer is deposited directly on a titanium nitride or other surface. As discussed further below, by performing operation 402, the subsequent elemental metal deposition may be performed on any surface.

[0037] After deposition of the nucleation layer, an optional operation 404 may be performed. In operation 404, lower temperature ALD cycles a metal conductor and a reducing agent are performed.

The "lower" temperature refers to the temperature in operation 404, if performed, being lower than the subsequent operation 406. Example temperatures may be less than 500°C, less than 550°C, less than 450°C, less than 400°C, or less than 350°C. In this operation, the reducing agent is different than in operation 402, and in particular examples may be hydrogen (H_2). In particular, H_2 may result in deposition of an elemental film with significantly fewer impurities than in the nucleation layer. The temperature may be the same temperature as used in operation 402 in some embodiments. The metal precursor may also be the same or a different precursor than in employed in operation 402. In some embodiments, the same precursor is used, with only the reducing agent changed. In some embodiments, operation 404 may facilitate conversion of the metal nitride or metal oxynitride nucleation layer to an elemental metal film. According to various embodiments, operation 404 may or may not deposit an appreciable amount of film of the main conductor.

[0038] In a further optional operation 406, the substrate temperature is raised. In embodiments, in which operation 404 is performed, operation 406 is also performed. In other embodiments, operation 406 may be performed. For example, if the nucleation layer deposition occurs at relatively low temperatures (e.g., below 400°C), the temperature may be raised in operation 406 to a higher temperature at which deposition of the main conductor will be performed. In some embodiments, the temperature may be greater than 500°C, and in some embodiments, greater than 600°C. In some embodiments, a lower temperature (e.g, between 400°C and 500°C, endpoints inclusive) may be used for bulk deposition. The temperature may or may not be raised, depending on the temperature of previous operations.

[0039] The method may then proceed to an operation 408 (from any of operation 402, 404, or 406) in which the main conductor is deposited by ALD. As in operation 404 (if performed), H_2 may be used as a reducing agent.

[0040] Examples of metal oxychloride and metal chloride precursors that may be employed in operations 404 and 408 include molybdenum pentachloride ($MoCl_5$) and molybdenum hexachloride ($MoCl_6$), molybdenum oxychlorides such as molybdenum dichloride dioxide (MoO_2Cl_2) and molybdenum oxytetrachloride ($MoOCl_4$), tungsten pentachloride (WCl_5), tungsten hexachloride (WCl_6), tungsten tetrachloride (WCl_4), tungsten dichloride (WCl_2), and tungsten oxychlorides (WO_xCl_y) such as tungsten oxytetrachloride ($WOCl_4$).

[0041] During one or more of operations 404–408, the nucleation layer is converted to an elemental metal layer. This may also be characterized as removing impurities, i.e., any non-metal constituent. The nucleation layer may have greater impurities than the subsequently deposited elemental layer, but they are sufficiently removed such that the stack resistivity is the same or similar to a stack that does not include a nucleation layer. The thickness will also decrease; for example, a 30Å as-deposited film may contribute about 10Å metal to the stack.

[0042] According to various embodiments, one or more of the following may be employed to facilitate conversion of the nucleation layer to an elemental metal film: 1) depositing the bulk conductor at a higher temperature (e.g., 550°C) than the nucleation layer is deposited, 2) performing lower temperature ALD H_2/metal precursor cycles as described with reference to operation 404 above, and 3) in-situ deposition of

the bulk layer, such that the nucleation layer is not exposed to air or otherwise oxidized before bulk deposition. Mo oxychlorides and W oxychlorides in particular are relatively easy to convert to elemental metal. The resulting converted nucleation layer and pure metal layer may each be characterized as having fewer than 1% atomic impurities.

[0043] Figure 5 shows results of forming a Mo-containing layer using NH_3 a reducing agent and a molybdenum oxychloride precursor to form a nucleation layer, then converting the Mo-containing layer to Mo as described above. Figure 5 shows the nucleation layer thickness, after conversion to Mo, is shown as a function of ALD cycles. At each temperature (350°C – low, 400°C – med, 450°C – high), deposition was performed on three different surfaces: an Al_2O_3 surface, a TiN surface, and a thermal SiO_2 surface. At each temperature, the growth rate is the same for all surfaces. Thus, while the growth rate is insensitive to temperature, it is insensitive to substrate surface. Notably, this is different from other deposition systems, which can be highly substrate dependent. For example, an H_2 and molybdenum oxychloride ALD deposition would deposit on TiN, deposit a small amount on SiO_2, and deposit almost nothing on Al_2O_3.

[0044] Figure 6 shows subsequent Mo growth from H_2 and molybdenum oxychloride ALD cycles on a nucleation layer deposited on an Al_2O_3 surface as described above as compared to Mo growth from H_2 and molybdenum oxychloride ALD cycles directly on an Al_2O_3 surface at 550°C. Curve A shows Mo growth on approximately 10Å nucleation layer deposited from NH_3/Mo oxychloride and curve B shows Mo growth on Al_2O_3. As can be seen, ALD deposition from H_2 reduction of the Mo precursor shows a steady growth on the Mo nucleation layer deposited from NH_3 reduction of the Mo precursor, with no nucleation delay. By contrast, the H_2/Mo precursor ALD cycles result in no deposition on Al_2O_3.

[0045] Figure 7 shows resistivity of various Mo films. Curve A represents resistivity of H_2/Mo oxychloride ALD film on a low temperature NH_3/Mo oxychloride nucleation layer, Curve B represents resistivity of H_2/Mo oxychloride ALD film on a high temperature NH_3/Mo oxychloride nucleation layer, and Curve C represents resistivity of H_2/Mo oxychloride ALD film on TiN. No increase in blanket resistivity is found using the nucleation layers described herein, indicating that they are converted to elemental Mo films.

[0046] While the description above refers to metal oxychloride and metal chloride precursors, the methods may also be performed with other halogen containing precursors including metal oxyfluoride and metal fluoride precursors.

[0047] In some embodiments, the methods may involve depositing a metal oxynitride or metal nitride nucleation layer followed by deposition of a pure metal layer by chemical vapor deposition (CVD).

Apparatus

[0048] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems. The process can be performed on multiple deposition stations in parallel.

[0049] In some embodiments, a nucleation layer deposition process is performed at a first station that is one of two, five, or even more deposition stations positioned within a single deposition chamber. For example, nucleation layer deposition may be performed at a first station, followed by lower temperature hydrogen reduction of a metal precursor at a second station, followed by high temperature hydrogen reduction of a metal precursor at a third station. Each station may have independent temperature control. In some embodiments, various steps for the process are performed at two different stations of a deposition chamber. For example, the substrate may be exposed to NH_3 in a first station using an individual gas supply system that creates a localized atmosphere at the substrate surface, and then the substrate may be transferred to a second station to be exposed to a metal chloride, metal fluoride, or metal oxychloride precursor precursor to deposit the nucleation layer. In some embodiments, the substrate may then be transferred back to the first station for a second exposure of NH_3. Then the substrate may be transferred to the second station for exposure to the metal precursor. The substrate may also be exposed to NH_3 at another station following the first metal chloride or metal oxychloride deposition. This may be repeated as necessary to complete nucleation layer deposition and proceed with bulk layer deposition in the same or different stations.

[0050] In some embodiments, multiple chambers are used to perform the methods described herein. For example, deposition of the nucleation layer may be performed in a first chamber and deposition of the bulk metal layer performed in a second chamber. The two chambers may be connected to a common vacuum chamber such that the substrate can be transferred between them without exposure. In alternate embodiments, the chambers are not connected under vacuum, with the substrate exposed to air during transfer. Any oxidation can be reduced in the subsequent processing as described above.

[0051] Figure 8 is a block diagram of a processing system suitable for conducting deposition processes in accordance with embodiments described herein. The system 800 includes a transfer module 803. The transfer module 803 provides a clean, pressurized environment to minimize the risk of contamination of substrates being processed as they are moved between the various reactor modules. Mounted on the transfer module 803 is a multi-station reactor 809 capable of performing ALD depositions as described herein. Chamber 809 may include multiple stations 811, 813, 815, and 817 that may sequentially perform these operations. For example, chamber 809 could be configured such that stations 811 and 813 perform nucleation layer deposition, and stations 813 and 815 perform bulk layer deposition. Each deposition station may include a heated wafer pedestal and a showerhead, dispersion plate or other gas inlet.

[0052] Also mounted on the transfer module 803 may be one or more single or multi-station modules 807 capable of performing plasma or chemical (non-plasma) pre-cleans. The module may also be used for various other treatments, e.g., reducing agent soaking. The system 800 also includes one or more (in this case two) wafer source modules 801 where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 819 first removes wafers from the source modules 801 to loadlocks 821. A wafer transfer device (generally a robot arm unit) in the transfer module 1103 moves the wafers from loadlocks 821 to and among the modules mounted on the transfer module 803.

[0053] In some embodiments, a high temperature showerhead is employed.

This allows single, rather than dual, plenum showerheads to be used. By maintaining showerhead internal wetted surfaces at greater than 150°C or 200°C, NH_3 and metal oxychloride or metal chloride precursors can be used in a single plenum showerhead without NH_4Cl condensation. Alternately dual-plenum showerheads may be used in which NH_3 is delivered through one plenum and metal chloride or oxychloride precursors can be delivered through the other plenum.

[0054] As noted above, in some embodiments, depositing both metal (nitride) nucleation and pure metal in a single process chamber facilitates the conversion of the as-deposited metal + O_x + NH_x + Cl_x nucleation film to pure metal by high-temperature reaction with H_2, metal (oxychloride), and their byproducts (HCl, OCl_x, Metal-Cl_x, ...). This may be done in a multi-station reactor with low-temperature at the first deposition station and high temperatures at subsequent deposition stations as described above. In some embodiments, the individual deposition stations in a multi-station deposition reactor can be isolated from each other by shaping the showerheads and pedestals such that in a pedestal-up process position, the two assemblies create a small process volume above the wafer and a very narrow gap to isolate the process volume from the main chamber. The narrow gap at the edge of the process volume can be augmented with an inert gas purge barrier to make it difficult for gas to diffuse from the main chamber into the process volume. The narrow gap at the edge of the process volume can also incorporate a local pumping plenum to prevent process gas from entering the main chamber. This can eliminate the risk of deposition or particle generation in the main chamber. The narrow edge gap by itself can eliminate the risk of gas from the main chamber diffusing back into the wafer processing volume such there is no station to station cross talk.

[0055] As noted above, in certain embodiments, a system includes two different deposition chambers. For example, referring to Figure 8, two deposition chambers may be mounted on transfer module 803. In such embodiments, each deposition chamber may be a single or multi-station chamber. Still further, two deposition chambers not under common vacuum may be employed.

[0056] In certain embodiments, a system controller 829 is employed to control process conditions during deposition. The controller will typically include one or more memory devices and one or more processors. The processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0057] The controller may control all of the activities of the deposition apparatus. The system controller executes system control software including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels if used, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the controller may be employed in some embodiments.

[0058] Typically, there will be a user interface associated with the controller. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0059] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard

coded or provided as software. The instructions may be provided by "programming." Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language. Alternatively, the control logic may be hard coded in the controller. Applications Specific Integrated Circuits, Programmable Logic Devices (e.g., field-programmable gate arrays, or FPGAs) and the like may be used for these purposes. In the following discussion, wherever "software" or "code" is used, functionally comparable hard coded logic may be used in its place.

[0060] The computer program code for controlling the deposition and other processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program.

[0061] The controller parameters relate to process conditions such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

[0062] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller. The signals for controlling the process are output on the analog and digital output connections of the deposition apparatus.

[0063] The system software may be designed or configured in many different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the deposition processes described herein. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0064] In some implementations, a controller 829 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the "controller," which may control various components or subparts of the system or systems. The controller 829, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings,

wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0065] Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0066] The controller 829, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller 829 may be in the "cloud" or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0067] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor

processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0068] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0069] The controller 829 may include various programs. A substrate positioning program may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control program may include code for controlling gas composition and flow rates and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck.

[0070] Examples of chamber sensors that may be monitored during deposition include mass flow controllers, pressure sensors such as manometers, and thermocouples located in pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0071] The foregoing describes implementation of embodiments of the disclosure in a single or multi-chamber semiconductor processing tool.

[0072] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically comprises some or all of the following steps, each step provided with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

[0073] In the description above and in the claims, numerical ranges are inclusive of the end points of the range. For example, "a thickness between 1 and 5 nm" includes 1 nm and 5 nm. Similarly, ranges represented by a dash are inclusive of the end points of the ranges.

CONCLUSION

[0074] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

Claims

1. A method comprising:

depositing a first layer from a metal oxychloride precursor and ammonia using a first atomic layer deposition (ALD) process; and

depositing an elemental metal layer on the first layer from a metal oxychloride precursor and hydrogen using a second ALD process.

2. The method of claim 1, wherein the first layer is a metal oxynitride or metal nitride layer.

3. The method of claim 2, wherein the first layer is converted to an elemental metal layer during or prior to the second ALD process.

4. The method of claim 3, wherein the converted elemental metal later contains less than 1 (atomic) % impurities.

5. The method of claim 1, wherein the first layer is an amorphous layer.

6. The method of claim 5, wherein the elemental layer is crystalline.

7. The method of claim 1, wherein the first and second ALD processes are performed in the same chamber and without exposure to air.

8. The method of claim 1, wherein the first layer is a template for metal grain growth in the second layer.

9. The method of claim 1, wherein the elemental layer contains less than 1 (atomic) % impurities.

10. The method of claim 1, wherein the elemental metal layer is elemental tungsten.

11. The method of claim 1, wherein the elemental metal layer is elemental molybdenum.

12. The method of claim 1, wherein the first layer is one of molybdenum oxynitride and molybdenum nitride.

13. The method of claim 1, wherein the first ALD process is performed at a temperature less than 400°C.

14. The method of claim 13, wherein the second ALD process is performed at a temperature greater than 400°C.

15. The method of claim 1, wherein deposition of the first layer and deposition of the elemental layer are performed in the same chamber.

16. The method of claim 15, wherein deposition of the first layer and deposition of the elemental layer are performed in different stations of the same chamber.

17. The method of claim 1, wherein deposition of the first layer is performed in a first chamber and deposition of the elemental layer is performed in a second chamber.

18. The method of claim 1, further comprising exposing the first layer to air prior to deposition of the elemental layer.

19. An apparatus comprising:

first and second process chambers each configured to house a substrate;

a substrate support in each of the process chambers;

gas inlets configured to direct gas into each of the process chambers;

a heater configured to heat the substrate support in each process chamber; and

a controller comprising program instructions for:

(a) sequentially inletting a metal oxychloride precursor and ammonia into the first process chamber while a substrate is housed in the first process chamber;

(b) after (a), transfer the substrate to the second process chamber and

(c) after (b), sequentially inletting a metal oxychloride precursor and hydrogen into the second process chamber while the substrate is housed in the second process chamber.

20. An apparatus comprising:

a process chamber having one or more stations, each configured to house a substrate;

a substrate support in each of the one or more stations;

gas inlets configured to direct gas into each of the one or more stations;

a heater configured to heat the substrate support in each station; and

a controller comprising program instructions for:

sequentially inletting a metal oxychloride precursor and ammonia into one of the one or stations; and

sequentially inletting a metal oxychloride precursor and hydrogen into one of the one or stations.

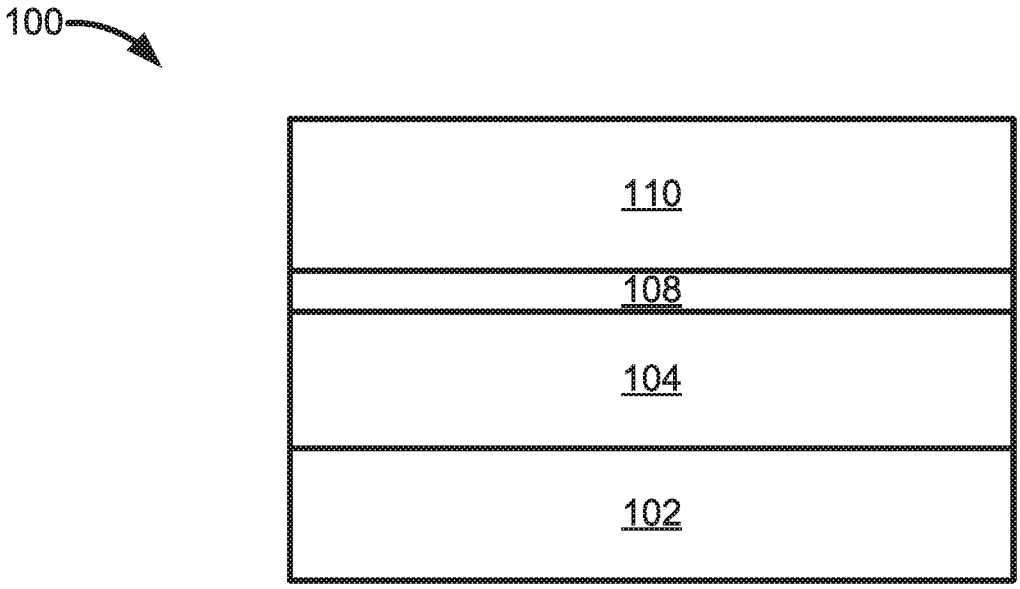

FIG. 1A

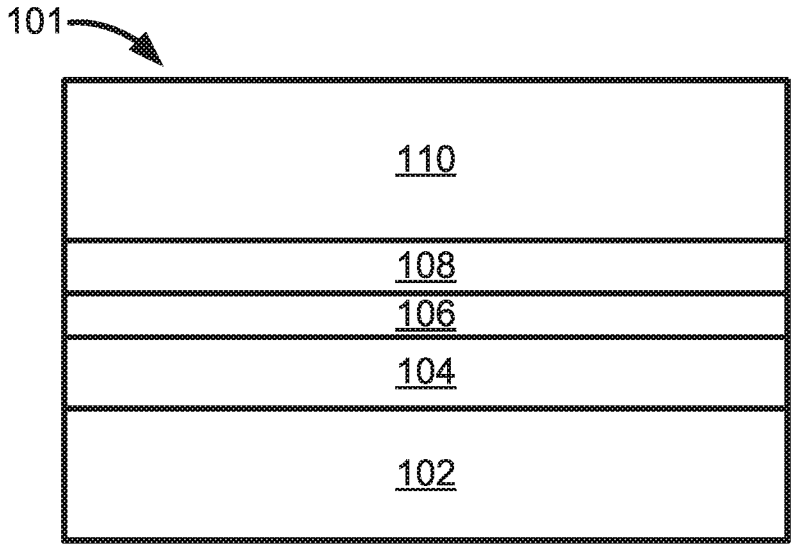

FIG. 1B

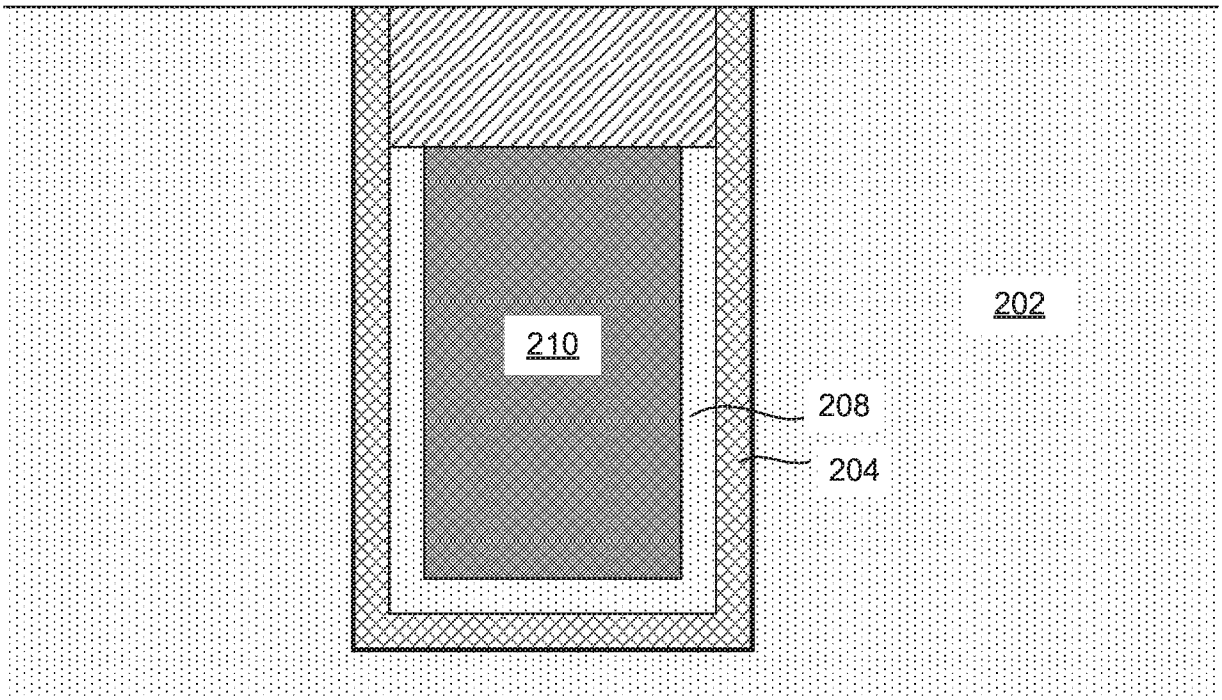

FIG. 2

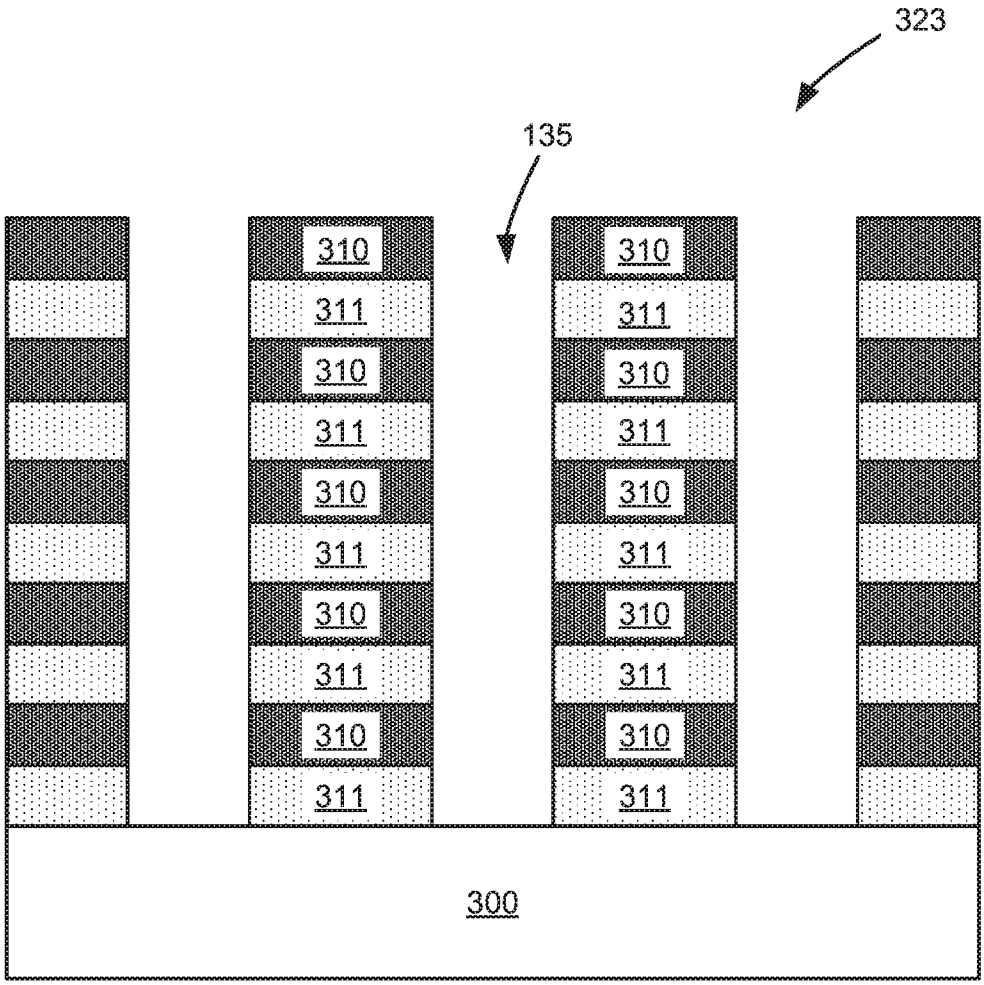
323
135
310
311
310
311
310
311
310
311
310
311
310
311
310
311
300

FIG. 3A

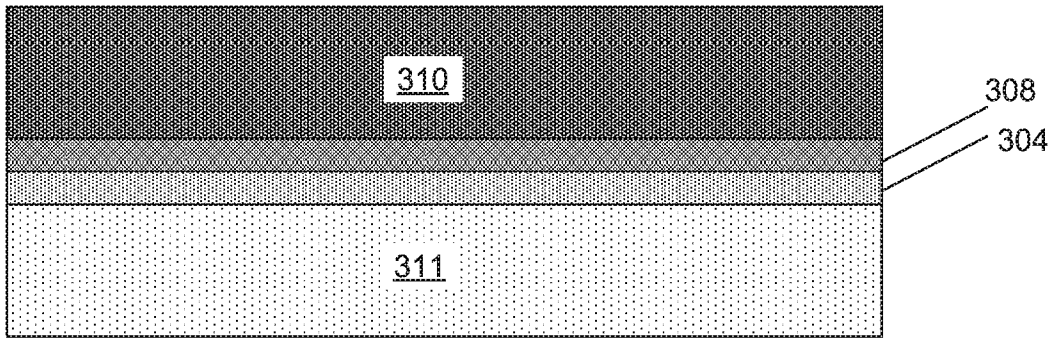
310
308
304
311

FIG. 3B

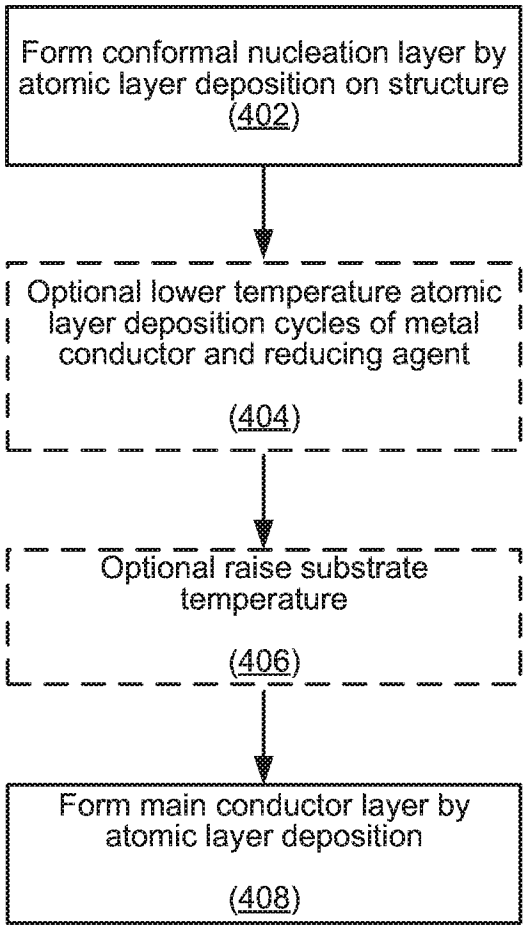
Form conformal nucleation layer by atomic layer deposition on structure (402)
Optional lower temperature atomic layer deposition cycles of metal conductor and reducing agent (404)
Optional raise substrate temperature (406)
Form main conductor layer by atomic layer deposition (408)

FIG. 4

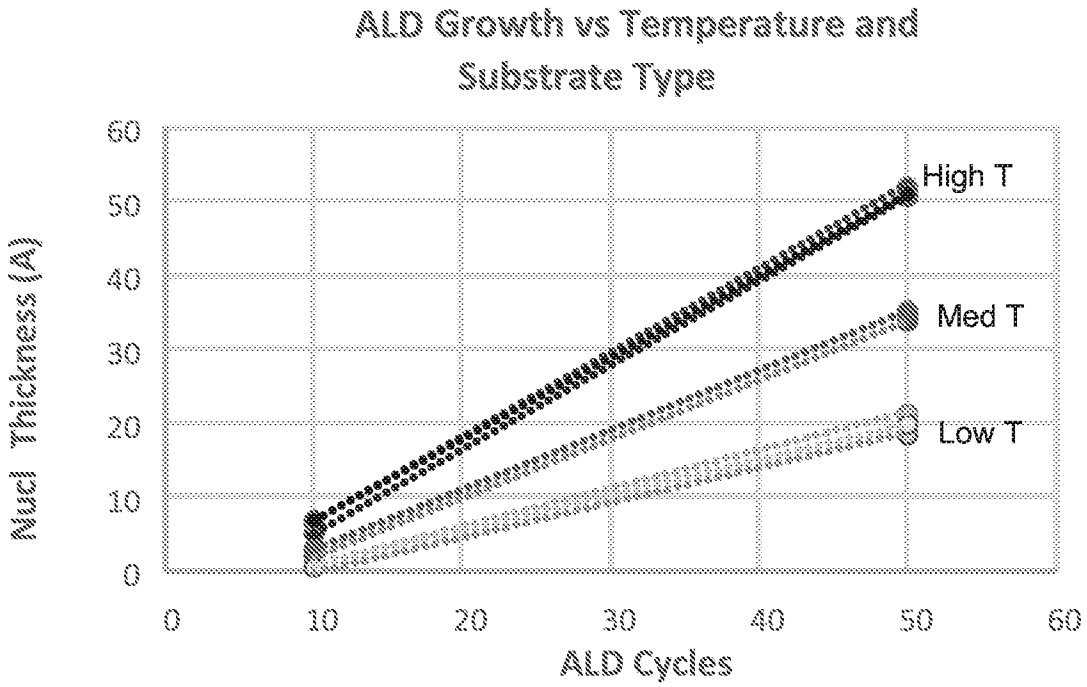
ALD Growth vs Temperature and Substrate Type
Nucl Thickness (A)
60
50
40
30
20
10
0
0
10
20
30
40
50
60
ALD Cycles
High T
Med T
Low T

FIG. 5

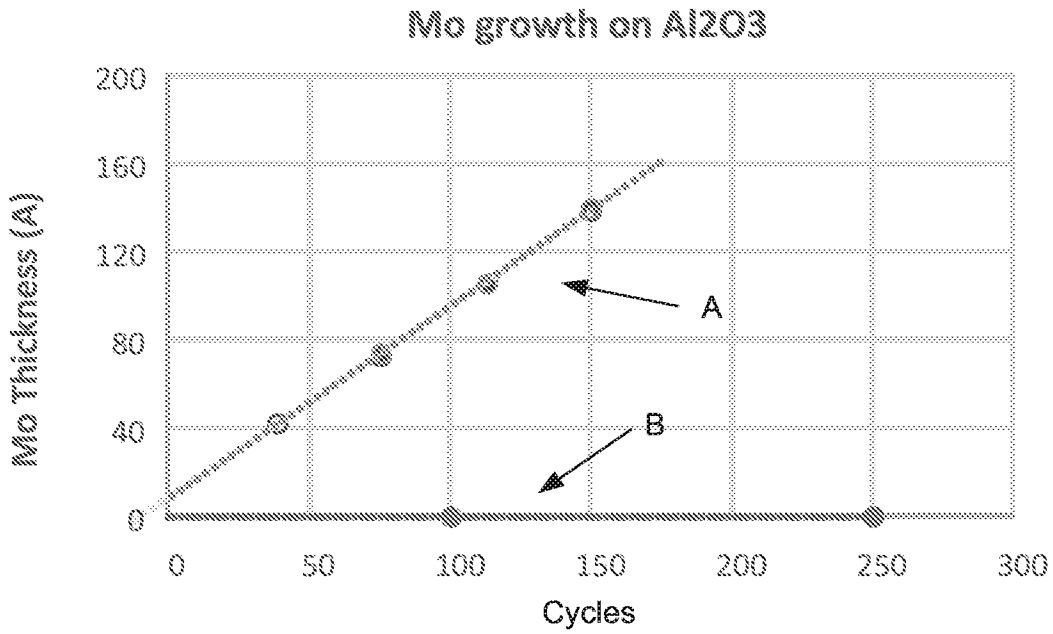
Mo growth on Al2O3
Mo Thickness (A)
200
160
120
80
40
0
0
50
100
150
200
250
300
Cycles
A
B

FIG. 6

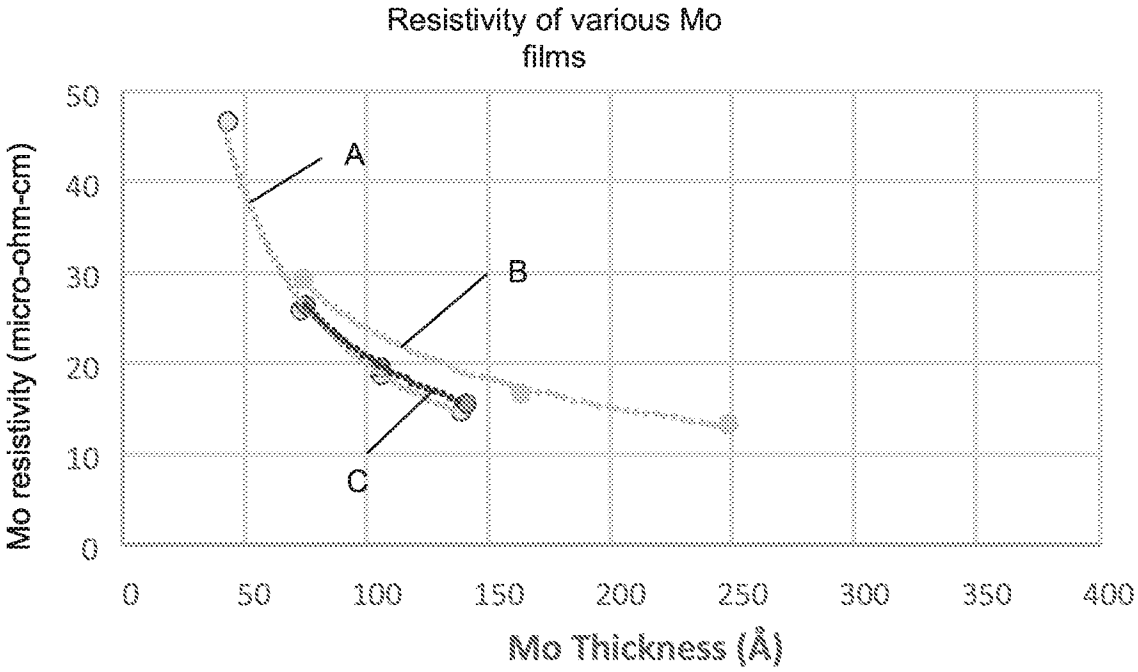
Resistivity of various Mo films
Mo resistivity (micro-ohm-cm)
50
40
30
20
10
0
0
50
100
150
200
250
300
350
400
Mo Thickness (Å)
A
B
C

FIG. 7

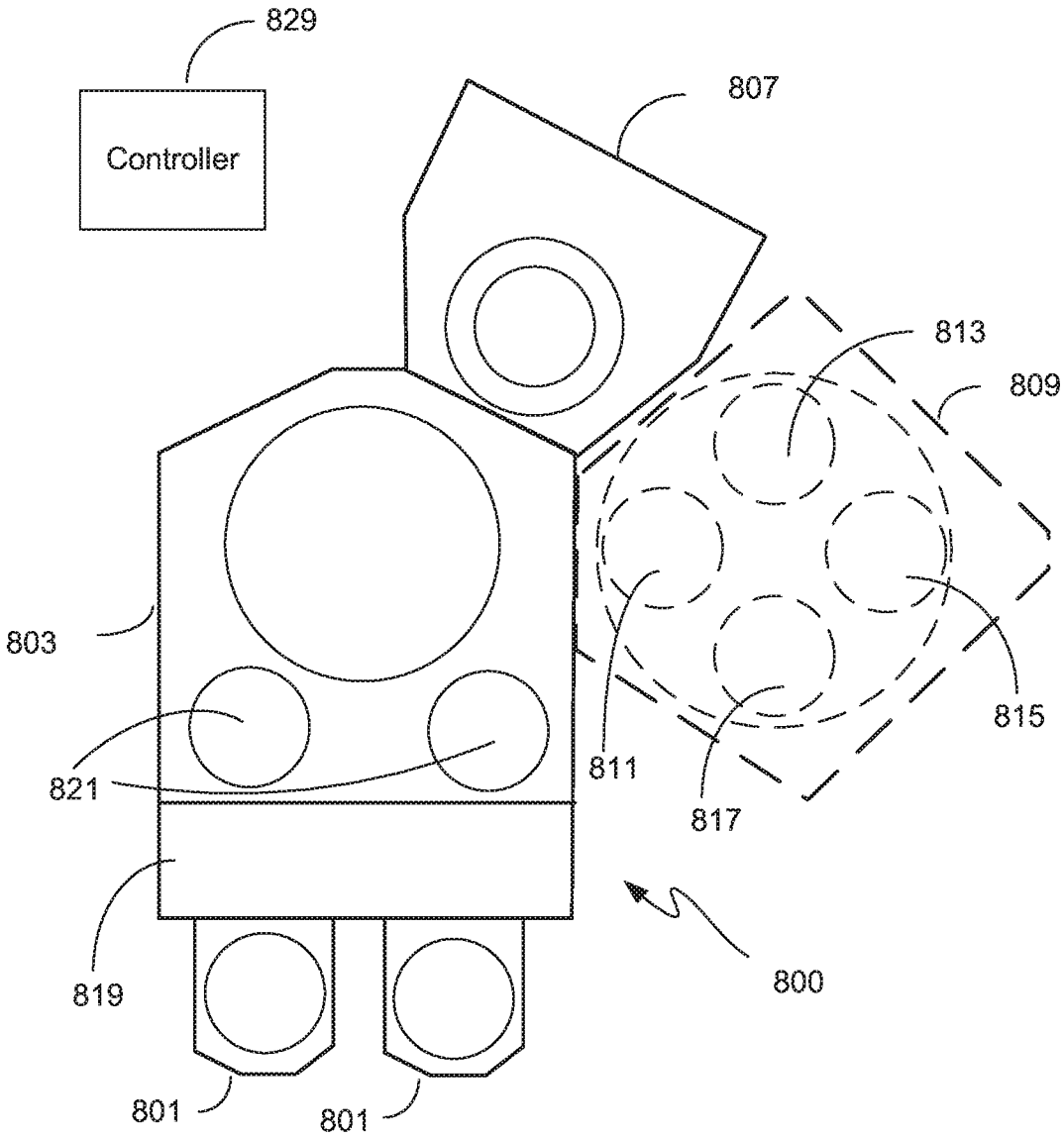

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/015241

A. CLASSIFICATION OF SUBJECT MATTER

C23C 16/455(2006.01)i, C23C 16/56(2006.01)i, C23C 16/30(2006.01)i, C23C 16/34(2006.01)i, H01L 21/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
C23C 16/455; C23C 16/00; C23C 16/06; C23C 1600; H01L 21/285; H01L 21/3205; H01L 21/44; C23C 16/56; C23C 16/30; C23C 16/34; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:convert, metal oxychloride precursor, ammonia, ALD, metal oxynitride, amorphous, template, hydrogen

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014-0147589 A1 (APPLIED MATERIALS, INC.) 29 May 2014 paragraphs [0017]-[0020], [0024], [0028], [0036], [0041], [0044], [0050] and claim 1	1-20
Y	US 10121671 B2 (APPLIED MATERIALS, INC.) 06 November 2018 column 6, lines 6-30, column 7, lines 21-24, column 8, lines 60-62, column 9, lines 52-64 and claims 1, 4, 9	1-20
Y	US 6103609 A (LEE et al.) 15 August 2000 claims 1-3	4-6,9
A	US 6306216 B1 (KIM et al.) 23 October 2001 column 7, lines 17-34, claim 1, and figure 3a	1-20
A	US 2011-0021024 A1 (CALVO-MUNOZ et al.) 27 January 2011 paragraphs [0074]-[0082]	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 May 2020 (29.05.2020)	**03 June 2020 (03.06.2020)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
LEE, Eon Su
Telephone No. +82-42-481-8539

Form PCT/ISA/210 (second sheet) (July 2019)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/015241

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0147589 A1	29/05/2014	US 9546419 B2	17/01/2017
US 10121671 B2	06/11/2018	US 10483116 B2	19/11/2019
		US 2017-0062224 A1	02/03/2017
		US 2019-0088489 A1	21/03/2019
US 6103609 A	15/08/2000	JP 11-238736 A	31/08/1999
		JP 3168421 B2	21/05/2001
		KR 10-0282436 B1	02/03/2001
		KR 10-0325297 B1	17/04/2002
US 6306216 B1	23/10/2001	EP 1069599 A2	17/01/2001
		EP 1069599 A3	04/12/2002
		EP 1069599 B1	09/12/2009
		JP 2001-068423 A	16/03/2001
		JP 3252960 B2	04/02/2002
		KR 10-0319494 B1	09/01/2002
		KR 10-2001-0009968 A	05/02/2001
		TW 466587 B	01/12/2001
US 2011-0021024 A1	27/01/2011	TW 201001549 A	01/01/2010
		TW I470696 B	21/01/2015
		US 8324104 B2	04/12/2012
		WO 2009-125255 A1	15/10/2009