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[Continued on next page]

(54) Title: **WAFER LEVEL OPTOELECTRONIC PACKAGE WITH FIBER SIDE INSERTION**

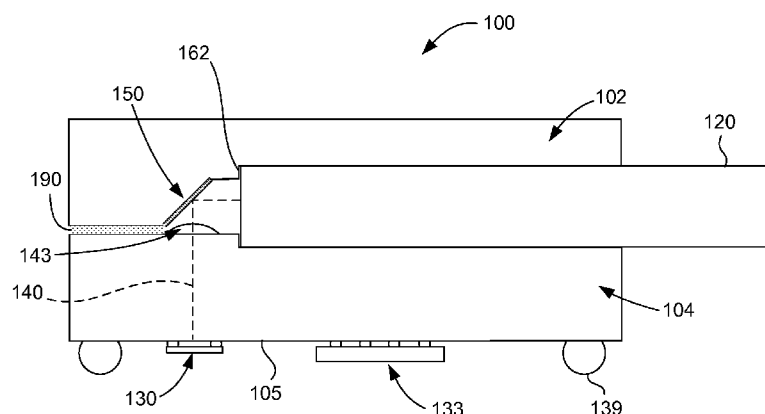


FIG. 1A

(57) **Abstract:** Optoelectronic packages and wafer level techniques for forming optoelectronic packages are described. In accordance with one apparatus aspect of the invention, a pair of substrates are bonded together to form an optical coupler. A first one of the substrates has a recess that faces the second substrate to at least in part define a channel suitable for receiving an optical transmission medium. A photonic device is mounted on a mounting surface of the second substrate that is opposite its bonded surface. The photonic device faces the reflective surface and an optical path is formed between the channel and the photonic element that both reflects off of the reflective surface and passes through the second substrate. In some embodiments an integrated circuit device and/or solder bumps are also attached to the mounting surface and the second substrate has conductive traces thereon that electrically couple the various electrical components as appropriate (e.g., the photonic device, the integrated circuit device, the solder bumps and/or other components). The substrates may be formed from a wide variety of materials including, glass, plastic and silicon. In some embodiments, at least the second substrate is formed from an optically transparent material and the optical path passes directly through the optically transparent material. In a method aspect of the invention, a variety of wafer level methods for forming such devices are described.





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WAFER LEVEL OPTOELECTRONIC PACKAGE WITH FIBER SIDE INSERTION**TECHNICAL FIELD**

[0001] The present invention relates generally to optoelectronic packages. More particularly, optoelectronic packages having side optical fiber insertion and wafer level
5 methods for forming such packages are described.

BACKGROUND

[0002] Many packaged optoelectronic devices include both photonic devices and integrated circuits ("IC"). Such packages generally need to provide a mechanism suitable for optically coupling photonic elements on the photonic device to optical fibers and
10 generally must be arranged in a manner that protects the integrated circuits and/or photonic devices from damage due to exposure to the outside environment. Accordingly, numerous conventional optoelectronic packages involve the formation of an optically transparent window or other transparent component that enables light to reach one or more photonic elements on the photonic device or, conversely, to be emitted by the
15 photonic elements and exit the device.

[0003] While many of the existing optoelectronic packaging arrangements work well, there are continuing efforts to provide more reliable and cost effective ways for packaging optoelectronic devices.

SUMMARY

[0004] To achieve the foregoing and other objects of the invention, a variety of improved optoelectronic packaging arrangements are described. In accordance with one apparatus aspect of the invention, a pair of substrates are bonded together to form an optical coupler. A first one of the substrates has a recess that faces the second substrate to at least in part define a channel suitable for receiving an optical transmission medium. A
20 photonic device is mounted on a mounting surface of the second substrate that is opposite its bonded surface. The photonic device has at least one photonic element thereon that faces the reflective surface. An optical path is formed between the channel and the photonic element that both reflects off of the reflective surface and passes through the second substrate.

[0005] In some embodiments an integrated circuit device and/or solder bumps are also attached to the mounting surface and the second substrate has conductive traces
30

thereon that electrically couple the various electrical components as appropriate (e.g., the photonic device, the integrated circuit device, the solder bumps and/or other components)

[0006] In some embodiments, the recess in the first substrate extends beyond the fiber channel and includes a tapered wall that supports the reflector. The recess may also
5 include a step that serves as an alignment stop for the optical fiber to precisely position the optical fiber relative to the reflector.

[0007] The optoelectronic device may be arranged to receive a single optical fiber or multiple optical fibers. When more than one photonic element is required, the photonic elements may be provided and positioned in a wide variety of different manners. For
10 example, a single die may have multiple photonic elements, or multiple photonic devices may be mounted on the second substrate. When multiple optical fibers are desired, the coupler may include a plurality of distinct channels, or a single channel that receives a plurality of fibers.

[0008] The substrates may be formed from a wide variety of materials including, for
15 example, glass, plastic and silicon. In some embodiments, at least the second substrate is formed from an optically transparent material and the optical path passes directly through the optically transparent material.

[0009] With many of the described arrangements, a longitudinal axis of the fiber channel extends substantially in parallel to the mounting surface of the second substrate,
20 which provides a low profile.

[0010] In a method aspect of the invention, a variety of wafer level methods for forming optoelectronic devices are described. In one aspect a pair of preprocessed substrates are bonded together. The substrates may be wafers or may take any other suitable form, and each have a multiplicity of device areas defined thereon. Each device
25 area on the first substrate includes a recessed region and a reflective surface formed on a wall of the recessed region. Any of the other desired features, including the conductive traces and other features mentioned above may also be formed during preprocessing of the substrates. The second substrate has a mounting surface opposite its bonded surface. Photonic devices and other appropriate components are attached to the mounting surface
30 such that each device area of the second substrate includes at least a photonic device.

[0011] After the bonding and component mounting has been completed, the bonded substrates (wafers) are singulated to form a multiplicity of singulated optoelectronic couplers, with each optoelectronic coupler corresponding to an associated device area on

the bonded substrates. Each singulated optoelectronic coupler has a channel suitable for receiving at least one optical fiber that extends between the first and second substrates and is defined at least in part by the corresponding recessed region in the first substrate. Optical fibers may then be inserted into the singulated optoelectronic couplers as desired.

- 5 The described approach provides an efficient, wafer level method for forming low profile optoelectronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention and the advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying
10 drawings in which:

[0013] FIG. 1(a) is a diagrammatic cross sectional side view of an optoelectronic package in accordance with one embodiment of the present invention.

[0014] FIG. 1(b) is a diagrammatic cutaway top view of the bottom substrate 104 of the optoelectronic package illustrated in FIG. 1(a).

15 [0015] FIG. 1(c) is a diagrammatic cutaway bottom view of the top substrate 102 of the optoelectronic package illustrated in FIG. 1(a).

[0016] FIG. 1(d) is a diagrammatic bottom view of the optoelectronic package illustrated in FIG. 1(a).

[0017] FIGS. 2(a)-2(g) are diagrammatic cross sectional side views of segments of
20 wafers used in the fabrication of the optoelectronic package of FIG. 1(a) in accordance with one embodiment of the invention at various stages of a fabrication process.

[0018] FIG. 3 is a diagrammatic cross sectional side view of an optoelectronic package in accordance with a second embodiment of the present invention that does not include a lens on the bottom substrate.

25 [0019] FIG. 4 is a diagrammatic cross sectional side view of an optoelectronic package in accordance with a third embodiment of the present invention.

[0020] FIGS. 5(a)-5(g) are diagrammatic cross sectional side views of segments of wafers used in the fabrication of the optoelectronic package of FIG. 4 in accordance with one embodiment of the invention at various stages of a fabrication process.

30 [0021] In the drawings, like reference numerals are sometimes used to designate like structural elements. It should also be appreciated that the depictions in the figures are diagrammatic and not to scale.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0022] The present invention relates generally to the packaging of optoelectronic devices. Referring initially to Fig. 1(a) – 1(d), an optoelectronic package 100 in accordance with one embodiment of the invention will be described. The package
5 includes a coupler 101 formed from a pair of substrates 102, 104 that are bonded together. The bonded substrates have facing fiber channel recesses 107, 109 that together form a side opening channel 111 suitable for receiving one or more optical fibers 120.

[0023] For the purposes of the description, the upper substrate 102 illustrated in Fig. 1(a) is referred to as the “top” substrate, and the lower substrate 104 in the drawing is
10 referred to as the “bottom” substrate. However, it should be appreciated that the described package may be oriented in virtually any direction so the designations of the substrates as top and bottom is used arbitrarily for descriptive purposes only and is not intended to infer a specific orientation of the illustrated device in use or operation.

[0024] The bottom substrate 104 carries a photonic device 130 and an integrated
15 circuit device 133. Electrical traces 135 (Fig. 1(d)) are formed on the bottom surface of the bottom substrate to electrically connect the integrated circuit device 133 to the photonic device 130 and to I/O pads 137. Electrical interconnects such as solder balls 139 may then be used to electrically and mechanically connect the I/O pads 137 (and thus the integrated circuit device 133) to external devices such as a printed circuit board or
20 other suitable device or substrate.

[0025] The photonic device 130 may be any type of device that includes at least one photonic element that transmits or receives light signals. By way of example, in various embodiments, the photonic device 130 may include a semiconductor laser diode, as for example, a vertical-cavity surface-emitting laser (VCSEL). In these embodiments, the
25 photonic device 130 may be configured to emit a laser beam. In one specific embodiment, the VCSEL may be configured to emit light having a wavelength of approximately 850 nm. In other embodiments, the photonic device 130 may include a photodetector that receives and detects light. In still other embodiments, the photonic device may function as a transceiver that both emits and receives light signals.
30 Additionally, the photonic device 130 may have any desired number of photonic elements. As will be appreciated with those familiar with the art, there are a number of commercially available photonic devices that include multiple laser diodes and/or multiple photodetectors. In the embodiment illustrated in Figure 1, a single photonic

device having a single photonic element is provided. However, it should be appreciated that in other embodiments multiple (indeed any desired number of) photonic devices may be mounted on the bottom substrate 104 and each photonic device may have any desired number of photonic elements. When multiple numbers of photonic devices are provided, appropriate traces 135 may be formed on the bottom surface 105 of the bottom substrate 104 to provide the desired electrical connections between components.

[0026] The integrated circuit device 133 may include any type of integrated circuit intended to work with the photonic device 130. In some embodiments, the integrated circuit device may take the form of a flip chip die, while in others it may be a packaged or partially packaged device. In the illustrated embodiment, a single integrated circuit device is provided. However, again, it should be appreciated that any number of integrated circuit devices or other electrical components (e.g. passive components) may be mounted on bottom substrate 104. In still other embodiments, the functionality of the integrated circuit device can be combined with the photonic device in a single die.

[0027] An optical path 140 (illustrated by a dash line) is provided between the optical fiber and the photonic element of photonic device 130. In the illustrated embodiment, the optical path passes from the photonic element through the bottom substrate 104, through a lens 143 provided on the top surface of the bottom substrate, and reflects off of a mirror (reflector or reflective surface) 150 carried by the top substrate to the optical fiber 120. The bottom substrate 104 is formed from an optically transparent material such as glass or plastic, which permits the optical path to pass through the substrate without requiring a through hole or via to be formed in the substrate 104.

[0028] As will be appreciated by those familiar with the art, in many optoelectronic applications it is desirable to precisely control the optical standoff distance between the photonic element and the optical transmission medium (e.g., optical fiber 120). The described arrangement permits good control of the optical distance between the photonic device 130 and the mirror 150. To precisely control the distance between the mirror 150 and the optical fiber 120, the fiber channel recess 107 formed in the top substrate has a step 162 arranged to function as an alignment stop for the optical fiber. The fiber channel recess 109 formed in the bottom substrate has an end wall 164 that is aligned with the step 162 such that the end wall 164 also functions as an alignment stop for the optical fiber. When the optical fiber 120 is inserted into the fiber channel 111 of optoelectronic package 100, it is pushed in until the fiber abuts against the alignment stops 162, 164.

This facilitates good control of the effective optical standoff distance between the photonic device 130 and the optical fiber 120.

[0029] As mentioned above, in the embodiment illustrated in Figs. 1(a) – 1(d), the bottom substrate 104 is formed from a material such as glass or plastic that is optically transparent or translucent to at least the wavelengths of light used by the optoelectronic device 100. In other embodiments, other materials such as silicon may be used as the bottom substrate 104. However, when an optically opaque material such as silicon is used as the bottom substrate, a via or throughhole is needed in the bottom substrate in order to provide an optical path that extends through the bottom substrate between the top photonic device 130 and the mirror 150.

[0030] The geometry of the fiber channel 111 is designed to receive the optical fiber 120. By way of example, when the optoelectronic device is designed to receive a single optical fiber 120 as in the embodiment illustrated in Fig. 1, the fiber channel 111 may have a substantially circular or diamond shaped cross section. In such embodiments, the geometry of the facing channel recesses 107, 109 would be substantially semicircular or V-shaped troughs. Of course, a wide variety of other cross section geometries may be used as well and in some embodiments it may be desirable to taper portions of the fiber channel to make it easier to insert the optical fiber. When the optoelectronic device is designed for use with more than one optical fiber, multiple single fiber channels, or one or more multi-fiber channels may be provided to receive the appropriate optical fibers 120. When multiple single fiber channels are provided, they may be arranged side by side in parallel or in any other desired configuration. In the illustrated embodiments, the channels are designed to directly receive the optical fibers. However, in alternative embodiments, the channels could be arranged to receive a coupler that holds the ends of one or more optical fibers.

[0031] Referring next to Fig. 2, a method of forming optoelectronic packages such as the package 100 illustrated in Fig. 1 will be described. In the described embodiment, the top and bottom substrates 102, 104 are formed from wafers 202, 204 respectively. Each wafer has a large array of device areas formed thereon, with each device area corresponding to an individual optoelectronic package 100 when fabrication is complete. The number of device areas on a wafer may vary widely, although generally, each wafer may be arranged to have tens, hundreds or thousands, or even tens of thousands of device areas formed thereon. For clarity, in all of the Figs. 2(a) – 2(g), only a small segment of

each wafer is illustrated that corresponds to just a single device area. However, it should be remembered that the fabrication would typically be done using substrates that have a large number of device areas defined thereon.

[0032] The device areas on the wafers 202 and 204 are arranged to match such that individual device areas align when the wafers are positioned adjacent one another. The geometry of the wafers may vary widely depending on the needs of any particular application. One advantage of the described approach is that it can be accomplished using conventional semiconductor fabrication equipment. Thus, in many applications, it may be desirable to utilize generally circular wafers sized to be handled by conventional semiconductor fabrication equipment. However, this is not a requirement and as previously mentioned, the size and geometry of the wafers may be widely varied.

[0033] The wafers may be formed from any material suitable for use as a substrate in an optoelectronic package and for use in wafer type processing. By way of example, glass, plastic and silicon wafers all work well. In some embodiments the wafers may be formed from transparent materials such as glass or high temperature optically transparent plastics (e.g., Ultem™ and Extrem™).

[0034] Figs. 2(a) and 2(b) illustrate steps in the preprocessing of the top wafer 202. Figs. 2(c) and 2(d) illustrate steps in preprocessing the bottom wafer 204. An advantage of the described wafer based approach to forming the substrates 102, 104 is that most or all of the features of the substrates may be formed at the wafer level using conventional wafer processing techniques.

[0035] The top wafer 202 may be formed from any material suitable for use as a substrate in an optoelectronic package and for use in wafer type processing. By way of example, glass, plastic and silicon wafers all work well. As seen in Fig. 2(a), the wafer 202 is initially patterned to form a recessed region in each device area. The recessed regions correspond to the fiber channel recesses 107 in the packaged devices and further include the alignment step 162 and a reflector support surface 168. The recesses may be formed in a variety of manners. In embodiments where the top wafer is formed from plastic, the recessed regions may be formed as part of a wafer molding operation. If materials that are not typically molded such as glass or silicon are used as the wafer substrate, then the top wafer may begin as a relatively standard blank wafer (not shown) and may be patterned to form a recessed region in each device area using standard wafer processing (e.g., etching) techniques.

[0036] The reflector support surface 168 may be tapered and is intended to support the reflector 150 in the finished package. The angle and geometry of the tapered surface may be varied to meet the needs of any particular application. By way of example, a simple tapered surface having a taper angle of 45 degrees works well in many applications. However, if desired, other reflective surface support geometries may be used, as for example a parabolic segment.

[0037] After the recessed regions have been formed a reflective surface may be deposited or otherwise formed on each of the reflector support surfaces as illustrated in Fig. 2(b). The reflective surfaces may be formed in a variety of manners, as for example by sputtering aluminum (Al) or silver (Ag) reflectors onto the tapered surfaces using conventional sputtering techniques. In the embodiment of the optoelectronic package 100 illustrated in Fig. 1, the mirror 150, the fiber channel recess 107 and the corresponding features (e.g., alignment step and tapered reflector surface 168 are the only features in the top substrate 102 and each of these features can be formed at the wafer level during preprocessing of the wafer 202 that forms the top substrate.

[0038] Most of the features of the bottom substrate 104 can also be formed at the wafer level during preprocessing of the bottom wafer 204. Like the top wafer 202, the bottom wafer 204 is patterned to form a recessed region in each device area as seen in Fig. 2(c). Again, the bottom wafer 204 may either be molded in a manner that includes the recessed regions or may begin as a relatively standard blank wafer (not shown) that is subsequently patterned using conventional semiconductor processing techniques. The recessed regions correspond to the fiber channel recesses 109 in the packaged optoelectronic devices 100 and the position of the end walls 164 are arranged to align with the steps 162 in top wafer 202 to serve as alignment stops for the optical fibers.

[0039] When desired, a lens 143 may also be formed or otherwise provided on the top surface of the bottom wafer 204 for each of the device areas. When the bottom wafer is formed from a transparent plastic material, the lenses may be formed together with the wafer as part of a molding operation. Wafers formed of different materials may have lenses formed thereon using appropriate processing techniques. In many embodiments the lenses are not necessary and may be eliminated completely.

[0040] After the appropriate recesses and lenses (if desired) have been formed, the back side of the wafer may be metalized to form the electrical traces 135 and I/O pads 137. Again, standard semiconductor wafer processing techniques can be used to form the

electrical traces and I/O pads. Any appropriate metallurgy that is compatible with the substrate and other components may be used to form the electrical traces and I/O pads. In the illustrated embodiment, the I/O pads are used to support solder bumps and therefore conventional underbump metallization materials work well.

5 [0041] If features in addition to the fiber channel recesses, the electrical traces 135, the I/O pads 137 and the lenses 143 are desired for the bottom substrates, they may be formed during the preprocessing of the bottom substrate wafer 204 as well.

[0042] Once both the top and bottom substrate wafers 202 and 204 have been preprocessed, they may be bonded together as illustrated in Fig. 2(e). A wide variety of
10 bonding techniques may be used to secure the wafers together. In the illustrated embodiment, an adhesive material 190 such as epoxy or Benzocyclobutene (BCB) may be used to bond the wafers together. In some embodiments, the adhesive may be a B-stageable materials such as B-stageable epoxies or a partially cured material such as Benzocyclobutene which can be applied during the wafer pre-processing. An advantage
15 of B-staging or partially curing the adhesive is that the adhesive may be applied and partially cured during wafer pre-processing so that it is hardened and easily handleable during subsequent processing. Later when the wafers are bonded together, the adhesive is softened and then more completely (or completely) cured thereby providing good adhesion between the bonded surfaces.

20 [0043] Although the described adhesive bonding techniques work well, it should be appreciated that in other embodiments a variety of other techniques may be used to attach the wafers together. For example, in some embodiments it may be desirable to solder the wafers together. When soldering is used, appropriate aligned metallic solder pads would typically be formed on the bottom surface of the top wafer 202 and the top surface of the
25 bottom wafer 204 during wafer preprocessing. In other applications it may be desirable to use anodic or diffusion bonding techniques to secure the wafers together. By way of example, such techniques work particularly well when silicon wafers are used for both the top and bottom wafers.

[0044] After the wafers have been bonded together, the photonic devices 130 and the
30 integrated circuit devices 133 may be mounted at the appropriate locations on the bottom wafer as illustrated in Fig. 2(g). Any of a wide variety of component attachment techniques may be used to secure the photonic and integrated circuit devices to the bottom. By way of example, in the illustrated embodiment, the photonic device 130 and

the integrated circuit device 133 are both flip chip type dice that may be soldered directly to appropriate bond pads formed on the bottom substrate. The bond pads may effectively be a part of the electrical traces 135 and utilize the same metallurgy as the I/O pads 137.

[0045] After the dice have been attached, solder bumps 139 may be formed on the bottom wafer using conventional wafer bumping techniques as illustrated in Fig. 2(g). After bumping, the bonded wafers are diced using standard wafer dicing techniques to produce a multiplicity of singulated optoelectronic packages. The optical fiber(s) may then be inserted into the packages and secured as desired.

[0046] In the process flow illustrated in Figs. 2(a)-2(g), only the die mounting and wafer bumping steps are performed after the wafers are bonded together. However, it should be appreciated that other steps may also be performed after wafer bonding if desired. In other embodiments, the wafer bumping and/or the die/device attachment steps may be performed before the wafer bonding. Thus, it should be appreciated that although a particular order of the steps is articulated in the process flow described above, the order of the steps may be varied and some of the described steps may be altered or even eliminated as appropriate to produce a desired final package structure.

[0047] Referring next to Figure 3, a second embodiment of the optoelectronic package 100(a) will be described. This embodiment is quite similar to the embodiment illustrated above in Fig. 1(a) but does not include a lens. Like the embodiment of Fig. 1(a), the bottom wafer is formed from a transparent material such as glass or plastic. The top wafer may be formed from any suitable material such as glass, plastic or silicon. In this embodiment, the bottom substrate 104(a) is thinner than the upper substrate 102. The illustrated package can be formed using the processes described above with respect to Figs. 2(a)-2(g).

[0048] Figure 4 illustrates a third embodiment of the optoelectronic package 100(b). This embodiment is similar to the embodiments described above but differs in that the bottom substrate 102(b) is not transparent. Since the bottom substrate 102(b) is not transparent, a through hole or via 178 is formed through the bottom substrate 102(b) to provide the optical path 140 between a photonic element on the photonic device 130 and the mirror 150. The via 178 may be a simple hole that is formed through the substrate or its edges may be metalized or otherwise coated with a reflective material so that light striking the via's sidewalls is not (or is less likely to be) absorbed by the substrate and

rather passes between the photonic device and the mirror. In still other embodiments, the vias may be filled with a transparent material.

[0049] Generally, the package 100(b) can be formed using the process described above with respect to Figs. 2(a)-2(g) with a few variations. A representative process for forming the optoelectronic package 100(b) is illustrated in Figs. 5(a)-5(g). Generally, the vias 178 are formed during preprocessing of the bottom wafer 104(b) as illustrated in Fig. 5(c). The vias may be formed by a variety of techniques including etching, punching or micro-drilling techniques. In other respects, the process closely resembles the process steps described above with respect to Figs. 2(a)-2(g).

10 [0050] If the top and bottom wafers 202, 204(b) are both formed from silicon, the wafer bonding may be done using ionic bonding, which provides a strong bond between the wafers.

[0051] Although only a few embodiments of the invention have been described in detail, it should be appreciated that the invention may be implemented in many other forms without departing from the spirit or scope of the invention. In the illustrated embodiments, the integrated circuit devices and the photonic devices took the form of flip chip style dice. However, it should be appreciated that either or both of these devices could take more heavily packaged forms. For example, the integrated circuit devices could be embodied in leadless leadframe packages (LLP) sometimes referred to as QFN (quad flat pack – no lead) packages; grid array type packages or a variety of other surface mount type packages.

[0052] As mentioned above, the substrates may be formed from a wide variety of materials. By way of example, plastic, glass and silicon wafers all work well. When transparent materials such as glass or plastic are used as the bottom substrate, vias do not necessarily need to be formed in the bottom substrate in order to provide an optical path between the photonic device and the reflective surface. When plastics are used, high-temperature rated thermoplastics that are suitable for use in semiconductor packaging applications such as polyetherimide (e.g., (e.g., UltemTM, SiltemTM, or ExtemTM) or other polyimides tend to work particularly well, although a variety of other plastics may be used as well.

30 [0053] It should be appreciated that the described arrangement provides a compact optical coupler structure that allows an optical fiber to be side inserted into the optoelectronic coupler in a manner such that its longitudinal axis substantially parallel to

the plane of the face of the photonic device. Stated another way, the longitudinal axis of the fiber channel, and thus the optical fiber extends in parallel with the surface (i.e., the bottom surface of the bottom substrate) that the photonic and integrated circuit devices are mounted on. This provides a low profile structure for optically coupling the photonic
5 device to the optical fiber.

[0054] The various embodiments may be formed using wafer level processes. Although specific sequences of steps have been described, it should be appreciated that in many instances the order of the steps may be varied and some steps eliminated and others added without departing from spirit of the invention. Therefore, the present embodiments
10 should be considered illustrative and not restrictive and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

WHAT IS CLAIMED IS:

1. An optoelectronic device comprising:
 - a first substrate including a reflector and a first surface having a first channel recess;
 - 5 a second substrate having opposing first and second surfaces, wherein the first surface of the second substrate is bonded to the first surface of the first substrate to form an optical coupler, the first surface of the second substrate having a second channel recess that is generally aligned with the first channel recess and cooperates with the first channel recess to form a fiber channel suitable for receiving an optical fiber;
 - 10 a photonic device mounted on the second surface of the second substrate, the photonic device having at least one photonic element thereon that faces the reflective surface, wherein an optical path is formed between the fiber channel and the photonic element that reflects off of the reflective surface and passes through the second substrate;
 - an integrated circuit device mounted on the second surface of the second
 - 15 substrate; and
 - electrical conductor traces formed on the second substrate, wherein at least some of the traces electrically connect the integrated circuit device to the photonic device.
2. An optoelectronic device comprising:
 - first and second substrates having first surfaces that are bonded together, the first
 - 20 and second substrates each having a channel recess in their first surface, the channel recesses being aligned and arranged to cooperate to define a channel suitable for receiving an optical transmission medium, the second substrate further including a second surface that is generally opposite the first surface of the second substrate;
 - a reflective surface on the first substrate; and
 - 25 a photonic device mounted on the second surface of the second substrate, the photonic device having at least one photonic element thereon that faces the reflective surface, wherein an optical path is formed between the channel and the photonic element that reflects off of the reflective surface and passes through the second substrate.
3. An optoelectronic device comprising:
 - 30 an optical fiber coupler formed from a pair of bonded substrates, the coupler being arranged to receive and align a first end of an inserted optical fiber, wherein the optical fiber has a longitudinal axis that extends substantially in parallel with a mounting surface of the coupler;

a photonic device mounted on the mounting surface, the photonic device including a photonic element that faces the mounting surface;

a mirror for redirecting light between the optical fiber and the photonic element, the mirror being formed on a first one of the substrates; and

5 wherein the mounting surface is an external surface of a second one of the substrates and the optical fiber is received in a fiber channel formed at least in part by a channel recess formed in a surface of the first substrate that is bonded to the second substrate.

4. An optoelectronic device as recited in any of the preceding claims further
10 comprising:

a multiplicity of I/O pads formed on the second surface of the second substrate, wherein at least some of the I/O pads are electrically connected to the integrated circuit device by associated electrical conductor traces; and

a multiplicity of solder bumps attached to I/O pads to facilitate electrical
15 connection of the optoelectronic device to an external device.

5. An optoelectronic device as recited in any of the preceding claims wherein:

the first surface of the first substrate and the first and second surfaces of the second substrate are generally parallel; and

the reflector is formed in a reflector recess formed in the first surface of the first
20 substrate that is contiguous with the first channel recess.

6. An optoelectronic device as recited in any of the preceding claims wherein the first fiber channel includes a step that serves as an alignment stop for an optical fiber and the optical fiber is arranged to register against the step.

7. An optoelectronic device as recited in any of the preceding claims further
25 comprising an optical fiber received by the fiber channel.

8. An optoelectronic device as recited in any of the preceding claims wherein the first surfaces of the first and second substrates each include a plurality of aligned channel recesses that cooperate to form a plurality of distinct fiber channels each suitable for receiving an optical fiber.

9. An optoelectronic device as recited in any of claims 1-7 wherein the fiber channel
30 is arranged to receive a plurality of optical fibers.

10. An optoelectronic device as recited in any of the preceding claims further comprising a plurality of optical fibers, wherein the photonic device includes a plurality

of photonic elements, there being an optical path between each photonic element and an associated one of the optical fibers.

11. An optoelectronic device as recited in any of claims 1-8 further comprising a plurality of optical fibers and wherein a plurality of photonic devices are mounted on the second substrate, each photonic device including at least one photonic element, there being an optical path between each photonic element and an associated one of the optical fibers.

12. An optoelectronic device as recited in any of the preceding claims wherein the second substrate is formed from an optically transparent material and the optical path passes directly through the optically transparent material.

13. An optoelectronic device as recited in any of the preceding claims wherein the first and second substrates are formed from materials selected from group consisting of glass, plastic and silicon.

14. An optoelectronic device as recited in claim 12 wherein the second substrate is formed from a plastic material and includes an integrally molded lens formed on the first surface of the second substrate in the optical path between the photonic element and the reflector.

15. An optoelectronic device as recited in any of claim 1-11 wherein the first and second substrates are formed from silicon and the substrates are ionically bonded together and the second wafer has a via formed therethrough that provides a portion of the optical path between the photonic element and the reflector.

16. An optoelectronic device as recited in any of the preceding claims wherein the reflector is formed on a tapered surface that is angled at approximately 45 degrees relative to an axis of the optical path between the photonic element and the reflector such that light passing between the photonic element and the fiber channel is redirected approximately 90 degrees by the reflector.

17. An optoelectronic device as recited in any of the preceding claims wherein a longitudinal axis of the fiber channel extends in a plane that is substantially parallel to the second surface of the second substrate.

18. An optoelectronic device as recited in any of the preceding claims wherein the mirror is located at an internal end of the recess in the first channel.

19. A method of forming optoelectronic devices, the method comprising:

providing a first substrate having a multiplicity of device areas defined therein, each device area of the first substrate including a recessed region and a reflective surface formed on a wall of the recessed region;

5 providing a second substrate having a multiplicity of device areas that generally correspond to the device areas of the first substrate;

bonding the second substrate to the first substrate such that the recessed regions on the first substrate face a first surface of the second substrate, whereby the bonded substrates have a multiplicity of device areas corresponding to the device areas of the first and second substrates;

10 attaching a multiplicity of photonic devices to a second surface of the second substrate located generally opposite the first surface of the second substrate such that each device area of the second substrate includes a photonic device, each device area in the second substrate further including an optical path through the second substrate arranged such that after the substrate bonding and photonic device attachment have been completed, the photonic devices may optically communicate with the mirrors in their associated device areas through the second substrate; and

15 singulating the bonded first and second substrates to form a multiplicity of singulated optoelectronic devices, each optoelectronic device corresponding to an associated device area on the bonded substrates, each singulated optoelectronic device having a channel suitable for receiving at least one optical fiber that extends between the first and second substrates and is defined at least in part by the corresponding recessed region in the first substrate.

20. A wafer level method of forming optoelectronic devices, the method comprising:

25 bonding a first surface of a first wafer substrate having a multiplicity of device areas defined therein, to a first surface of a second wafer substrate having a corresponding multiplicity of device areas, wherein each device area of the first substrate includes a recessed region and a reflective surface formed on a wall of the recessed region and each device area;

30 attaching a multiplicity of photonic devices to a second surface of the second substrate located generally opposite the first surface of the second substrate such that each device area of the second substrate includes a photonic device, each device area in the second substrate further including an optical path through the second substrate arranged

such that after the substrate bonding and photonic device attachment have been completed, the photonic devices may optically communicate with the mirrors in their associated device areas through the second substrate; and

5 singulating the bonded first and second substrates to form a multiplicity of singulated optoelectronic devices, each optoelectronic device corresponding to an associated device area on the bonded substrates, each singulated optoelectronic device having a channel suitable for receiving at least one optical fiber that extends between the first and second substrates and is defined at least in part by the corresponding recessed region in the first substrate.

10 21. A method as recited in claim 19 or 20, wherein the second substrate further includes a plurality of recessed regions and the channels formed in the singulated optoelectronic devices are also defined in part by the corresponding recessed regions in the second substrate.

22. A method as recited in claim 21, wherein:

15 each recess in the first substrate includes a step such that each recess in the first substrate includes a deeper portion and a shallower portion and wherein the shallower portion includes the reflective surface;

each recess in the second substrate includes a side wall that is aligned with the step when the first and second substrates are bonded; and

20 the step and side wall cooperate to serve as an alignment stop for an optical fiber received by the channel after singulation.

23. A method as recited in any of claims 19 - 22, wherein each recess in the first substrate includes a step such that each recess in the first substrate includes a deeper portion and a shallower portion, wherein the shallower portion includes the reflective surface, and wherein the step is suitable for serving as an alignment stop for an optical fiber received by the channel after singulation.

24. A method as recited in any of claims 19 - 23, wherein the second surface of the second substrate has a plurality of conductive traces formed on each device area of the second substrate, the method further comprising attaching a plurality of dice to the second surface of the second substrate prior to singulation such that each device area of the second substrate includes a die capable of electrical communication with the photonic device associated with the device area over at least one of the conductive traces associated with the device area.

25. A method as recited in claim 24, further comprising attaching a plurality of solder bumps to the second surface of the second substrate prior to singulation, wherein at least some of the conductive traces associated with each device area electrically couple the die associated with the device area to solder bumps associated with the device area to facilitate attachment of the associated optoelectronic device to an external device after singulation.

26. A method as recited in any of claims 19-25, wherein the first and second substrates are each wafers formed from the group consisting of glass, plastic and silicon.

27. A method as recited in any of claims 19-25, wherein the first and second substrates are substantially formed from a glass or plastic material that is transparent or semi-transparent to wavelengths of light in an intended operational range of the optoelectronic devices.

28. A method as recited in any of claims 19-25, wherein:
the first and second substrates are each wafers are formed substantially from silicon;

the wafers bonding is accomplished by ionic bonding; and

the second wafer has a plurality of vias formed therein, each via being formed in an associated device area to provide the optical path between the photonic device and the mirror associated with the device area.

29. A method as recited in any of claims 19-28, wherein the substrates are bonded together by soldering.

30. A method as recited in any of claims 19-29, further comprising a plurality of lenses formed on the second substrate, each lens being associated with an associated device area and positioned such that after bonding and singulation, light passing between a photonic element on the associated photonic device and the associated reflective surface pass through the lens.

31. A method as recited in any of claims 19-30, wherein each device area includes a plurality of photonic devices.

32. A method as recited in any of claims 19-31, further comprising, for each of a plurality of the singulated optoelectronic devices:

inserting an optical fiber optic into the channel of such that an end of the optical fiber registers against an alignment stop associated with the channel; and

wherein the photonic device is arranged to optically communicate with the optical fiber via an optical path in which light passes through the second substrate and reflects off of the reflective surface as the light passes between the photonic device and the optical fiber.

- 5 33. A method of assembling an optoelectronic device, the method comprising:
providing an optoelectronic device having a photonic device and a pair of
substrates, wherein the pair of substrates are bonded together and a channel is defined
between the substrates, the channel including a reflective surface formed on a first one of
the substrates and an alignment stop, and wherein the photonic device is mounted on a
10 surface of the second substrate that faces away from the channel, there being an optical
path between the photonic device and reflective surface that passes through the second
substrate; and

inserting an optical fiber into the channel such that an end of the optical registers
against the alignment stop; and

- 15 wherein the photonic device is arranged to optically communicate with the optical
fiber via an optical path in which light passes through the second substrate and reflects off
of the reflective surface as the light passes between the photonic device and the optical
fiber.

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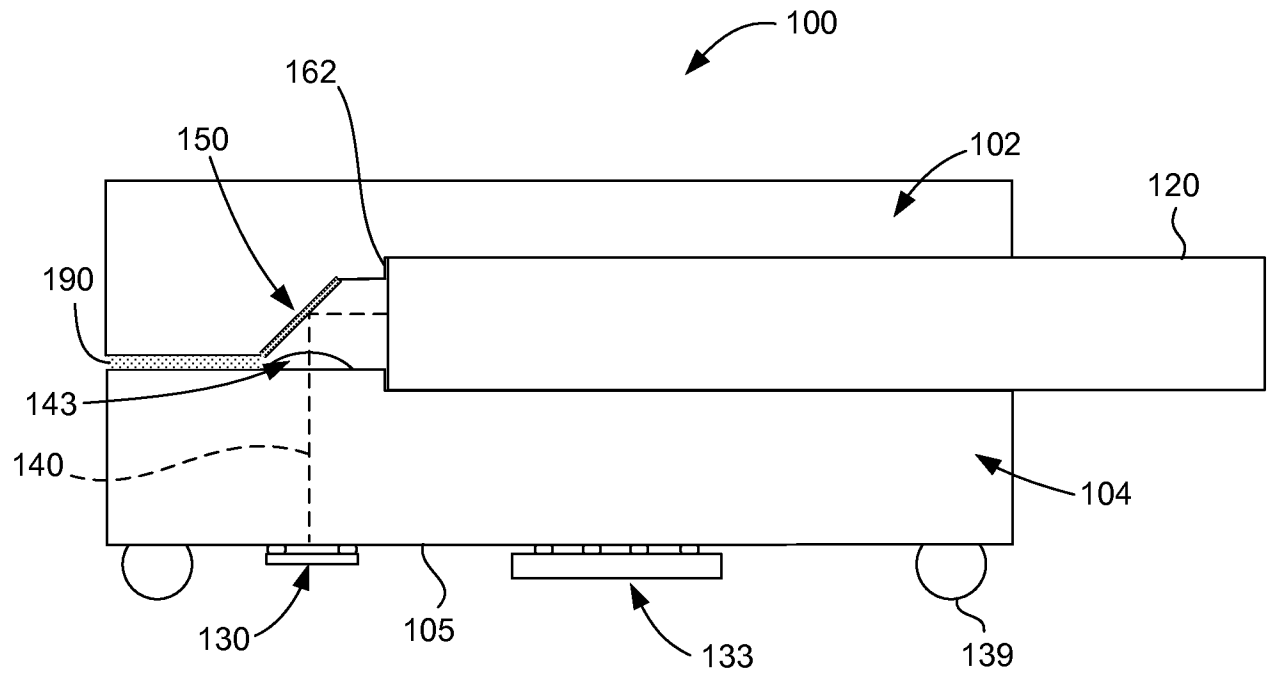


FIG. 1A

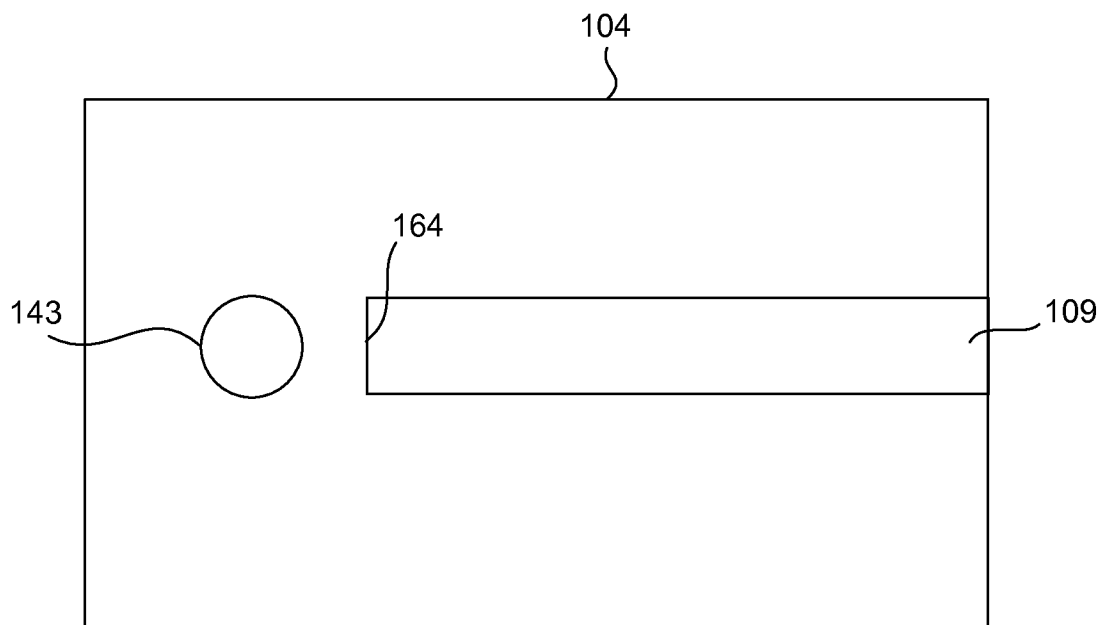


FIG. 1B

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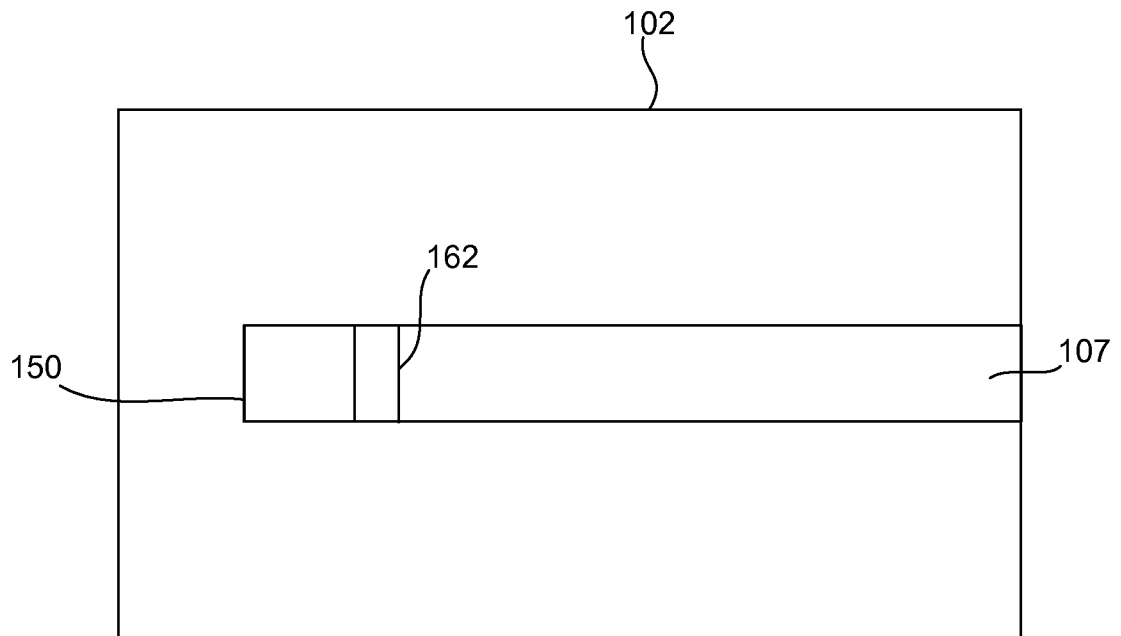


FIG. 1C

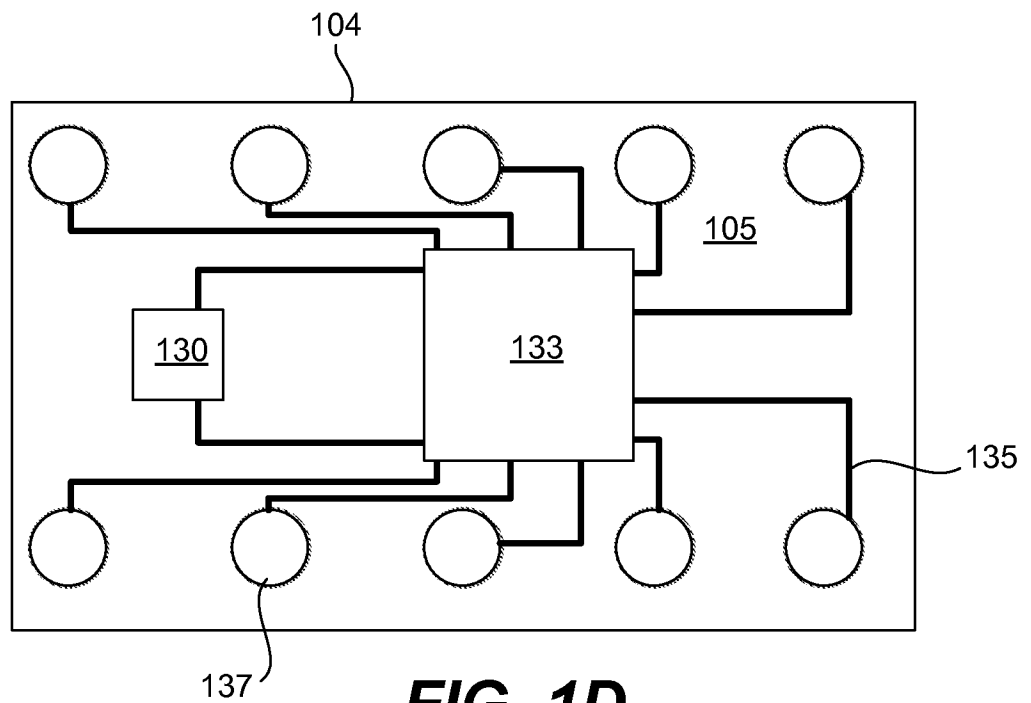
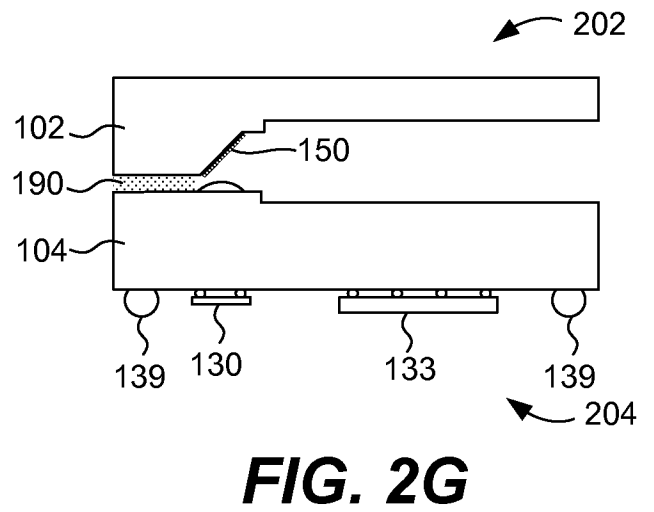
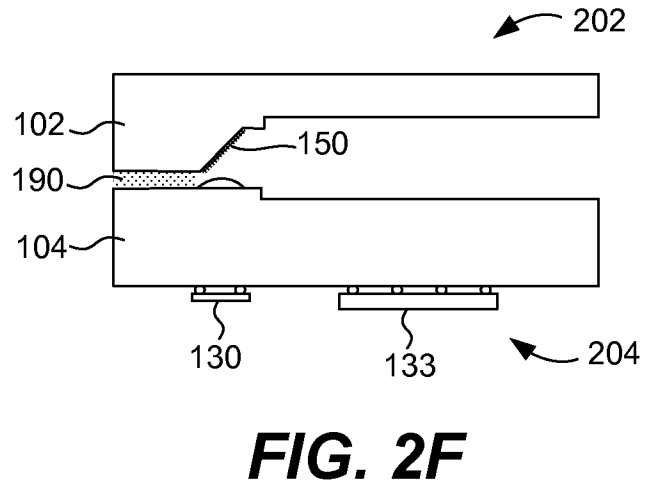
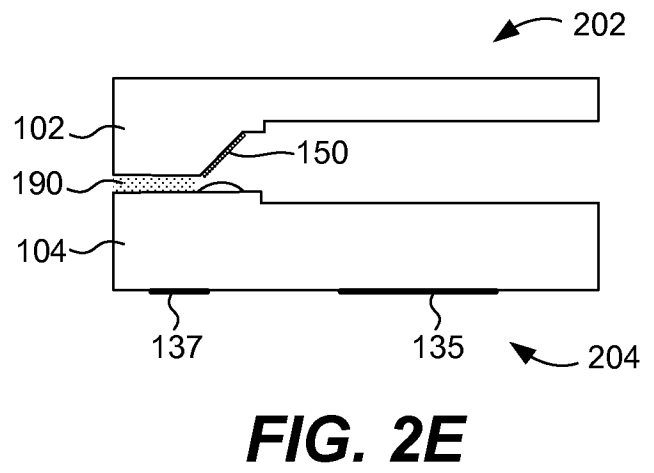
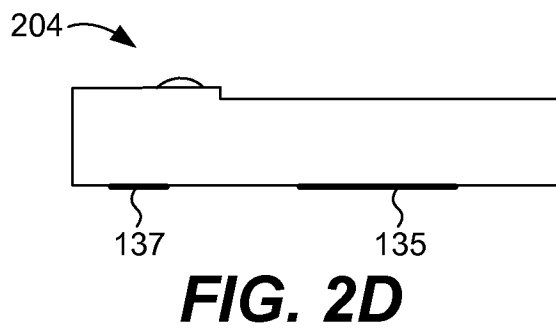
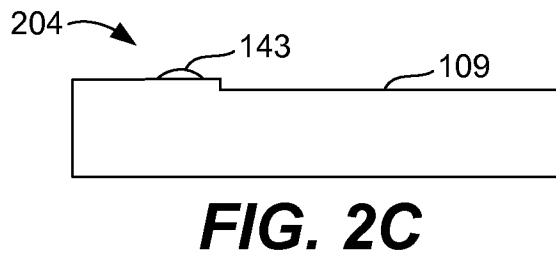
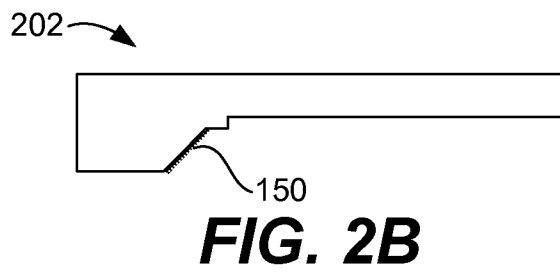
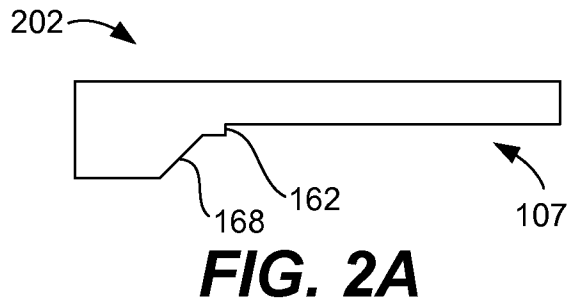
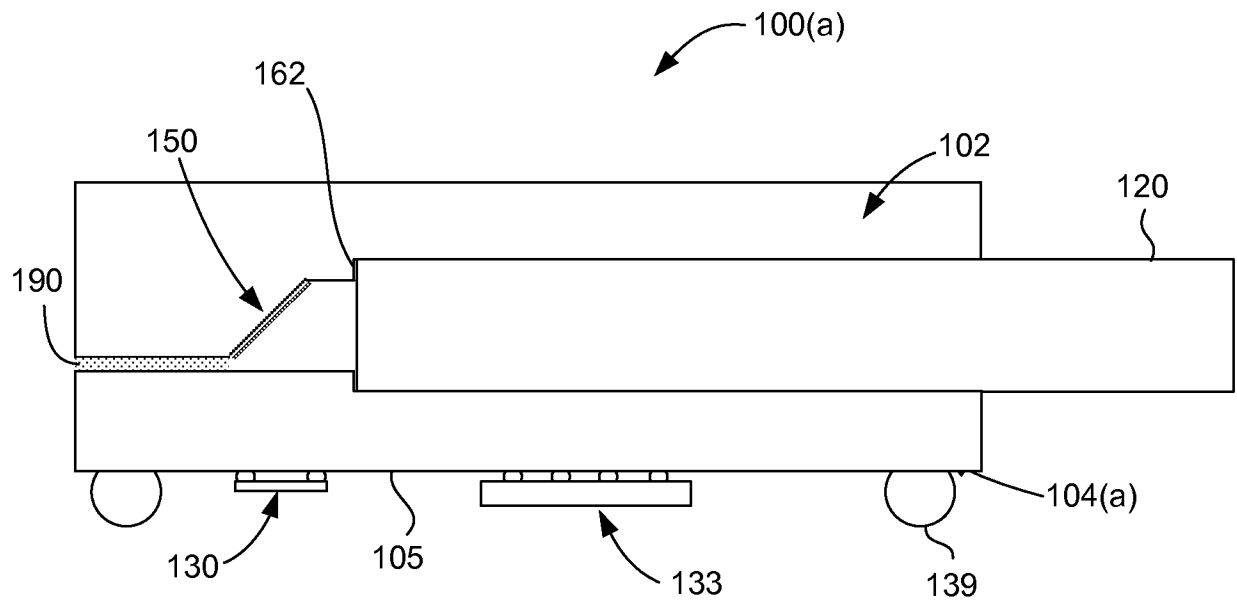
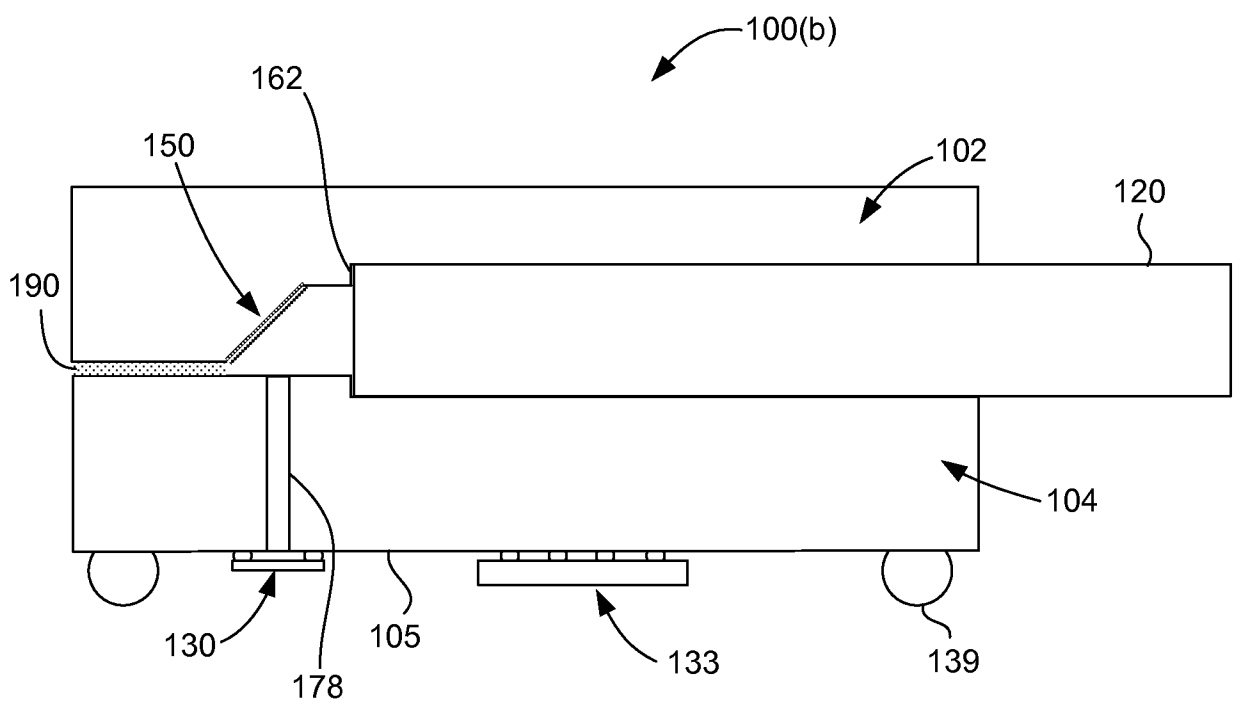
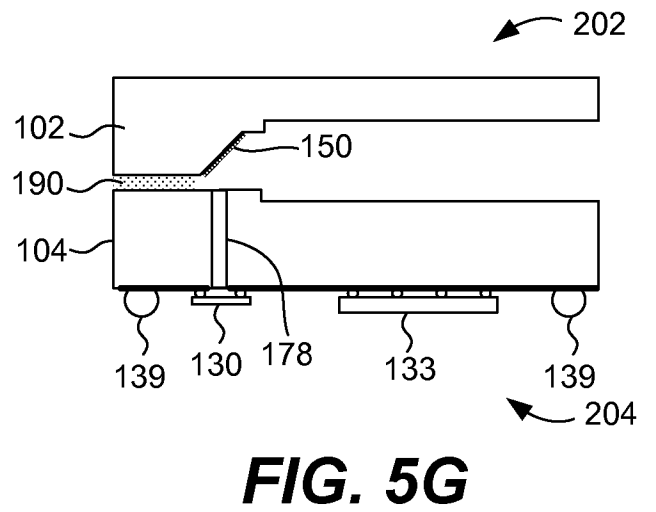
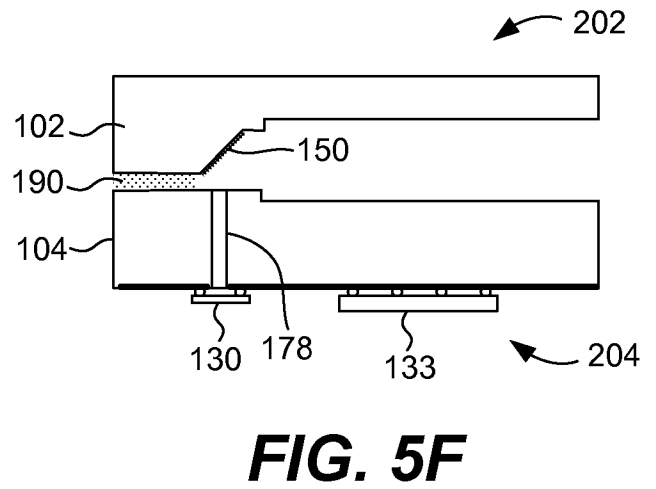
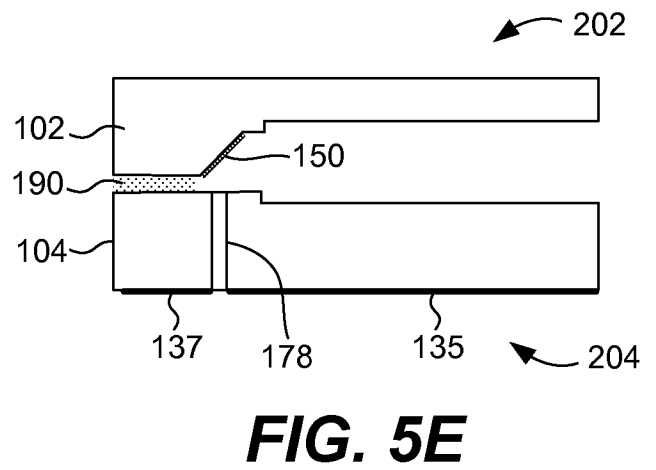
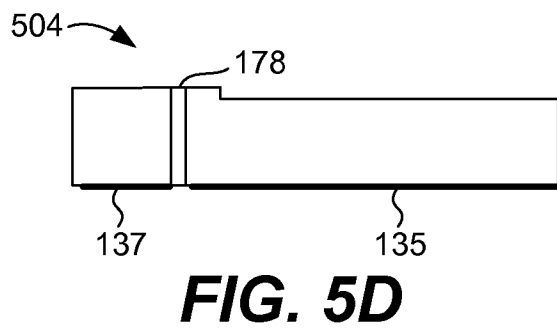
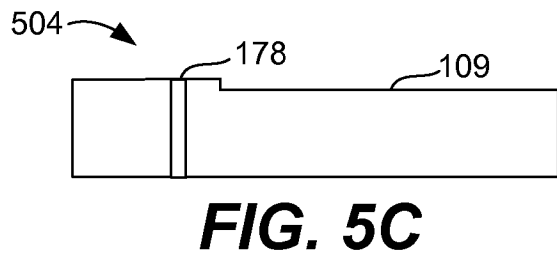
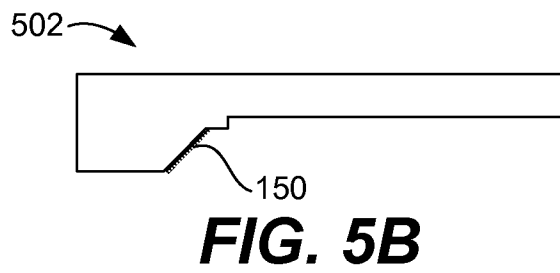
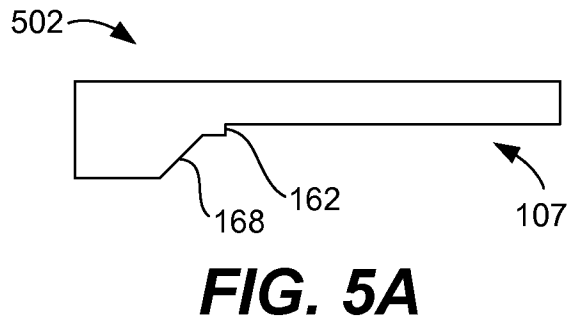


FIG. 1D



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**FIG. 3****FIG. 4**



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/056693**A. CLASSIFICATION OF SUBJECT MATTER****G02B 6/12(2006.01)i, G02B 6/42(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02B 6/12; G02B 27/00; G02B 6/30; G02B 6/32; G02B 6/36; H01L 23/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

(Chinese Patents and application for patent)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:"photoelectronic, nanoscale, semiconductor, cathode, electron, hole, multiplication region, anode, quenching structure, depletion region, ohmic contact, layer, thickness, pillar structure, breakdown voltage, avalanche, charge"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 4945400 A1 (BLONDER; GREG E. et al.) 31 July 1990 see abstract, col.3 line 30 - col. 5 line 31, claims 1-12, figures 1-11.	2 1,3 19-22,33
X Y A	US 7306378 B2 (ALDUINO et al.) 11 December 2007 see abstract, col.2 line 3 - col.6 line 52, claims 1-13, figures 1-5.	2 1,3 19-22,33
A	US 5369529 A1 (KUO; SHUN-MEEN et al.) 29 November 1994 see abstract, col.2 line 34 - col.6 line 38, claims 1-20, figures 1-2.	1-3, 19-22, 33



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 APRIL 2010 (06.04.2010)

Date of mailing of the international search report

16 APRIL 2010 (16.04.2010)

Name and mailing address of the ISA/KR

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Facsimile No. 82-42-472-7140

Authorized officer

KIM, Sung Hoon

Telephone No. 82-42-481-8505



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2009/056693**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 25
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claim 25 depend on the unsearchable claim 24 does not comply with Rule 6.4(a)
3. ☒ Claims Nos.: 4-18,23-24,26-32
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2009/056693

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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