United States Patent

[11] 3,631,387

[72] Inventors **Frank W. Hill**
Moline;
Joseph E. Meschi, Lyon, both of Ill.; Peter G. Bartlett, Davenport, Iowa

[21] Appl. No. **827,083**
[22] Filed **Apr. 1, 1969**
[45] Patented **Dec. 28, 1971**

[73] Assignee **Gulf & Western Industries**
New York, N.Y.

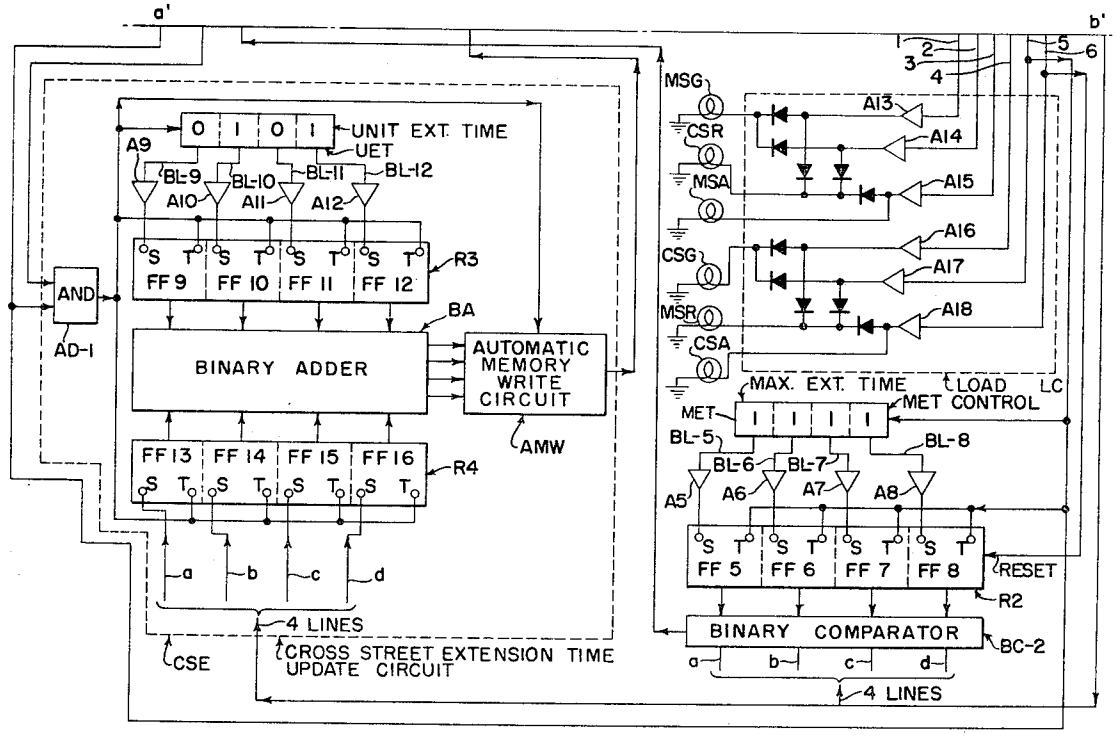
[54] **UNIT EXTENSION CIRCUIT MEANS FOR TRAFFIC CONTROL SYSTEM**
20 Claims, 11 Drawing Figs.

[52] **U.S. Cl.** **340/37,** 340/36
[51] **Int. Cl.** **G08g 1/08**
[50] **Field of Search** ..... 340/37, 31 R, 31 A, 36

[56] **References Cited**
UNITED STATES PATENTS
3,376,546 4/1968 Cress, Jr. et al. 340/37

Primary Examiner—Kathleen H. Claffy
Assistant Examiner—Randall P. Myers
Attorney—Meyer, Tilberry and Body

ABSTRACT: An activated traffic control system is disclosed herein for controlling the time duration that a traffic signal displays a go signal to at least one traffic lane in accordance with traffic demand. The system includes a go extension interval memory and an extension interval control circuit for acting upon the memory to change the time duration of the go extension interval. The system also includes a plurality of traffic interval time storage memories which are electrically alterable and electrically interrogatable for storing binary signals having corresponding values representative of the desired time durations of the associated traffic intervals.



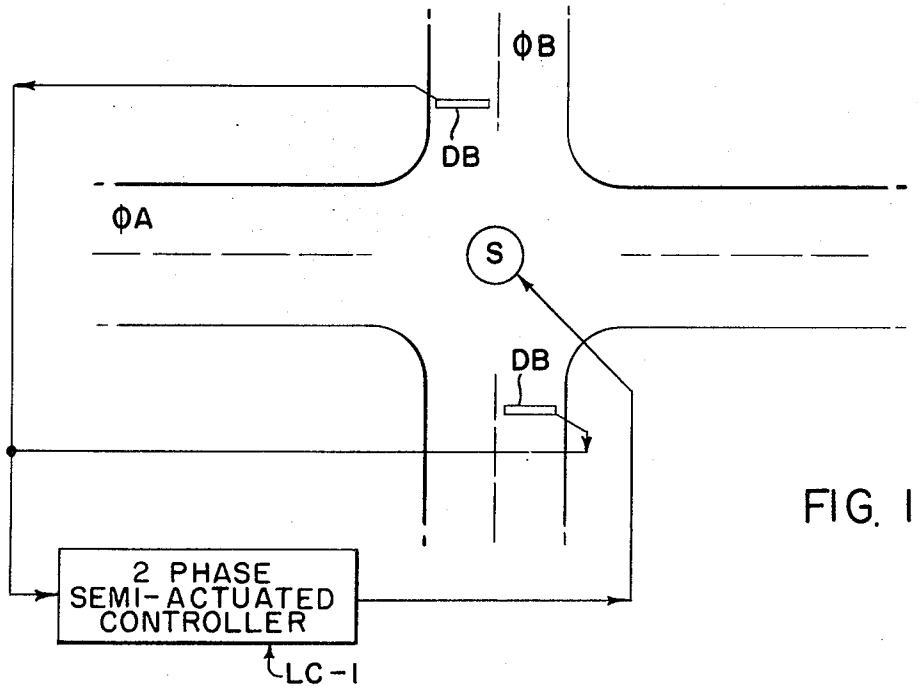


FIG. 1

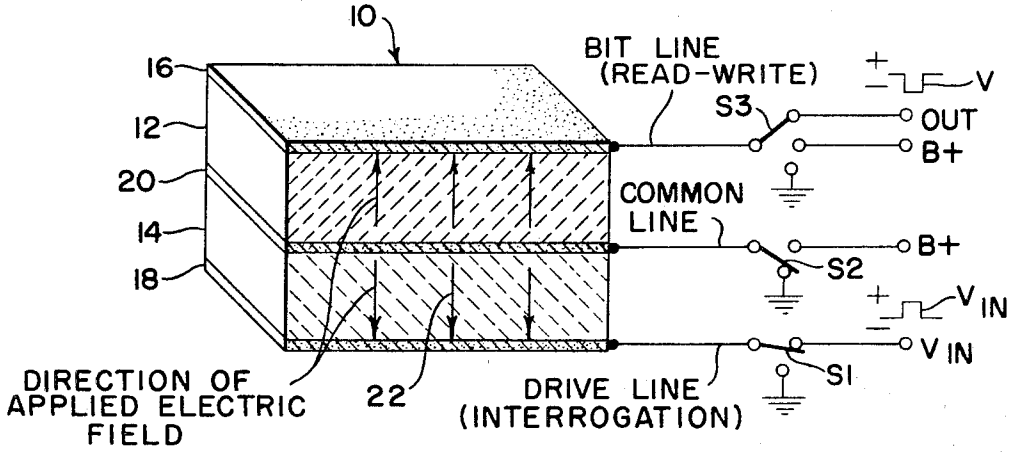


FIG. 2

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

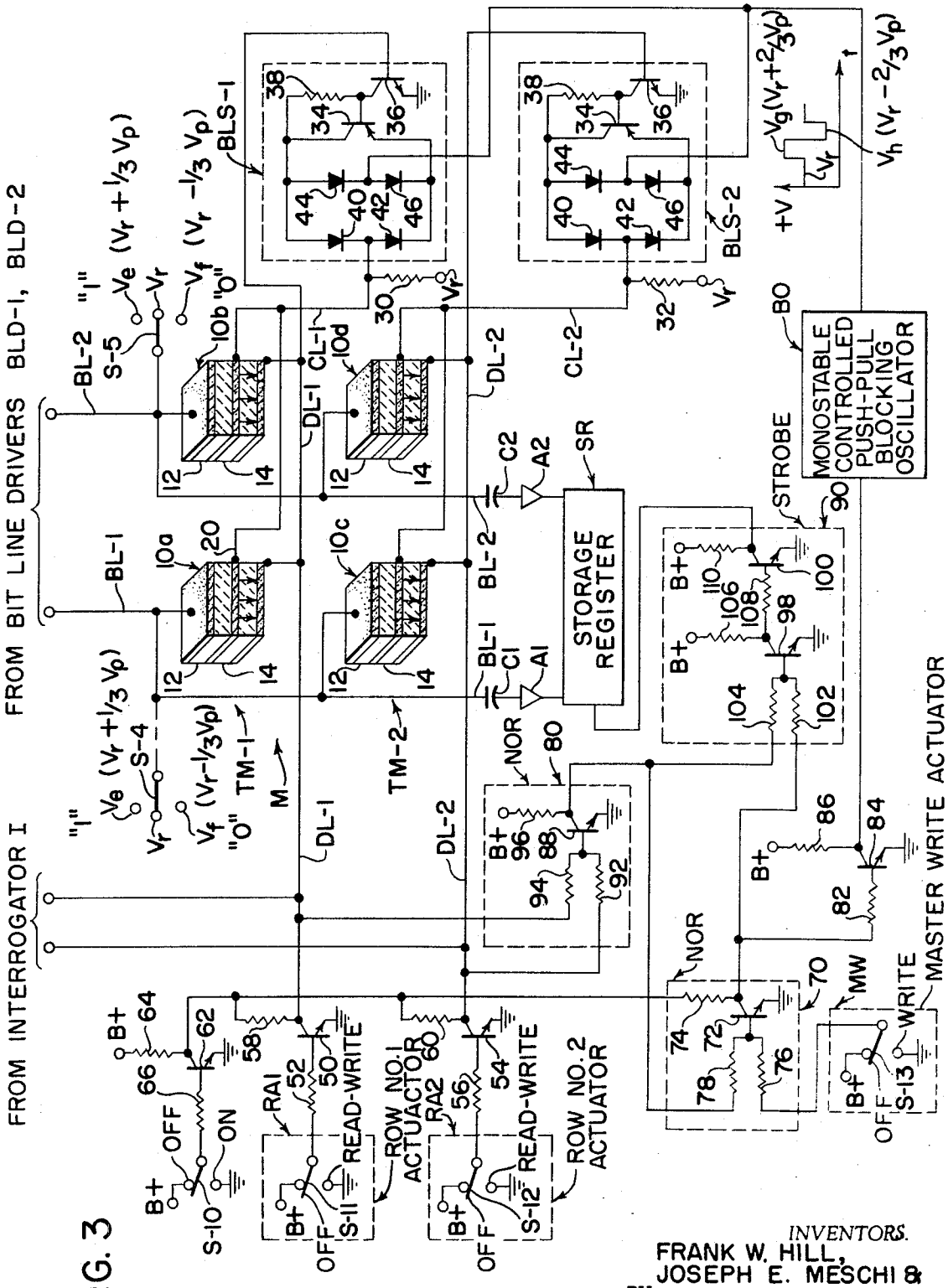


FIG. 3

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

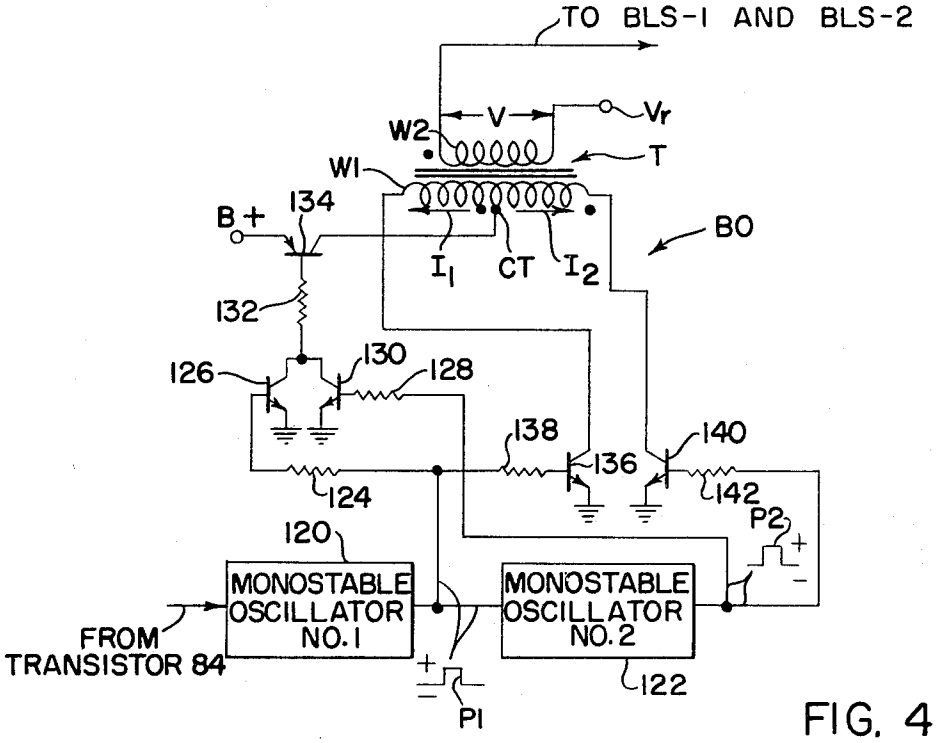


FIG. 4

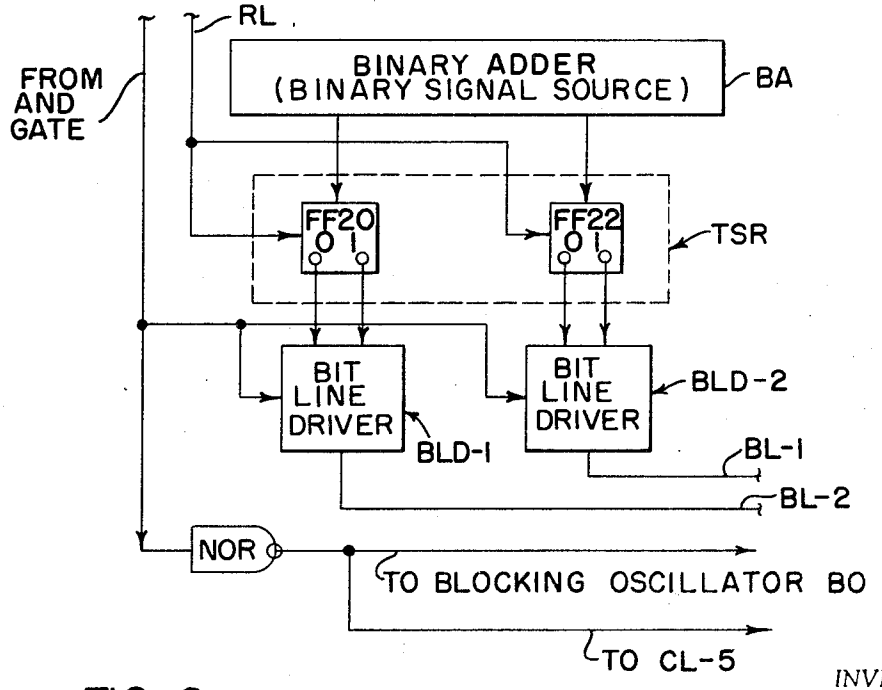


FIG. 6

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

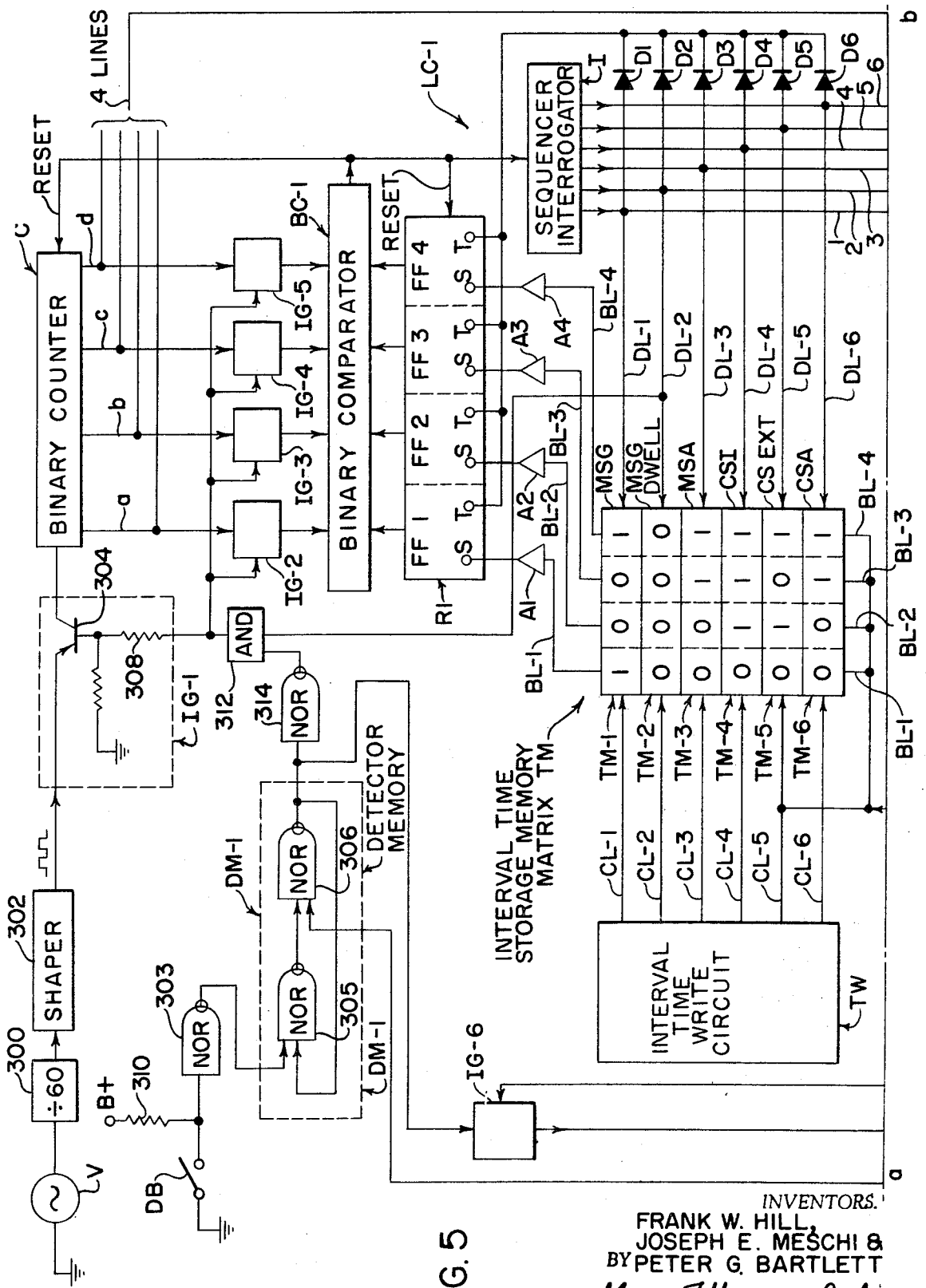


FIG. 5

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

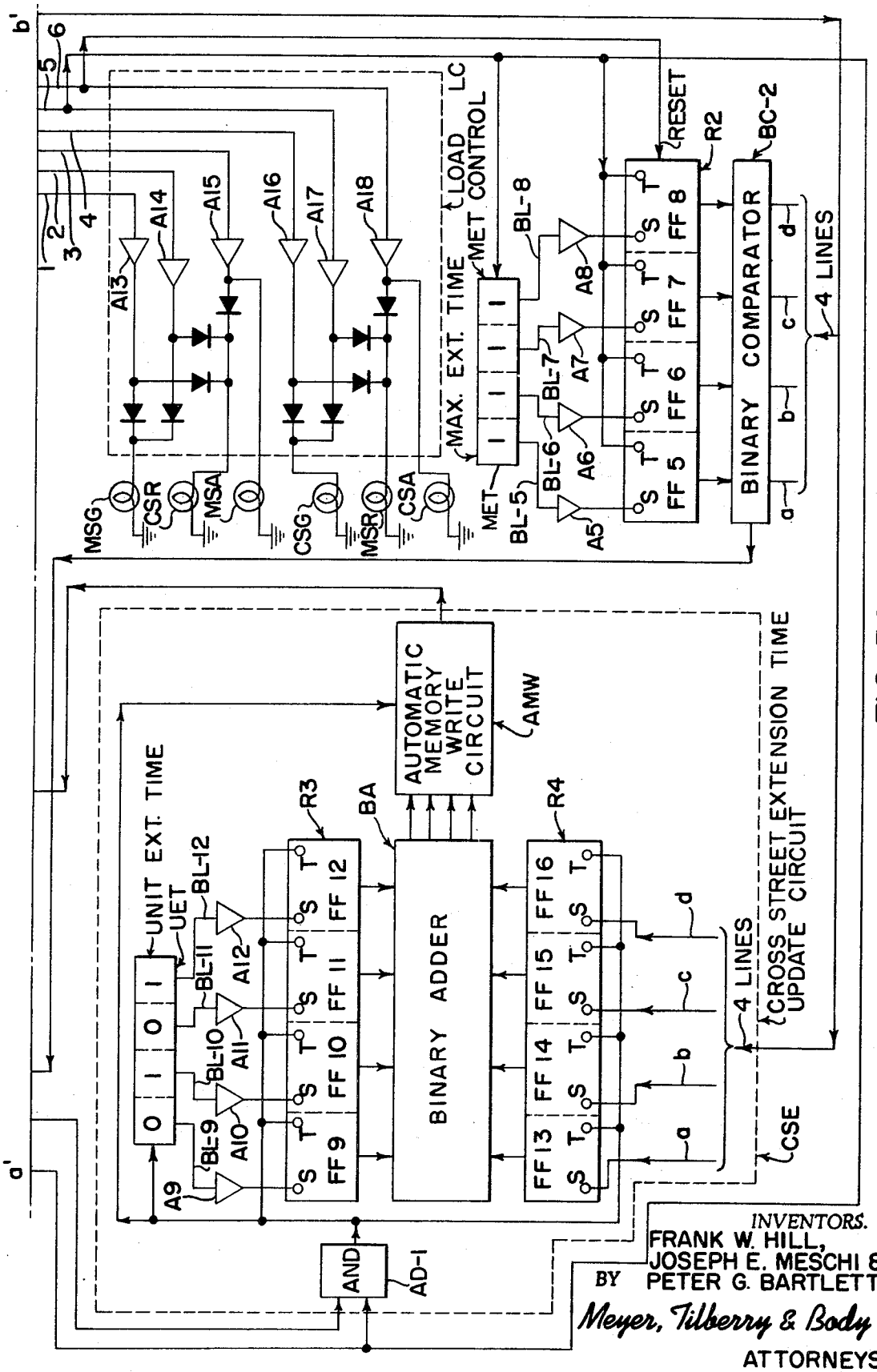


FIG. 5A

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
PETER G. BARTLETT
BY
Meyer, Tilberry & Body
ATTORNEYS

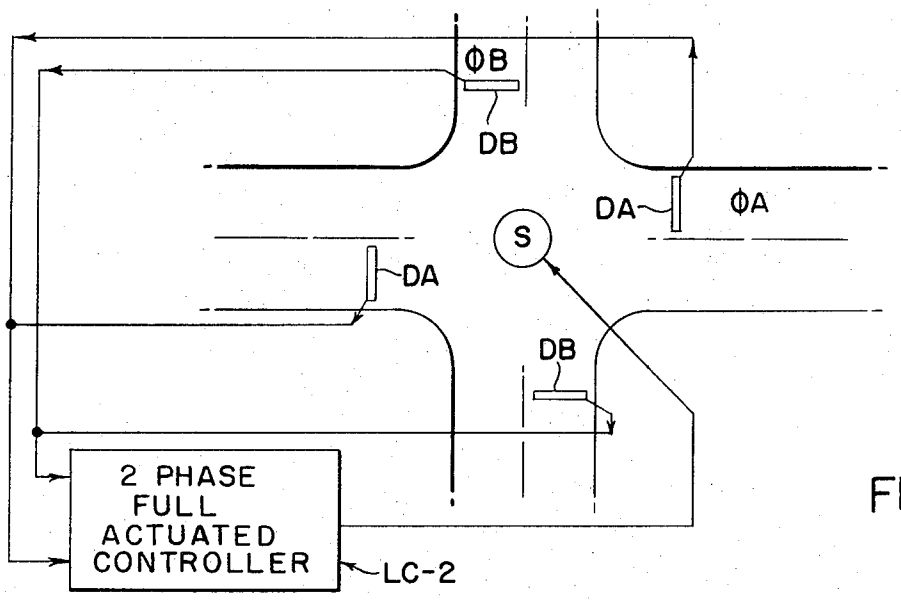


FIG. 8

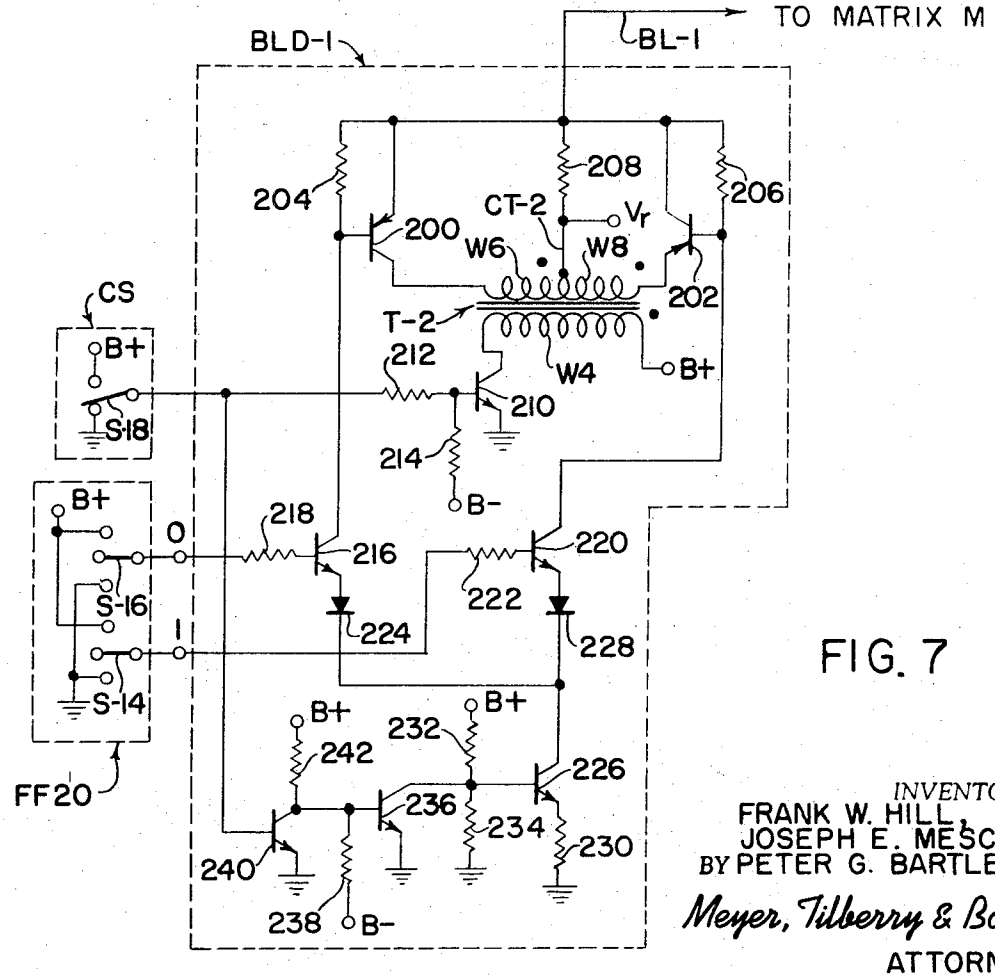
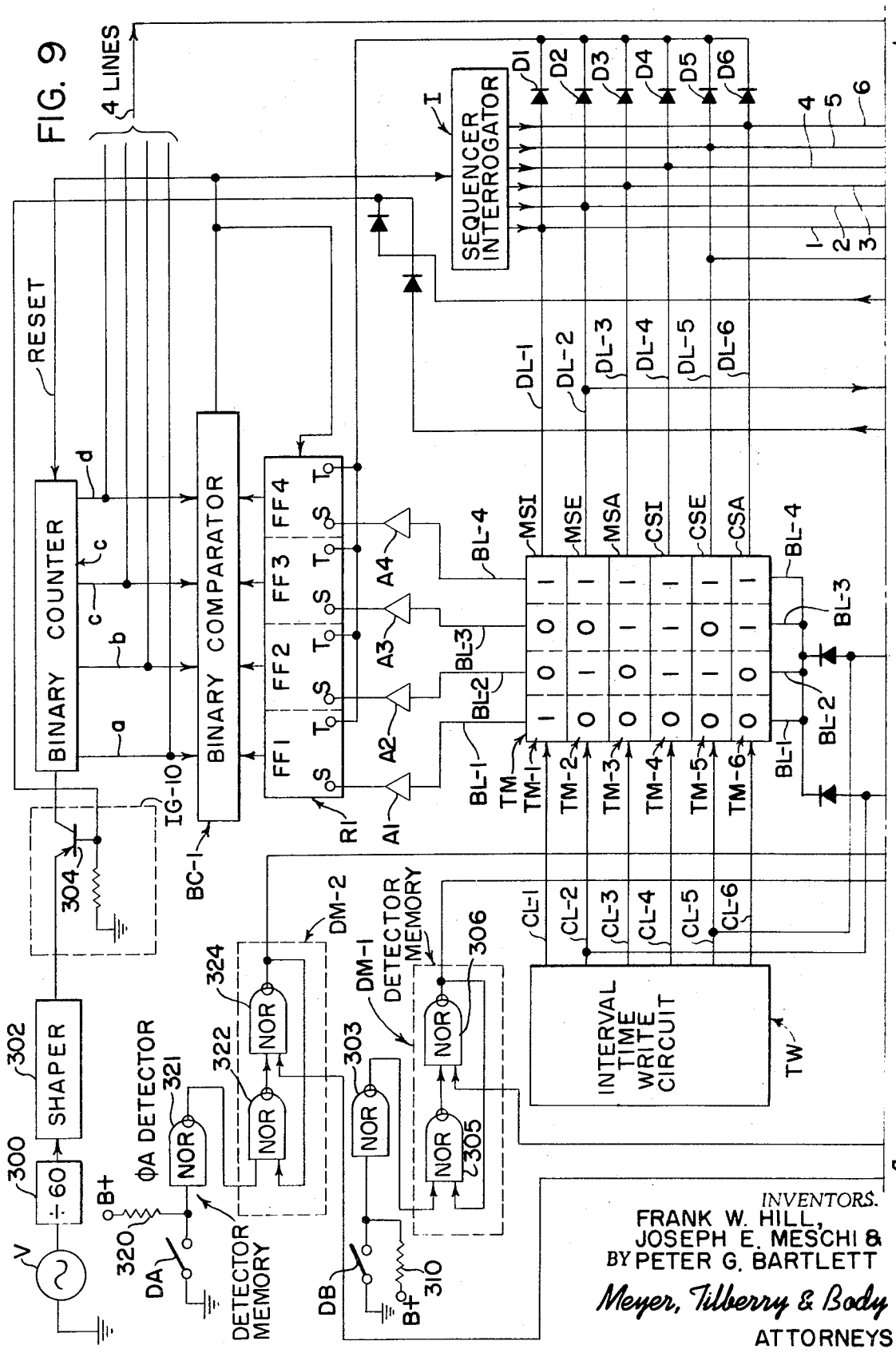


FIG. 7

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

FIG. 9



INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

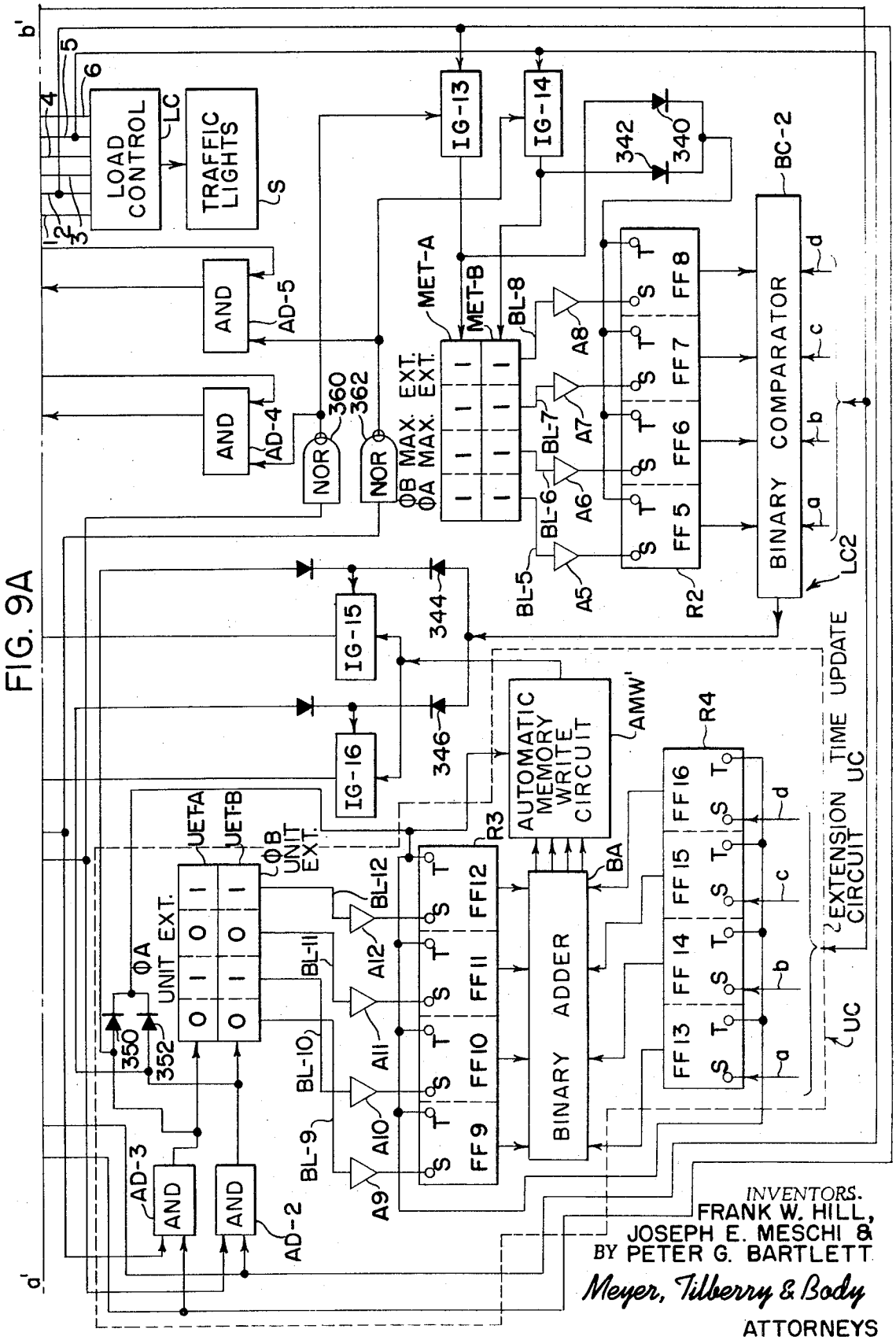


FIG. 9A

INVENTORS.
FRANK W. HILL,
JOSEPH E. MESCHI &
BY PETER G. BARTLETT
Meyer, Tilberry & Body
ATTORNEYS

UNIT EXTENSION CIRCUIT MEANS FOR TRAFFIC CONTROL SYSTEM

This invention relates to the art of traffic control and, more particularly, to controlling traffic flow in accordance with the traffic demand as registered with a traffic controller by associated traffic detectors.

The invention is particularly applicable as used in conjunction for a semiactuated or full actuated controller for two or more conflicting traffic lanes, requiring two or more phases or movements of traffic in the operation of the controller and will be described with particular reference thereto; although, it is to be appreciated that the invention has broader applications, such as an addition to an already existing traffic controller, or system, or a replacement for a portion of the circuitry of an existing traffic controller, or system.

Traffic actuated controllers, as distinguished from pretimed controllers, control traffic signal lights to display go, caution, and stop signals to traffic in the lanes controlled in accordance with traffic demand as registered with the controllers by traffic detectors associated with the conflicting lanes. A semiactuated controller has a detector associated with at least one lane, but not all lanes, associated with the controller. A full actuated controller has a detector associated with all lanes controlled by the controller.

Traffic actuated controllers known in the prior art frequently include circuitry to provide a minimum initial period of go time followed by a unit extension interval for each vehicle detected in the traffic actuatable phase after the minimum initial period of time has been terminated. Circuitry may also be provided to limit the unit extension intervals to a maximum time duration. The circuitry used thus far for these purposes includes, for example, an RC timer with a potentiometer being set for a given time duration, such as for the minimum initial or maximum time periods. A fixed time, resettable RC timer, which is reset for each traffic detection, may be used for the unit extension timer. The foregoing circuits are analog and, hence, their timing accuracy is subject to variations with changes in temperature. Also, these circuits are not readily adjustable to provide for interval timing changes during operation.

The present invention is directed toward an improved traffic actuated traffic control system which controls traffic flow in accordance with traffic demand without using prior art analog timing circuits, as described, and whereby readily adjustment may be made of interval timings.

In one form, the present invention contemplates the provision of a traffic control system for controlling the time duration that a traffic signal light displays a go signal in at least one traffic lane, and having unit extension circuit means for extending the time duration that the go signal is displayed to that phase in dependence upon traffic detected in that phase by a vehicle detector means.

In accordance with this form of the invention there is provided an improvement in the unit extension circuit means which comprises: binary signal storage go extension memory means for storing binary signals wherein the decimal equivalent of the binary content of the stored binary signals is representative of the time duration of a go extension interval; a source of trigger pulses; means for providing an output signal, representative of the termination of the go extension interval, when the decimal number of the trigger pulses is equal to the decimal equivalent of the stored binary signals; and, extension interval control means for acting upon the go extension memory means to change the pattern of binary signals stored therein and thereby vary the time duration of the go extension interval.

In accordance with another aspect of the present invention, the improvement in the unit extension circuit means includes: a binary signal storage go extension memory means for storing a binary signal consisting of binary digits wherein the content of the stored binary signal digits is representative of the time duration of the go extension interval; a source of trigger pulses; binary counting means for counting the trigger pulses and providing binary signals which changes in accordance with the number of trigger pulses counted; means coupled to the binary counting means and the go extension memory means for providing an output signal, representative of the termination of the go extension interval, when the value of the two sets of binary signals is the same; and, extension interval control means including circuit means adapted to be coupled to a traffic detector means for acting upon the go extension memory means to change the binary signals stored thereby in dependence upon traffic detected by the detector means and thereby change the time duration of the go extension interval.

In accordance with another aspect of the present invention, there is provided a traffic actuated traffic controller for controlling the time duration that a traffic signal displays a go signal in each of at least two traffic lanes wherein the controller is actuatable by traffic in at least one lane which has means associated therewith for registering detected traffic in that lane with the controller, and comprising: a plurality of traffic interval time storage memories wherein each said memory includes a plurality of electrically alterable and electrically interrogatable bistable memory means each for storing a binary "1" or binary "0" signal so that the binary content of a memory is representative of a desired time duration for an associated traffic interval, with each memory means having an input for receiving an interrogation signal and an output for carrying the binary signal in response to receipt of an interrogation signal; interrogating means for sequentially applying interrogation signals to the plurality of memories so that when any one memory is interrogated the outputs of its plurality of its memory means provides a set of binary signals; a source of equitime-spaced trigger pulses; means for actuating the interrogating means to interrogate the next succeeding of the plurality of memories when a decimal number of the trigger pulses received is equal to the decimal equivalent of binary signals on the outputs of the memory means of the memory last interrogated; each traffic lane having associated therewith at least one memory serving as a go initial time storage memory and each the lane for which the controller is actuatable also having associated therewith another memory serving as a go extension time storage memory; and, extension interval control means including circuit means adapted to be coupled to a traffic detector means associated with such lane for electrically altering the go extension memory means to change the pattern of binary signals stored thereby in dependence upon traffic detected by the detector means and thereby change the time duration of the go extension interval.

The primary object of the present invention is to provide an improved traffic actuated traffic control system having improved digital timing circuits and which system is relatively inexpensive to manufacture and is relatively economical to operate.

Another object of the present invention is to provide an improved traffic actuated traffic control system having electrically alterable and electrically interrogatable interval time storage memories.

Another object of the present invention is to provide a traffic actuated traffic control system having interval time storage memories which incorporate ferroelectric storage capacitors.

A still further object of the present invention is to provide a traffic control system having an improved unit extension circuit means which includes electrically alterable time storage memory means.

A still further object of the present invention is to provide an improved unit extension circuit means having a time storage memory wherein the stored information may be changed in dependence upon traffic detections.

A still further object of the present invention is to provide an electrically interrogatable maximum interval time storage memory for use in limiting the total time duration of a go extension interval.

These and other objects and advantages of the invention will become apparent from the following description of the preferred embodiments of the invention as read in connection with the accompanying drawings in which:

FIG. 1 is a schematic illustration of one application of the invention to a semiactuated traffic control system;

FIG. 2 is a schematic illustration of a single bit ceramic memory;

FIG. 3 is a combined block diagram, schematic illustration of a ceramic memory matrix and associated circuitry;

FIG. 4 is a schematic illustration of the blocking oscillator used in FIG. 3;

FIG. 5 and 5A constitute a single drawing of a combined block diagram schematic illustration of a two-phase semiactuated traffic controller constructed in accordance with the present invention;

FIG. 6 is a block diagram illustration of the automatic write circuitry for FIG. 5;

FIG. 7 is a schematic illustration of a portion of the automatic write circuitry;

FIG. 8 is a schematic illustration of another application of the invention to a full actuated traffic control system; and,

FIGS. 9 and 9A constitute a single drawing of a combined block diagram schematic illustration of a two-phase full actuated traffic controller constructed in accordance with the present invention.

Referring now to the drawings, wherein the showings are for purposes of illustrating the preferred embodiments of the invention, and not for purposes of limiting same, FIG. 1 illustrates one embodiment of the invention in the form of a two-phase, semiactuated traffic controller LC–1. This controller serves to control traffic signal S which displays go and caution signals to main street, phase A, and to cross street, phase B.

BACKGROUND DISCUSSION

Before describing the preferred embodiments of the invention, attention is directed toward the following description of a single bit memory device constructed in accordance with the teachings of U.S. Pat. application, Ser. No. 527,223. As shown in FIG. 2, that structure includes a single bit ceramic memory device **10**, which generally comprises a memory plate **12** constructed of ferroelectric material, such as barium titanate, Rochelle salt, lead metaniobiate or lead titanate zirconate composition, for example. In its preferred form, however, memory plate **12** is constructed of lead titanate zirconate composition since it is easy to polarize. Drive plate **14** is preferably constructed of ferroelectric material having piezoelectric characteristics, such as lead titanate zirconate composition. However, the drive plate may be constructed of any material that will change its dimensions upon application of an electric signal, such as, for example, magnetostrictive material which upon application of current thereto will undergo physical dimension changes. Drive plate **14** is permanently polarized and need not be constructed of easily polarizable material, such as lead titanate zirconate composition.

Plates **12** and **14** are, in their unstressed condition, approximately flat, and are oriented so as to be in substantial superimposed parallel relationship. The upper surface of plate **12** is coated with an electrically conductive layer **16**, and the lower surface of plate **14** is coated with an electrically conductive layer **18**. Layers **16** and **18** may be of any suitable electrically conductive material, such as silver. Interposed between facing surfaces of plates **12** and **14** there is provided a third layer **20** of electrically conductive material. Layer **20** may be constructed of a conductive epoxy, such as epoxy silver solder, so that facing surfaces of plates **12** and **14** are electrically connected together, as well as mechanical secured together. In this manner, as will be described below, when drive plate **14** is stressed it, in turn, transmits mechanical forces to plate **12** so as to mechanically stress plate **12** in directions acting both laterally and perpendicularly of its plane.

Drive plate **14** may be permanently polarized by applying an electric field across its opposing flat surfaces. Thus, as shown in FIG. 2, layer **18** is electrically connected to a single pole, double throw switch S1 which serves to connect layer **18** with either an electrical reference, such as ground, or to an interrogating readout voltage source V_{in}. Similarly, layer **20** is connected with the single pole, double throw switch S2. Switch S2 serves to connect layer **20** with either an electrical reference, such as ground, or to a source of polarizing voltage $+V_p$. Plate **14** may now be polarized by connecting layer **20** with the $+V_p$ voltage and layer **18** to ground potential. Thus, an electrical field of sufficient magnitude to polarize plate **14** is applied across the opposing faces of the plate. The direction of the electric field is indicated by arrows **22**. Thereafter, switches S1 and S2 may be returned to positions as shown in FIG. 1 for a subsequent readout operation.

Binary information may be stored in memory plate **12** by applying an electric field between the opposing faces of the plate in either one of two directions, so that the plate stores either a binary "1" or a binary "0" signal. Layer **16** is connected to a single pole switch S3. Switch S3 serves to connect layer **16** with either a ground potential, or a $+V_p$ source of polarizing potential, or to an output circuit OUT. When it is desired to store a binary "1" signal in memory plate **12**, switches S2 and S3 are manipulated so that $+V_p$ potential is applied to layer **16** and ground potential is applied to layer **20**. As shown in FIG. 2, however, memory plate **12** stores a binary "0" signal, which results from having applied $+V_p$ potential to layer **20** and ground potential to layer **16**.

With switches S1, S2 and S3 in the positions shown in FIG. 1, an interrogating input voltage V_{in} is applied to layer **18**. If the applied voltage V_{in} is of a polarity opposite to the direction of polarization of the drive plate, then the magnitude of this interrogating voltage is kept well below the polarization voltage threshold, i.e., the voltage required to permanently polarize drive plate **14**, so that the readout process is nondestructive. Application of the readout voltage pulse causes the drive plate to contract or expand in the direction dependent on its prepolarization, as well as the polarity of the applied readout voltage pulse. The direction of contraction or expansion will be both laterally and perpendicularly of the plane defined by plate **14**. Since plates **12** and **14** are bonded together, as by the layer **20** or conductive epoxy, any change in physical dimensions of plate **14** will cause corresponding changes in physical dimensions of plate **12**. When the memory plate is thus stressed, it develops a voltage which appears between layers **16** and **20**, with the polarity at layer **20** being positive or negative, dependent on the state of prepolarization of the memory plate, as well as the direction of mechanical stress. Thus, with reference to FIG. 1, the output voltage V_o will be a negative pulse representative that a binary "0" signal is stored by plate **12**. For a further description of a dual-plate ceramic memory device as shown in FIG. 1, which provides nondestructive readout as explained in U.S. Pat. application, Ser. No. 527,223, now U.S. Pat. No. 3,462,746 reference should be had to said patent.

CERAMIC MEMORY MATRIX

Having now described the single bit ceramic memory device, together with the manner in which binary information is stored and interrogated, reference is now made to the ceramic memory matrix M of FIG. 3. For purposes of simplification, this matrix is shown as including only four ceramic memory devices **10***a*, **10***b*, **10***c*, **10***d*, each corresponding with the single bit ceramic memory device **10** illustrated in FIG. 2. These four memory devices are arranged in two vertical columns and two horizontal rows: to wit, a first column includes devices **10***a* and **10***c*, a second column includes devices **10***b* and **10***d*, a first row includes devices **10***a* and **10***b*, and a second row includes devices **10***c* and **10***d*. A common bit line BL–1 is electrically connected to the upper surface of memory plates **12** of the ceramic memory devices **10***a* and **10***c*. A second common bit line BL–2 is electrically connected to the upper surfaces of memory plates **12** of ceramic memory devices **10***b* and **10***d*. Bit line BL–1 is also connected to a three position switch S4 for respectively applying to the bit line

either an open circuit potential, a first direct current voltage level V_e or a second direct current voltage V_f. Voltage level V_e is equal to a reference potential $V_r + \frac{1}{3}V_p$, where V_p is the value of the polarization potential required to polarize a memory plate **12**. Also, voltage level V_f is equal to $V_r - \frac{1}{3}V_p$. Similarly, bit line BL–2 is also connected to a three-position switch S5 for selectively connecting bit line BL–2 with either an open circuit potential or direct current voltage level V_e or direct current voltage V_f. Accordingly, if the reference voltage is 104 volts and the polarization voltage is 120 volts, then voltage level V_e is equal to 144 volts and voltage level V_f is equal to 64 volts.

A common line CL–1 is electrically connected to the lower surface of memory plates **12** in the ceramic memory devices **10***a* and **10***b*. Similarly, a common line CL–2 is electrically connected to the lower surfaces of memory plates **12** in memory devices **10***c* and **10***d*. Resistors **30** and **32** are respectively connected between ground and common lines CL–1 and CL–2.

Common lines CL–1 and CL–2 are respectively coupled to bilevel switch circuits BLS–1 and BLS–2. These circuits are identical and each includes a PNP-transistor **34**, an NPN-transistor **36**, a resistor **38**, and four diodes **40**, **42**, **44** and **46**. Diodes **40** and **42** are connected together in series across the collector to emitter circuit of transistor **34**. The junction between diodes **40** and **42** is connected to the common line CL–1 for circuit BLS–1, or to the common line CL–2 for circuit BLS–2. Also, diodes **44** and **46** are connected together in series across the collector to emitter circuit of transistor **34**. The junctions of diodes **44** and **46** in both circuits BLS–1 and BLS–2 are coupled to the output of a monostable controlled push-pull oscillator BO. Resistor **38** is connected across the base to collector circuit of transistor **34** and then to the collector of transistor **36**. The emitter of transistor **36** is connected to ground.

The output of the blocking oscillator BO is a positive voltage and incorporates two voltage levels with respect to a reference voltage V_r. These levels include voltage level V_g and voltage level V_h, as shown by the graph of voltage versus time in FIG. **3**. Voltage level V_g may, for example, be equal to voltage level V_r plus two-thirds of the value of polarization potential V_p. Similarly, voltage level V_h may be equal to the voltage level V_r less two-thirds of the value of polarization potential V_p. Thus, for example, if the polarization potential is 120 volts, and the value of this potential is dependent upon the thickness of a memory plate **12** as well as the type of material employed, then with a reference voltage V_r equal to 104 volts, it is seen that voltage level V_g is 184 volts and voltage V_h is 24 volts.

Common line CL–1 is also electrically connected to the upper surfaces of driver plates **14** of memory devices **10***a* and **10***b*, by means of the electrically conductive epoxy **20** between plates **12** and **14**. Similarly, common line CL–2 is electrically connected to the upper surfaces of driver plates **14** of memory devices **10***c* and **10***d*. A drive line DL–1 is electrically connected to the lower surfaces of driver plates **14** of memory devices **10***a* and **10***b*, as well as to the base of transistor **36** in the bilevel switch circuit BLS–1.

Bit line BL–1 is coupled through a series circuit including capacitor C1 and bit line amplifier A1 to a storage register SR. Similarly, bit line BL–2 is coupled through a series circuit including capacitor C2 and bit line amplifier A2 to the storage register SR. The storage register SR may take any suitable form, such as a temporary storage register.

In FIG. **3**, a pair of row actuators RA1 and RA2 are provided for respectively actuating row No. **1**, i.e., the row which includes memory devices **10***a* and **10***b*, and row No. **2**, i.e., the row that includes memory devices **10***c* and **10***d*. Actuator RA1 includes a two-position switch S11 for connecting the base of an NPN-transistor transistor **50** with either B+ potential (off position) or ground potential (read-write position). Switch S11 is coupled to the base of transistor **50** through a suitable resistor **52**. The collector of transistor **50** is connected directly with drive line DL–1. Similarly, actuator RA2 includes a two-position switch S12 which is coupled to the base of an NPN-transistor **54** through a resistor **56**. The collector of transistor **54** is directly connected with drive line DL–2.

The collectors of transistors **50** and **54** are respectively connected through resistors **58** and **60** to the collector of an NPN-transistor **62**. Transistor **62** has its emitter connected to ground and its collector connected through a resistor **64** to a B+ voltage supply source. Also, the base of transistor **62** is coupled through a resistor **66** to a two-position switch S10. Switch S10 serves to connect resistor **66** with either a B+ potential (off position) or with ground potential (on position).

A master write actuator circuit MW is also included in the embodiment of FIG. **3**, and includes a two-position switch S13 for connecting one input of a NOR-circuit **70** with either a ground potential (write position) or B+ potential (off position). NOR-circuit **70** is an RTL NOR circuit and includes an NPN-transistor **72** having its emitter connected to ground and its collector connected through a resistor **74** to the collector of transistor **64**. The base of transistor **72** is connected through a resistor **76** to the switch S13 in master write actuator circuit MW. A second input to the base of transistor **72** is taken through a resistor **78** from the output circuit of another NOR-circuit **80**. The output of NOR-circuit **70** is taken at the collector of transistor **72** and is applied to the input of a strobe circuit **90** as well as through a resistor **82** to the base of an NPN-transistor **84**. Transistor **84** has its emitter connected to ground and its collector connected through a resistor **86** to a B+ voltage supply source. Also, the collector of transistor **84** is connected through a resistor **86** to a B+ voltage supply source. Also, the collector of transistor **84** is connected to the input of blocking oscillator BO.

NOR-circuit **80** is identical to NOR-circuit **70** and includes an NPN-transistor **88**, a pair of input resistors **92** and **94** which are coupled to the base of the transistor. More particularly, resistor **94** connects the collector of transistor **50** and the base of transistor **88** and resistor **92** connects the collector for transistor **54** with the base of transistor **88**. The collector of transistor **88** is connected through a resistor **96** to a B+ voltage supply source. The output of NOR-circuit **80** is taken at the collector of transistor **88** and is connected both to one input, at resistor **78**, of NOR-circuit **70**, as well as to one input of strobe circuit **90**.

Strobe circuit **90** includes a pair of NPN-transistors **98** and **100**. Transistor **98** is connected in a NOR-circuit configuration with one input to its base being taken through a resistor **102** from the collector of transistor **72**. The other input to the base of transistor **98** is taken through a resistor **104** from the collector of transistor **88**. The collector of transistor **98** is connected through a resistor **106** to a B+ voltage supply source. Transistor **100** has its base connected through a resistor **108** to the collector of transistor **98** and its emitter connected to ground. Also, transistor **100** has its collector connected through a resistor **110** to a B+ voltage supply source. The output of strobe circuit **90** is taken at the collector of transistor **100** and is connected to the storage register SR.

BLOCKING OSCILLATOR

The preferred form of blocking oscillator BO is shown in FIG. **4**, and it includes a pair of series-connected monostable oscillators **120** and **122**. The input for oscillator **120** is taken from the collector of transistor **84** and the output of oscillator **120** is applied to the input of oscillator **122**. The output of oscillator **120** is connected through a resistor **124** to the base of an NPN-transistor **126** having its emitter connected to ground. Similarly, the output of oscillator **122** is connected through a resistor **128** to the base of an NPN-transistor **130** having its emitter connected to ground. The collectors of transistors **126** and **130** are connected together in common and then through a resistor **132** to the base of a PNP-transistor **134** having its emitter connected to a B+ voltage supply source. The collector of transistor **134** is connected to a

center tap CT on a primary winding W1 of a transformer T. The left end of primary winding W1 is connected to the collector of NPN-transistor **136** having its emitter connected to ground and its base connected through a resistor **138** to the output of oscillator **120**. Similarly, the right end of winding W1 is connected to the collector of an NPN-transistor **140** having its emitter connected to ground and its base connected through a resistor **142** to the output of oscillator **122**. The secondary winding W2 of transformer T has its right end connected to the reference voltage source V and its left end connected in common to all of the bilevel switch circuits BLS–1 and BLS–2 (see FIG. 4). The transformer windings are connected in accordance with the polarity of the black dots shown in FIG. 4.

The operation of oscillator BO commences when transistor **84** (see FIG. 3) is biased into conduction. As transistor **84** is biased into conduction, a negative going signal is applied from the collector of transistor **84** to oscillator **120**. Oscillator **120** is a typical monostable oscillator and, as is well known, serves upon receipt of a negative going signal to provide a positive output pulse P1 (see FIG. 4) of a given magnitude and given duration. Pulse P1 is applied to the base of transistor **126** as well as the input circuit of monostable oscillator **122**. Monostable oscillator **122** does not provide an output pulse P2 until it receives the trailing or negative going edge of pulse P1. In the meantime, pulse P1 serves to forward bias transistor **126** which, in turn, forward biases transistor **134**. Accordingly, essentially B+ potential is applied to the center tap CT of winding W1. Pulse P1 also serves to bias transistor **136** into conduction so that essentially ground potential is applied to the left end of winding W1. Thus, for the duration of pulse P1 current flows from the center tap CT through the left half of winding W1 to ground, in accordance with the direction of arrow I1. A voltage V is induced in secondary winding W2 of a polarity in accordance with the black dots shown in FIG. 4. Thus, voltage V adds to voltage V_r. The magnitude of voltage V is on the order of $\frac{2}{3}V_p$, as determined by such factors as the transformer winding ratio.

On the negative going, or trailing, edge of pulse P1, monostable oscillator **122** is actuated to provide output pulse P2. This pulse forward biases transistors **130** and **140**. Also, since transistor **130** is now biased into conduction, transistor **134** becomes conductive to apply essentially B+ potential to the center tap CT. Since transistor **140** is also forward biased it essentially applies ground potential to the right end of winding W1. Accordingly, current flows, during the duration of pulses P2, through the right half of winding W1 in accordance with the direction of arrow I2. The induced voltage V in the secondary winding W2 will subtract from the reference voltage V_r. From the foregoing discussion, it is seen that each time transistor **84** is biased into conduction a train of two pulses V_g and V_h (see FIG. 2) are applied to all of the bilevel switch circuits BLS–1 and BLS–2.

OPERATION OF MATRIX

If it is desired to store a binary "1" signal in a memory plate **12**, then the upper surface of that memory plate should be connected to voltage level V_e. If, however, a binary "0" signal is to be stored, the upper surface of a memory plate **12** must be connected with voltage level V_f. As will be discussed hereinafter, voltage levels V_g and V_h are applied at different times to the lower surfaces of memory plates **12**. If the potential on the upper surface of a memory plate is V_e and the potential on the lower surface is V_g, then the potential difference is $-\frac{1}{3}V_p$, which is not sufficient to polarize the memory plate. However, if the potential on the lower surface is V_h then the potential difference is $+V_p$, which positively polarizes the memory plate to store a binary "1" signal. Similarly, if the potential on the upper surface of a memory plate **12** is V_f and the potential on the lower surface is V_h, then the voltage difference is $-\frac{1}{3}V_p$, which is insufficient to polarize the memory plate. However, if the potential on the lower surface of that memory plate is V_g, then the potential difference is $-V_p$ which serves to negatively polarize that memory plate to store a binary "0" signal.

Application of binary information to be stored in matrix M is accomplished one row at a time. First, switches **S4** and **S5** are manipulated, as desired, for storage of either binary "1" or binary "0" signals. Then, switch **S10** is manipulated to its "on" position so that transistor **62** is reverse biased. This applies essentially B+ potential to the collectors of transistors **50**, **54** and **72**. During the write operation of row No. **1**, the next step is to manipulate switch **S11** from its "off" position to its "read-write" position. This reverse biases transistor **50** so that the positive potential at its collector is applied as an actuating signal to forward bias transistor **36** in bilevel switch circuit BLS–1. After switch **S11** has been manipulated to its "read-write" position, the operator then manipulates switch **S13** in the master write actuator circuit MW to its "write" position. Since the potential on the collector of transistor **50** is essentially at B+ potential and the potential on the collector of transistor **54** is essentially at ground potential, transistor **88** in NOR-circuit **80** is biased into conduction. Accordingly, the potential on the collector of transistor **88** is essentially at ground and this potential is applied through resistor **78** in NOR-circuit **70** to the base of transistor **72**. Since switch **S13** now applies a ground signal through resistor **76** to the base of transistor **72**, this transistor is reverse biased and its collector applies essentially a B+ potential to the base of transistor **84**. Accordingly, transistor **84** is biased into conduction to energize oscillator BO. The output circuit of blocking oscillator BO carries a train of two voltage pulses respectively of voltage levels V_g and V_h. These voltage levels are applied at different times to the bilevel switch BLS–1, which has been actuated into conduction due to the positioning of switch **S11** to the "read-write" position. Accordingly, memory devices **10***a* and **10***b* now become polarized to store binary signals in accordance with positioning of switches **S4** and **S5**.

After row No. **1** has been written as discussed above, switch **S11** is returned to its "off" position and switch **S13** is returned to its "off" position. The circuitry is now in condition for applying binary signals to row No. **2**. The same steps discussed above are repeated for this operation.

When it is desired to interrogate one of the rows, the associated row actuator switch **S11** or **S12** is manipulated to its "read-write" position. However, during this operation, the master write actuator switch **S13** is left in its "off" position. During the interrogation of row No. **1**, switch **S11** is manipulated to its "read-write" position. This reverse biases transistor **50** so that its collector applies essentially a B+ potential to drive line DL–1. Thus, the voltage difference between the upper and lower surfaces of memory plates **14** in row No. **1** is changed by the value of the B+ potential. This potential corresponds with interrogation voltage V_{in}, discussed previously with respect to FIG. **1**. The output voltages of memory devices **10***a* and **10***b* appear on bit lines BL–1 and BL–2 in accordance with the polarities of the stored binary signals. These output voltages are applied through capacitors C1 and C2 and amplifiers A1 and A2 to storage register SR. The register is strobed by strobe circuit **90** so that it is gated into conduction to receive these output signals from memory devices **10***a* and **10***b* only during the time that the matrix X is being interrogated. The gating signal to the storage register SR takes the form of a negative going signal. During the interrogation operation of row No. **1**, the potential at the collector of transistor **88** of NOR-circuit **80** is essentially at ground potential. Since the master write actuator switch **S13** is in its "off" position, the output taken at the collector of transistor **72** of NOR-circuit **70** is essentially at ground potential. Accordingly, transistor **98** in strobe circuit **90** is reversed biased so that essentially a B+ forward biasing potential is applied to the base of transistor **100**. This causes the potential on the collector of transistor **100** to decrease in a negative direction so that the storage register SR is gated on to receive the binary signals from ceramic memory devices **10***a* and **10***b*. The same

procedure as discussed above with reference to interrogating row No. 1 is repeated when interrogating row No. 2.

TRAFFIC CONTROLLER–FIRST EMBODIMENT

Having now described a ceramic memory matrix, circuitry for altering the binary information stored, and circuitry for interrogating the matrix, a description is now presented as to the manner in which the matrix is interconnected in accordance with the present invention to provide a semiactuated traffic controller. As shown in FIG. 5 and 5*a*, the traffic controller generally includes: an alternating current voltage source V, which may take any suitable form, such as a 60 c.p.s. line frequency source; a binary counter C; a binary comparator BC–1; a temporary storage register R1; a time memory matrix TM; a sequencer interrogator I; an interval time write circuit TW; a maximum extension time memory MET; a temporary storage register R2; a binary comparator BC–2; a cross street extension time update circuit CSE, which includes a unit extension time memory UET, a temporary storage register R3, a binary adder BA, a temporary storage register R4, and an automatic write circuit AMW; a detector memory circuit DM–1; and, a load control circuit LC.

The alternating current voltage source V is coupled to a suitable frequency dividing circuit **300** which serves to divide a 60 c.p.s. frequency of source V into a frequency signal of 1 c.p.s. The output of frequency divider circuit **300** is applied to a pulse shaper **302** which serves to provide a train of equitimed spaced pulses exhibiting a frequency of 1 pulse per second. The output of shaper **302** is applied to the input of binary counter C through the emitter to collector path of a PNP-transistor **304** which serves as an inhibit gate IG–1.

Binary counter C is a four stage counter and has four outputs *a*, *b*, *c* and *d* which have decimal values of 8, 4, 2, 1, respectively, for providing binary signals, the decimal equivalent of which increases in accordance with the decimal number of the pulses counted. The four outputs, *a*, *b*, *c* and *d*, and the binary counter C are coupled to the binary comparator BC–1 through inhibit gates IG–2, IG–3, IG–4 and IG–5, respectively. Each of the inhibit gates IG–2 through IG–5 as well as the remaining inhibit gates to be referred to hereinafter in this specification may take the form as shown in detail with respect to inhibit gate IG–1.

The interval time storage memory matrix TM include six word line memories TM–1, TM–2, TM–3, TM–4, TM–5 and TM–6, each of which may be constructed as schematically illustrated in FIG. 3 with respect to word line memories TM–1 and TM–2, respectively, coupled to common lines CL–1 and CL–2. Preferably, however, matrix TM, in FIG. 5, is constructed in accordance with an improved matrix disclosed in U.S. Pat. No. 3,401,377. For purposes of simplifying the description of this invention, however, the simplified showing of matrix M in FIG. 3 is believed sufficient for a complete understanding of the invention. As shown in FIG. 3, each of the two word line memories TM–1 and TM–2 includes two ferroelectric bistable memory means **10***a*, **10***b*, **10***c* or **10***d* which serve to store a binary "1" signal or a binary "0" signal so that the decimal equivalent of the binary content of a word line memory is representative of a desired time duration for an associated load interval. Each of the memory means **10***a*, **10***b*, **10***c* and **10***d* in FIG. 3 has an input in the form of a drive line (DL–1 or DL–2) which are all connected together in common for any one word line memory and then to one of the outputs 1, 2, 3 or 4 of the interrogator I for receiving interrogation signals. Also, each of the bistable memory means has an output in the form of a bit line BL–1 or BL–2, etc., which serves to carry a binary signal in response to receipt of an interrogation signal. These bit lines for associated bits in the various word line memories may be connected together, as shown in FIG. 3. The bit line output circuits of the matrix TM include circuits BL–1, BL-2, BL—3 and BL–4 which are respectively coupled through bit line amplifiers A1, A2, A3 and A4 to a type D, four stage flip-flop register R1. Register R1 includes four type flip-flops FF1, FF2, FF3 and FF4, each having a set terminal S and a toggle terminal T. The outputs of amplifiers A1 through A4 are respectively connected to set terminals S of flip-flops FF1, FF2, FF3 and FF4. The output circuits of these flip-flops are connected to the binary comparator BC–1. In a manner similar to the outputs of binary counter C, the bit line output circuits BL–1, BL–2, BL–3 and BL–4 of matrix TM and the corresponding outputs of register R1 have decimal values of 8, 4, 2 and 1, respectively.

The output of binary comparator BC–1 is connected to a reset input of binary counter C, a reset input of register R1, and to the input of the sequencer-interrogator I. Circuit I may take the form of a circulating ring counter having its output circuits 1, 2, 3, 4, 5 and 6, respectively, connected to drive lines DL–1, DL–2, DL–3, DL–4, DL–5 and DL–6 for matrix TM. The interrogator circuit I serves to sequentially energize its output circuits 1, 2, 3, 4, 5 and 6 in a cyclically fashion in response to actuating trigger pulses received from the binary comparator BC–1. An equivalent function of interrogator circuit I is that as performed by the read circuits described previously with reference to the simplified matrix M shown in FIG. 3. Diodes D1 through D6, poled as shown in FIG. 5, connect the six output circuits of interrogator circuit I in common and then to the toggle terminals T of the four stage flip-flop register R1.

Interval time write circuit TW has six output circuits respectively coupled to word line memories TM–1 through TM–6 for purposes of electrically altering the binary state of each memory means in the associated word line memories. This circuitry may take the form as described previously with reference to the write function of the circuitry illustrated in FIG. 3.

The outputs 1 through 6 of the sequencer-interrogator circuit I are coupled to the load control circuit LC for purposes of energizing selected ones of traffic signal lamps MSG (main street green), MSA (main street amber), CSR (cross street red), CSG (cross street green), CSA (cross street amber), and MSR (main street red). Output circuits 1 through 6 of the interrogator I are coupled to these lamps through amplifiers A13 through A18, respectively, as well as through the diode logic circuitry with the diodes being poled as shown in FIG. 5. Thus, with this circuitry, whenever output circuits 1 or 2 are energized, the main street green lamp MSG is energized. Similarly, whenever output circuit 3 is energized, the main street amber light MSA is energized. Also, whenever output circuits 4 or 5 are energized, the cross street green lamp CSG is energized. Also, whenever output circuit 6 is energized, the cross street amber light CSA is energized. It will also be noted that the cross street red lamp CSR is energized whenever any of these circuits 1, 2 or 3 is energized. Similarly, the main street red lamp MSR is energized whenever any of the output circuits 4, 5 or 6 is energized.

Output circuit 5 of the sequencer-interrogator I is connected as a drive line input to a maximum extension time word line memory MET. The output bit lines BL–5 through BL–8 of this word line memory are respectively coupled through bit line amplifiers A5 through A8 to the set terminals S of flip-flops FF–5 through FF–8 of a temporary storage register R2. Output circuit 6 of the sequencer-interrogator I is also coupled to the toggle terminals T of each of these flip-flops FF–5 through FF–8. Also, the output circuit 6 of the sequencer-interrogator I is coupled to the reset input of resister R2. The outputs of each of the four flip-flops FF–5 through FF–8 are coupled to a binary comparator BC–2 having four inputs taken from output circuits *a*, *b*, *c*, and *d* of the binary counter C. In a manner similar to the outputs of binary counter C, the bit line output circuits BL–5 through BL–8 of word line memory MET and the corresponding outputs of register R2 have decimal values of 8, 4, 2 and 1, respectively.

The cross street extension time update circuit CSE includes a unit extension time word line memory UET having four bits and with its bit line output circuits BL–9 through BL–12 respectively coupled through bit line amplifiers A9 through

A12 to the set terminals S of flip-flops FF–9 through FF–12, respectively, of a temporary storage register R3. In a manner similar to that of the word line memory MET, bit lines BL–9 through BL–12 together with the corresponding outputs of flip-flops FF–9 through FF–12 have decimal values of 8, 4, 2, 1, respectively. The outputs of flip-flops FF–9 through FF–12 are coupled to a binary adder BA. Register R4 of this circuitry has its set terminals S coupled to output circuits *a*, *b*, *c* and *d* of binary counter C. The outputs of flip-flops FF–13 through FF–16 are applied to the binary adder BA. The toggle terminals T of register R4 together with the toggle terminals T of register R3 are connected together in common to the output of an AND-circuit AD–1. The output of the AND-circuit AD–1 is also connected to the drive line input of the unit extension time word line memory UET, as well as to one input of an automatic memory write circuit AMW. The binary adder BA serves to add the binary content on the output circuit of registers R3 and R4 and apply the output through four output circuits to the automatic memory write circuit AMW. The output of the automatic write circuit AMW is coupled both to bit lines BL–1 through BL–4 as well as to common lines CL–5 of word line TM–5 of the time storage memory matrix TM.

The detector memory DM–1 is coupled to the phase B detectors DB, shown as a simple normally open switch in FIG. 5. The detector memory includes a pair of NOR-gates **305** and **306** connected together to define a two-input bistable multivibrator circuit as shown in FIG. 5. One input to NOR-gates **305** is taken from the normally open detector switch DB through a single input NOR-gate **303**, serving as a single inverter, and another input of NOR-gate **305** is taken from the output of NOR-gate **306**. The input of NOR- **303** is also coupled through a resistor **310** to a B+ voltage supply source. The output of the detector memory DM–1 is taken through a single input NOR-gate **314**, serving as a signal inverter, to one input of an AND-gate **312**. The output of AND-gate **312** is coupled to the base of transistor **304** in inhibit gate IG–1 through a resistor **308**. The output of NOR-gate **306** is also connected through inhibit gate IG–6 to one input of AND-gate AD–1. The second input to AND-gate AD–1 is taken from output circuit **5** of the sequencer-interrogator I. The output of binary comparator BC–2 is connected to the control input of inhibit gate IG–6. Output circuit **2** of the sequencer-interrogator circuit I is also connected to the second input of AND-gate **312**.

AUTOMATIC WRITE CIRCUIT

The automatic write circuit AMW is shown in greater detail in FIGS. **6** and **7**. The circuitry in FIG. **6** includes bit line drivers BLD–1 and BLD–2, having their outputs coupled to bit lines BL–1 and BL–2, respectively. The bit line drivers BLD–1 and BLD–2 are coupled to a temporary storage register TSR having two flip-flops FF–20 and FF–22. These are standard flip-flops or bistable multivibrator circuits, each having a "0" output and a "1" output taken, for example, from the collectors of two NPN transistors. The "0" and a "1" outputs of flip-flop FF–20 are coupled to bit line driver BLD–1. Similarly, the "0" and "1" outputs of flip-flop FF–22 are coupled to bit line driver BLD–2. A common strobe CS is coupled to both bit line drivers BLD–1 and BLD–2. As is conventional, flip-flops FF–20 and FF–22 may be reset by application of a trigger signal over line RL so that neither of their outputs "0" nor "1" are energized.

Referring now to FIG. **7**, there is shown a schematic illustration of the circuitry of bit line driver BLD–1. It is to be understood that the circuitry for bit line driver BLD–2 is identical to that of bit line driver BLD–1. Flip-flop FF–20 is shown in FIG. **7**, in a simplified manner, as being represented by two three position switches S14 and S16. These two switches may be selectively manipulated to connect output **1** (for switch S14) or output **0** (for switch S16) with either ground potential, or B+ potential, or to open circuit. Similarly, the common strobe CS from AND-gate AD–1 is shown in simplified manner in FIG. **7** as including a two-position switch S18 which is normally connected to ground potential and may be manipulated to connect the bit line driver BLD–1 with B+ potential. It is to be understood that these switches S14 and S16 and S18 are illustrative of the operation of a flip-flop as well as a common strobe, and would normally be comprised of well-known solid-state circuitry.

Bit line driver BLD–1 includes a saturable core transformer T–2 having a primary winding W–4 and a secondary winding divided into two winding portions W–6 and W–8 by means of a center tap CT–2. The center tap CT–2 is connected with the reference voltage source V_r. The left end of winding portion W–6 is connected to the collector of a PNP-transistor **200** having its emitter connected to bit line BL–1. Similarly, the right end of winding portion W–8 is connected to the emitter of a PNP-transistor **202** having its collector connected to bit line BL–1. A resistor **204** is connected between the base and emitter of transistor **200**. Similarly, a resistor **206** is connected between the base and emitter of transistor **202**. A resistor **208** is connected between bit line BL–1 and the reference voltage source V_r. The primary winding W–4 has its right end connected to a B+ voltage supply source and its left end connected to the collector of an NPN-transistor **210**, having its emitter connected to ground and its base connected through a resistor **212** to the switch S18 of the common strobe CS. A resistor **214** is coupled to the junction of resistor **212** and the base of transistor **210** and then to a B− voltage supply source.

The base of transistor **200** is also connected to the collector of an NPN-transistor **216**, having its base connected through a resistor **218** to the movable element of switch S16 in the flip-flop FF–20. Similarly, the base of transistor **202** is connected to the collector of an NPN-transistor **220**, having its base connected through a resistor **222** to the movable element of switch S14 in the flip-flop FF–1. The emitter of transistor **216** is coupled through a diode **224**, poled as shown, to the collector of an NPN-transistor **226**. Similarly, the emitter of transistor **220** is connected through a diode **228**, poled as shown, to the collector of transistor **226**. Transistor **226** has its emitter connected to ground through a resistor **230** and its base connected to the junction of a voltage divider, including resistors **232** and **234** connected between the B+ voltage supply source and ground. The junction of resistor **232** and **234** is also connected to the collector of an NPN-transistor **236**, having its emitter connected to ground and its base connected through a resistor **238** to the B− voltage supply source. The junction of resistor **238** and the base of transistor **236** is connected to the collector of an NPN-transistor **240**, having its emitter connected to ground, and which serves as a signal inverter. Also, the collector of transistor **240** is connected through a resistor **242** to the B+ voltage supply source. The base of transistor **240** is connected to the movable element of switch S18 in the common strobe CS. The black dots shown adjacent the transformer T–2 are polarity dots of the winding arrangement, whereby when a voltage is applied to primary winding W–4 the induced voltage in winding portion W–6 subtracts from the reference voltage V_r and the induced voltage in winding portion W–8 adds to the reference voltage.

BIT LINE DRIVER OPERATION

The purpose of the bit driver circuitry shown in FIG. **7** is to apply voltage level V_e or voltage level V_f to bit line BL–1. These voltage levels are respectively representative of a binary "1" signal and a binary "0" signal. If a binary "1" signal is to be written into the memory devices of FIG. **3**, to which bit line BL–1 is connected, then switch S14 is connected with the B+ voltage supply source so as to provide a positive signal at output **1** of flip-flop FF–20. As will be discussed hereinafter, this will result in a voltage level V_e being carried by bit line BL–1. If, on the other hand, it is desired to write a binary "0" signal in the ceramic memory devices to which bit line BL–1 is connected, then switch S16 is connected to the B+ voltage supply source which results in voltage level V_f being carried on bit line BL–1. Neither voltage level V_e or V_f will appear on bit line

BL–1 unless the common strobe CS is actuated to apply a positive potential to transistor **210** in each of the bit line drivers BLD–1 and BLD–2 during the write operation.

In the event it is desired to write a binary "1" signal in memory plates **12** in memory devices **10***a* and **10***c* in matrix M of FIG. **3**, then flip-flop FF–**20** (FIG. **5**) must receive two pulses from a binary signal source so that its output circuit **1** carries a positive signal. This is equivalent to manipulating switch S**14** in the illustration of FIG. **7** to apply a positive signal to output circuit **1**. This forward biases transistor **220**. At the point in time that it is desired to write the binary information, the common strobe CS, i.e., AND-gate AD–**1** in FIG. **5**, is actuated to apply positive signals to all of the bit line drivers. Accordingly, in FIG. **7**, this is equivalent to manipulating switch **18** to apply positive potential to the base of transistor **210**. Transistor **210** is forward biased into conduction, whereupon essentially B+ voltage is impressed across primary winding W–**4**. Since the positive signal applied to transistor **210** is also applied to base of transistor **240**, then this transistor is forward biased into conduction to reverse bias transistor **236**. Since transistor **236** is reverse biased, transistor **226** is biased into conduction through resistor **232**. Since transistors **220** and **226** are now biased into conduction, a potential approaching that of ground potential is applied to the base of PNP-transistor **202** so that this transistor is biased into conduction. Accordingly, the voltage impressed across winding W–**4** causes a voltage to be induced in winding portion W–**8**. This induced voltage is on the order of 40 volts, as determined by the turns ratio between the primary and secondary windings. The polarity of this voltage is in accordance with the polarity dots shown in FIG. **7**. Therefore, this induced voltage in winding portion W–**8** adds to the reference voltage V_r and the combined voltage is carried by bit line BL–**1**. If the reference voltage V_r is 104 volts and the induced voltage in winding portion W–**8** is 40 volts, then bit line BL–1 carries 144 volts, which, as discussed hereinbefore, is the voltage required for writing binary "1" signals in memory devices **10***a* and **10***c* of the matrix M in FIG. **3**.

The operation for writing a binary "0" signal is essentially the same with the exception that transistor **200** is forward biased into conduction and that the induced voltage in winding W–**6** will subtract from the reference voltage V_r. If the induced voltage is 40 volts and the reference voltage is 104 volts, when a voltage of 64 volts will be carried on bit line BL–**1**, which, as discussed hereinbefore, is the voltage required for writing a binary "0" signal in memory devices **10***a* and **10***c*.

OPERATION OF TRAFFIC CONTROLLER

During the operation of the local controller LC–1 it may be assumed that the cross street amber signal lamp CSA has just been extinguished and that the cross street red lamp CSR and main street green lamp MSG have just become energized. During these conditions, output circuit **1** of the sequencer-interrogator circuit applies a positive interrogating voltage to drive line DL–**1** for interrogating word line TM–**1** of the interval time storage matrix TM. Inhibit gate IG–**1** is forward biased and, accordingly, pulses from shaper **302** are applied to the input binary counter C. This counter was reset to a binary count of zero at the initiation of the main street green time interval. Since word line TM–**1** is programmed with a binary signal 1001 representing decimal signal 9 a time interval of 9 seconds must be now timed. Accordingly, the binary counter C will count nine pulses taken from shaper **302** and, when nine pulses have been counted, its output circuits *a*, *b*, *c* and *d* will carry the binary digits of binary signal 1001. Since inhibit gates IG–**2** through IG–**5** are open, this binary signal is applied to one side of the binary comparator BC–**1**. Similarly, since word line TM–**1** is interrogated by output circuit **1** of the sequencer-interrogator I, the binary signal 1001 of this word line is applied through bit line amplifiers A**1** through A**4** and applied to the temporary storage register R**1**. The corresponding outputs of the temporary storage register R**1** carry a binary 1001 and this is applied to the other side of the binary comparator. Since a match is now obtained the binary comparator BC–**1** applies a binary "1" signal to reset the binary counter C, as well as the temporary register R**1**, as well as to actuate the sequencer-interrogator circuit I.

Output circuit **2** of the sequencer-interrogator circuit I is now energized to carry a binary "1" signal. However, it will be noted that the binary information stored in word line TM–**2** is a binary signal pattern 0000 representative of a zero count. Also, output circuit **2** is coupled to one input of AND-gate **312**. The other input of AND-gate **312** is connected to the output of NOR-gate **314**. The output of AND-gate **312** is connected to inhibit gates IG–**1** through IG–**5** so that while this output circuit is energized these inhibit gates are closed to prevent the binary counter from performing a counting function and prevent the binary comparator from making a comparison function. Accordingly, so long as no vehicle is detected in phase B the controller will dwell in this position so that the main street green lamp MSG and a cross street red lamp CSR are energized.

Upon detection of traffic in phase B, the phase B detector switch db. FIG. **5**, will be momentarily closed. Accordingly, a ground or binary "0" signal is applied to the input of detector memory DM–**1** which provides a binary "1" signal at its output circuit. This positive signal is applied to NOR-gate **314**. The output of AND-gate **312** now carries a binary "0" signal, whereby inhibit gates IG–**1** through IG–**5**, become open. Immediately, the binary "0" signal pattern in the binary counter C is applied to one side of the binary comparator BC–**1**. Also, the binary zero pattern in word line TM–**2** is applied through bit line amplifiers A–**1** through A–**4** to the other side of the binary comparator BC–**1**. Accordingly, a match is obtained and binary counter BC–**1** resets the binary counter C as well as the temporary storage register R**1**. In addition, the binary comparator BC–**1** actuates the sequencer-interrogator I so that word line TM–**3** is interrogated.

Word line TM–**3** stores a binary 0011 representative of 3 seconds for the main street amber time duration. Accordingly, once the binary counter has counter 3 seconds, a match will be obtained and the binary counter BC–**1** will again reset binary counter C and temporary storage register R**1**. In the meantime, of course, both the cross street red lamp CSP and the main street amber lamp MSA are energized. The sequencer-interrogator is then actuated by the binary comparator BC–**1** so that only output circuit **4** of the interrogator I is energized. Accordingly, interrogator I now interrogates word line TM–**4**.

The word line TM–**4** being interrogated, the main street red lamp MSR and the cross street green lamp CSG are energized. The cross street initial interval is set for a binary 0111 representative of 7 seconds. Accordingly, once the binary counter C has counted seven pulses from shaper **302** a match is obtained and the binary comparator BC–**1** resets counter C as well as the temporary storage register R**1**. Sequencer-interrogator I is now actuated to energize only its output circuit **5** for purposes of interrogating word line TM–**5**. During the period that this word line is energized both the main street red lamp MSR and the cross street green lamp CSG are energized. The cross street extension interval is initially set for a binary 0101, representative of 5 seconds. Since output circuit **5** of the interrogator is coupled to the input of NOR-gate **306** in the detector memory DM–**1**, the memory is reset and its output circuit carries a binary "0" signal.

If, however, a vehicle in phase B now actuates the phase B detector, then a momentary closure of switch DB will occur. This applies a binary "1" signal through normally open inhibit gate IG–**6** and one input of AND-gate AD–**1**. Since output circuit **5** of interrogator I is energized, a binary "1" signal is also applied to the second input of the AND-gate AD–**1**. Accordingly, AND-gate AD–**1** applies an interrogating signal to the unit extension time word line memory UET. This word line carries a binary 0101 representative of 5 seconds. This signal

pattern is applied through bit line amplifiers A9 through A12 to flip-flops FF–9 through FF–12 and temporary storage register R3. The corresponding outputs of register R3 are applied to the binary adder BA. Binary adder BA receives the current time count from binary counter C by means of the temporary storage register R4. If, for example, during this cross street extension interval only three pulses had been counted by binary counter C, then this binary signal; to wit, 0011, would be added to the binary signal in the unit extension word line memory UET to obtain a total of 8 seconds, or a binary 1000. This is applied to the automatic write circuit AMW which serves, as described in detail hereinbefore, to rewrite word line TM–5 to obtain a new binary signal 1000. If no further vehicles are detected in phase B, then when the binary counter C has an output count representative of 8 seconds, a match will be obtained and the binary comparator BC–1 will actuate the sequencer-interrogator I. If, however, a second car is detected before the binary counter C has reached a count of 8 seconds, then an additional 5 seconds will be allocated for the second vehicle extension. This, of course, means that the automatic write circuit, in the manner just described, will rewrite word line memory TM–5 to provide a time storage of 13 seconds, or a binary 1101. This process may continue until such time as the maximum extension time has been reached.

Once output circuit 5 of the interrogator I has been energized, it applies an interrogating signal to the maximum extension word line memory MET. As shown in FIG. 5, this word line memory is programmed to store a binary signal of 1111, which is representative of 15 seconds. This binary signal pattern is applied through bit line amplifiers A5 through A8 to the temporary storage register R2. Once the binary counter C has counted 15 pulses; to wit, 15 seconds in the cross street extension interval, a match will be obtained at binary comparator BC–2. At that time, binary comparator BC–2 applies a positive signal to inhibit gate IG–6 to close this gate to prevent further phase B detections from obtaining additional unit extension times. Since the cross street extension time update circuit CSE will no longer rewrite memory word line TM–5 in the interval time storage memory matrix TM, the remaining time from the last vehicle will be timed out and when a match is obtained at binary comparator BC–1, the binary counter C and the temporary storage register R1 will be reset. Also, at this time, binary comparator BC–1 actuates sequencer-interrogator I to energize drive line DL–6 to interrogate word line memory TM–6. This memory stores the cross street amber interval and, as shown in FIG. 5, is programmed with a binary signal pattern of 0011, representative of 3 seconds. Accordingly, until a match is obtained at binary comparator BC–1, the cross street amber lamp CSA as well as the main street red lamp MSR are energized. When the binary counter C has counted three pulses a match is obtained and the sequencer-interrogator I is actuated to deenergize drive line DL–6 and energize drive line DL–1 to interrogate word line memory TM–1. As described hereinbefore, once word line memory TM–1 is interrogated, the main street green lamp MSG and the cross street red lamp CSR are energized. When the binary counter C has counted nine pulses, a match will be obtained with the binary signal stored in word line TM–1 and the binary comparator BC–1 will again actuate sequencer-interrogator I so that the controller steps to the main street green dwell interval where it will rest until such time as a traffic detection takes place in phase B. If, however, a detection was registered with the detector memory DM–1 during the cross street amber interval, the controller will immediately step to the main street amber interval. Thereafter, the operation is essentially the same as that which has been described previously.

TRAFFIC CONTROLLER-SECOND EMBODIMENT

Reference is now made to FIGS. 8 and 9 which illustrate a second embodiment of the invention in the form of a two-phase, full-actuated, traffic controller LC–2. As shown in FIG. 8, this controller serves to control traffic signal S which displays go and caution signals to main street phase A and to cross street lane B. Traffic detectors DA serve to detect traffic in lane A and traffic detectors db. serve to detect traffic in phase B. These detectors may be spot detectors of any well-known variety, such as a treadle pad, or, alternatively, may be presence detectors, such as ultrasonic or loop detectors. As shown and described in FIGS. 8 and 9, the detectors are spot detectors.

Reference is now made to FIG. 9 which illustrates the controller in detail. As is immediately apparent, this controller is quite similar to controller LC–1 described previously with respect to FIG. 5. For purposes of simplifying the understanding of this invention, like components in FIGS. 5 and 9 are identified with like character references.

Controller LC–2, like controller LC–1, generally includes: an alternating current voltage source V, which may take any suitable form, such as a 60 cycle per second line frequency source; a binary counter C; a binary comparator BC–1; a temporary storage register R1; a time memory matrix TM; a sequencer-interrogator I; an interval time write circuit TW; a phase A maximum extension time memory MET–A; a phase B maximum extension time memory MET–B; a temporary storage register R2; a binary comparator BC–2; an extension time-up-date circuit UC, which includes a phase A unit extension time memory UET–A, a phase B unit extension time memory UET–B, a a phase B maximum extension time memory MET–B; a temporary storage register R2; a binary computer BC–2; an extension time-up-date circuit UC, which includes a phase A unit extension time memory UET–A, a phase B unit extension time memory UET–B, a temporary storage register R3, a binary adder BA, a temporary storage register R4, and an automatic write circuit AMW'; a phase B detector memory circuit DM–1 and a phase A detector memory circuit DM–2; and, a load control circuit LC' for controlling traffic lights S.

Wave shaper 302 in local controller LC–2 is coupled through inhibit gate IG–10 to the binary counter C. As in the case of local controller LC–1, this inhibit gate may include, for example, a PNP transistor. The collector of transistor 304 is connected to the input of binary counter C. The output of binary comparator BC–1 is coupled to the reset input of binary counter C, to the input of sequencer-interrogator I, and to the reset input of temporary storage register R1.

The interval time storage memory matrix TM, like the similar matrix in FIG. 5, includes six word line memories TM–1 through TM–6. These six word line memories serve to respectively store binary signals representative of the time periods for the main street initial interval MSI, the main street extension interval MSE, the main street amber interval MSA, the cross street initial interval CSI, the cross street extension interval CSE, and the cross street amber interval CSA. Outputs 1 through 6 of sequencer-interrogator I are coupled to drive lines DL–1 and DL–6 of the word line memories TM–1 through TM–6 of the memory TM.

The phase B and phase A detector memories DM–1 and DM–2 are substantially similar to detector memory DM–1 in FIG. 5. Thus, connected together to define a two input bistable multivibrator circuit. One input to NOR-gate 305 is coupled through a NOR-gate 303 to detector DB as well as through resistor 310 to the B+ voltage supply source. The output of NOR-gate 306 is connected to one input of AND gate AD–2 in the extension time-up-date circuit UC, as well as to one input of AND-gate AD–4. The output of NOR-gate 360 is also coupled to the control input of inhibit gate IG–13.

Detector memory DM–2 includes a pair of NOR-gates 323 and 324 connected together to define a two input, bistable multivibrator circuit. One input of NOR-gate 323 is coupled through a NOR-gate 321 to detector DA as well as through resistor 320 to the B+ voltage supply source. The output of NOR-gate 324 is connected to one input of AND-gate AD–3 in the extension time-up-date circuit UC as well as to the input of AND-gate AD–5 through NOR-gate 362. The output of

NOR gate is also coupled to the control input of inhibit gate IG–14.

AND-gate AD–4 has a second input taken from drive line DL–2 and an output connected through a diode to the control input of inhibit gate IG–10. AND-gate AD–5 has its second input taken from drive line DL–5 and its output connected through a diode to the control input of inhibit gate IG–10. AND-gate AD–5 has its second input taken from drive line DL–5 and its output connected through a diode to the control input of inhibit gate IG–10.

The inputs of inhibit gates IG–13 and IG–14 are respectively taken from output circuits 2 and 5 of the sequencer-interrogator circuit I. The output of inhibit gate IG–13, in turn, is applied as a drive line to the phase A maximum extension word line MET–A as well as through a diode 340 to the toggle input terminals T of the resistor R2. Similarly, the output of inhibit gate IG–14 is coupled as the interrogating drive line circuit to the phase B maximum extension word line MET–B as well as through a diode 342 to the toggle terminals T of register R2.

The output of binary comparator BC–2 is coupled through a diode 344 to the control input of an inhibit gate IG–15. Similarly, the output of binary comparator BC–2 is also connected through a diode 346 to the control input of inhibit gate IG–16. The outputs of inhibit gates IG–15 and IG–16 are respectively coupled to word lines TM–5 and TM–2 as well as being connected through diodes to the bit lines BL–1 through BL–4. The inputs to inhibit gates IG–15 and IG–16 are taken from the outputs of the automatic memory write circuit AMW′ which is preferably constructed in a manner similar to that discussed hereinbefore with reference to write circuit AMW shown in FIG. 5.

The extension time-up-date circuit UC in addition to AND gates AD–2 and AD–3 and the memory write circuit AMW′ also includes temporary storage registers R3 and R4 and a binary adder BA. The outputs of AND-gates AD–3 and AD–2 are respectively coupled as the interrogating input circuits to the phase A unit extension word line memory UET–A and the phase B unit extension word line memory UET–B. The bit line outputs BL–9 through BL–12 of these word line memories are respectively coupled through bit line amplifiers A9 through A12 to the register R3 in the manner described previously with reference to the up-date circuit CSE in FIG. 5. The outputs of AND-gates AD–3 and AD–2 are respectively coupled through diodes 350 and 352 to the toggle terminals T of register R3 as well as to the toggle terminals T of register R4 and to the input of automatic memory write circuit AMW′.

OPERATION OF SECOND EMBODIMENT

The operation of local controller LC–2 is quite similar to that of local controller LC–1 described hereinbefore. Accordingly, for purposes of simplifying the understanding of this invention, only the differences in operation will be discussed in detail hereinafter.

In the operation of controller LC–2 it may be assumed that the phase B amber interval has terminated and the phase A initial interval MSI has just commenced. Accordingly, output circuit 1 of the sequencer-interrogator circuit I is energized to interrogate word line TM–1 of the memory matrix TM. The binary counter is reset and now commences to count pulsations from shaper 302 until the output count of counter C matches that from word line TM–1. In this case, word line TM–1 carries a binary 1001 and it will be necessary that nine pulses be counted in order to obtain a match. During this interval, output circuit 1 of interrogator I is applied through a suitable load control circuit LC′ for energizing the main street green signal light as well as the cross street red signal light in a manner similar to that as described hereinbefore with reference to the load control circuit LC shown in FIG. 5. Once the match has been obtained the binary comparator BC–1 applies a positive pulse to reset binary counter C and to actuate the sequencer-interrogator to energize only its output circuit 2.

Once sequencer output circuit 2 is energized the controller will either rest in main street green dwell or will proceed to time out unit extensions as required for main street, then time the main street amber period and cycle to the cross street initial interval. If, at the time sequencer output circuit 2 is initially energized, no traffic has been detected by the phase B detector DB, then the phase B detector memory circuit DM–1 applies a binary "0" signal to the input of NOR-gate 360 which, in turn, applies a binary "1" signal to the input of AND-gate AD–4. A binary "1" signal is applied to the second input of AND-gate AD–4 from output circuit 2 of the sequencer-interrogator I. Accordingly, AND-gate AD–4 applies a binary "1" signal through a diode to the input of inhibit gate IG–10 to maintain this gate closed and thereby prevent pulses from being applied to the binary counter C. This is the dwell condition and the controller will remain in this condition displaying a go signal indication to lane A and a stop signal indication to lane B until such time as traffic is detected in phase B.

Upon detection of traffic in lane B, the lane B detector memory DM–1 applies a binary "1" signal to the input of NOR-gate 360 which, in turn, applies a binary "0" signal to the input of AND-gate AD–4. NOR-gate 360 also applies a binary "0" signal to inhibit gate IG–13 so that the positive output on interrogator circuit 2 may be passed through the inhibit gate to interrogate the phase A maximum extension word line MET–A.

Since inhibit gate IG–10 is now open, the binary counter will commence to count pulses supplied by shaper 302. If no additional detections occur during this period at the phase A detector DA, then when the binary counter has reached a count of five pulses a match will be obtained, since word line TM–2 is set with a binary 0101 representative of 5 seconds. This will terminate the main street extension interval and sequencer I will interrogate the memory matrix TM to allocate the main street amber interval.

If, however, a vehicle is detected in phase A prior to five pulses being counted in the example given above, then word line TM–2 will be rewritten to provide an additional unit extension period of time in a manner similar to that described hereinbefore with reference to the cross street extension time-up-date circuit CSE in FIG. 5. Thus, if a vehicle is detected in phase A during this period, a binary "1" signal is applied to one input of AND-gate AD–3. Since output circuit 2 of interrogator I is energized, a binary "1" signal is also applied to the second input of AND-gate AD–3. Accordingly, AND-gate AD–3 interrogates the phase A unit extension word line UET–A, which is set with a binary 0101 representative of 5 seconds. This signal is applied to temporary storage register R3 and is added to the outstanding pulse count by binary adder BA. If the pulse count at the movement is three, then the binary adder will provide a binary signal corresponding to decimal eight. The automatic memory write circuit AMW′ which corresponds with the memory write circuit AMW in FIG. 5 applies the necessary information through inhibit gate IG–16 to rewrite word line TM–2 to store a binary 1000 representative of 8 seconds. This process will continue until such time as a match is obtained at binary counter BC–2 between the outstanding count and the binary signal stored in the phase A maximum extension word line MET–A. In this instance, the binary signal pattern is 1111 representative of 15 seconds. Once 15 pulses have been counted, during the main street extension interval, the maximum timer will time out, that is, a match is obtained at the binary comparator BC–2. When this match is obtained binary comparator BC–2 applies a binary "1" signal to inhibit gate IG–16 to prevent the automatic write circuit AMW′ from rewriting word line TM–2. Therefore, since any further traffic detections in phase A will not result in rewriting word line TM–2, the binary signal pattern stored in word line TM–2 is fixed. Assuming that the fixed pattern is representative of 15 seconds, then once the total count from the commencement of the main street extension interval is 15 pulses, as counted by binary counter C, then a

match is obtained at binary comparator BC–1, which actuates sequencer-interrogator I so that only its output circuit 3 is energized.

With output circuit 3 of sequencer-interrogator I being energized, the main street amber interval will now be timed. During this period, the main street amber signal light will be energized and the cross street red signal light will be energized. As shown in FIG. 9, the main street amber word line memory TM–3 is set for a binary 0011, representative of 3 seconds. Accordingly, once three pulses have been counted by binary comparator C a match is obtained at binary comparator BC–1. Thus, comparator BC–1 will actuate sequencer-interrogator I to energize only its output circuit 4. With output circuit 4 of sequencer-interrogator I being energized, the controller will commence its cross street initial interval with the timing being allocated in accordance with the binary signal stored in word line TM–4. In the example shown in FIG. 9, word line memory TM–4 is set with a binary 0111 representative of 7 seconds. Once seven pulses have been counted by binary counter C a match is obtained. During the interim period, the main street red lamp is energized and the cross street green lamp is energized. Once a match is obtained, the binary comparator BC–1 actuates sequencer-interrogator I to energize only its output circuit 5. The operations which ensue during the cross street extension interval and the succeeding cross street amber interval are the same as that discussed hereinbefore with reference to the main street extension interval MSE and the main street amber interval MSA, respectively, and no further discussion is deemed necessary for a complete understanding of this invention.

Although the invention has been shown in connection with preferred embodiments, it will be readily apparent to those skilled in the art that various changes in form and arrangements of parts may be made to suit requirements without departing from the spirit and scope of the invention as defined by the appended claims.

I claim:

1. In a traffic control system for controlling the time duration that a traffic signal means displays a go signal in at least one traffic lane and having unit extension circuit means for extending the time duration that said go signal is displayed in that lane in dependence upon traffic detected in that lane by a vehicle detector means; the improvement in said unit extension circuit means comprising:

binary signal storage go extension, dual-plate, nondestructive readout, ceramic memory means for storing binary digits wherein the numerical value of said stored binary digits is representative of the time duration of a go extension interval;

a source of trigger pulses;

comparison means responsive to said trigger pulses and to said binary signal storage go extension means for providing an output signal, representative of the termination of said go extension interval, when the number of said trigger pulses is equal to the said stored binary signal; and,

extension interval control means responsive to vehicle detection for acting upon said go extension memory means to change the binary signal stored and thereby vary the time duration of said go extension interval.

2. In a traffic control system as set forth in claim 1, the improvement wherein said extension interval control means includes circuit means adapted to be coupled to a said traffic detector means for varying the binary signal stored by said go extension memory means in dependence upon traffic detected by said detector means.

3. In a traffic control system for controlling the time duration the traffic signal means displays a go signal in at least one traffic lane and having unit extension circuit means for extending the time duration that said go signal is displayed in that lane in dependence upon traffic detected in that lane by vehicle detector means; the improvement in said unit extension circuit means comprising:

binary signal storage go extension memory means for storing binary digits wherein numerical value of said stored binary digits is representative of the time duration of a go extension interval;

a source of trigger pulses;

means for providing an output signal, representative of the termination of said go extension interval, when the number of said trigger pulses is equal to the said stored binary signal; and

extension interval control means, responsive to vehicle detection, for acting upon aid go extension memory means to change the binary signal stored and thereby vary the time duration of said go extension interval,

said extension interval control means including:

binary signal storage unit extension memory means for storing binary signals wherein the numerical value of said stored binary signals is representative of the duration of a unit extension interval;

means for providing a reference binary signal which increases in value in accordance with the number of said trigger pulses provided thus far during the extension interval; and,

memory control means for acting upon said go extension memory means to change the binary signals stored therein in dependence upon the sum of said reference binary signals and the binary signals stored by said unit extension memory means.

4. In a traffic control system as set forth in claim 3, the improvement including means for adding the binary signals stored by said unit extension memory means to said reference binary signals and providing a summation binary signal having a numerical value equal to the summation of the numerical values of said added signals.

5. In a traffic control system as set forth in claim 4, the improvement wherein said memory control means is interposed between said binary adder means and said go extension memory means for changing the binary signals stored therein so that the resultant numerical value is that of said summation of binary signals.

6. In a traffic control system as set forth in claim 3, the improvement including maximum extension interval control means for limiting the time duration of said go extension interval.

7. In a traffic control system as set forth in claim 6, the improvement wherein said maximum extension interval control means includes:

binary signal storage maximum extension memory means for storing a binary signal representative of the duration of the maximum extension interval; and,

means for overriding said memory control means when the number of said trigger pulses provided thus far during the extension interval is equal to the decimal numerical value of the binary signal stored by said maximum extension memory means.

8. In a traffic control system as set forth in claim 7, the improvement including binary counter means for counting said trigger pulses and providing a binary signal which changes in accordance with the number of trigger pulses counted, and

said overriding means includes a binary comparator means for providing an override signal when each of the digits of the binary signal from said counter means is equal to the corresponding digit of the binary signal stored by said maximum extension memory means.

9. In a traffic control system for controlling the time duration that a traffic means displays a go signal in at least one traffic lane and having unit extension circuit means for extending the time duration that said go signal is displayed in that lane in dependence upon traffic detected in that lane by a vehicle detector means; the improvement in said unit extension circuit means comprising:

binary signal storage go extension memory means for storing binary signal digits wherein the numerical value of said stored binary signal digits is representative of the time duration of a go extension interval;

a source of trigger pulses;

binary counting means for counting said trigger pulses and providing a binary signal composed of digits which changes in numerical value in accordance with the number of trigger pulses counted;

means coupled to said binary counting means and said go extension memory means for providing an output signal, representative of the termination of said go extension interval, when the digits of the two binary signals are the same; and,

extension interval control means including circuit means adapted to be coupled to a said traffic detector means for acting upon said go extension memory means to change the binary signal stored thereby in dependence upon traffic detected by said detector means and thereby change the time duration of said go extension interval.

10. In a traffic control system as set forth in claim **9**, the improvement wherein said extension interval control means includes:

binary signal storage unit extension memory means for storing a binary signal representative of the duration of a unit extension interval; and,

memory control means for acting upon said go extension memory means to change the binary signal stored therein in dependence upon the total value of said two binary signals.

11. In a traffic control system as set forth in claim **10**, having maximum extension interval control means for limiting the time duration of said go extension interval the improvement including:

binary signal storage maximum extension interval memory means for storing a binary signal representative of the duration of a maximum extension interval; and,

means for providing an overriding signal, for overriding said memory control means, when the binary signal from said binary counting means equals the binary signal stored by said maximum extension interval memory means.

12. In a traffic control system as set forth in claim **10**, the improvement wherein said unit extension memory means includes a plurality of electrically interrogatable bistable memory means each for storing a binary one or a binary zero signal, each said bistable memory means having an input for receiving an interrogation signal and an output for carrying a binary signal of the character of the stored binary one or binary zero signal in response to receipt of an interrogation signal; and,

unit extension memory actuating means adapted to be coupled to a said traffic detector means and controlled thereby for applying a said interrogation signal to said unit extension memory means so that the outputs of the bistable memory means thereof carry an output binary signal numerically equal to the binary signal stored therein.

13. In a traffic control system as set forth in claim **12**, the improvement including binary adder means for adding said output binary signal of said unit extension memory means to the output binary signal of said binary counting means and providing a summation binary signal numerically equal to the summation of the said added binary signals.

14. In a traffic control system as set forth in claim **13**, the improvement wherein said memory control means includes circuit means for receiving said summation binary signal and acting on said go extension memory means to store a binary signal numerically equal to said summation binary signal to thereby extend the total time duration of said go extension interval.

15. In a traffic control system as set forth in claim **14**, wherein each said bistable memory means includes:

ferroelectric storage capacitor plate means having a surface, said plate means adapted to be polarized in one of two stable states; and,

piezoelectric driving plate means having a portion thereof secured to at least a portion of said surface in such a manner that application of a said interrogation signal to said driving means causes transmission of mechanical forces to said memory plate means in directions acting both laterally and perpendicularly of said surface so that said memory plate means provides an output signal of a binary character in accordance with the state of polarization of said memory means.

16. A traffic actuated traffic controller for controlling the time duration that a traffic signal means displays a go signal in each of at least two traffic lanes wherein for at least one lane the controller is traffic actuatable having traffic detector means associated therewith for registering detected traffic in that lane with the controller and comprising:

a plurality of traffic interval time storage memories wherein each said memory includes:

a plurality of electrically alterable and electrically interrogatable bistable memory means each for storing a binary one or a binary zero signal so that the binary content of a said memory is representative of a desired time duration for an associated traffic interval, each said memory means having an input for receiving an interrogation signal and an output for carrying a said binary signal in response to receipt of an interrogation signal;

interrogating means for sequentially applying interrogation signals to said plurality of bistable memories so that when any one memory is interrogated the outputs of its plurality of bistable memory means provide a binary signal;

a source of equi-time-spaced trigger pulses;

means for actuating said interrogating means to interrogate the next succeeding of said plurality of memories when the number of said trigger pulses received is equal to the numerical value of the binary signal on the outputs of the memory means of the memory last interrogated;

each said traffic lane having associated therewith at least one said memory serving as a go initial time storage memory and each said lane also having associated therewith another memory serving as a go extension time storage memory; and,

extension interval control means including circuit means adapted to be coupled to a traffic detector means associated with said lane for electrically altering said go extension memory means to change the binary signal stored thereby in dependence upon traffic detected by said detector means and thereby change the time duration of the go extension interval.

17. A traffic actuated traffic controller as set forth in claim **16** wherein said extension control means includes a unit extension time storage memory constructed as each of said plurality of memories for storing a binary signal wherein the numerical value of the binary content is representative of the duration of a unit extension interval;

unit extension actuating means adapted to be coupled to a said detector means associated with said lane and controlled thereby for applying an interrogation signal to said unit extension time storage memory so that the outputs of the bistable memory means thereof carry an output binary signal numerically equal to the binary signals stored therein; and,

circuit control means for electrically altering said go extension time storage memory so that the binary signals stored therein provide at least one unit extension interval.

18. A traffic-actuated traffic controller as set forth in claim **17** including binary counter means for counting said trigger pulses and providing a binary signal which changes in accordance with the number of trigger pulses counted;

binary adder means for adding said output binary signal of said unit extension time storage memory to the output binary signal of said binary counting means and providing a summation binary signal equal to the summation of the said added binary signals; and,

said circuit control means includes circuit means for receiving said summation binary signal and electrically altering said go extension time storage memory to store a binary signal equal to the summation binary signal to thereby extend the total time duration of said go extension interval.

19. A traffic-actuated traffic controller as set forth in claim 18 including maximum extension interval control means for limiting the duration of said go extension interval.

20. A traffic-actuated traffic controller as set forth in claim 19 wherein said maximum extension interval control means includes:

a maximum extension time storage memory constructed as each of said plurality of bistable memories for storing a binary signal wherein the binary content is representative of the duration of a maximum extension interval, said maximum extension time storage memory being coupled to said interrogating means so as to be interrogated concurrently with said go extension time storage memory; and,

comparator means for providing an overriding signal, for use in overriding said extension interval control means, when the binary signal stored by said maximum extension time storage memory is equal to output binary signal from said binary counter means.

* * * * *