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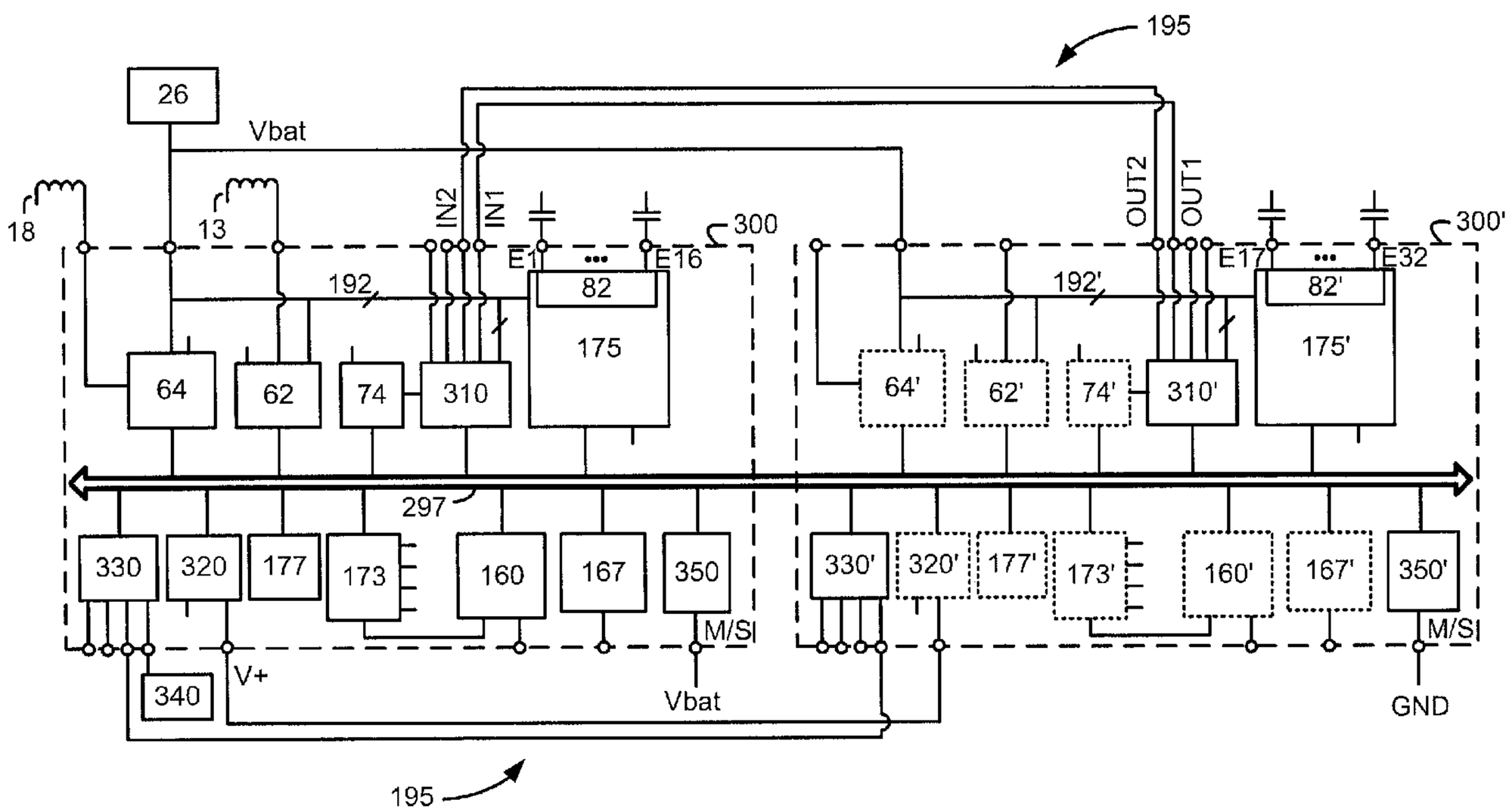
(54) Title: ARCHITECTURES FOR AN IMPLANTABLE MEDICAL DEVICE SYSTEM HAVING DAISY-CHAINED ELECTRODE-DRIVER INTEGRATED CIRCUITS



(57) Abrégé/Abstract:
Architectures for an implantable neurostimulator system having a plurality of electrode-driver integrated circuits (ICs) in provided. Electrodes from either or both ICs can be chosen to provide stimulation, and one of the IC acts as the master while the other acts as the slave. A parallel bus operating in accordance with a communication protocol couples the ICs, and certain functional blocks not needed in the slave are disabled. Stimulation parameters are loaded via the bus into each IC, and a stimulation enable command is issued on the bus to ensure simultaneous stimulation from the electrodes on both ICs. Clocking strategies are also disclosed to allow clocking of the master and slave ICs to be independently controlled, and to ensure that relevant internal and bus clocks used in the system are synchronized.

ABSTRACT

Architectures for an implantable neurostimulator system having a plurality of electrode-driver integrated circuits (ICs) in provided. Electrodes from either or both ICs can be chosen to provide stimulation, and one of the IC acts as the master while the other acts as the slave. A parallel bus operating in accordance with a communication protocol couples the ICs, and certain functional blocks not needed in the slave are disabled. Stimulation parameters are loaded via the bus into each IC, and a stimulation enable command is issued on the bus to ensure simultaneous stimulation from the electrodes on both ICs. Clocking strategies are also disclosed to allow clocking of the master and slave ICs to be independently controlled, and to ensure that relevant internal and bus clocks used in the system are synchronized.

ARCHITECTURES FOR AN IMPLANTABLE MEDICAL DEVICE SYSTEM HAVING DAISY-CHAINED ELECTRODE-DRIVER INTEGRATED CIRCUITS

FIELD

The present invention relates generally to implantable medical devices, and more particularly to improved architectures for an implantable neurostimulator utilizing a plurality of electrode-driver integrated circuits.

BACKGROUND

Implantable neurostimulator devices are devices that generate and deliver electrical stimuli to body nerves and tissues for the therapy of various biological disorders, such as pacemakers to treat cardiac arrhythmia, defibrillators to treat cardiac fibrillation, cochlear stimulators to treat deafness, retinal stimulators to treat blindness, muscle stimulators to produce coordinated limb movement, spinal cord stimulators to treat chronic pain, cortical and deep brain stimulators to treat motor and psychological disorders, and other neural stimulators to treat urinary incontinence, sleep apnea, shoulder subluxation, etc. The description that follows will generally focus on the use of the invention within a Spinal Cord Stimulation (SCS) system, such as that disclosed in U.S. Patent 6,516,227. However, the present invention may find applicability in any implantable neurostimulator.

As shown in Figures 1A and 1B, a SCS system typically includes an Implantable Pulse Generator (IPG) 100, which includes a biocompatible device case 30 formed of a conductive material such as titanium for example. The case 30 typically holds the circuitry and battery 26 necessary for the IPG to function, although IPGs can also be powered via external RF energy and without a battery. The IPG 100 includes one or more electrode arrays (two such arrays 102 and 104 are shown), each containing several electrodes 106. The electrodes 106 are carried on a flexible body 108, which also houses the individual electrode leads 112 and 114 coupled to each electrode. In the illustrated embodiment, there are

eight electrodes on array 102, labeled E_1-E_8, and eight electrodes on array 104, labeled E_9-E_{16}, although the number of arrays and electrodes is application specific and therefore can vary. The arrays 102, 104 couple to the IPG 100 using lead connectors 38a and 38b, which are fixed in a non-conductive header material 36, which can comprise an epoxy for example.

As shown in Figure 2, the IPG 100 typically includes an electronic substrate assembly 14 including a printed circuit board (PCB) 16, along with various electronic components 20, such as microprocessors, integrated circuits, and capacitors mounted to the PCB 16. Two coils (more generally, antennas) are generally present in the IPG 100: a telemetry coil 13 used to transmit/receive data to/from an external controller 12; and a charging coil 18 for charging or recharging the IPG's battery 26 using an external charger 50. The telemetry coil 13 is typically mounted within the header 36 of the IPG 100 as shown, and may be wrapped around a ferrite core 13'.

As just noted, an external controller 12, such as a hand-held programmer or a clinician's programmer, is used to wirelessly send data to and receive data from the IPG 100. For example, the external controller 12 can send programming data to the IPG 100 to dictate the therapy the IPG 100 will provide to the patient. Also, the external controller 12 can act as a receiver of data from the IPG 100, such as various data reporting on the IPG's status. The external controller 12, like the IPG 100, also contains a PCB 70 on which electronic components 72 are placed to control operation of the external controller 12. A user interface 74 similar to that used for a computer, cell phone, or other hand held electronic device, and including touchable buttons and a display for example, allows a patient or clinician to operate the external controller 12. The communication of data to and from the external controller 12 is enabled by a coil (antenna) 17.

The external charger 50, also typically a hand-held device, is used to wirelessly convey power to the IPG 100, which power can be used to recharge the IPG's battery 26. The transfer of power from the external charger 50 is enabled by a coil (antenna) 17'. The external charger 50 is depicted as having a similar construction to the external controller 12, but in reality they will differ in accordance with their functionalities as one skilled in the art will appreciate.

Wireless data telemetry and power transfer between the external devices 12 and 50 and the IPG 100 takes place via inductive coupling, and specifically magnetic inductive coupling. To implement such functionality, both the IPG 100 and the external devices 12 and 50 have coils which act together as a pair. In case of the external controller 12, the relevant pair of coils comprises coil 17 from the controller and coil 13 from the IPG 100. In case of the external charger 50, the relevant pair of coils comprises coil 17' from the charger and coil 18 from the IPG 100. As is well known, inductive transmission of data or power can occur transcutaneously, i.e., through the patient's tissue 25, making it particularly useful in a medical implantable device system. During the transmission of data or power, the coils 17 and 13, or 17' and 18, preferably lie in planes that are parallel, along collinear axes, and with the coils as close as possible to each other. Such an orientation between the coils 17 and 13 will generally improve the coupling between them, but deviation from ideal orientations can still result in suitably reliable data or power transfer.

U.S. Patent Publication 2008/0319497 ("the '497 application"), owned by the present assignee discloses an improved architecture 150 for an IPG 100, which is shown in Figures 3A-3C. Because of its pertinence to the present disclosure, some time is spent discussing pertinent aspects of the '497 application's architecture.

The improved IPG architecture 150 of Figure 3A involves integration of various IPG functional circuit blocks on a single integrated circuit (IC) 200 via a bus 190 governed by a communication protocol, discussed further below. The centralized bus 190 is a parallel bus containing a plurality of multiplexed address and data lines operating in parallel. However, this is not strictly necessary, and instead bus 190 can comprise a serial bus as well. To communicate with the bus 190 and to adhere to the protocol, each circuit block includes bus interface circuitry 215 adherent with that protocol. Because each circuit block complies with the protocol, any given circuit block can easily be modified or upgraded without affecting the design of the other blocks, facilitating debugging and upgrading of the IPG circuitry. Moreover, because the centralized bus 190 can be

taken off the integrated circuit, extra circuitry can easily be added off chip to modify or add functionality to the IPG, a point discussed further below.

Each of the circuit blocks performs standard functions in an IPG. For example, telemetry block 62 couples to the IPG telemetry coil 13, and includes transceiver circuitry for communicating with the external controller 12 (Fig. 2). The charging/protection block 64 couples to the IPG charging coil 18, and contains circuitry for rectifying power received from the external charger 50 (Fig. 2), and for charging the power source (battery) 26 in a controlled fashion. Stimulation circuit block 175 is coupled to the electrodes E1-E16 and includes circuitry for setting the program (magnitude, and polarity) for the stimulation pulses appearing at those electrodes. Block 175 also includes the drivers for the electrodes, with a Digital-to-Analog Converter (DAC) 82 being responsive to the stimulation program to supply the specified electrodes currents. Notice that the electrodes E1-E16 are connected to off-chip decoupling capacitors C1-CN prior to connection to the corresponding electrodes 106 on the leads 102 and 104 (Fig. 1A); such decoupling capacitors C1-CN prevents direct DC current injection from the IPG into the patient, which is advisable for safety, but otherwise such decoupling capacitors do not affect stimulation performance. EPROM block 177 caches any relevant data in the system (such as log data), and additional memory 66 can also be provided off-chip via a serial interface block 167. Analog-to-Digital (A/D) block 74 digitizes various analog signals for interpretation by the IPG 100, such as the battery voltage Vbat or voltages appearing at the electrodes, and is coupled to an analog bus 192 containing such voltages. Interrupt controller block 173 receives various interrupts from other circuit blocks, which because of their immediate importance are received independent of the bus 190 and its communication protocol. Note that because it handles both analog and digital signals, IC 200 comprises a mixed mode chip.

Stimulation circuit block 175 is coupled to the electrodes E1-E16 and includes circuitry for setting the program (magnitude, and polarity) for the stimulation pulses appearing at those electrodes. Block 175 also includes the drivers for the electrodes, with a Digital-to-Analog Converter (DAC) 82 being responsive to the stimulation program to supply the specified electrodes currents.

Notice that the electrodes E1-E16 are connected to off-chip decoupling capacitors C1-CN prior to connection to the corresponding electrodes 106 on the leads 102 and 104 (Fig. 1A); such decoupling capacitors C1-CN prevent direct DC current injection from the IPG into the patient, which is advisable for safety, but otherwise such decoupling capacitors do not significantly affect stimulation performance.

Internal controller 160 acts as the master controller for all other circuit blocks. Specifically, each of the other circuit blocks contains set-up and status registers (not shown). The set-up registers are written to by the controller 160 upon initialization to configure and enable each block. Each circuit block can then write pertinent data at its status register, which can in turn be read by the controller 160 as necessary. Aside from such control imposed by the master controller 160, the circuit blocks outside of the controller 160 can employ simple state machines to manage their operation, which state machines are enabled and modified via the set-up registers.

As can be seen in Figure 3A, the IC 200 contains several external terminals 202 (e.g., pins, bond pads, solder bumps, etc.), such as those necessary to connect the power source 26, to connect the coils 18, 13, to connect the external memory 66, and to connect the stimulation electrodes. Other external terminals 202 are dedicated to the various signals that comprise the centralized bus 190 to allow this bus to communicate with other devices outside of the IC 200.

The various signals comprising the bus 190 can be seen in Figure 3B, which also discloses the protocol for communications on the bus. As shown, the centralized bus 190 comprises a clock signal (CLK) for synchronization, time-multiplexed address and data signals (A/Dx); an address latch enable signal (ALE); an active-low write enable signal (*W/E), and an active-low read enable signal (*R/E). The frequency for the clock signal, CLK, can be in the range of 32 kHz to 1 MHz, which is generally slow for a computerized protocol, but is suitably fast for operation of the IPG, which typically provides stimulation pulses on the order of tens of microseconds to milliseconds. As shown, the protocol uses a fairly simple address-before-data scheme in which an address is followed by pertinent data for that address. To discern between address and data, the address

latch enable signal (ALE) is active only upon the issuance of an address, which allows the address to be latched upon the falling edge of the clock. Whether the data corresponding to a particular address is to be written or read on the next falling clock edge depends on the assertion of the write and read enable signals (*W/E; *R/E).

The nature of this protocol means that all functional blocks coupled to the centralized bus 190 are designated an address, or more likely, a range of addresses. For example, the address for a data register holding the value for the compliance voltage (in A/D block 74) might be ADDR[3401], while the address for the magnitude and duration of stimulation to be provided by electrode E6 (in stimulation circuitry block 175) may be ADDR[7655] and ADDR[7656] respectively. To assist the various functional blocks in recognizing pertinent addresses, and to ensure each block's ability to function in accordance with the centralized bus 190's protocol, each block contains bus interface circuitry 215. As this bus interface circuitry was described in detail in the above-identified '497 application, such details are not repeated here.

As noted in the '497 application, when the circuit blocks are coupled via the bus 190 and communicate using the protocol, it becomes a relatively simple matter to make changes to any particular block to fix circuit errors, and/or to upgrade the IC 200 for use in next-generation IPGs. Additionally, because the bus 190 is provided outside of the IC 200, it is easy to modify or add functionality to the IPG 100 outside of the IC 200. For example, and as shown in Figure 3C, more memory 300 (preferably, nonvolatile memory) can be added. Or, systemic control can be added outside of the IC 200, for example, via an external microcontroller 240. Should an external microcontroller 240 be used in conjunction with the IC 200, the '497 application discusses manners in which control is arbitrated between the microcontroller 204 and the internal controller 160 in the IC 200. Again, such details are not repeated here.

In another off-chip extension of the architecture noted in the '497 application, and as particularly pertinent to the present disclosure, another IC 200' can be added which is similarly constructed to the first IC 200. This allows the IPG 100 in which the IC 200 and 200' are placed to provide 32 stimulation

electrodes, i.e., 16 each from both of the ICs. In other words, the capacity of the IPG can be increased by "daisy chaining" a plurality of stimulation ICs together. In such an embodiment, the internal controller 160 in one of the ICs 200 or 200' can be inactivated so only one controller 160 acts as the master controller for the system.

Practical concerns arising from the use of electrode drivers in two different ICs 200 are addressed in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B show an implantable pulse generator (IPG), and the manner in which an electrode array is coupled to the IPG in accordance with the prior art.

Figure 2 illustrates an IPG, an external controller, and an external charger in accordance with the prior art.

Figures 3A-3C illustrate aspects of an IPG architecture using a centralized bus, as disclosed in U.S. Patent Publication 2008/0319497.

Figures 4A-4C illustrate aspects of an improved architecture for an IPG utilizing a plurality of electrode-driver ICs.

Figure 5 illustrates circuitry, timing, and bus commands for simultaneously providing a situation pulse at electrodes on different of the electrode-driver ICss in the improved architecture.

Figure 6 illustrates sample and hold circuitry in the master IC, and illustrates bus commands for monitoring a voltage at an electrode at the master IC using the sample and hold circuitry.

Figures 7A and 7B illustrate sample and hold circuitry in the master and slave ICs, and illustrates bus commands for monitoring a voltage at an electrode at the slave IC using the sample and hold circuitry at the master IC.

Figures 8A and 8B illustrate sample and hold circuitry in the master and slave ICs, and illustrates bus commands for monitoring a resistance between an electrodes at the slave IC and an electrode at the master IC using the sample and hold circuitry at the master IC.

Figures 9A-9C illustrate sample and hold circuitry in the master and slave ICs, and illustrates bus commands for monitoring a resistance between two electrodes at the slave IC using the sample and hold circuitry at the master IC.

Figure 10 illustrates aspects of the improved architecture relating to the clocking circuitry, and shows circuitry for disabling clocking at the slave IC as a power saving measure.

DETAILED DESCRIPTION

Figure 4A shows an improved system 290 for an IPG 295 having an improved architecture in which two electrode driver ICs 300 and 300' are daisy chained to double the electrode capacity in the IPG, i.e., from 16 to 32 electrodes as shown. (The metallic case of the IPG 295 can also comprise an electrode, but this is not shown for simplicity). In this example, one of the ICs 300 acts as a master, while the other 300' acts as a slave, as will be explained in further detail below. Both ICs 300 and 300' are connected to a bus 297, which is similar to the bus described in the Background, but which includes additional control signals for selecting either of the two chips: CS_m, which comprises a chip select for the master 300, and CS_s, which comprises a chip select for the slave 300'. Note that while the clock signal (CLK; Fig. 3B) remains important in the communication protocol, it is not included as one of the bus signals shared by all ICs in the system; clocking circuitry in the system 290 is discussed further with reference to Figure 10 below.

Also connected to the bus is a microcontroller 305, which provides for control of functions in the system 290 not handled by various circuit blocks in the ICs 300 and 300', and otherwise generally acts as the system's master. For example, bus communications are ultimately controlled by the microcontroller 305, which controls the issuance of clocks needed for the communication protocol as explained further below, and which also issues the bus control signals (e.g., ALE, W/E*, R/E* in Fig. 3B). In another example, microcontroller 305 schedules when the IPG 295 is to listen for telemetry from the external controller 12 (Fig. 2). See, e.g., U.S. Patent 7,725,194, discussing this issue in further detail. Microcontroller 305 also connects to a memory (Flash EPROM) chip 307 in the

system 290, which can hold the operating software for the system, and which can also act as a free space to log data in the system, e.g., data to be reported to the external controller 12 for analysis and/or feedback to the patient.

In the embodiment shown, each of the ICs 300 and 300', which will be explained in detail shortly, are fabricated identically, even though they are destined to act as master or slave in the system. Fabricating only a single electrode-driver IC is a great convenience, as the manufacturer does not have to different fabricate, track, and test, separate master and slave ICs for the system 290. Whether any given IC operates as a master or slave in the system depends on how it is connected to the remainder of the system 297, i.e., such chips are bond programmable. As shown in Figure 4A, each IC has an input, M/S, which when provided a voltage informs the IC that it is the master 300, and when not informs the IC that it is a slave 300'. This can be accomplished by connecting the M/S input to a particular node on the IPG's PCB, such as Vbat, the battery 26 voltage (Fig. 2), in the case of the master 300, or ground (GND) in the case of the slave 300'. When a given IC understands that it is operating as a slave, it deactivates certain of its circuit blocks, as will be explained later.

Also shown in Figure 4A are certain off-bus signals 195. These signals and their functions will be discussed in more detail later.

Figure 4B shows the circuit blocks in either of the identical master 300 or slave 300' ICs. Many of these circuit blocks were discussed earlier in conjunction with the Background (see Fig. 3A), and so discussion of those blocks is not repeated here. Of particular note and new to Figure 4B are the sample and hold block 310, the compliance voltage (V+) generator block 320, the clock generator block 330, and a master/slave (M/S) controller 350. As with other circuit blocks on the IC, these circuit blocks contain interface circuitry 215 to allow them to communicate on, and be controlled by, the bus 297 in accordance with the protocol discussed earlier.

Sample and hold circuitry block 310 will be explained in detail later, but for now merely note that it contains circuitry for sampling and holding various analog voltages comprising the analog bus 192, including the electrode voltages. Once sample and hold block 310 has operated to resolve a particular voltage, it

can be sent to the A/D block 74, where it is digitized and disseminated via the communication bus 297 to wherever in the system 290 it is needed for analysis. Signals IN1, IN2, OUT1 and OUT2 are used to route various analog signals between the two ICs 300 and 300', as explained later.

V+ generator block 320 generates a compliance voltage, V+, which is used by the current sources (DAC 82) in the stimulation circuitry block 175. It does so by voltage boosting the battery voltage, Vbat, to an appropriate V+ voltage used to power the current sources to an optimal level, which optimal level can be deduced in part by monitoring the electrode voltages during stimulation. See, e.g., U.S. Patents 7,872,884; 7,444,181; 7,539,538, for further details concerning the generation of compliance voltage V+ in an IPG.

Clock generator 330 generates the communications clocks used by the communications protocol on the bus 297. As noted earlier though, a clocking signal does not comprise part of the communication bus 297. Operation of the clock generator 330 will be explained in detail with respect to Figure 10.

Master/slave controller 350 receives the M/S input mentioned earlier, and interprets that input to inform the IC whether it is operating and a slave or master, and this is illustrated further in Figure 4C. In Figure 4C, the master and slave 300 and 300' are shown as connected, including bus-based 297 and off-bus 195 connections. Note that corresponding circuit blocks in the slave IC 300' are denoted by a prime symbol. As described earlier, the M/S inputs to the master/slave controllers 350 differ (high; low) depending on which IC is acting as the master or slave. In the slave IC 300' the master/slave controller 350' interprets the grounded input, and informs certain other circuit blocks that they are to be disabled in favor of use of those same circuit blocks in the master IC 300. Specifically, the charging/protection block 64', telemetry block 62' A/D block 74', V+ generator 320', interrupt controller 173', and the internal controller 160' are all disabled in the slave IC 300', and are shown in dotted lines to illustrate that fact. Disabling of each of these circuit blocks can occur in accordance with the state machines operating at each block upon receipt of information from the master/slave controller 350, and such disabling can be effected by disabling the bus drivers and bus receivers operating in the interface circuitry in the affected

blocks (see the above-identified '497 application). Still operative in the slave IC 300' however are the stimulation circuitry block 175' coupled to the electrodes, the sample and hold circuit block 310', the clock generation circuitry 330', and the master/slave controller 350' itself.

With regard to the various off-chip signals 195, note that the compliance voltage, V+, generated in the master IC 300 is routed to the slave IC 300' for use in the slave's stimulation circuitry block 175'. The changing and telemetry coils 18 and 13 are only coupled to the master IC 300 where their corresponding blocks 64 and 62 are active. The battery 26 (Fig. 2) voltage, Vbat, is shared by both ICs 300 and 300' (as well as the microcontroller 305), and other components internal to the IPG 100. An external crystal oscillator 340 is coupled to the CLKIN input only on the master IC 300.

Figures 5-9C illustrate the operation of the sample and hold circuitry blocks 310 and 310' active in both ICs 300 and 300', and further illustrate how off-bus signal 195 carried between IN1, IN2, OUT1, and OUT2 are used in the system to monitor analog signals in both ICs. Additionally, these Figures provide examples of commands used on the bus 297 to provide the desired stimulation and monitoring functions.

Figure 5 shows an example of the stimulation that can be provided by the system 290, and in particular shows the provision of a monophasic pulse train to a patient's tissue, which is represented in Figure 5 as a resistance, R. (System 290 can similarly provide biphasic pulses as one skilled in the art understands, and as is explained in the above-identified concurrent application. However, monophasic pulses are illustrated for simplicity). In the example shown, electrode E1 from the master IC 300 is used as the anode which sources a current +I for a pulse duration of t_D, and electrode E17 from the slave IC 300 is used as the cathode for the sink of that current (-I). The pulses at both electrodes have a periodicity of t_P.

The currents (+I, -I) appearing at each electrode are set by Digital-to-Analog Converters, or DACs 82, which comprises part of the stimulation circuitry 175. As is known, the DACs 82 provide the desired current based on digital control signals (<P>, <N>), which control signals specify the amount that a reference current, Iref, is to be amplified. A DAC used as the anodic source is

called a PDAC, while a DAC used as the cathodic sink is called a NDAC. See, e.g., U.S. Patent Publication 2007/0038250, for further details concerning the specifics of PDAC and NDAC circuitry useable in a system such as system 290. Because electrodes E1 and E17 in this example are respectively driven by the master and slave ICs 300 and 300', the stimulation circuitry 175 and 175' and DACs 82 and 82' at each are implicated in providing the desired pulses. Of course, more than one electrode in each of the stimulation circuitries 175 and 175' may be enabled at one time, but only a single electrode for each is shown in Figure 5 for simplicity.

Prior to the delivery of the desired pulses, the stimulation circuitry 175 in each of the ICs is loaded with the appropriate stimulation parameters. These parameters (magnitude and polarity of current) are communicated via bus 297 from the microcontroller 305 based upon the therapy program that has been established for the patient, which therapy program can be changed from time to time by the external controller 12 (Fig. 2). As noted earlier, the bus-based communication protocol allows for these parameters to be sent to various addresses designated for the various circuit blocks. For example, the magnitude for the current at electrode E1 may be stored at ADDRi in the stimulation circuitry 175, while the polarity is stored at ADDRj. These parameters can be loaded serially for each electrode, and in advance of the issuance of the pulse. Thus, and referring to the command table in Figure 5, it is seen that these parameters are loaded for each of electrodes E1 and E17 before t1—the first pulse in the train.

When ICs 300 and 300' are daisy chained as disclosed, it is important to properly differentiate between active circuit blocks in each of the two ICs. For example, and as discussed earlier with respect to Figure 4C, the stimulation circuitry block 175', the sample and hold circuit block 310', and the clock generation circuitry 330', are active in both ICs, and share the same addresses. Differentiation between the two ICs occurs by use of the chip select signals, CS_m and CS_s. Thus, as shown in Figure 5, although E1 and E17 are associated with the same addresses ADDRi and ADDRj, the chip select signal is used to differentiate them and to program the stimulation circuitry 175 in the appropriate ICs. Thus, the stimulation parameters for electrode E1 are written to ADDRi and j

with CS_m asserted, indicating programming of the stimulation circuitry 175 in the master IC 300 (i.e., that which drives electrodes E1-E16). By contrast, the stimulation parameters for electrode E17 are written to ADDRi and j with CS_s asserted, indicating programming of the stimulation circuitry 175 in the slave IC 300' (i.e., that which drives electrode E17-E32).

It is important to synchronize therapeutic pulses occurring at electrodes in each of the ICs 300 and 300'. Thus, after the stimulation parameters have been loaded, it must be ensured that the stimulation pulses will issue from the various electrodes on the ICs 300 and 300' at the same time. For example, if the anodic pulse issues from electrode E1 issues slightly prior to the issuance of the cathodic pulse at electrode E17, charge will be injected into the patient's tissue during that slight time with no return path. Likewise, if the anodic pulse ceases from electrode E1 issues slightly prior to cessation of the cathodic pulse at electrode E17, charge will be depleted from the patient's tissue during that slight time. Such charge build up can impede therapy, or could injure the patient.

To ensure simultaneous issuance of the pulses, bus-based communication is used in system 290 to simultaneously trigger the issuance of both pulses. As shown in Figure 5, at time t1, i.e., after the stimulation parameters for each electrode have been loaded to each of the ICs 300 and 300', a paralleled multi-bit stimulation enable command is issued on the bus with both of the chip select signals asserted (i.e., CS_m = CS_s = 1). This allows both of stimulation circuitries 175 and 175' to receive the stimulation enable signal at the same time, and to provide the pre-stored stimulation parameters to their DACs 82 and 82', thus producing the desired currents simultaneously. Specifically, the stimulation enable command simultaneously enables both of DACs 82 and 82' by issuing the appropriate control signals <P> and <N> for an appropriate length of time. In this example, the stimulation enable command is sent to a register with ADDRk. If not pre-loaded as a stimulation parameter, the pulse duration t_D can be included with the simulation enable command.

Another important issue, and one addressed in the improved system 290, deals with monitoring various voltages in the ICs 300 and 300', such as the electrode voltages. Assessing such voltages is beneficial for many reasons.

Knowing the voltages present at the electrodes during stimulation can be useful in setting the compliance voltage, V+, at the V+ generator 320 (Fig. 4B) to an appropriate and power-efficient magnitude. See, e.g., U.S. Patent 7,444,181. Also, knowing the electrode voltages allows the resistance between the electrodes, R, to be calculated, which is useful for a variety of reasons.

Voltage monitoring in any given IC 300 is performed by the sample and hold circuitry 310, which is shown in Figure 6. As shown, sample and hold circuitry 310 comprises two multiplexers (MUX1 ad MUX2), either of which can select from a plurality of signals comprising the analog bus 192 (Fig. 4B), such as the electrode voltages (E1-E16), the voltage on the metallic case, the battery voltage (Vbat), the compliance voltage (V+), or ground (GND). Each MUX receives a control signal to choose one of these various inputs. (In reality, the control signal for each MUX may comprise a plurality of digital control signals. For example, if the MUX is capable of selecting from 16 different inputs, then four control signals may be used).

Figure 6 shows the example of measuring the voltage on electrode E1 during stimulation. MUX1 chooses this electrode via control signal(s) SEL_E1, which allows the voltage on E1 to pass to OUT1. MUX2 chooses ground (GND) as a reference (e.g., 0 Volts), which is passed to OUT2. As shown in the command table in Figure 6, both of these selections can be made via the bus 297 at an appropriate time during the duration of the pulse (i.e., during t_D), where it is assumed that MUX1 is accessible via ADDRr and MUX2 via ADDRs. Because the voltage, V_{E1}, being monitored is already present at the master IC 300, the chip select signals are set accordingly (CS_m = 1, CS_s = 0). Intervening between these outputs OUT1 and OUT2 is holding circuitry 312. Holding circuitry 312 can comprise any circuitry suitable for holding and stabilizing the voltage to be measured, and as illustrated comprises a single capacitor, C. However, more sophisticated holding circuitry 312 can be used, such as the circuitry disclosed in above-identified concurrent application. Alternatively, and particularly when DC voltages are being monitored, holding circuitry 312 can be dispensed with altogether.

The voltages on each plate of the capacitor are sent to a differential amplifier 314, which after a settling period outputs the difference between the two, which in this case is $V_{E1} - 0$ or V_{E1}. This analog voltage can then be sent to A/D block 74 (Fig. 4B), where it is digitized. This value can then be read (at ADDRt in A/D block 74), and used elsewhere in the system, such as the V+ generator 320 (Fig. 4B).

When the voltage being measured comes from the slave IC 300' instead of the master 300, the interconnection between the two sample and hold circuitries 310 and 310' is implicated, as shown in Figure 7A. Such interconnection involves the use of off-bus signals IN1, IN2, OUT1, and OUT2, which were briefly mentioned earlier, and which are shown at a high level in Figure 4A. As shown there, and in further detail in Figure 7A, note that OUT1 from MUX1 on the slave IC 300' is sent to IN1 in the master IC 300, which in turn is sent as an input to both of the master IC's MUXes. OUT2 from MUX2 on the slave IC 300' is sent to IN2 in the master IC 300, which again is sent as in input to both of the master IC's MUXes. This interconnection of the sample and hold circuitries 310 and 310' operates to pull any relevant voltages to be monitored from the sample and hold circuitry 310' in the slave IC 300' to the sample and hold circuitry 310 in the master IC 300. Because the holding circuitry 312' and differential amplifier 314' are not used in the slave IC 300', they are illustrated in dotted lines in Figure 7A. This interconnection of the sample and hold circuitries 310 and 310' also result in inputs IN1 and IN2 to the MUXes in the slave not being used, and the outputs OUT1 and OUT2 in the master not being used, which again is represented by dotted lines. Routing on the PCB between the two IC 300 and 300' establishes the proper connections between OUT1 and OUT2 from the slave IC 300', and IN1 and IN2 in the master IC 300.

Figure 7A illustrates monitoring the voltage on electrode E17 (that is, E1 from the slave IC 300'), with the command table for doing the same provided in Figure 7B. E17 is selected at MUX1 via its MUX address ADDRr, but with the slave IC selected (CS_s = 1, CS_m = 0). Because no other voltage is of interest is pulled from the slave IC, MUX2 in the slave selects no value. The output from MUX1, OUT1, is routed off chip to input IN1 on the master IC 300, where it is

selected at MUX1. Again, MUX1 is addressed at ADDRr, but this time with the master selected (CS_m = 1, CS_s = 0), which routes the voltage on E17 to the top plate of the capacitor in sample and hold circuit 312. Because in this example it is desired to know the absolute value of the voltage on E17, MUX2 (address ADDRs) in the master selects the ground input, which routes ground to the bottom plate of the capacitor. After allowing for settling, differential amplifier 314 outputs the difference between its two inputs, V_{E17}, which can then be passed to A/D block 74 for interpretation as discussed before.

Monitoring the voltages at electrodes during stimulation is further useful in calculating the resistance between electrodes, and examples using sample and hold circuitry 310 to do so are shown in Figures 8A-9C. Figure 8A and 8B continue the example of Figure 5, but with the goal of determining the resistance R between anode electrode E1 and cathode electrode E17. Such a resistance measurement requires assessment of the voltages at both electrodes, V_{E1} and V_{E17}. Here, only one of the voltages (E17) needs to be pulled from the slave IC 300' to the sample and hold circuit 310 in the master IC 300. Because this electrode is the cathode, MUX2 is selected at the slave (ADDRs; CS_s = 1; CS_m = 0) to pull this voltage to IN2 at the master IC 300. Anode electrode E1 is selected by MUX1 at the master (ADDRr; CS_m = 1; CS_s = 0), and IN2 (E17 as pulled from the slave IC 300') is selected by MUX2 at the master (ADDRs; CS_m = 1; CS_s = 0). The resulting voltage difference across the capacitor in holding circuitry 312 ($V_{E1} - V_{E17}$) is then reflected at the output of the differential amplifier 314. Because the current used to form these voltages is known (I), the resistance between the electrodes can be calculated in the IPG 295 as $(V_{E1} - V_{E17}) / I$, with perhaps some adjustment to the calculation to account for small voltage drops across the decoupling capacitor, a point discussed in further detail in the concurrent application.

Figures 9A-9C illustrate a more complicated case in which the resistance between anode electrode E32 and cathode electrode E17 are measured as shown in Figure 9A. Here, both electrodes appearing in the slave IC 300'. Because of this, and as shown in Figure 9B, the voltages for each of these electrodes are selected by MUX1 and MUX2 respectively in the slave, which pass them to the master IC

300 at inputs IN1 and IN2 respectively. The MUXes in the master sample and hold circuit 310 then choose these inputs IN1 and IN2, placing the voltage of the anode (E32) on top of the capacitor, and the voltage of cathode E17 on the both of the capacitor in the holding circuit 314. As before, the differential amplifier 314 outputs the difference between the two ($V_{E32} - V_{E17}$), and the resistance between then can then be calculated using the known current, I.

Another significant issue addressed by improved system 290 involves clocking, the details of which are shown in Figure 10. Each of the devices (the microcontroller 305, the master IC 300, and the slave IC 300') requires clocks to function. Each requires clocks to run their internal functions ("internal clocks"), as well as clocks to communicate on the bus 297 ("bus clocks") according to the protocol described earlier (see Fig. 3B). For communications on the bus 297 to be orderly, the bus clocks should be synchronized at each of the devices.

However, there may be times during operation of system 290 when certain internal or bus clocks are not needed. For example, when either the master IC 300 or slave IC 300' are performing an internal operation (e.g., providing stimulation) not requiring bus communications, bus clocking is not required, and only the devices' internal clocks need to be active. In another example, there may be periods of time when only the master IC 300 needs to be clocked. Consider the use of the system 290 when only electrodes on the master IC 300 (E1-E16) are required for patient therapy. During such periods of time, the slave IC 300' may not need to be clocked at all, as that device will neither need to communicate on the bus 297 nor perform any internal operations. In short, not all of the devices in the system 290 will require their internal or bus clocks to be active at a given time. When a particular clock is not required, it is desirable to disable it: significant power can only be drawn during clock transitions, and so shutting down unnecessary clocks in the system save powers, which power is usually limited by the capacity of the battery 26 (Fig. 4B). The disclosed system therefore uses discrete bus and internal clocks in the system, which clocks can be selectively enabled or disabled as needed. Because independent control of particular clocks is desired, a master clock signal is not distributed by the bus 297, as will be made clear below.

Figure 10 shows the various internal and bus clocks. Microcontroller 305 uses clock signal BUSCLKμc to communicate on the bus 297, and uses clock CLKμc as its internal clock. As noted earlier, the bus protocol can operate relatively slowly, and so BUSCLKμc can be relatively slow, e.g., on the order of 100 kHz. By comparison, the internal clock signal CLKμc that runs the internal functions of the microcontroller 305 can be relatively fast, on the order of several MHz or more, or even GHzs if modern day processors are used.

Master IC 300 uses clock signal BUSCLKm to communicate on the bus 297, and uses clock signal CLKm as its internal clock. Likewise, slave IC 300' uses clock signal BUSCLKs to communicate on the bus 297, and uses clock signal CLKs as its internal clock. As shown, each of the bus clocks BUSCLKm and BUSCLKs are provided to the various functional blocks (Block1, Block 2) in their respective ICs, and more specifically to the bus interface circuitry 215 of such bocks. These functional blocks can comprise any of the functional blocks described earlier with respect to Figure 4B. The internal clocks CLKm and CLKs are used by the ICs to run internal functions. Although not shown, one important use for internal clocks is to provide reference clocking for the provision of stimulation to the electrodes, which can occur independently of bus communications (or more accurately, after bus communications have already provided the stimulation parameters).

Figure 10 further illustrates how these various clocks are generated in the system 290, and specially shows the clock generation circuitry blocks 330 and 330' operating in the master and slave ICs 300 and 300' respectively. Communication on the bus 297 is controlled by microcontroller 305, which issues a control signal, BUSCLKen, when communications on the bus 297 are required, i.e., when the microcontroller 305 needs to send or receive data to or from either of the master or slave ICs 300 or 300'. This control signal BUSCLKen is sent to the corresponding input of the master IC 300, but not to the corresponding input of the slave IC 300' by virtue of off-chip routing as shown in Figures 4A and 10.

Also received at the master IC 300 at input CLKIN (but not at the slave IC 300') is an initial clock signal, CLKi, generated off chip by a crystal oscillator 340. As will be seen, all of the internal and bus clock signals (expect for the

microcontroller's internal clock CLKμc) are generated from (and hence synchronized with) CLKi. It is assumed in Figure 10 that CLKi from the crystal oscillator 340 is of a proper frequency, which again may be on the order of 100 kHz. However, the signal from the crystal oscillator 340 may also be processed or buffered within the clock generator circuitry 330 to achieve an appropriate clock CLKi (not shown). Although use of a crystal oscillator 340 is shown, other types of clocking circuitries (e.g., ring oscillators) could also be used. Moreover, although CLKi is shown in Figure 10 as generated off-chip, an on-chip clock generator could also be used. In this case, the M/S controllers 350 and 350' could be used to enable the on-chip clock generator in the master IC 300, but to disable that same generator in the slave IC 300'. CLKi is generally always running, provided the battery 26 in the IPG has not depleted.

CLKi is ANDed with control signal BUSCLKen at AND gate 360 to produce the communication clock BUSCLKμC for the microcontroller 305 at output CLKOUT1. This results in BUSCLKμC being active (and synchronized with CLKi) when BUSCLKen is asserted, and grounded when BUSCLKen is not asserted. Note that the corresponding input for BUSCLKen is grounded in the slave IC 300', which grounds the output to AND gate 360', inactivating output CLKOUT1 on the slave, as represented by the dotted lines.

Once BUSCLKμC is active and the microcontroller 305 can communicate on the bus 297, the microcontroller 305, acting as the system master, can assess which clocks in the master and slave ICs 300 and 300' need to be enabled. Depending on that assessment, the microcontroller 305 can write via the bus 297 to registers 380 and 380' in the master and slave respectively. Specifically shown are three register bits, E, B, and I, which stand for "external," "bus," and "internal." B and B' comprise enable signals for generation of the bus clocks BUSCLKm and BUSCLKs respectively. I and I' comprise enable signals for generation of the internal clocks CLKm and CLKs respectively. (Each of the master and slave can have more than one internal clock, and hence more than one internal clock register value, but only one such clock in shown in Figure 10 for simplicity). E comprises an enable signal for porting a clock external to the IC 300 (CLKext) to a downstream slave IC such as 300'. Register values E, B, and I

are each accessible at their own addresses (e.g., ADDRx, ADDRy, and ADDRz), and each of these addresses can be selectively written to by the microcontroller 305 using the chip select signals CS_m and CS_s discussed earlier.

Starting with the master IC 300, notice that the bus interface circuitry 215 receives the initial clock, CLKi. Because the microcontroller 305's bus clock BUSCLKμc is synchronous with CLKi, this enables register values E, B, and I in register 380 to be set by the microcontroller 305 even though the microcontroller has not yet enabled the remainder of the master IC 300 to fully communicate on the bus 297. Should master IC 300 require its bus clock BUSCLKm to communicate with the microcontroller 305, register value B would be set high by the microcontroller 305. Should master IC 300 require its internal clock CLKm, register value I would be set. When not needed, these registers would be set low. Such register values may default to a high state upon initialization. Like BUSCLKμc, BUSCLKm and CLKm are generated from CLKi using AND gates 365 and 366 respectively, with register values B and I enabling those clocks. As noted earlier, BUSCLKm is sent to the interface circuitry 215 in all other functional blocks within the master IC 300, thus enabling full communication between the microcontroller 305 and all functions in the master IC 300 when BUSCLKm is enabled.

It should be noted that registers B and I are not strictly required in the master IC 300 in all useful embodiments of system 297. Instead, the initial clock signal CLKi can be used directly as the master bus clock BUSCLKm and as the master internal clock CLKm. However, doing so would however prevent the microcontroller 305 from selectively disabling those clock signals at useful times during operation of the system.

The slave IC 300' only receives a clock issued by the master IC 300, namely clock signal CLKext. This occurs when the microcontroller 305 sets the external register E in the master IC 300. Like BUSCLKμc, BUSCLKm, and CLKm, CLKext is formed by ANDing an enable signal (in this case, E) with CLKi, and therefore CLKext is synchronized with all of these other clocks. As shown in Figure 10, CLKext is output from the master IC 300 and is received at the slave IC 300' at the CLKIN input in the master, effectively taking CLKi's

place in the slave. If operation of the slave IC 300' is not required—if slave IC 300' require neither a bus nor internal clock—E is set low, which will ground CLKext and disable the clock signal to the slave IC 300'. Without receipt of a clock signal, the slave IC 300' will draw only nominal power.

If the slave IC 300' is to be operational, E is set high at the master IC 300 and CLKext is enabled. Thereafter, the microcontroller 305 can set the various registers B' and I' in the slave IC 300' depending on whether a bus clock (BUSCLKs) and/or internal clock (CLKs) is required at a given point in time. (Corresponding register E' in the slave IC 300' is irrelevant in the embodiment shown, as the system 290 contains no further downstream slave ICs. As such, the effect of register E' in the slave IC 300' has been depicted with dotted lines). Writing to registers B' and I' occurs at the same addressees (ADDRy and ADDRz) as registers B and I in the master, but with CS_s = 1. The status of B' and I' respectively determine whether clocks BUSCLKs and CLKs are enabled, and in the slave these enable signals are ANDed with CLKext at AND gates 365' and 366' respectively. BUSCLKs is sent to the interface circuitry 215 in all other functional blocks within the slave IC 300'. However, this does not necessarily mean that all circuit blocks in the slave will be operative, or that full communications with the slave IC 300' can be had. By way of review, certain circuit blocks in the slave IC 300' will have their interface circuitry 215 disabled by the M/S controller 350' (see Fig. 4C), and thus will be unable to communicate on the bus 297, despite receipt of BUSCLKs.

Because CLKext is ultimately derived from CLKi in the master, clocks BUSCLKs and CLKs are also synchronized with CLKi. To summarize, all of clocks BUSCLKμc, BUSCLKm, BUSCLKs, CLKm and CLKs are synchronized with CLKi, and all will have the same frequency (again, about 100 kHz). Any small delays between these clocks caused by routing or gating are irrelevant given the relatively low operating speed of CLKi. Synchronization is particularly important as concerns the bus clocks, which need to be synchronized for reliable communications on the bus 297. However, synchronization of the internal clocks is important as well to ensure synchronicity in the internal operations between the master and slave, such as during the provision of a stimulation pulse.

It should be noted again that registers B' and I' are not strictly required in the slave IC 300' in all useful embodiments of system 297. Instead, the external clock signal CLKext can be used directly as the slave bus clock BUSCLKs and as the slave internal clock CLKs. However, doing so would however prevent the microcontroller 305 from selectively disabling those clock signals at useful times during operation of the system.

To summarize, by setting register values E, B, I, B', and I', the microcontroller 305 can selectively control the various bus and internal clocks signals needed by the master and slave IC 300'. Importantly, at periods in time when the slave IC 300' is not needed by the system, its clocks can be completely disabled (by setting E low in the master), or partially (by setting E high in the master, but by setting either or both of B' and I' low).

Although Figure 10 depicts only a single master and slave IC, note that the technique is extendible to control the clock of additional downstream slave ICs.

WHAT IS CLAIMED IS:

1. A method for providing stimulation to a patient's tissue using an implantable stimulator device comprising a first integrated circuit with a plurality of first electrodes and a second integrated circuit with a plurality of second electrodes, and a bus in communication with both the first and second integrated circuits, the method comprising:

determining stimulation parameters for at least one of the first electrodes and at least one of the second electrodes;

loading the stimulation parameters for the at least one first electrode at the first integrated circuit via the bus;

loading the stimulation parameters for the at least one second electrode at the second integrated circuit via the bus; and

issuing a stimulation enable command on the bus to execute the loaded stimulation parameters for the first and second electrodes, thereby causing simultaneous stimulation at the at least one first and second electrodes.

2. The method of claim 1, wherein the stimulation parameters comprise a magnitude and a polarity of stimulation for the at least one of the first electrode and the at least one of the second electrodes.

3. The method of claim 1 or 2, wherein the bus comprises a first chip select signal for the first integrated circuit and a second chip select signal for the second integrated circuit, and wherein the first chip select signal is asserted when loading the stimulation parameters for the at least one first electrode, and wherein the second chip select signal is asserted when loading the stimulation parameters for the at least one second electrode.

4. The method of any one of claims 1 to 3, wherein the stimulation enable command is issued with both the first and second chips select signals asserted.

5. The method of claim 3 or 4, wherein the stimulation enable command provides the loaded stimulation parameters to digital-to-analog converter (DAC) circuitry in the first and second integrated circuits to cause the simultaneous stimulation at the at least one first and second electrodes.

6. The method of any one of claims 1 to 5, wherein the stimulation parameters for the at least one of the first electrodes is issued on the bus before the stimulation parameters for the at least one of the second electrodes.

7. The method of any one of claims 1 to 6, wherein a conductive case houses the first and second integrated circuits, and wherein that at least one of the first electrodes or the at least one of the second electrodes comprises the case.

8. An implantable stimulator device comprising a plurality of first electrodes and a plurality of second electrodes configured to provide stimulation to a patient's tissue, comprising:

a first integrated circuit, the first integrated circuit comprising

a first stimulation circuitry block for controlling stimulation of the plurality of first electrodes, and

a plurality of first functional blocks; and

a second integrated circuit identical in construction to the first integrated circuit, the second integrated circuit comprising

a second stimulation circuitry block identical to the first stimulation circuitry block for controlling stimulation of the plurality of second electrodes, and

a plurality of second functional blocks identical to the plurality of first functional blocks,

wherein the plurality of first functional blocks are enabled, and wherein the plurality of second functional blocks are disabled.

9. The device of claim 8, further comprising:

a bus;

a first input to the first integrated circuit;

a second input to the second integrated circuit,

wherein the first input is set to enable communication between of the plurality of first functional blocks and the bus, and wherein the second input is set to disable communication between the plurality of second functional blocks and the bus.

10. The device of claim 8 or 9, further comprising a telemetry antenna for receiving and transmitting data from and to an external controller, wherein one of the plurality of first functional blocks comprises a first telemetry circuitry block coupled to the telemetry antenna, and wherein one of the plurality of second functional blocks comprises a second telemetry circuitry block not coupled to the telemetry antenna.

11. The device of any one of claims 8 to 10, further comprising a battery with a battery voltage, and wherein one of the plurality of first functional blocks comprises a first charging block for charging the battery, and wherein one of the plurality of second functional blocks comprises a second charging block.

12. The device of claim 11, wherein the battery voltage is routed to both the first and second integrated circuits.

13. The device of claim 11 or 12, further comprising a charging antenna for receiving power from an external charger, wherein the charging antenna is coupled to the first charging block, and wherein the charging antenna is not coupled to the second charging block.

14. The device of any one of claims 8 to 13, wherein one of the plurality of first functional blocks comprises a first compliance voltage generation block for generating a compliance voltage for the first and second stimulation circuitry blocks, wherein one of the

plurality of second functional blocks comprises a second compliance voltage generation block.

15. The device of any one of claims 8 to 14, wherein the first integrated circuit further comprises a first master/slave controller, and wherein the second integrated circuit further comprises a second master/slave controller identical to the first master slave controller, and wherein the first master/slave controller enables the plurality of first functional blocks, and wherein the second master/slave controller disables the plurality of second functional blocks.

16. An implantable stimulator device, comprising:

a first integrated circuit comprising a plurality of first electrodes configured to provide stimulation to a patient's tissue;

a second integrated circuit comprising a plurality of second electrodes configured to provide stimulation to the patient's tissue;

an initial clock signal received at the first integrated circuit;

an external clock signal issuing from the first integrated circuit and derived from the initial clock signal, the external clock received at the second integrated circuit; and

a bus in communication with the first and second integrated circuits, wherein the external clock signal is selectively enabled at the first integrated circuit by an external clock enable signal via a command from the bus.

17. The device of claim 16, wherein the initial clock signal is provided by an oscillator circuit.

18. The device of claim 16, wherein the oscillator circuit comprises a crystal oscillator external to the first integrated circuit.

19. The device of any one of claims 16 to 18, further comprising a register in the first integrated circuit for receiving the command and for setting the external clock enable signal.

20. The device of any one of claims 16 to 19, wherein the external clock signal is formed by ANDing the initial clock signal with the external clock enable signal.

21. The device of any one of claims 16 to 20, wherein the command is issued from a microcontroller separate from the first integrated circuit.

22. An implantable stimulator device, comprising:

a first integrated circuit comprising a plurality of first electrodes configured to provide stimulation to a patient's tissue, the first integrated circuit for receiving an initial clock signal and for selectively issuing an external clock signal and a microcontroller bus clock signal derived from the initial clock signal;

a second integrated circuit comprising a plurality of second electrodes configured to provide stimulation to the patient's tissue, the second integrated circuit receiving the external clock signal; and

a microcontroller external to the first and second integrated circuits receiving the microcontroller bus clock signal.

23. The device of claim 22, further comprising a bus in communication with the first and second integrated circuits and the microcontroller.

24. The device of claim 22 or 23, wherein the first integrated circuit comprises first logic circuitry for deriving a first internal clock signal and a first bus clock signal from the initial clock signal, and wherein the second integrated circuit comprises second logic circuitry for deriving a second internal clock signal and a second bus clock signal from the external clock signal.

25. The device of claim 24, wherein the first bus clock enables the first integrated circuit to communicate on the bus, and wherein the second bus clock enables the second integrated circuit to communicate on the bus.

26. The device of claim 24 or 25, wherein the first internal clock signal, the first bus clock signal, the second internal clock signal, and the second bus clock signal are selectively enabled by the microcontroller.

27. The device of any one of claims 22 to 26, wherein the first integrated circuit receives an enable signal from the microcontroller, and wherein the microcontroller bus clock signal is formed by ANDing the enable signal with the initial clock signal.

28. The device of any one of claims 22 to 27, wherein the microcontroller bus clock signal enables the microcontroller to communicate on the bus.

29. The device of any one of claims 22 to 28, wherein the microcontroller bus clock signal is distinct from an internal microcontroller clock.

30. The device of any one of claims 22 to 29, wherein the initial clock signal, the external clock signal, and the microcontroller bus clock signal are synchronized.

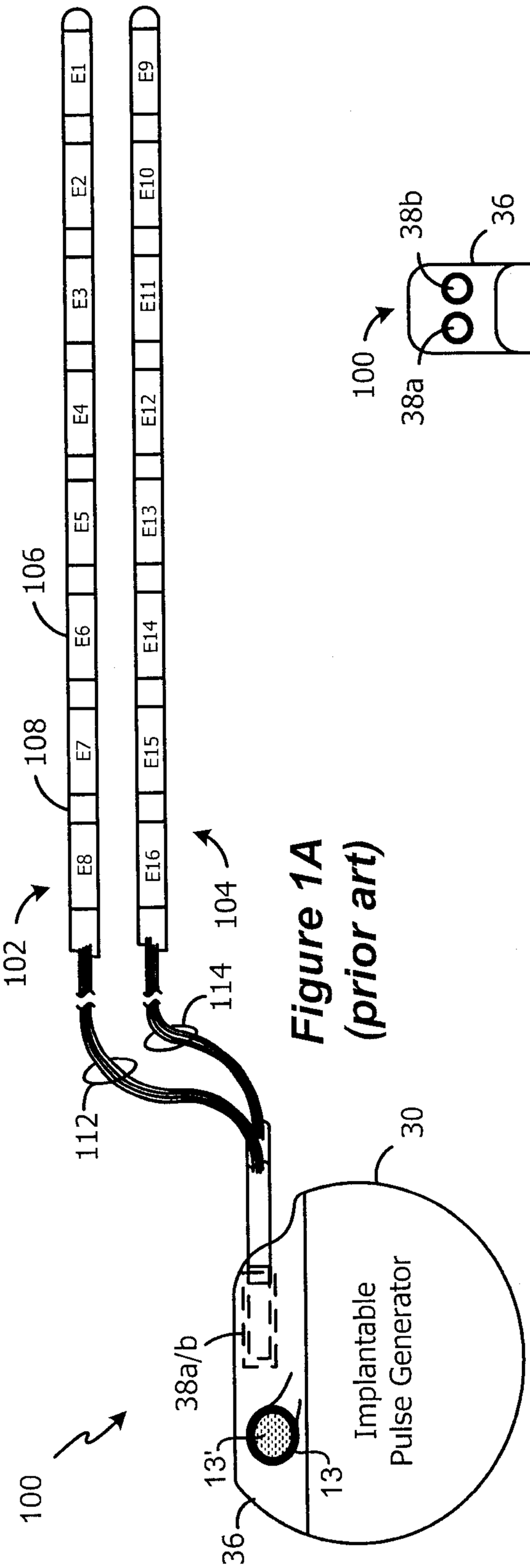


Figure 1A
(prior art)

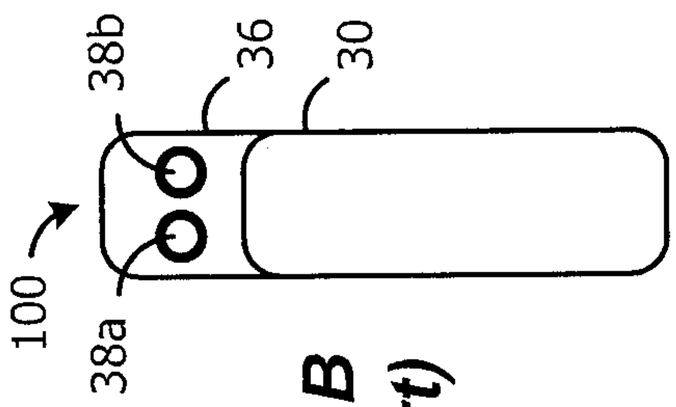


Figure 1B
(prior art)

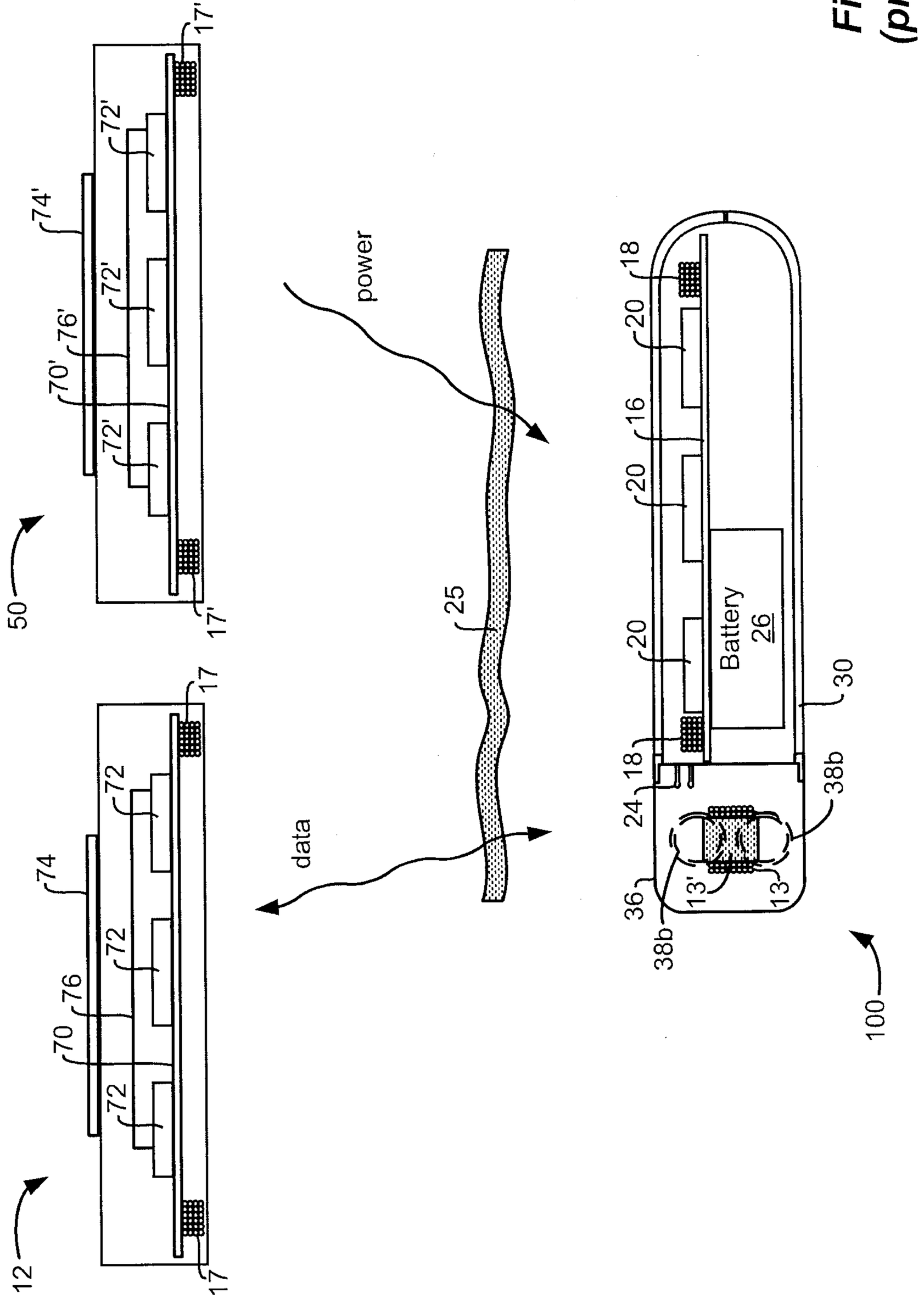


Figure 2
(prior art)

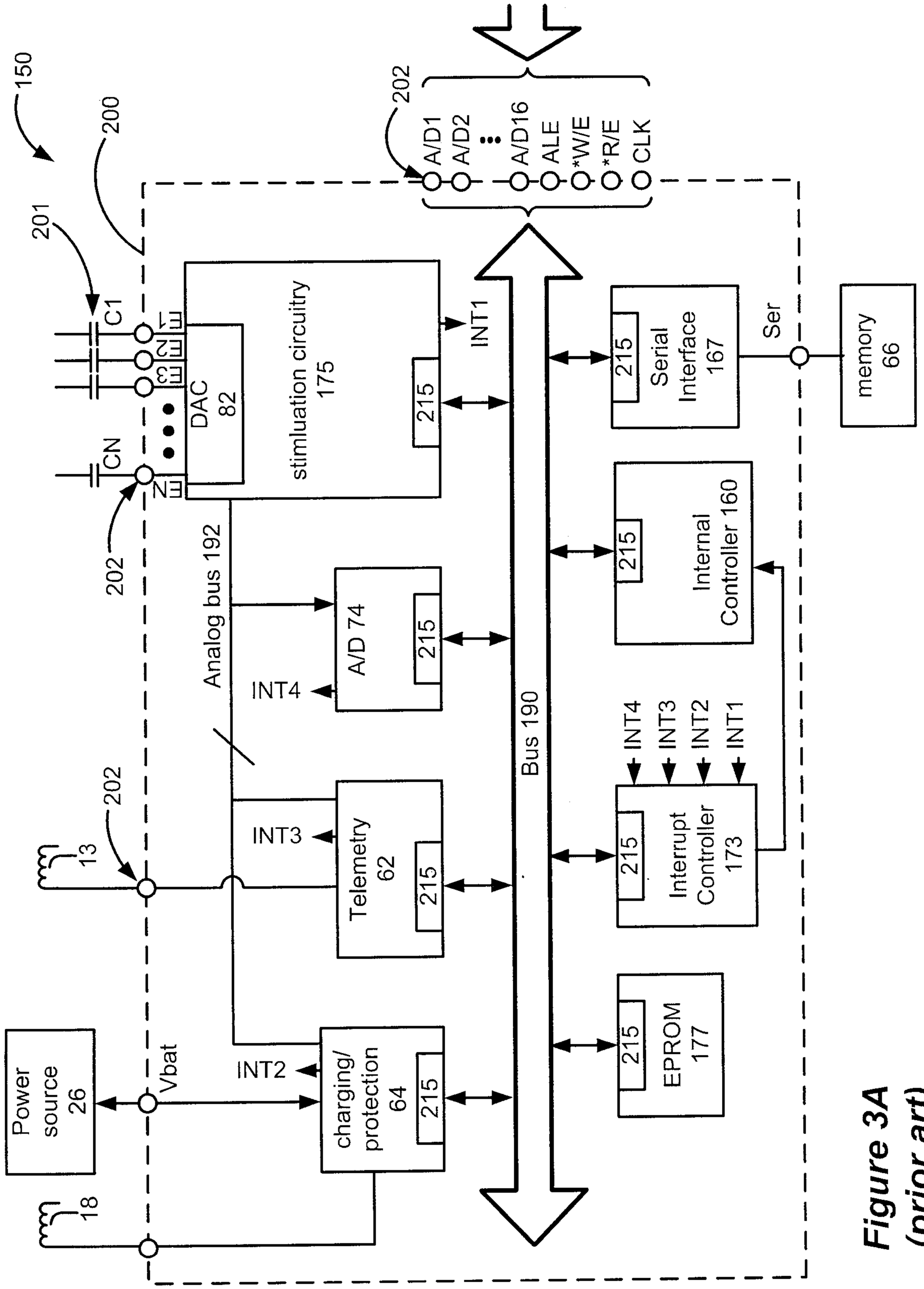


Figure 3A
(prior art)

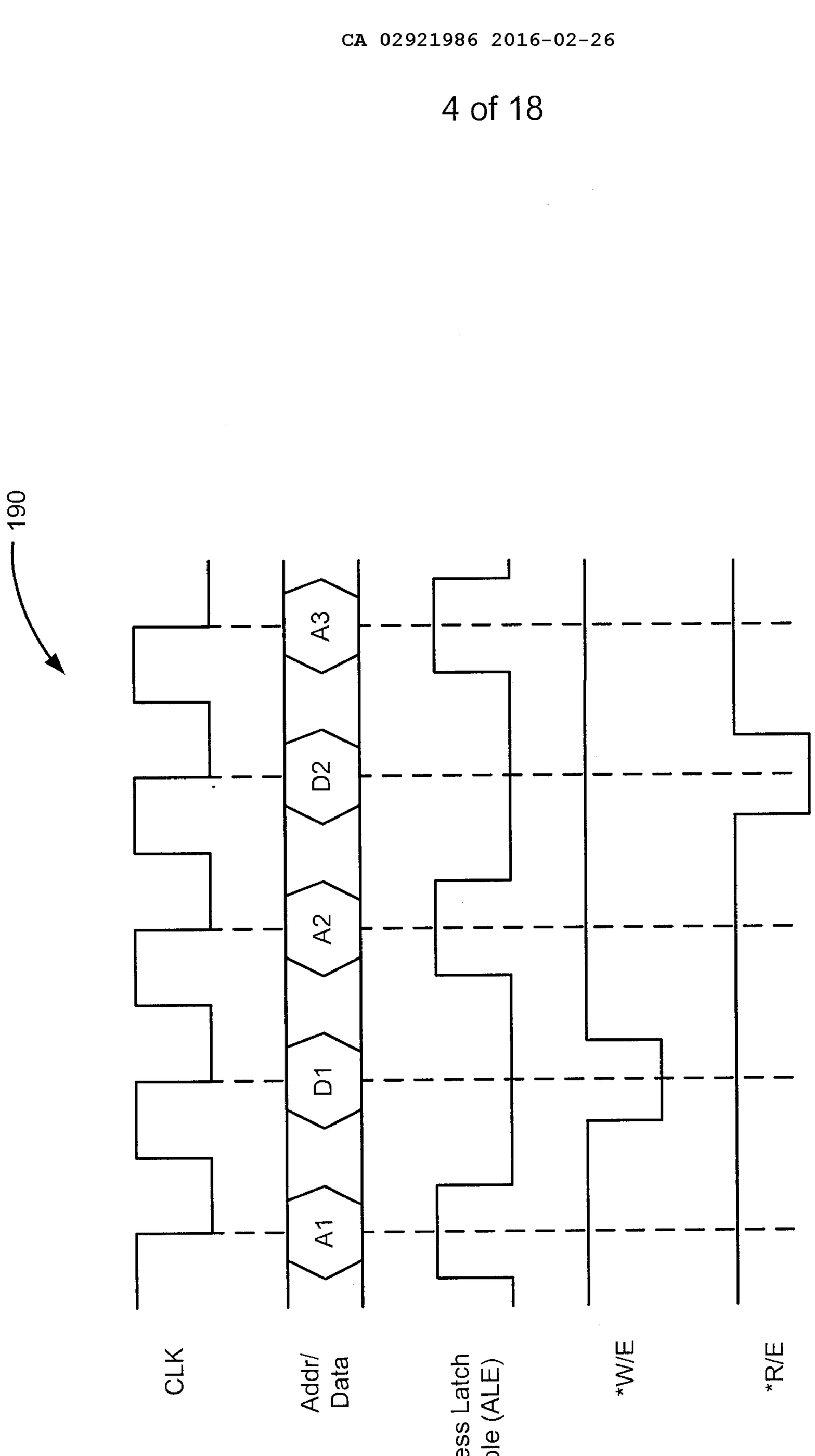


Figure 3B (prior art)

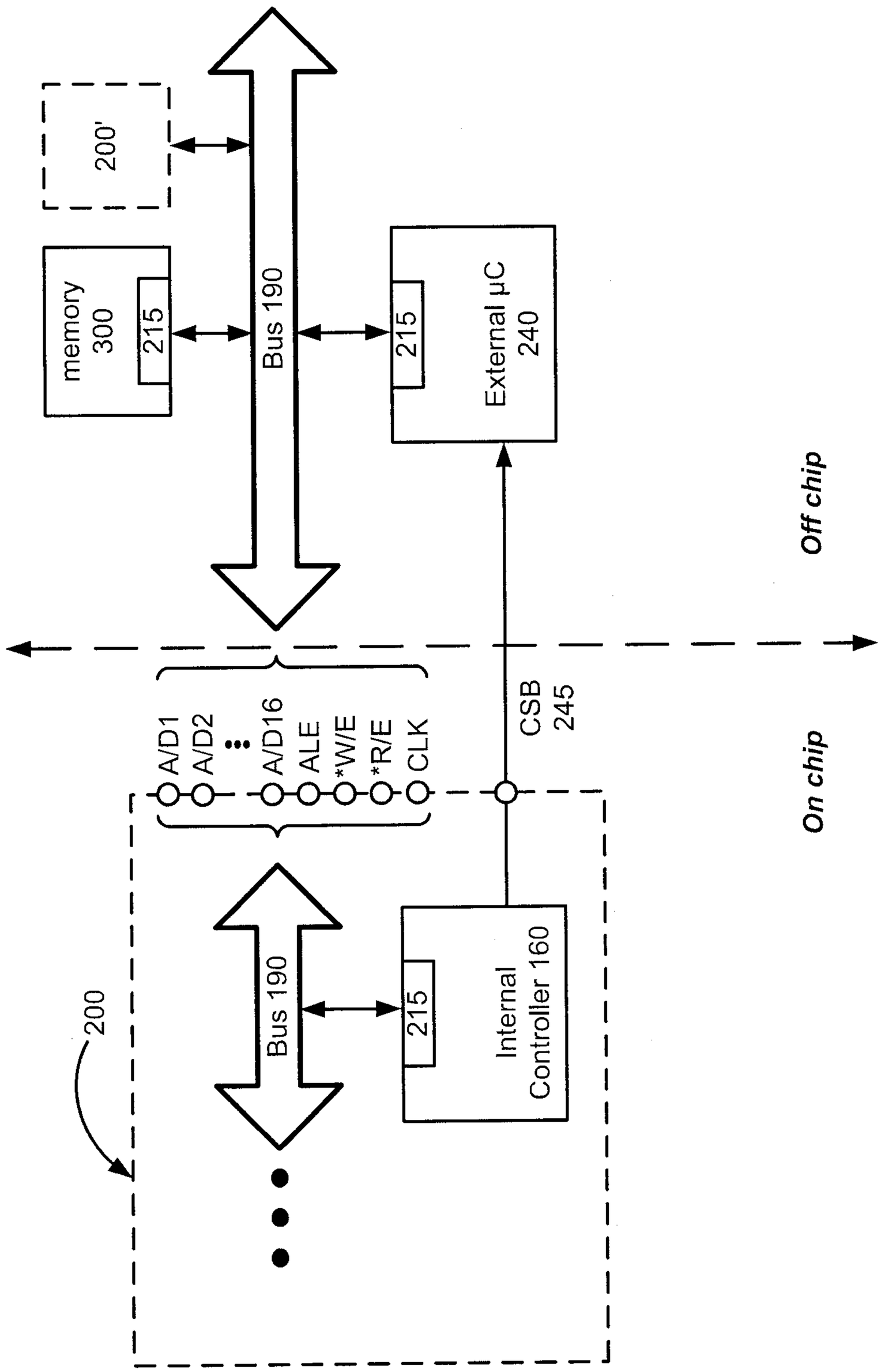


Figure 3C (prior art)

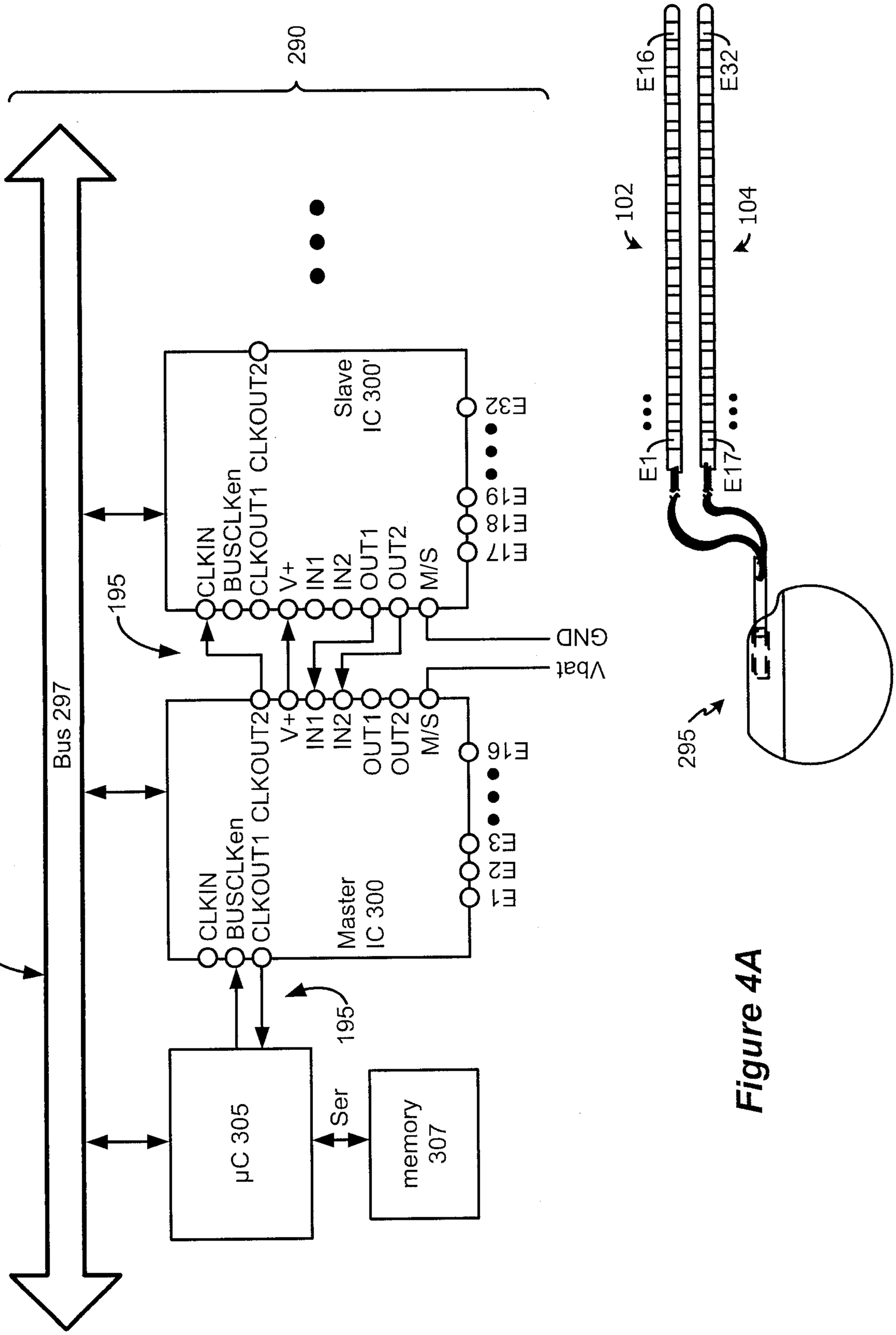

290
<A/D1:16>, ALE, *W/E, *R/E, CS_m, CS_s
Bus 297
195
CLKIN
BUSCLKen
CLKOUT1
CLKOUT2
V+
IN1
IN2
OUT1
OUT2
M/S
Slave
IC 300'
E32
E19
E18
E17
GND
Vbat
Master
IC 300
E16
E3
E2
E1
195
µC 305
Ser
memory
307
102
104
E1
E17
E16
E32
295

Figure 4A

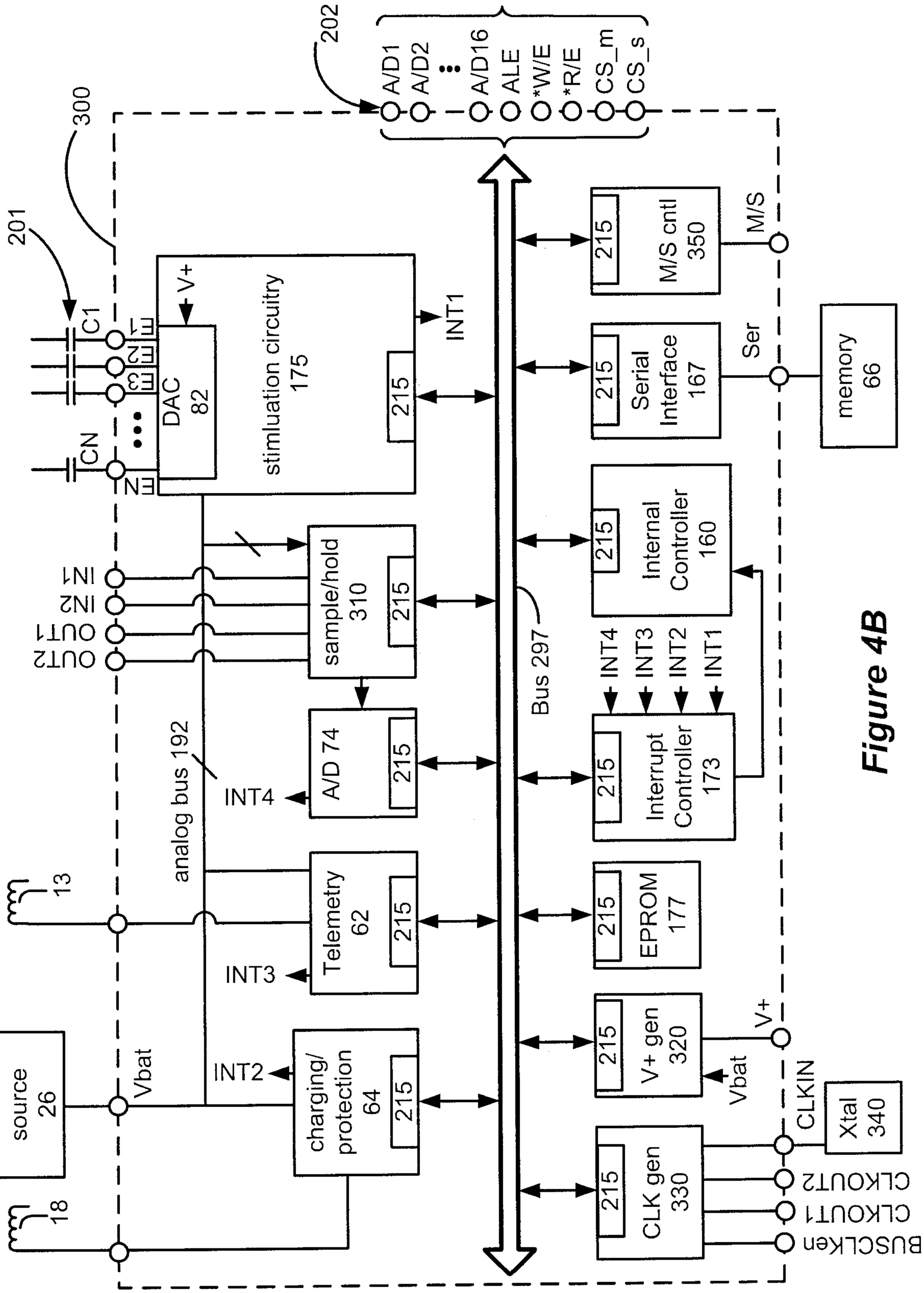

202
300
A/D1
A/D2
A/D16
ALE
*W/E
*R/E
CS_m
CS_s
201
C1
C2
C3
CN
DAC
82
V+
stimluation circuitry
175
215
INT1
IN1
IN2
OUT1
OUT2
sample/hold
310
215
analog bus 192
INT4
A/D 74
215
13
INT3
Telemetry
62
215
Power
source
26
Vbat
INT2
charging/
protection
64
215
18
Bus 297
215
M/S cntl
350
M/S
215
Serial
Interface
167
Ser
memory
66
215
Internal
Controller
160
INT4
INT3
INT2
INT1
215
Interrupt
Controller
173
215
EPROM
177
215
V+ gen
320
V+
Vbat
215
CLK gen
330
CLKIN
Xtal
340
CLKOUT2
CLKOUT1
BUSCLKen

Figure 4B

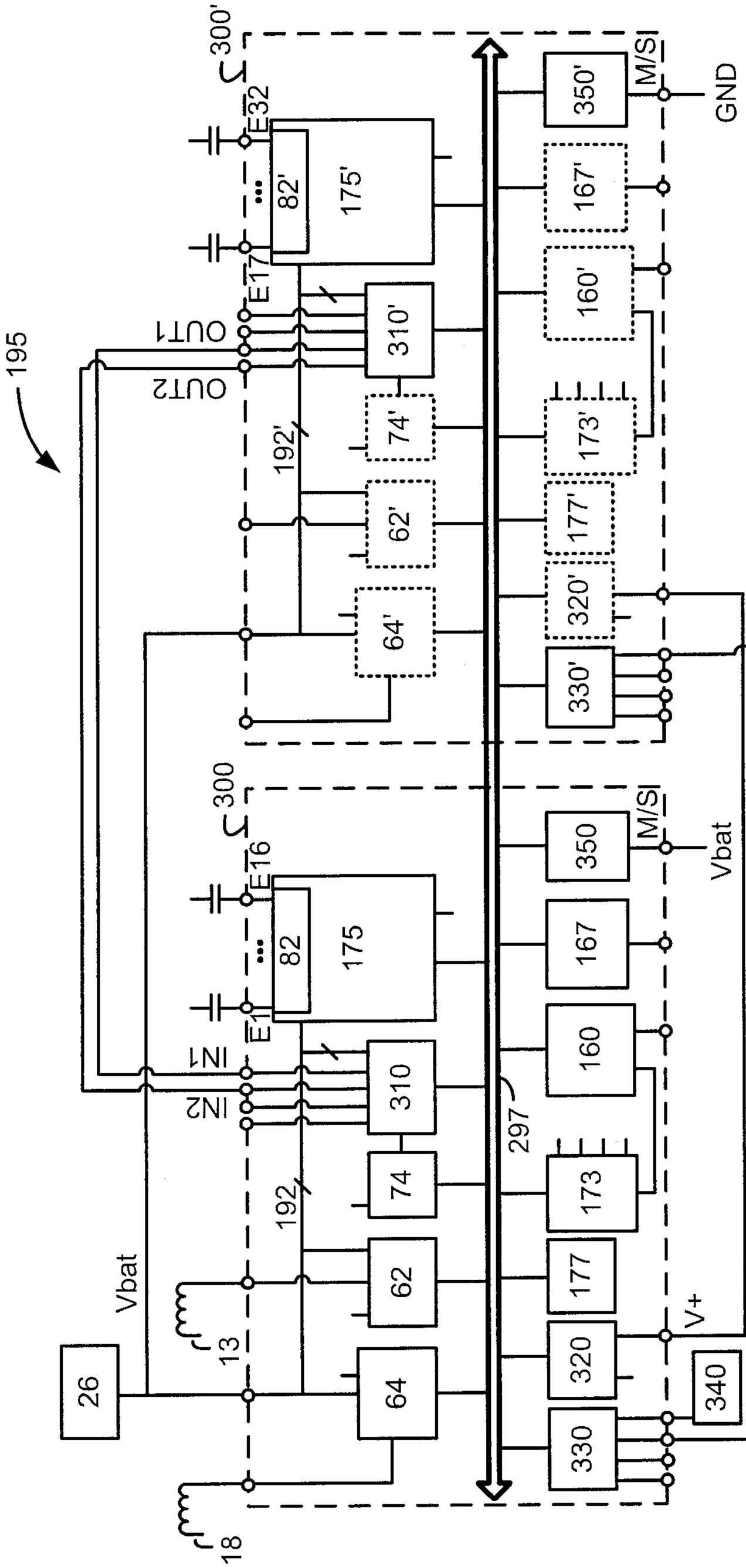
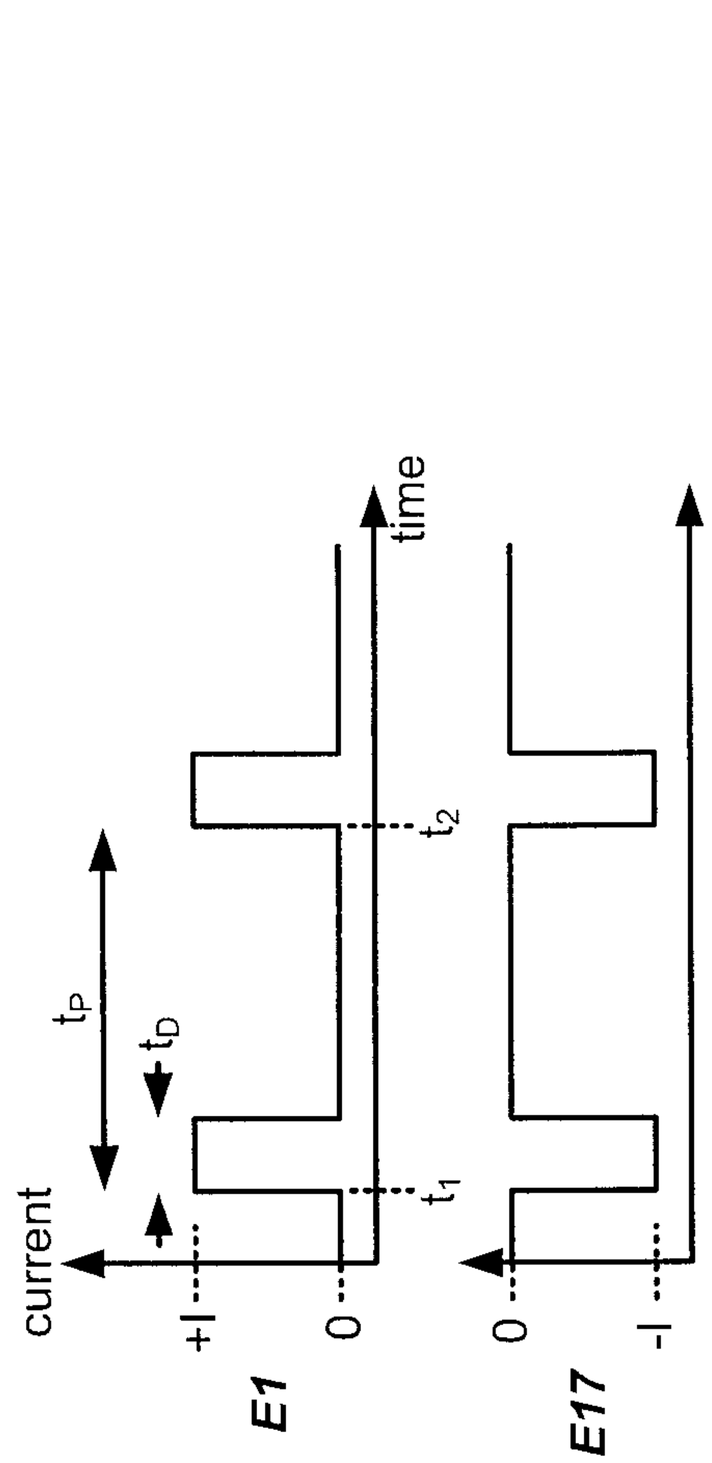

195
OUT1
OUT2
IN1
IN2
E32
E17
E16
E1
300'
300
82'
175'
82
175
310'
310
74'
74
192'
192
62'
62
64'
64
26
13
18
Vbat
350'
350
M/SI
GND
167'
167
160'
160
173'
173
177'
177
320'
320
330'
330
297
340
V+

Figure 4C



Time	Bus Command	Chip Select
Before t_1	Set E1 with magnitude I, polarity source at ADDRi-j	CS_m = 1, CS_s = 0
Before t_1	Set E17 with magnitude I, polarity sink at ADDRi-j	CS_m = 0, CS_s = 1
At t_1	Issue stimulation enable command at ADDRk, including duation t_D of pulse	CS_m = 1, CS_s = 1
Before t_2	Set E1 with magnitude I, polarity source at ADDRi-j	CS_m = 1, CS_s = 0
•••		

Figure 5

Time	***Bus Command***	***Chip Select***
During t_D	Select E1 at MUX1 at ADDRr	CS_m = 1, CS_s = 0
	Select GND at MUX2 at ADDRs	CS_m = 1, CS_s = 0
(settle)		
	Read A/D at ADDRt	CS_m = 1, CS_s = 0
•••	•••	•••

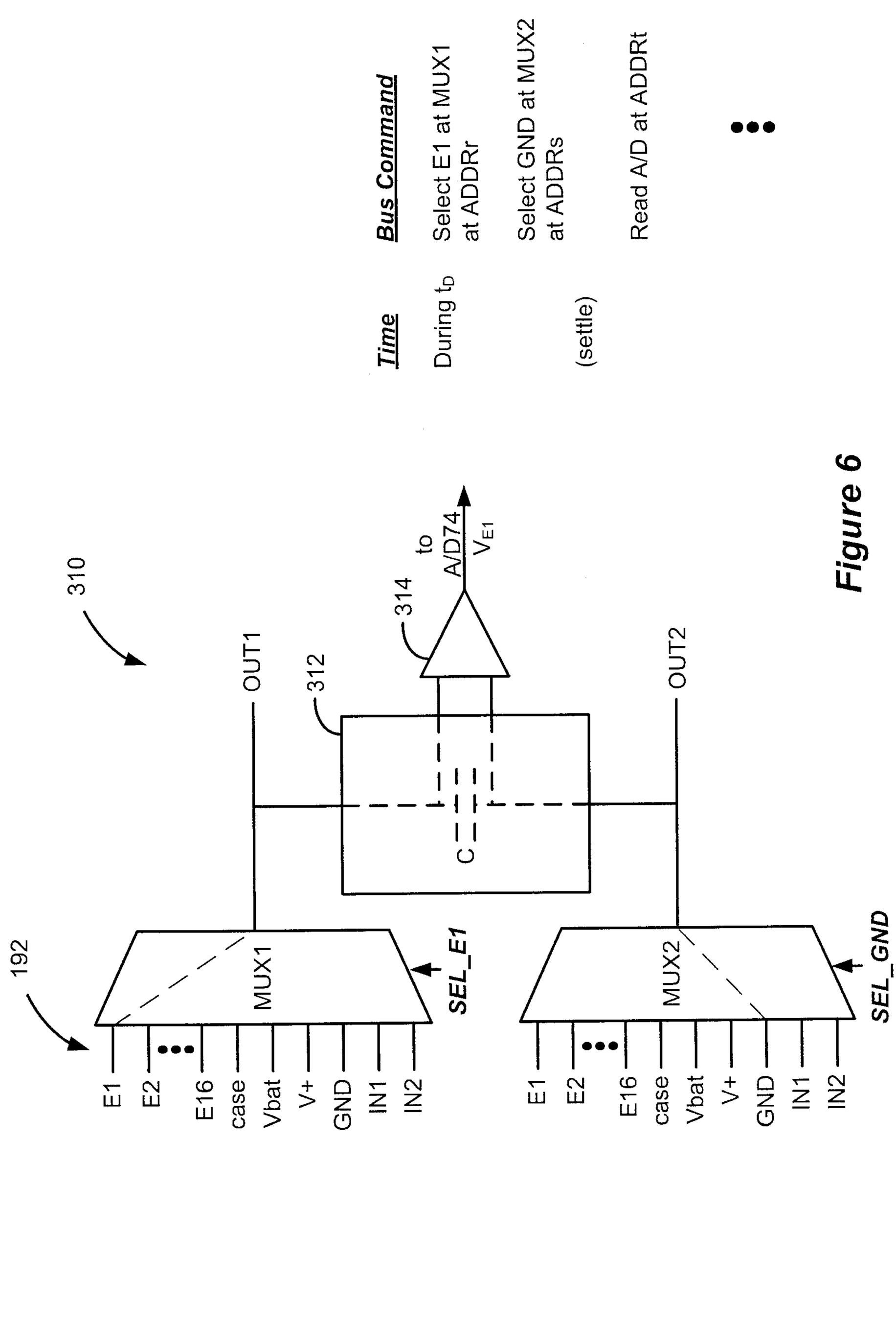


Figure 6

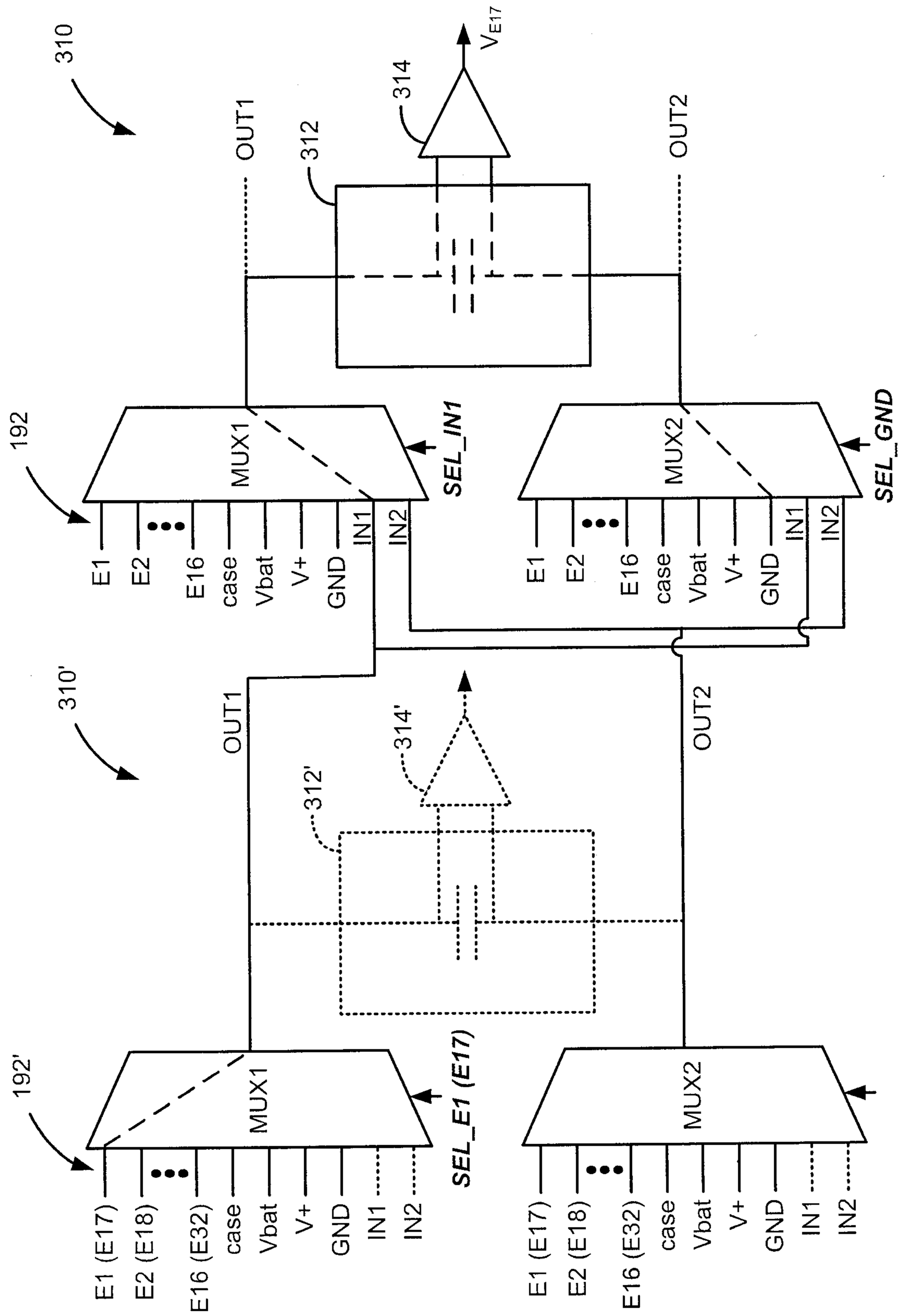

310
192
E1
E2
E16
case
Vbat
V+
GND
IN1
IN2
MUX1
SEL_IN1
OUT1
312
314
V_{E17}
MUX2
SEL_GND
OUT2
310'
192'
E1 (E17)
E2 (E18)
E16 (E32)
312'
314'
SEL_E1 (E17)

Figure 7A

Time	***Bus Command***	***Chip Select***
During t_D	Select E1 (E17) at MUX1 at ADDRr	CS_m = 0, CS_s = 1
	Select IN1 at MUX1 at ADDRr	CS_m = 1, CS_s = 0
	Select GND at MUX2 at ADDRs	CS_m = 1, CS_s = 0
(settle)		
	Read A/D at ADDRt	CS_m = 1, CS_s = 0

Figure 7B

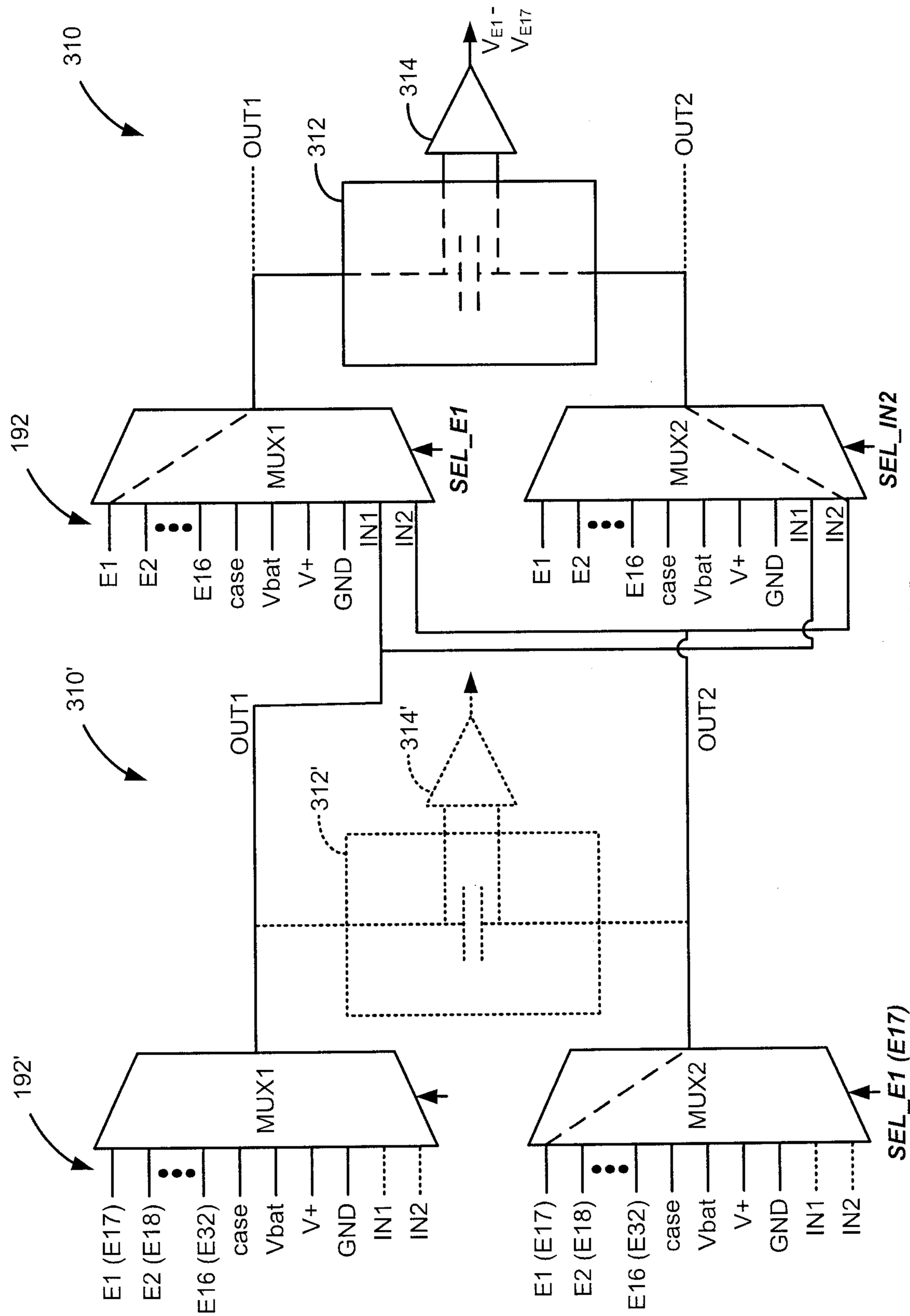
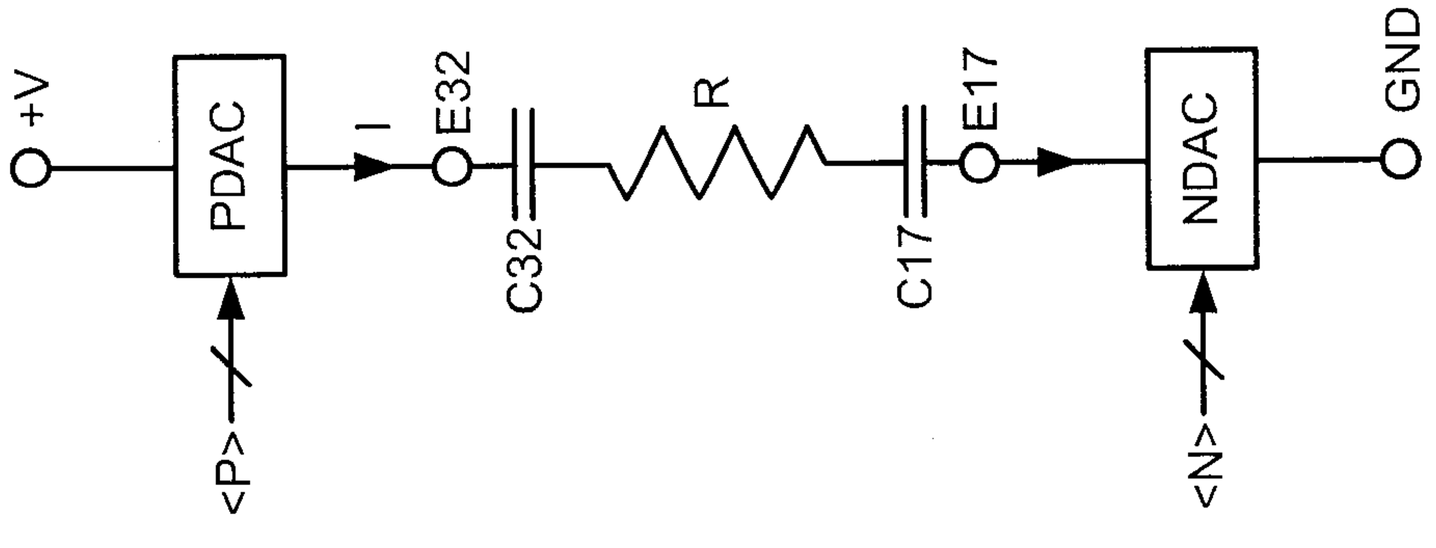

310
OUT1
312
314
V_{E1} - V_{E17}
OUT2
192
MUX1
SEL_E1
MUX2
SEL_IN2
E1
E2
E16
case
Vbat
V+
GND
IN1
IN2
310'
OUT1
312'
314'
OUT2
192'
MUX1
MUX2
SEL_E1 (E17)
E1 (E17)
E2 (E18)
E16 (E32)

Figure 8A

Time	***Bus Command***	***Chip Select***
During t_D	Select E1 (E17) at MUX2 at ADDRs	CS_m = 0, CS_s = 1
	Select E1 at MUX1 at ADDRr	CS_m = 1, CS_s = 0
	Select IN2 at MUX2 at ADDRs	CS_m = 1, CS_s = 0
(settle)		
	Read A/D at ADDRt	CS_m = 1, CS_s = 0

Figure 8B

Figure 9A



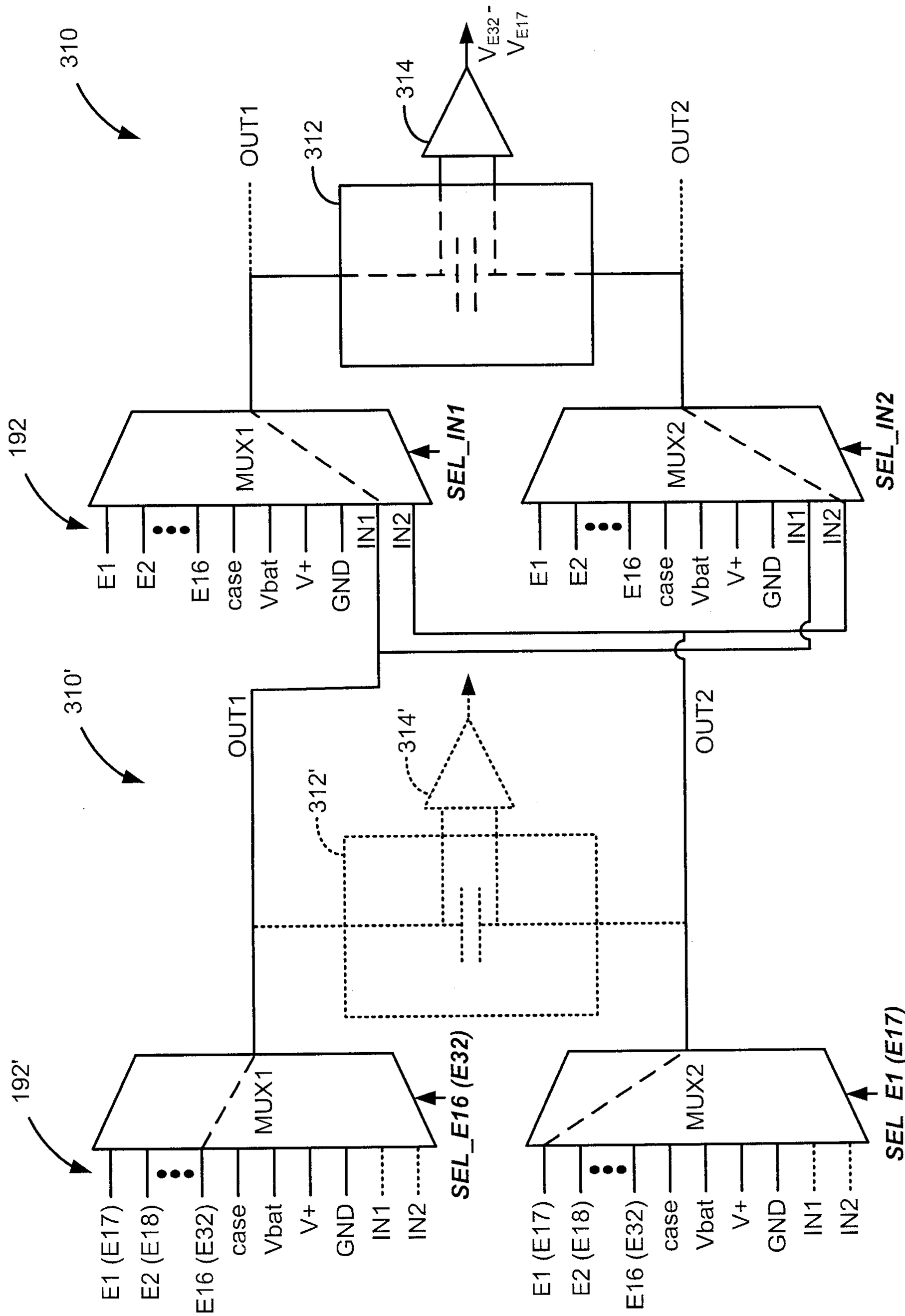

310
OUT1
312
314
$V_{E32} - V_{E17}$
OUT2
192
MUX1
MUX2
SEL_IN1
SEL_IN2
E1
E2
E16
case
Vbat
V+
GND
IN1
IN2
310'
OUT1
312'
314'
OUT2
192'
MUX1
MUX2
SEL_E16 (E32)
SEL_E1 (E17)
E1 (E17)
E2 (E18)
E16 (E32)
case
Vbat
V+
GND
IN1
IN2

Figure 9B

Time	***Bus Command***	***Chip Select***
During t_D	Select E16 (E32) at MUX1 at ADDRr	CS_m = 0, CS_s = 1
	Select E1 (E17) at MUX 2 at ADDRs	CS_m = 0, CS_s = 1
	Select IN1 at at MUX1 at ADDRr	CS_m = 1, CS_s = 0
	Select IN2 at MUX2 at ADDRs	CS_m = 1, CS_s = 0
(settle)	Read A/D at ADDRt	CS_m = 1, CS_s = 0

Figure 9C

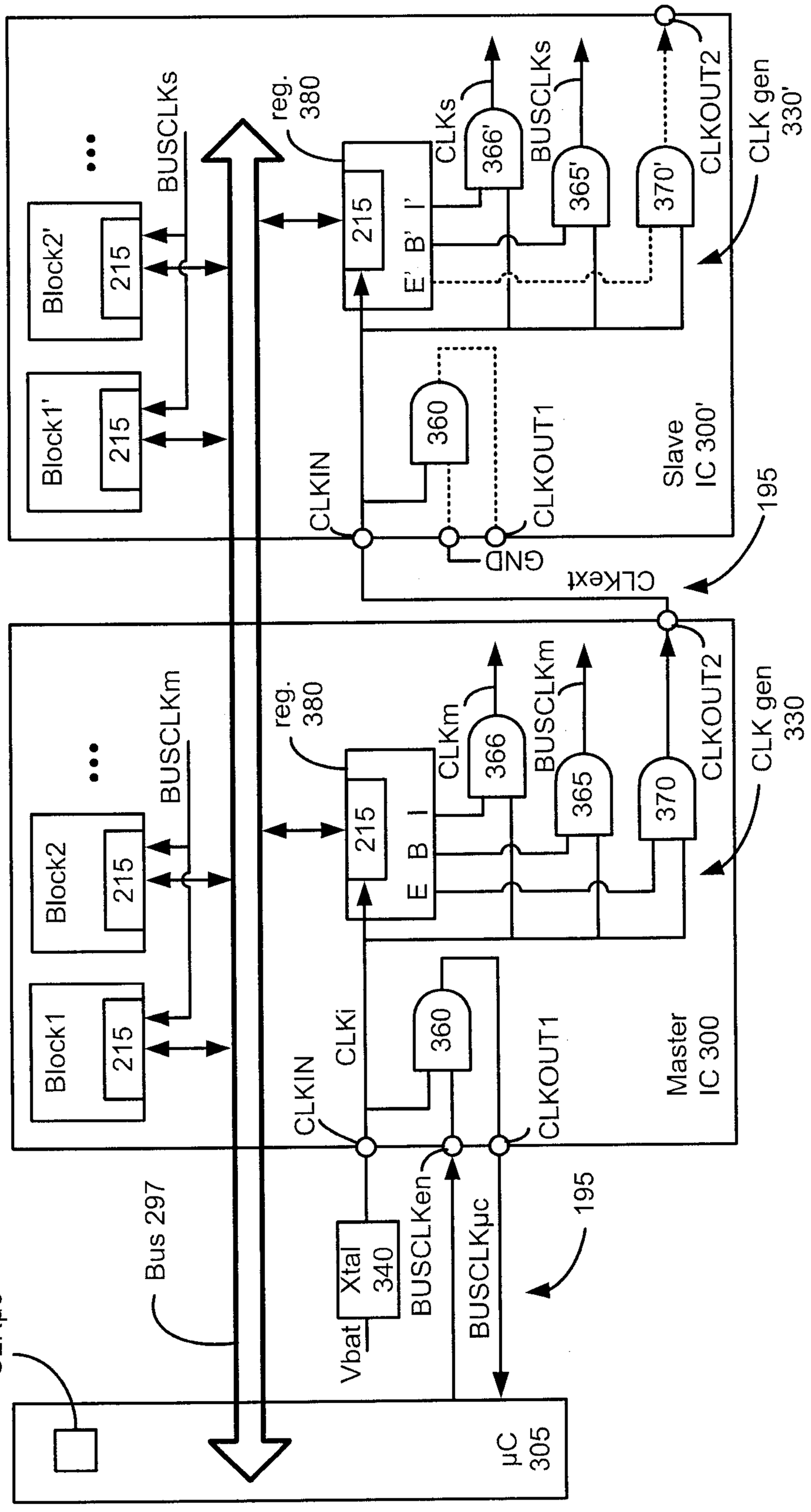
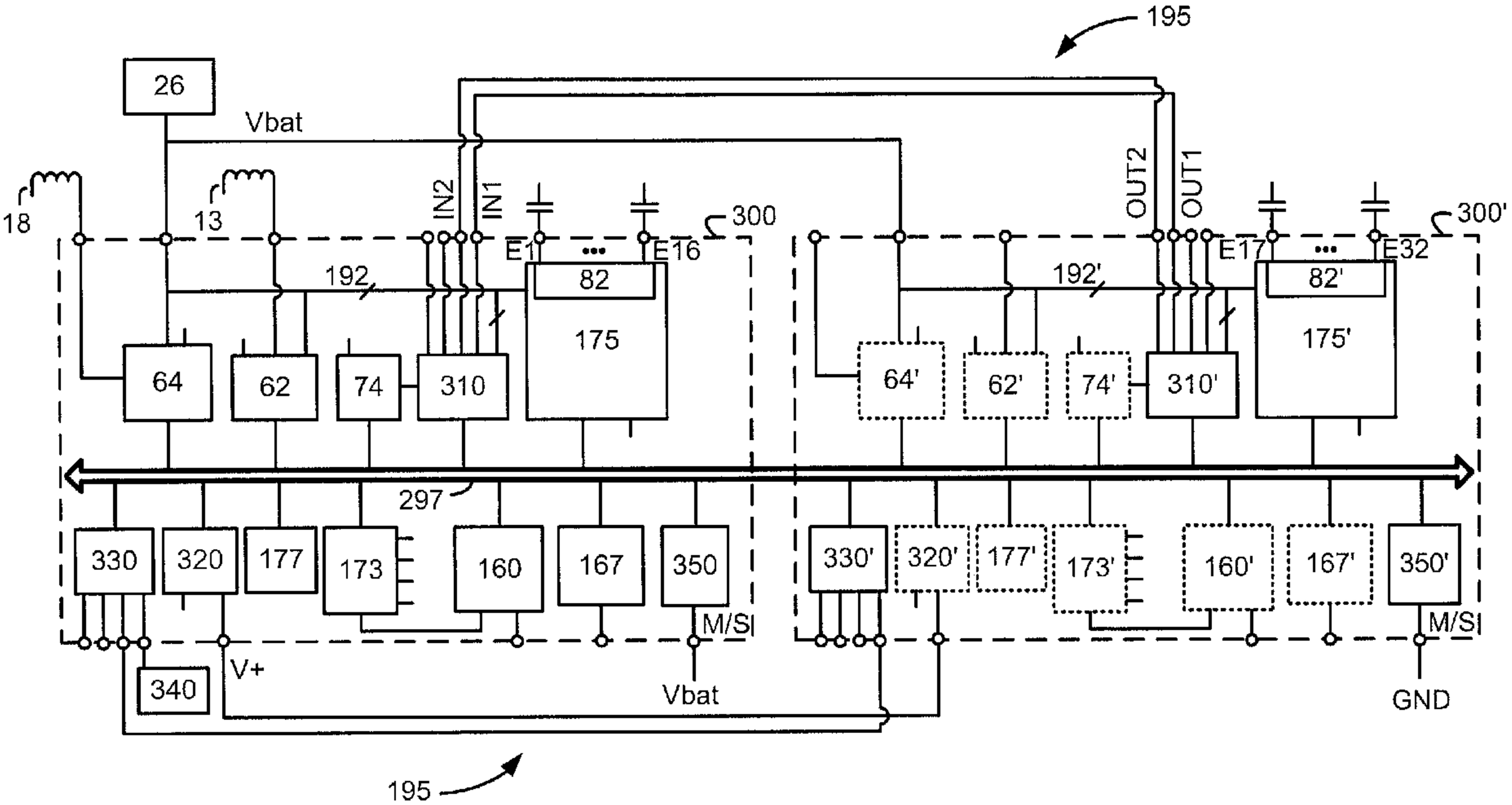

Block1'
215
Block2'
215
BUSCLKs
reg.
380
215
E' B' I'
CLKs
366'
365'
370'
BUSCLKs
CLKOUT2
CLK gen
330'
360
CLKIN
CLKOUT1
GND
Slave
IC 300'
195
CLKext
Block1
215
Block2
215
BUSCLKm
reg.
380
215
E B I
CLKm
366
365
370
BUSCLKm
CLKOUT2
CLK gen
330
360
CLKIN
CLKi
CLKOUT1
Master
IC 300
Bus 297
Xtal
340
Vbat
BUSCLKen
BUSCLKμc
195
CLKμc
μC
305

Figure 10


195
26
Vbat
18
13
IN2
IN1
E1
E16
300
OUT2
OUT1
E17
E32
300'
192
82
175
64
62
74
310
192'
82'
175'
64'
62'
74'
310'
297
330
320
177
173
160
167
350
330'
320'
177'
173'
160'
167'
350'
M/S
M/S
340
V+
Vbat
GND
195