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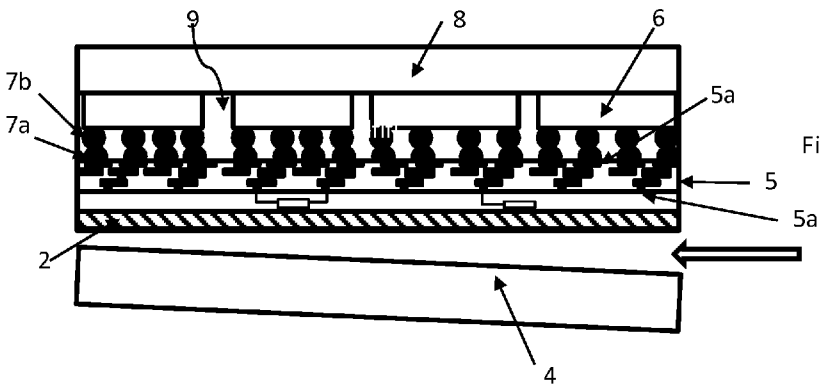

Figure 7

(57) Abstract: The invention concerns a method of forming a semiconductor structure comprising: introducing, at selected conditions, hydrogen and helium species (e.g., ions) in a temporary support (1) to form a plane of weakness (2) at a predetermined depth therein, and to define a superficial layer (3) and a residual part (4) of the temporary support (1); forming on the temporary support (1) an interconnection layer (5); placing at least one semiconductor chip (6) on the interconnection layer (5); assembling a stiffener (8) on a backside of the at least one semiconductor chip (6); and providing thermal energy to the temporary support (1) to detach the residual part (4) and provide the semiconductor structure. The interconnection layer (5) forms an interposer free from any through via.

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METHOD FOR FABRICATION OF A SEMICONDUCTOR STRUCTURE INCLUDING AN INTERPOSER FREE FROM ANY THROUGH VIA

FIELD OF THE INVENTION

The present invention relates to a method for fabrication of a semiconductor structure including an interposer.

BACKGROUND OF THE INVENTION

Interposers are commonly used as passive elements allowing to stack semiconductor chips or dies side by side, to connect them to each other's and to the external environment. Interposers allow to mix chips or dies having different functions (processing units, memory, input/output) to form packaged semiconductor devices presenting high bandwidth configurations and compact form factors. It avoids integrating all the functional elements at the die level, and accelerate devices development time.

US2013/0214423 recalls that an interposer is usually formed of a sufficiently thick layer of material to be rigid (for instance of about 200 micrometers or more), presenting on its opposing faces contact pads for connection to the semiconductor chips and/or to external connectors. An interposer also comprises conductive vias that extend through it, to electrically connect contact pads on its opposing faces.

It is usually difficult to form vias having high aspect ratio (defined as the length of a via divided by the dimension of its section), for instance ratio greater than 5. Therefore,

vias have a minimum cross sectional dimension that are typically greater than 20 micrometers. This dimension limits the number of vias that can be formed in a given surface of the interposer, and therefore limits the integration density of the final, packaged, semiconductor device. Less compact devices are problematic as such, since they may not be placed in items having a small dimension (smart phones, connected watches, etc.). Less compact devices also limit the performance, since the necessary longer connection lines may affect the bandwidth and latency of propagating signals.

New interposer approach, such as the one described in US2014/0191419, that does not require through via, are growing much attention.

For instance, US20030219969 discloses a manufacturing method of a semiconductor device that is packaged with a fine-structured interposer that is fabricated using a silicon substrate. The method includes the steps of forming a peelable resin layer on a silicon substrate, forming the wiring layer on the peelable resin layer, mounting semiconductor chips on the wiring substrate, forming semiconductor devices by sealing the plurality of semiconductor chips by a sealing resin, individualizing the semiconductor devices by dicing the semiconductor devices from the sealing resin side but leaving the silicon substrate, and peeling each of the individualized semiconductor devices from the silicon substrate.

This manufacturing process is particularly difficult to implement. It requires to finely control the adhesive forces at the successive interfaces in the structure such that on applying traction forces on the devices it is possible remove the complete device from the substrate precisely at the resin layer. At the same time the resin layer should provide sufficient adhesion to hold together the different layers on

the silicon substrate during the initial stage of the manufacturing process.

OBJECT OF THE INVENTION

The present invention aims at forming a semiconductor device including at least one semiconductor chip or die, and an interposer to route the electrical signals from/to conductive features of the at least one semiconductor chip. The interposer is free from any through via and the manufacturing process is simple to implement.

SUMMARY OF THE INVENTION

To this effect, the invention relates to a method of forming a semiconductor structure that comprises:

- implanting hydrogen and helium ions in a temporary support, at selected implantation conditions, to form a plane of weakness at a predetermined depth therein, and to define a superficial layer and a residual part of the temporary support;
- forming on the temporary support an interconnection layer, the interconnection layer comprising contact pads and electrically conductive paths between the contact pads;
- placing at least one semiconductor chip on the interconnection layer to electrically couple conductive features of the chip with contact pads of the interconnection layer;
- assembling a stiffener on a backside of the at least one semiconductor chip;
- providing thermal energy, and optionally mechanical energy, to the temporary support to detach the

residual part and provide the semiconductor structure.

The step of providing thermal energy to the temporary support further weakens the plane of weakness and may at the same time reinforce the adhesion of the stiffener to the rest of the structure. It facilitates the detachment of the residual part of the support and its removal by application of moderate forces, and without the risk of detaching the stiffener from the rest of the structure.

According to further non limitative features of the invention, either taken alone or in any technically feasible combination:

- the selected conditions of introduction of the helium species comprises implanting helium ions at a dose comprised between 1 to 2 10^16 at/cm^3; and at an implantation energy comprised between 40 keV to 200 keV;

- the selected conditions of introduction of the hydrogen species comprises implanting hydrogen ions at a dose comprised between 0,5 to 1,5 10^16 at/cm^3; and at an implantation energy comprised between 25 keV to 200keV;

- the interconnection layer presents a first surface on the side of the semiconductor chip and a second surface opposite the first surface, and wherein the contact pads are disposed on both the first and second surfaces;

- the method comprises removing the superficial layer after the detachment of the residual part to expose

at least some contact pads of the second surface of the interconnection layer;

- the method comprises forming emerging feature, such as microbumps or metal studs, on the contact pads of the first surface to facilitates the electrical coupling of conductive features of the semiconductor chip with the contact pads;

- the method comprises forming elementary devices on and/or in the superficial layer;

- the superficial layer presents a thickness less than about 10 micrometers, preferably less than 1 micrometer, and more preferably comprised between 50 and 600nm;

- the distance separating two juxtaposed contact pads is comprised between 0,2 micrometersto 2 micrometers;

- the assembling step is performed after or before the step of placing the at least one semiconductor chip on the interconnection layer;

- the assembling step further comprises a step of underfilling to provide a filling material in the free space surrounding the at least one chip;

- the method comprises a step of dicing the semiconductor structure to provide at least one raw semiconductor device, and a step of packaging the at least one raw semiconductor device to form a final semiconductor device;

- the interconnection layer presents a thickness comprised between 200 nm and 20 micrometers;

- the thermal budget associated with the formation of the interconnection layer is less than 250°C for 4 hours or is less than or 20 minutes at 350°C;

- the step of providing thermal energy comprises applying a temperature comprised between 200°C and 450°C for a period comprised between 10 minutes and 2 hours.

FIGURES

Many other features and advantages of the present invention will become apparent from reading the following detailed description, when considered in conjunction with the accompanying drawings, in which:

- Figure 1 and 2 represent semiconductor structures that can be fabricated by the method according to the invention;

- Figure 3 represents a step of introducing hydrogen and helium species in a temporary support;

- Figure 4 represents a step of forming an interconnection layer;

- Figure 5 represents a step of placing at least one semiconductor chip on the interconnection layer;

- Figure 6 represents a step of assembling a stiffener;

- Figure 7 represents a step of providing energy to the temporary support to detach a residual part;

- Figure 8 represents the semiconductor structure after the removal of the residual part of the temporary support.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS OF THE INVENTION

For simplification of the following description, the same references are used for identical elements or elements achieving the same function in the different embodiments of the invention that will be described.

Figure 1 represents a semiconductor structure 10 that can be fabricated by the method of the present invention.

The semiconductor structure 10 comprises an interposer consisting of an interconnection layer 5. The interconnection layer 5 comprises contact pads 5a preferably disposed on both of its surfaces; and electrically conductive paths 5b between the contact pads 5a. The interconnection layer 5 may present a thickness comprised between 200nm and 20 micrometers, and typically comprised between 5 and 10 micrometers. Some contact pads 5a are electrically coupled to conductive features 6a of at least one semiconductor chip 6. Other contact pads 5a, in particular those disposed on the exposed surface of interconnection layer 5, may provide external input/output connection of the semiconductor structure 10.

As represented on figure 1, the contact pads 5a may be disposed on each surfaces of the interconnection layer 5 at a great density. For instance, the distance separating two

juxtaposed pads 5a may be comprised between 0,2 to 2 micrometers.

Preferably, a plurality of semiconductor chips 6 are disposed and electrically coupled to the interconnection layer 5. The chips 6 may be of different sizes, have different functions and be made according to different technologies. For instance, one chip 6 may be a 14nm technology CPU, while another chip 6 may be a 0,25 micrometers technology input/output chip. Each chip 6 may be, for instance, a DRAM or a SRAM memory chip, a CPU, a GPU, a microcontroller, or an an input/output chip.

Optionally, the semiconductor structure 10 may comprise additional chips 6 positioned on the exposed surface of the interconnection layer 5 (not represented on figure 1).

Interconnection layer 5 allows to co-integrate those different chips having different function to realize a functional semiconductor device. Electrically conductive paths 5b of interconnection layer 5 allows to electrically connect the conductive features 6a of the different chips 6 together so they can functionally cooperate. To allow complex interconnection scheme, the interconnection layer 5 may be composed of a plurality of stacked interconnection sublayers, for instance 2 to 4 sublayers.

To facilitate the electrical coupling of the conductive features 6a of chips 6 with the contact pads 5a of the interconnection layer 5, the contact pads and/or the conductive features 6a may be provided with emerging features 7a, 7b, such as micro bumps.

The semiconductor structure 10 of figure 1 also comprises a stiffener 8 placed on the backside of the chips 6

to provide a rigid support to the structure. Stiffener 8 may be made of any suitable material, such as silicon or epoxy material. The free space between the chips 6, the stiffener 8 and the interconnection layer 5 may be filled with insulating filling material, such as silicon dioxide, for protection and increased rigidity of the semiconductor structure 10.

Optionally, and as represented on figure 2, the semiconductor structure 10 may comprise a superficial layer 3 over, or partially over, the interconnection layer 5, on its surface opposite the chips 6. The superficial layer 3 may comprise elementary devices 11 coupled to some of the contact pads 5a of the interconnection layer 5. Elementary devices 11 may provide additional functions to the chips 6. They may correspond to thin film transistors, PN diodes, or photonics devices for instance.

The semiconductor structure 10 of figure 1 or 2 may be diced to form raw semiconductor devices, which may then be packaged to form final semiconductor devices as it is usual in the art. Packaging may comprise the formation of wire bonds on some of the contact pads 5a disposed on the exposed surface of interconnection layer 5 to provide external connection to the devices.

The present invention is directed to a method of fabrication of the semiconductor structure 10, such as the one represented on figure 1 or 2.

With reference to figure 3, the method comprises a step of introducing hydrogen and helium species, such as hydrogen ions and helium ions, in a temporary support 1 to form a plane of weakness 2 at a predetermined depth in the support 1. The hydrogen and helium species may be introduced by implantation.

The plane of weakness 2 defines a superficial layer 3 and a residual part 4 of the temporary support 1.

For reasons of cost and availability, the support may correspond to a silicon wafer, of circular shape and of normalized dimensions. For instance, the silicon wafer may present a diameter of 200 or 300mm, and a thickness comprised between 300 to 900 micrometers. But the method according to the invention is not limited to such material, shape and size of the temporary support. In general terms, the temporary support is selected to provide a cheap, rigid, self-supporting piece of material. The temporary support 1 may be coated with one or more surface layers of material, such as a semiconductor material, a conductor material or an insulating material. Consequently, superficial layer 3 may also comprise one or more of the surface layers of temporary support 1.

Depending on the implantation conditions that will be detail in greater details in a following part of the description, the superficial layer 3 may present a thickness less than about 10 micrometers, or less than 1 micrometer. Preferably, this thickness is comprised between 50 to 600nm. In some instances, the superficial layer 3 will be completely removed from the final structure, such that its thickness is not of particular importance. A thinner superficial layer 3 nevertheless facilitates its removal.

The superficial layer thickness is typically one or two decade lower than the thickness of the residual part 4. Therefore, the thickness of the residual part 4 is very similar to the thickness of the temporary support 1.

The plane of weakness 2 is provided to allow and to facilitate the removal of the temporary support (and more precisely, of the residual part 4 of the temporary support 1),

in a subsequent detachment step of the method for fabricating the semiconductor structure 10.

The plane of weakness 2 should therefore be precisely controlled such that it remains sufficiently stable in the following step of the process, prior to the removal of the residual part 4. The weakening of the plane 2 may be particularly affected by the thermal budgets involved in these following steps. By “sufficiently stable” it is meant that the weakening of the plane 2, or any other evolution of the plane of weakness 2 during the following steps of the method prior to detachment, should not develop into the deformation of the superficial layer 3 (for instance through blistering of the implanted surface) or should not provoke the premature detachment of the residual part 4.

The plane of weakness 2 should however be sufficiently weakened, such that providing a reasonable amount of energy at the detachment step, allows the removal of the residual part 4.

According to the invention, the degree of weakening of plane 2 is precisely controlled by selecting the condition of introduction (i.e. implantation) of the hydrogen and helium species. The selection should take into consideration the material of the temporary support 1, that may affect the evolution of the weakening of the plane 2, and also take into consideration the thermal budgets (or more generally the energy budget) associated with the processing steps applied to the temporary support prior to the detachment step.

For instance, implantation of hydrogen and helium ions may be performed at the following implantation conditions in particular in a silicon temporary support:

- A hydrogen dose comprised between 0,5 to 1,5 10^16 at/cm^3; and at an implantation energy of 25 keV, or more generally comprised between 10 keV and 200 keV, or between 10 keV and 80 keV.
- A helium dose comprised between 1 to 2 10^16 at/cm^3; and at an implantation energy of 40 keV, or more generally comprised between 10 keV and 200 keV, or between 10 keV and 80 keV.

The hydrogen ions and the helium ions may be successively implanted in the temporary support 1, for instance by implanting first the helium ions. It is also possible to implant the hydrogen ions first. Generally speaking, the implantation energy of the helium and hydrogen species are selected in the proposed ranges, such that the peaks of their respective distribution profile along the depth of the temporary support are located close to each other, i.e. less than 150 nm.

With these implanted species and implantation conditions, it has been shown that the temporary support may receive a thermal budget equivalent to about 4 hours of treatment at 250°C without exhibiting surface deformation or provoking detachment of the residual part 4. By "equivalent thermal budget", it is meant that higher temperature during a shorter period of time; or a lower temperature for a longer period of time may also be applied to the temporary support 1.

It is also to be noted that this thermal budget is applied to the temporary support without providing a stiffener to the implanted surface. Therefore, and for the same implantation conditions and applied thermal budget, the dynamics of blister development is different from the fracture dynamics of an implanted substrates that would have been provided with a stiffener.

The inventors of the present invention have observed that the acceptable thermal budget (i.e. that does not provoke surface deformation and/or premature detachement) is wider than the one that could have been applied to a temporary support provided with a plane of weakness that would have been formed by hydrogen species alone, helium species alone, or any other species. They have notably observed that it is possible to apply a thermal budget of 4 hours of treatment at 250°C (or less) or a thermal budget of 350°C for 20 minutes (or less) without exhibiting surface deformation or provoking detachment of the residual part 4.

In some instances, the method according to the invention may comprise a step of forming elementary devices 11 in and/or on the superficial layer 3. This step may be performed before or after the formation of the plane of weakness 2. Elementary devices 11 may correspond to thin film transistors, PN diodes, or photonics devices for instance. Preferably elementary devices are performing simple electrical or light guiding functions, that does not require high performance levels since the material quality of superficial layer 3 may be deteriorated by the formation of the plane of weakness 2.

Elementary devices are formed by all techniques known in the semiconductor industry, such as deposition, etching, dopant implantation or diffusion, etc.

The elementary devices 11 may be formed after the formation of the plane of weakness 2, but preferably elementary devices 11 are formed before such that their formation does not contribute to the acceptable thermal budget that may be received by temporary support 1.

The thermal budget associated with the formation of elementary devices 11, in the case they are formed after the creation of the plane of weakness 2, should be much less than the acceptable thermal budget, i.e. much less than about 250°C for 4 hours or much less than about 350°C for 20 minutes, for instance.

As represented on the figure 4, the method according to the invention also comprises a step of forming, on the temporary support 1, the interconnection layer 5 comprising contact pads 5a and an electrically conductive path 5b between the contact pads 5a.

At this stage of the process, the interconnection layer 5 present a fist surface, in contact with the temporary support 1 and a second, exposed, surface. Preferably, the contact pads 5a are disposed on both surfaces of the interconnection layer 5.

The interconnection layer 5 may be formed using conventional technique such as metallization or dual damascene. It may comprise successive steps of dielectric deposition, etching according to defined photoresist patterns, barrier deposition, aluminum or copper deposition (for instance by electroplating), and planarization (for instance by chemical-mechanical planarization). The interconnection layer 5 may be constituted of a plurality of stacked interconnected sublayers, for instance 2 to 4 sublayers, to create more complex interconnection scheme. The interconnection scheme is designed such that the chip 6 of the semiconductor structure 10 are functionally coupled together and to external connections.

The thermal budget associated with the formation of the interconnection layer 5 is typically below 250°C for a few

hours depending on the number of sublayers are comprised in the interconnection layer 5. In combination with all other thermal budgets that precede the detachment step, it should not exceed the acceptable thermal budget of, for instance, 4 hours of treatment at 250°C.

Because the contact pads 5a and conductive paths 5b are essentially formed by deposition technique, the interconnection layer 5 does not require the formation of vias in a thick and rigid material. The density of contact pads 5a at the first or second surface can be particularly high. For instance, the distance separating two juxtaposed contact pads 5a may be comprised between 0,2 micrometersand 2 micrometers. The dimension of each pad (of its surface section) may be of the same size, between 0,2 micrometersand 2 micrometers. This is at least 5 times smaller than the dimension of a typical via that are necessary in the traditional interposer approach.

This step of forming the interconnection layer 5 may also comprise forming emerging features 7a on at least some of the contact pads 5a of the exposed surface to facilitate coupling with the conductive features 6a of the chips 6. The emerging features 7a on contact pads 5a may consists of micro bumps. Such micro bumps 7a may be formed by selective metal growth on the contact pads 6a. Alternatively, metal studs may be formed by etching the insulating material surrounding the pads 6a to have them emerge over the exposed surface, followed by melting the emerging metal to form the studs.

If the process of forming the emerging features 7a involves significant thermal budget, the overall thermal budget applied to the plane of weakness 2 that precede the detachment step, should not exceed the acceptable thermal budget of, for instances, 4 hours of treatment at 250°C or 20 minutes at 350°C.

As represented on figure 5, the method of fabricating the semiconductor structure 10 further comprises a step of placing at least one chip 6 on the interconnection layer 5 and electrically couple the conductive feature 8a of the chip 8 with contact pads 5a.

The chip 6 may comprise emerging features 7b, similar to those described in reference to emerging features 7a formed on contact pads 5a, such as micro bumps or metal studs to facilitate their electrical connection to the interconnection layer 5. The emerging features 7b of the chips 6 may contact the emerging features 7a of interconnection layers (as represented on figure 5) or directly be in contact with contact pads 5a.

Alternatively, a direct contact may be formed between the conductive features 8a of the chips 6 and the contact pads 5a, for instance by direct "molecular" bonding or adhesive bonding of the two elements.

Preferably, the step of placing at least one chip 6 involve placing a plurality of chips 6. This can be achieved by well know "pick and place" techniques.

This step is preferably performed at room temperature, such that is does not contribute significantly to the acceptable thermal budget that precede the detachment step.

As explained above, the chips 6 may be of different size, technology and functions. Each chip 6 may be a DRAM or SRAM memory, a CPU, a GPU, a microcontroller, an input/output device.

A selected group of chips, for instance a DRAM chip, a GPU chip and an I/O chip can be placed at their intended position on the interconnection layer 5 and electrically coupled together by the interconnection layer 5 in a functional way.

The semiconductor structure 10 may be composed of a plurality of such group so that, after dicing and packaging, a plurality of semiconductor devices can be manufactured collectively.

Once the chip 6 have been placed on the interconnection layer 5, the free space surrounding the chips 6, over the interconnection layer 5 may be filled with an insulating filling material 9, to protect and rigidify the assembly. The filling material may consist of silicon oxide disposed on interconnection layer 5 and around the chips 6 by a spin on glass technique. The deposition and underfilling of the material is facilitated if it presents a low density.

Preferably also, and as represented on the figure 6, the process according to the invention comprises a step of assembling a stiffener 8 on the backside of the chips 6. The stiffener 8 is made of a sufficiently thick and rigid material such that the semiconductor structure 10 is self-standing once the temporary substrate 1 is removed.

The stiffener 8 can be made for instance of a silicon wafer or a piece of epoxy material. Its dimension should at least correspond to the dimension of the temporary support 1.

The assembly can be made by adhesive bonding, by direct bonding or any other technique. Preferably, the chosen technique does not involve exposition to temperature higher than room temperature, to avoid affecting the plane of

weakness 2 and to provoke the premature detachment of the residual part 4 of the support 1.

In an alternative approach, the backside of the chips 6 may be first positioned and fixed at predetermined position on the stiffener 8, and then the assembly formed of the chips 6 and stiffener 8 placed over connection layer 6, and electrically couple all conductive features 6a of the chips 6 with contact pads 5a.

Whatever the chosen approach for placing the chips 6 on the interconnection layer 5 and assembling the stiffener 8, the process results in the configuration represented on figure 6.

If the process of assembling the stiffener or the step of underfilling the space around the chip 6 with insulating material 9 involves significant thermal budget, the overall thermal budget applied to the plane of weakness 2 that precede the detachment step, should however not exceed the acceptable thermal budget of, for instance, 4 hours of treatment at 250°C.

The method of fabricating the semiconductor structure 10 further comprise a step of providing energy to the temporary support 1, and in particular to the plane of weakness 2, to detach the residual part 4 and provide the semiconductor structure 10. This step is represented on figure 7.

The provided energy can be a thermal energy, such as annealing around 400°C, and more generally comprised between 200°C and 450°C, for a period of 10 minutes to about 2 hours. Any other thermal treatment that leads to the detachment of the residual part 4 from the temporary support 1 may be suitable. In addition to the thermal treatment (and in some

instance alternatively to the thermal energy), the provided energy is a mechanical energy, such as the insertion of a blade at the level of the plane of weakness 2 of the temporary support 1.

Whatever its form, the applied energy, in combination with the energy received at the plane of weakness in the preceding steps, lead to the detachment of the residual part 4 of the support 1, to provide the semiconductor structure 10 represented on figure 8.

The step of providing thermal energy to the temporary support 1 is particularly advantageous, because it further weakens the plane of weakness and at the same time reinforce the adhesion of the stiffener 8 to the rest of the structure. Therefore, it facilitates the detachment of the residual part 4 of the support 1, and its removal by application of moderate forces, and without the risk of detaching the stiffener 8 from the rest of the structure.

In an optional following step, the superficial layer 3 may be removed either completely (if no elementary devices 11 have been formed in a previous step) or partly (to preserve the elementary devices 11). Removal can be performed by selective dry or wet etching, for instance using KOH in the case temporary support is in silicon.

The semiconductor structures 10 that may result from the exposed method are represented on figure 1 and 2.

Naturally, the invention is not limited to the particular embodiment of the method that has been described. The invention also includes all alternative embodiments or additional steps within the scope the appended claims.

For instance, elementary devices 11 or additional elementary devices 11 may also be formed in the the superficial layer 3, after the step of providing energy and detachment of the residual part 4 of temporary support 1.

In an optional step that can take place after the step of detachment, additional chip 6 may be placed over the exposed surface of interconnection layer 5, and electrically coupled to contact pads 5a.

As mentioned above, this semiconductor structure 10 may be diced to form raw semiconductor devices, which may then be packaged to form final semiconductor devices as it is usual in the art. Packaging may comprise the formation of wire bonds on some of the contact pads 5a disposed on the exposed surface of interconnection layer 5 to provide external connection to the devices.

CLAIMS

1. A method of forming a semiconductor structure (10) comprising:
   - introducing, at selected conditions, hydrogen and helium species in a temporary support (1) to form a plane of weakness (2) at a predetermined depth therein, and to define a superficial layer (3) and a residual part (4) of the temporary support (1);
   - forming on the temporary support (1) an interconnection layer (5), the interconnection layer comprising contact pads (5a) and electrically conductive paths (5b) between the contact pads (5a);
   - placing at least one semiconductor chip (6) on the interconnection layer (5) to electrically couple conductive features of the chip (6a) with contact pads (5a) of the interconnection layer (5);
   - assembling a stiffener (8) on a backside of the at least one semiconductor chip (6);
   - providing thermal energy, and optionally mechanical energy, to the temporary support (1) to detach the residual part (4) and provide the semiconductor structure (10).

2. The method as claimed in claim 1, wherein the selected conditions of introduction of the helium species comprises implanting helium ions at a dose comprised between 1 to 2 10^16 at/cm^3; and at an implantation energy comprised between 40 keV and 200 keV.

3. The method as claimed in any preceding claim, wherein the selected conditions of introduction of the hydrogen species comprises implanting hydrogen ions at a dose comprised between 0,5 to 1,5 10^16 at/cm^3; and at an implantation energy comprised between 25 keV and 200keV.

4. The method as claimed in any preceding claim, wherein the interconnection layer (5) present a first surface on the side of the semiconductor chip (6) and a second surface opposite the first surface, and wherein the contact pads (5a) are disposed on both the first and second surfaces.

5. The method as claimed in claim 4, further comprising at least partly removing the superficial layer (3) after the detachment of the residual part (4) to expose at least some contact pads (5a) of the second surface of the interconnection layer (5).

6. The method as claimed in claim 4 or 5, further comprising forming emerging feature (7a), such as microbump or metal studs, on the contact pads (5a) of the first surface to facilitates the electrical coupling of conductive features (6a) of the semiconductor chip (6) with the contact pads (5a).

7. The method as claimed in any preceding claim, further comprising the step of forming elementary devices (11) on and/or in the superficial layer (3).

8. The method as claimed in any preceding claim, wherein the superficial layer (3) present a thickness less than about 10 micrometers, preferably less than 1 micrometer, and more preferably comprised between 50 and 600nm.

9. The method as claimed in any preceding claim, wherein the distance separating two juxtaposed contact pads (5a) is comprised between 0,2 micrometer to 2 micrometers.

10. The method as claimed in claim 1 wherein the assembling step is performed after the step of placing the at least one semiconductor chip (6) on the interconnection layer (5).

11. The method as claimed in claim 1 wherein the assembling step is performed after the step of placing the at least one semiconductor chip (6) on the interconnection layer (5).

12. The method as claimed in the two preceding claims, wherein the assembling step further comprises a step of underfilling to provide a filling material (9) in the free space surrounding the at least one chip (6).

13. The method as claimed in any preceding claim, further comprising a step of dicing the semiconductor structure (10) to provide at least one raw semiconductor device, and a step of packaging the at least one raw semiconductor device to form a final semiconductor device.

14. The method as claimed in any preceding claim, wherein the interconnection layer (5) presents a thickness comprised between 200 nm and 20 micrometers.

15. The method as claimed in any preceding claim, wherein the thermal budget associated with the formation of the interconnection layer (5) is less than 250°C for 4 hours or is less than or 20 minutes at 350°C.

16. The method as claimed in any preceding claim, wherein the step of providing thermal energy comprises applying a temperature comprised between 200°C and 450°C for a period comprised between 10 minutes and 2 hours.

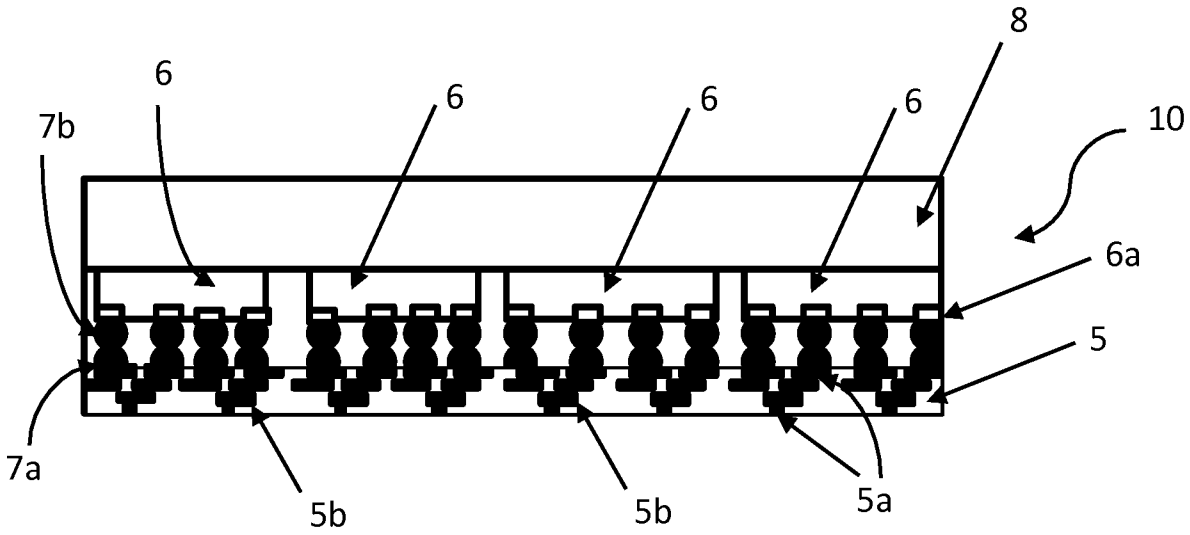

FIG.1

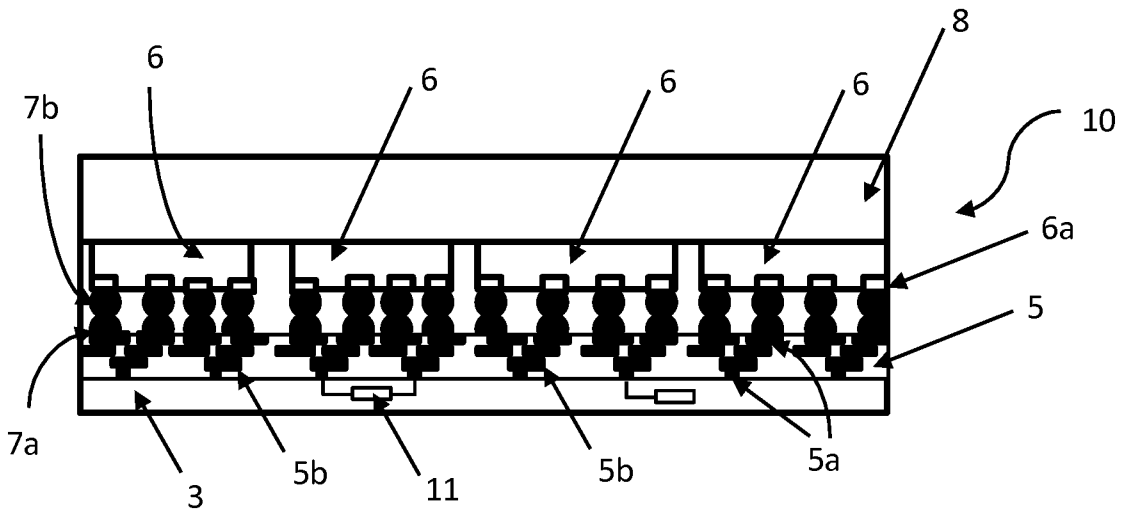

FIG.2

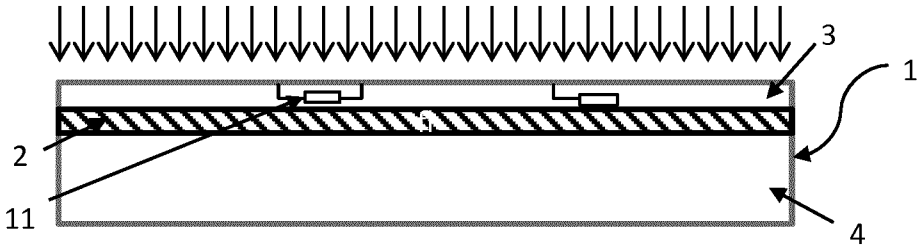

Figure 3

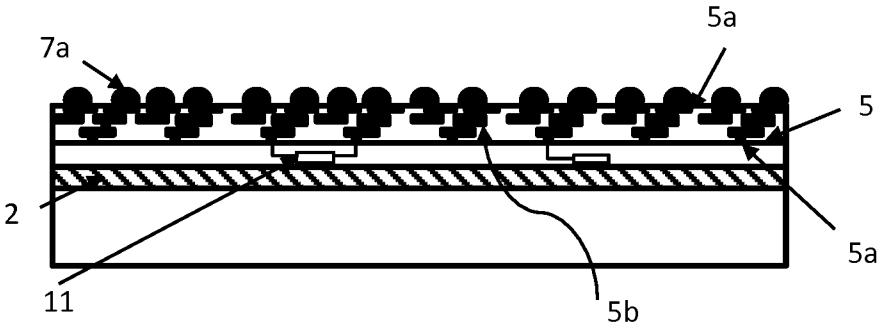

Figure 4

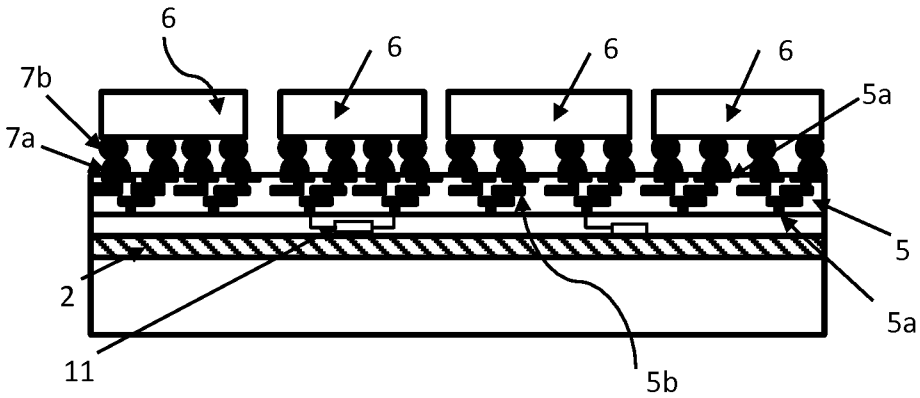

Figure 5

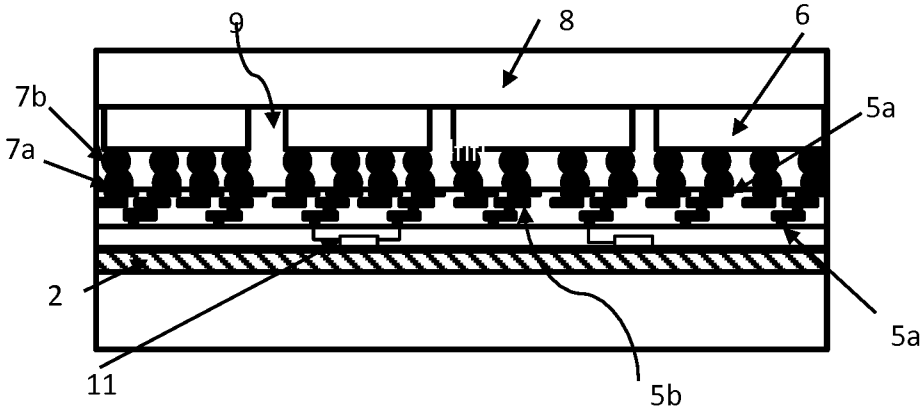

Figure 6

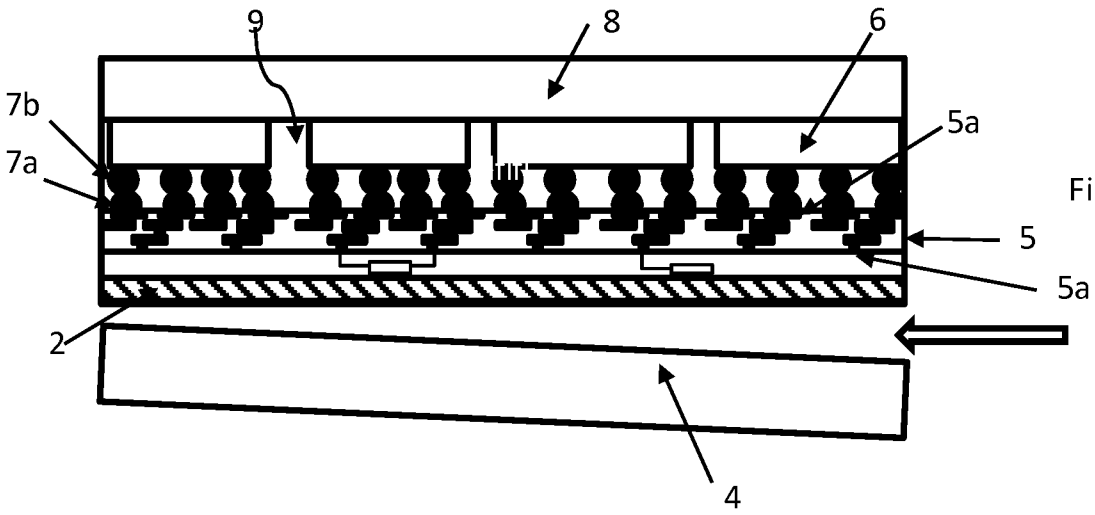

Figure 7

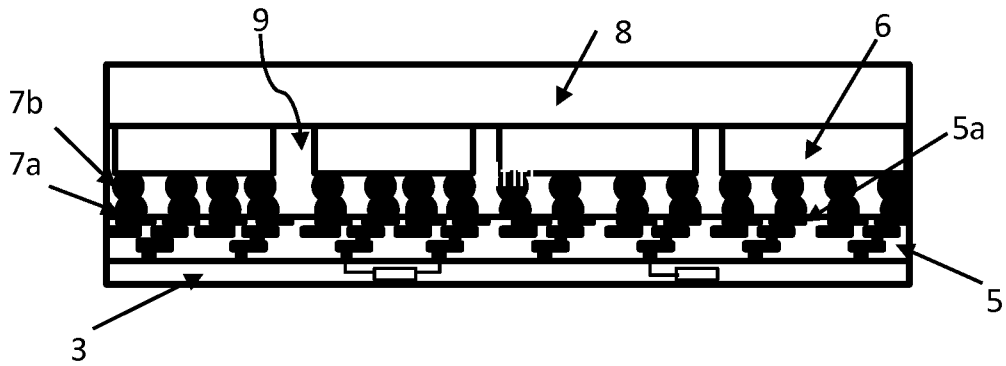

Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/062556

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/48 H01L21/60 H01L21/683 H01L21/762 H01L21/56
H01L25/065 H01L21/98 H01L23/485
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010/075461 A1 (CLAVELIER LAURENT [FR] ET AL) 25 March 2010 (2010-03-25) the whole document -----	1,3,4,7, 8,10,11 2,6,12, 13,15,16
Y	US 2014/339706 A1 (YEE ABRAHAM F [US] ET AL) 20 November 2014 (2014-11-20) the whole document -----	1-4,6-8, 10-13, 15,16
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 August 2017	30/10/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Maslankiewicz, Pawel

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	LAGAHE-BLANCHARD C ET AL: "Hydrogen and helium implantation to achieve layer transfer" In: BENGTSSON S ET AL (Eds.): "Semiconductor Wafer Bonding VII: Science, Technology, and Applications, Proceedings of the International Symposium, April/May 2003, Paris, France, Electrochemical Society Proceedings", 2003, The Electrochemical Society, Inc., XP009193304, vol. 19, pages 346-358, the whole document	1-4,6-8, 10-13, 15,16
Y	US 6 503 778 B1 (YAMAUCHI KAZUSHI [JP] ET AL) 7 January 2003 (2003-01-07)	6
A	column 3, line 37 - column 9, line 34 column 12, line 46 - column 13, line 46 column 18, lines 53-61 column 19, lines 12-25 figures 1-9, 14-15	1-4,7,8, 10-13, 15,16
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A	WO 2009/106177 A1 (SOITEC SILICON ON INSULATOR [FR]; COMMISSARIAT ENERGIE ATOMIQUE [FR];) 3 September 2009 (2009-09-03) page 1, lines 10-15 page 2, lines 5-7 page 3, lines 8-9 page 3, lines 18-29 page 4, lines 4-7 page 6, lines 24-28 page 8, lines 4-11 page 9, lines 13-16 page 10, lines 13-17 page 11, lines 3-7 page 11, lines 18-21 figures 1-5	1-4,6-8, 10-13, 15,16

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FR 2 748 851 A1 (COMMISSARIAT ENERGIE ATOMIQUE [FR]) 21 November 1997 (1997-11-21) the whole document	2,3,15, 16
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A	US 2013/214423 A1 (SADAKA MARIAM [US]) 22 August 2013 (2013-08-22) cited in the application paragraph [0053] - paragraph [0056] figures 7-8	6
A	US 2010/109169 A1 (KOLAN RAVI KANTH [SG] ET AL) 6 May 2010 (2010-05-06) paragraph [0050] - paragraph [0055] paragraph [0058] - paragraph [0061] paragraph [0077] - paragraph [0078] figures 1(A)-(I), 2(G)	1-4,6-8, 10-13, 15,16
A	EP 0 853 337 A1 (FUJITSU LTD [JP]) 15 July 1998 (1998-07-15) column 120, line 13 - column 122, line 24 figures 135-141	10,11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2017/062556

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-4, 6-8, 10-13, 15, 16

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 6-8, 10-13, 15, 16

see the subinventions in items 1.1-1.6 below

1.1. claims: 1-3, 15, 16

Method as in claim 1,
with details concerning the conditions of implanting hydrogen and helium and the thermal budgets associated with the formation of the interconnection layer or with the detachment step.

The technical effect is associated with formation of the plane of weakness so that it remains stable during the process steps before the detachment of the temporary support but provides the detachment during the detachment step. The problem to be solved is how to avoid a premature detachment of the temporary support and an efficient detachment thereof when desired.

1.2. claims: 4, 6

Method as in claim 1,
wherein the contact pads are disposed on both the first and second surfaces of the interconnection layer,
further comprising forming an emerging feature on the contact pads of the first surface for coupling with the semiconductor chip

The technical effect is associated with the formation of an interposer allowing for external interconnection of the chip. The problem to be solved is how to form an interposer designed for external input/output interconnection of the semiconductor structure. A further technical effect is associated with providing means for coupling with the semiconductor chip. The problem to be solved is how to efficiently bond chip electrodes with the corresponding pads of the interconnection layer.

1.3. claim: 7

Method as in claim 1,
further comprising formation of elementary devices on and/or in the superficial layer.

The technical effect is associated with the formation of an interposer having other functionalities apart from the conductive lines. The problem to be solved is how to provide additional functionalities to the semiconductor structure.

1.4. claim: 8

Method as in claim 1,
with details concerning the thickness of the superficial layer.

The technical effect is associated with a compromise between the stability of the superficial layer and hence of the whole structure during the manufacturing process, before the detachment step, on the one hand and, on the other hand, the amount of the temporary support removed during the detachment step, influencing the number of times the temporary support may be reused, as well as the easiness of removal of the superficial layer from the final structure should this be desired. The problem to be solved is how to provide a superficial layer which provides the required stability but does not excessively limit the reusability of the temporary support and may easily be removed if needed.

1.5. claims: 10-12

Method as in claim 1,
further comprising assembling the stiffener after placing the semiconductor chip on the interconnection layer.

The technical effect is associated with the possibility of separately adjusting the position of the chip on the interposer and then of the stiffener on the chip-interposer assembly. The problem to be solved is how to choose the order of method steps so as to obtain good alignment of the components.

1.6. claim: 13

Method as in claim 1,
further comprising a dicing step followed by a packaging step.

The technical effect is associated with the manner of forming the final semiconductor component. The problem to be solved is how to finalise the production of a semiconductor component ready for integration is an electronic device.

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2. claim: 5

Method as in claim 1,
wherein the contact pads are disposed on both the first and second surfaces of the interconnection layer,
further comprising at least partly removing the superficial layer after the detachment of the residual part to expose at least some contact pads of the second surface of the interconnection layer

The technical effect is associated with the formation of an interposer allowing for external interconnection of the chip. The problem to be solved is how to form an interposer

designed for external input/output interconnection of the semiconductor structure. A further technical effect is associated with the possibility of external electrical connection to the exposed contact pads. The problem to be solved is how to provide for easy external connection to the interconnection layer.

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3. claims: 9, 14

A method as in claim 1,
with details concerning the distance between two juxtaposed contact pads or the thickness of the interconnection layer

The technical effect is associated with the density of contact pads at the first and second surface of the interconnection layer (for claim 9) and (hence) with the miniaturisation of the structure (for claims 9 and 14). The problem to be solved is how to find the appropriate distance separating two juxtaposed contact pads and/or the appropriate thickness of the interconnection layer such that the semiconductor structure is small but functional.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2017/062556

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International application No
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