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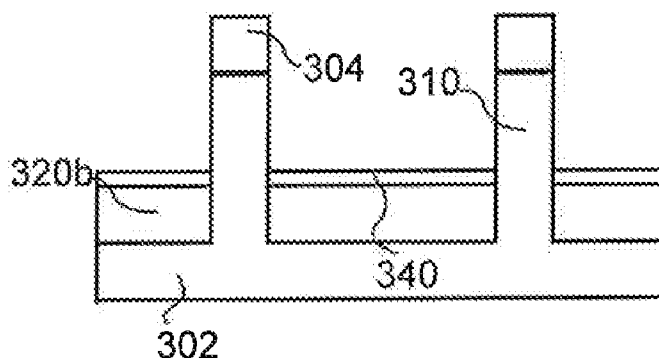


FIG. 3h

(57) Abstract: A technique for forming 3D structures is disclosed, in one particular exemplary embodiment, the technique may be realized as a method for forming 3D structures. The method may comprise providing a substrate comprising at least two vertically extending fins that are spaced apart from one another to define a trench; depositing a dielectric material in the trench between the at least two vertically extending fins; providing an etch stop layer within the dielectric material, the etch stop layer having a first side and a second opposite side; removing the dielectric material near the first side of the etch stop layer.

TECHNIQUES FOR FORMING 3D STRUCTURES

FIELD

The present disclosure relates to a method for processing a substrate, more particularly for a method for processing a substrate with 3D structures.

5 BACKGROUND

In response to an increased need for smaller electronic devices with denser circuits, devices with three dimensional (3D) structures have been developed. An example of such devices includes FinFETs having conductive fin-like structures that are raised vertically above the horizontally extending substrate. Referring to FIG. 1a, there is shown a perspective view of a
10 conventional FinFET 100 formed on a substrate 102. The substrate 102 may comprise, for example, a semiconducting substrate, or silicon-on-insulator. In one example, the substrate 102 may comprise a semiconducting substrate 102a and an oxide layer 102b disposed on the semiconducting substrate 102a. FinFET 100 may also comprise a source region 112 and drain region 114 that are connected to one another by a fin structure 116 serving as the channels. For
15 convenience, FIG. 1a shows FinFET device 100 with only two fin structures 116. However, those of ordinary skill in the art will recognize that other FinFET devices may contain a single fin structure, or three or more fin structures. The conventional FinFET device 100 may also include a gate structure 122 formed across the fin structures 116, and a gate dielectric 124 that electrically isolates the gate structure 122 from the fin structure 116. In the conventional FinFET
20 device 100, the surface area of the fin structure 116 in contact with gate dielectric 124 may be the effective channel region. Referring to FIG. 1b, there is shown a cross sectional view of the FinFET 100 shown in FIG. 1a. For convenience, the source region 112 and the drain region 114 are omitted from the figure. As illustrated, the fin structures 116 may extend vertically from the substrate 102. In another example, the fin structures may be disposed above the oxide layer so
25 that it is electrically isolated from the semiconducting substrate.

Referring to FIG. 2a-2f, there is shown a conventional method for manufacturing FinFET device 100 having fin structures 116 shown in Fig. 1. As illustrated in FIG. 2a, a substrate 202 such as a silicon wafer may be provided. On the substrate 202, a layer of hardmask 204 is formed (FIG. 2b). Thereafter, a layer of photoresist may be deposited onto the hardmask 204. After
30 depositing the resist, the photoresist may be patterned. As known in the art, various methods including photolithography may be used to pattern the photoresist 206. Thereafter, the pattern of the resist 206 may be transferred onto the hardmask 204 and a portion of the substrate 202 via an etching process. The resulting structure may include the patterned hardmask 204 and fin structure 210 corresponding to the pattern of the photoresist 206, as illustrated in FIG. 2c. Those skilled in
35 the art will recognize that the fins structures 210 formed in this process may be the fin structure

116 shown in FIG. 1a and 1b. An oxide layer 220, such as SiO₂, may be deposited on the substrate, as shown in FIG. 2d. Thereafter, a chemical-mechanical polishing/planarization (CMP) process may be performed to planarize the resulting structure (FIG. 2e). As illustrated in FIG. 2e, the CMP process may be performed until either the patterned hardmask 204 or the fin structure 210 is exposed. After the CMP process, a wet or dry etching process may be performed to remove a portion of the oxide layer 210 until the sidewalls of the fin structures 210 are exposed (FIG. 2f). The structure that may be formed after the etching process may include a substrate 202, the oxide layer 220, and one or more fin structures 210 extending above the oxide layer 220.

The above process, although adequate, contains several shortcomings. One of such shortcomings may be found in the uniformity of oxide layer 220 and the fin structures 210. In particular, the etching process used to expose the fin structures 210 may be a non-uniform process with non-uniform etch rate across the substrate 202. The oxide layer 220 in one part of the substrate 202 may be etched at a greater rate compared to the other parts of the substrate 202. Accordingly, the oxide layer 220, with varying thickness, may form.

In addition, the fin structures 210 in one part of the substrate 202 may be exposed before fin structures 210 in other parts of the substrate 202. Moreover, the fin structures 210 exposed earlier part of the etch process may be exposed to etchants for longer period of time. Ultimately, the fin structures 210 with non-uniform widths and heights may form across the substrate 202. Other processes including CMP process may also contribute to a non-uniform oxide layer 220 and fin structures 210. Moreover, the etching process used to expose the fin structures 210 is a timed etching process with a great number of variables. A slight variation in the etching process may result in reduced repeatability or increased substrate-to-substrate non-uniformity. The fin structures 210 on different substrates 202 may have different height and/or width. As the performance of the FinFET devices may be influenced by the properties of the fin structures 210, it may be desirable to form more uniform fin structures 210. As such, uniformity and repeatability of the process used to form the fin structures are highly desirable.

Further, if a wet etching process is used to expose the fin structure 210, a phenomenon such as corner rounding 211 may occur. Such a phenomenon may contribute to less than optimal performance of the FinFET devices.

Accordingly, a new method for forming the fin structure is needed.

SUMMARY

A technique for forming 3D structures is disclosed. In one particular exemplary embodiment, the technique may be realized as a method for forming 3D structures. The method may comprise providing a substrate comprising at least two vertically extending fins that are spaced apart from one another to define a trench; depositing a dielectric material in the trench

between the at least two vertically extending fins; providing an etch stop layer within the dielectric material, the etch stop layer having a first side and a second opposite side; removing the dielectric material near the first side of the etch stop layer.

5 In accordance with other aspects of this particular exemplary embodiment, the dielectric material near the second side of the etch stop layer is not removed while the dielectric material near the first side of the etch stop layer is removed.

In accordance with further aspects of this particular exemplary embodiment, the method further comprises exposing a portion of the at least two vertically extending fins.

10 In accordance with additional aspects of this particular exemplary embodiment, the providing the etch stop layer comprises implanting etch stop layer forming particles into the dielectric material.

In accordance with further aspects of this particular exemplary embodiment, the species of the particles comprises at least one of Si and Ge.

15 In accordance with additional aspects of this particular exemplary embodiment, the species of the particles comprises at least one of N and C.

In accordance with further aspects of this particular exemplary embodiment, the species of the particles comprises at least one of H, He, Ne, Ar, Kr, and Xe.

In accordance with additional aspects of this particular exemplary embodiment, the providing the etch stop layer further comprises annealing the substrate.

20 In accordance with other aspects of this particular exemplary embodiment, the etch stop layer extends horizontally.

In accordance with additional aspects of this particular exemplary embodiment, the etch stop layer extends vertically.

25 In accordance with another exemplary embodiment, the technique may be realized as a method for forming FinFET structure, where the method comprises providing an etch stop layer within a dielectric layer deposited on the substrate, the substrate comprising at least one vertically extending fin.

In accordance with other aspects of this particular exemplary embodiment, the providing an etch stop layer comprises implanting ions into the dielectric layer.

30 In accordance with further aspects of this particular exemplary embodiment, the ions comprise at least one of Si containing ions and Ge containing ions.

In accordance with additional aspects of this particular exemplary embodiment, the ions comprise at least one of N containing ions and C containing ions.

35 In accordance with further aspects of this particular exemplary embodiment, the ions comprises at least one of H containing ions, He containing ions, Ne containing ions, Ar containing

ions, Kr containing ions, and Xe containing ions.

In accordance with additional aspects of this particular exemplary embodiment, the providing the etch stop layer further comprises annealing the substrate after implanting ions into the dielectric material.

5 In accordance with further aspects of this particular exemplary embodiment, the ions are implanted at a temperature ranging between about 25° C to about 750° C.

In accordance with additional aspects of this particular exemplary embodiment, the etch stop layer has a first side and a second opposite side.

10 In accordance with other aspects of this particular exemplary embodiment, the method further comprises removing the dielectric material disposed on the first side of the etch stop layer without removing the dielectric material disposed on the second side of the etch stop layer.

The present disclosure will now be described in more detail with reference to exemplary embodiments thereof as shown in the accompanying drawings. While the present disclosure is described below with reference to exemplary embodiments, it should be understood that the present disclosure is not limited thereto. Those of ordinary skill in the art having access to the teachings herein will recognize additional implementations, modifications, and embodiments, as well as other fields of use, which are within the scope of the present disclosure as described herein, and with respect to which the present disclosure may be of significant utility.

BRIEF DESCRIPTION OF THE DRAWINGS

20 In order to facilitate a fuller understanding of the present disclosure, reference is now made to the accompanying drawings, in which like elements are referenced with like numerals. These drawings should not be construed as limiting the present disclosure, but are intended to be exemplary only.

Fig. 1a and 1b illustrates a conventional 3D structure.

25 Fig. 2a-2f illustrate a conventional method for forming conventional 3D structure.

Fig. 3A-3j illustrate an exemplary method for forming 3D structure in accordance with one embodiment of the present disclosure.

FIG. 4 illustrates an exemplary system for forming 3D structure in accordance with one embodiment of the present disclosure.

30 FIG. 5 illustrates another exemplary system for forming 3D structure in accordance with another embodiment of the present disclosure.

DETAILED DESCRIPTION

Herein a novel technique for forming a 3D structure is disclosed. The structure may have one or more protrusions or trenches that extend in vertical direction relative to the substrate. The substrate, herein, may be metallic, semiconducting, or insulating substrate, or a combination

thereof. For purpose of clarity, the embodiments are introduced in context of "particles." The particles may be charged or neutral, sub-atomic, atomic, or molecular particles that process the substrate.

Referring to FIG. 3a-3i, there is shown an exemplary technique for forming a 3D structure according to one embodiment of the present disclosure. Initially, a substrate 302 is provided as illustrated in FIG. 3a. On the substrate 302, a layer of hardmask 304 is deposited as shown in FIG. 3b. Thereafter, a layer of resist 306, for example, a photoresist, may be deposited onto the hardmask 304 and patterned via various patterning processes. Examples of the patterning process may include photolithography, EUV lithography, double patterning lithography, and nano-imprint lithography. The pattern formed on the resist 306 may be transferred onto the hardmask 304 and/or the substrate 302 via, for example, an etching process. The resulting structure may include fin structures 310 corresponding to the pattern of the patterned resist 306 as shown in FIG. 3c. In the present embodiment, the hardmask 304 may remain on the fin structures 310. In another embodiment, the hardmask 304 may be removed during the pattern transferring process. Thereafter, an insulating material may be deposited to form an insulating layer 320 (as shown in FIG. 3d). In the present disclosure, various insulating materials may be deposited. Examples of the insulating materials may include SiO_2 and SiN . In some embodiments, different insulating materials may be deposited. For example, SiN may be deposited first, and SiO_2 may be deposited on top of the SiN , or vice versa. Those of ordinary skill in the art will recognize that the present disclosure does not preclude a scenario where other insulating materials are deposited on the substrate 302. After the insulating layer 320 is formed, the CMP process may be performed to planarize the resulting structure as illustrated in FIG. 3e.

After the CMP process, etch stop layer 340 may be provided within the oxide layer 320 at a desired depth as shown in FIG. 3g. In the present embodiment, the etch stop layer 340 is provided after the CMP process. However, the present disclosure does not preclude provision of the etch stop layer 340 prior to the CMP process. In some embodiments, the etch stop layer 340 may be provided during formation of the insulating layer 320.

Various processes may be used to provide the etch stop layer 340. In one embodiment, the etch stop layer 340 shown in FIG. 3g may be provided via a deposition process. In the present embodiment, the etch stop layer 340 may be provided by introducing etch stop layer forming particles 330 in the form of ions. In another embodiment, the particles 330 in another form may be introduced using other processes.

In the present disclosure, particles 330 may contain various species. The preferred species may be silicon (Si). Silicon is preferred as the species may form a buried Si rich etch stop layer 340 when provided into the insulating layer 320. However, those of ordinary skill in the art

will recognize that in other embodiments, other species, including metallic and other non-metallic species, may be used. Examples of other species may include nitrogen (N) to form SiN rich etch stop layer 340. In another example, carbon (C) particles 330 may be implanted to form SiC rich etch stop layer 340. Yet in other embodiments, other species including boron (B), aluminum (Al), gallium (Ga), indium (In), germanium (Ge), tin (Sn), phosphorous (P), arsenic (As). Moreover, the species of the particles 330 chosen may include the species found in the fin structure 310. Such species may include, among others, Si and Ge. Further, other types of particles, including sub-atomic particles (e.g. protons or electrons) may also be implanted. When provided, one or more species may be provided at uniform rate such that the dose of the particles 330 introduced across the dielectric layer 320 may be uniform, or at varying rate such that doses of the particles 330 in different portions of the dielectric layer differ.

In the present disclosure, a single species may be introduced into the insulating layer 320. Alternatively, two or more species may be co-implanted. For example, particles 330 of C or N species may be implanted together, or with additional particles 330 of Si species. Alternatively, all three species may be implanted. Moreover, other species including hydrogen (H), helium (He), neon (Ne), argon (Ar), krypton (Kr), xenon (Xe), and other inert species, or a combination thereof, may be co-implanted with Si, C, and/or N. In the present embodiment, the implantation process may preferably be performed so as to minimize or reduce possible amorphization or damage to the fin structures 310. For example, the implantation process may be performed while the fin structures 310 are maintained at an elevated temperature ranging between about 25° C to about 750 ° C so as to minimize amorphization or damage to the fin structure 310.

Optionally, the substrate 302 may be annealed to enhance formation of the etch stop layer 340, as shown in FIG. 3g. In the present embodiment, the implanted particles 330 having a Gaussian implant depth profile may change into a box-like implant depth profile during the annealing process via thermal diffusion. As a result, concrete etch stop layer 340 with substantially uniform depth may form.

After providing the etch stop layer 340, the resulting structure may comprise, among others, the substrate 302 having the fin structures 310, an upper and lower insulating layers 320a and 320b spaced apart by the etch stop layer 340. Although the figure shows only the etch stop layer 340 extending along the horizontal direction, the etch stop layer 340, in other embodiments, may extend along the vertical direction, proximate to the vertically extending surface of the fin structures 310. For example, the particles 330 may also be implanted into the insulating layer 320 at one or more angles deviating from the angle normal to the horizontally extending surface of the substrate 302 ("zero angle"). The particles 330 implanted at a non-zero angle may form the vertically extending etch stop layer near the sidewall of the fin structures 310.

In addition to the orientation, other properties of the etch stop layer 340 may be adjusted. For example, the thickness of the etch stop layer 340 may be adjusted by controlling the dose and the energy of the particles 330 and/or the duration in which the particles 330 are exposed to elevated temperature. Further, the depth of the etch stop layer 340 may also be adjusted by
5 adjusting the energy by which the particles 330 are implanted, the material of the insulating layer 310, and/or species of the particles 330 implanted. For example, the density of the SiO_2 (~ 1.8) may be greater than that of SiN (~ 3.44). By depositing insulating materials with higher density and/or implanting lighter particles 330, an etch stop layer 340 with a shallower depth may be achieved. Accordingly, by controlling the parameters of the implant and annealing process,
10 and/or the type of insulating material and the particles species, an etch stop layer 340 with desired properties may be achieved.

After forming the etch stop layer 340, the upper insulating layer 320a may be removed via a dry or wet etching process (FIG. 3h). Unlike the conventional process, the upper insulating layer 320a may be removed more uniformly even if a non-uniform etching process is used. In
15 particular, the etching process may continue until the etch stop layer 340 is exposed and until the upper insulating layer 320a is removed uniformly. The wet or drying etching process may be followed by the ion assisted selective etching process to remove the now exposed etch stop layer 340 (FIG. 3i). In the present embodiment, the ion assisted selective etching process may be performed. In this process, the etch stop layer 340 may be removed with minimal removal of the
20 fin structures 310 or the lower insulating layer 320b. During or after removing the etch stop layer 340, the hard mask 304 may be removed from the fin structures 310 (FIG. 3j). As illustrated in FIG. 3j, more uniform fin structures 310, and insulating layer 320b with more uniform thickness may form across the substrate 302. In addition, higher substrate-to-substrate uniformity may be achieved.

25 Herein, several exemplary systems for forming the etch stop layer 340 are provided. Referring to FIG. 4, there is shown a simplified figure of an exemplary system 400 according to one embodiment of the present disclosure. The figure is not drawn to scale. In this figure, a particle implantation system 400 for implanting particles 322 into the insulating layer 320 is shown. The particle implantation system 400 may comprise a particle source 402 for generating
30 desired particles 40. The generated particles 40 may be emitted from the particle source 402 and travel along one or more paths toward a substrate 412 disposed downstream. The substrate 412 may be supported on a platen 414, which may or may not provide DC or RF bias to the substrate 412. The substrate 412 and the platen 414 may be moved in one or more directions and/or dimensions (e.g., translate, rotate, tilt, and combination thereof) relative to the particles 40
35 incident on the substrate 412.

Optionally, the ion implantation system 400 may include a series of complex beam-line components 422 through which the particles 40 may pass. If included, the series of beam-line components 422 may include at least one of a mass analyzer (not shown), a first acceleration or deceleration stage (not shown), a collimator (not shown), and a second acceleration or deceleration stage (not shown). Much like a series of optical lenses that manipulate a light beam, the beam-line components 422 can shape, filter, focus, and manipulate the particles 40. For example, the second acceleration or deceleration stage of the beam line components 422 can vary the energy of the particles 40, and the substrate 412 may be implanted with particles 40 at one or multiple energies. In addition, the beam-line components may shape the particles 40 into a spot or ribbon shaped particle beam 40 having one or more desired energies.

Further, the beam-line components may scan the particle beam 40 in one or more directions and/or dimensions relative to the substrate 412. The scanning of the particle beam 40 may occur in conjunction with the movement of the substrate 412. Accordingly, either the particle beam 40 may move in one or more directions/dimensions relative to a stationary substrate 412, or vice versa. Or, both the particle beam 40 and the substrate 412 may move in one or more directions/dimensions relative to one another at the same time. In the present disclosure, the particle beam 40 and/or the substrate 412 may move at a constant or varied rate. By moving the particle beam 40 and/or the substrate 412 relative to one another at a constant rate, particles 322 may be implanted with uniform dose. If, however, the particle beam 40 and/or the substrate 412 move relative to one another at a varied rate, particles 322 may be implanted with non-uniform doses. Implanting particles with non-uniform dose rates across the substrate 412 may compensate one or more non-uniform processes subsequent to the implantation process. For example, if the annealing process is performed after the implantation process, and if the annealing process is less than optimally uniform across the substrate, a non-uniform particle implantation process may be performed in order to compensate the non-uniformity in the annealing process. The non-uniform implantation may include implantation with varied energy or dosage across the substrate. In one embodiment, the particles may be an implantation at different dose rates from the center to the edge of the substrate. After the annealing process, the particles may be activated at a more uniform rate.

Referring to FIG. 5, there is shown a simplified figure of another exemplary system 500 according to one embodiment of the present disclosure. The figure is not drawn to scale. In this figure, a plasma based particle implantation system 500 for implanting particles 322 into the insulating layer 320 is shown. The particle implantation system 500 may comprise a chamber in which a substrate 512 is disposed. The substrate 512 is disposed on a platen 514, which is electrically coupled to a first power source 514. The first power supply 516 may provide to the

platen 514 and the substrate 512 continuous or pulsed, positive or negative, RF or DC bias.

The system 500 may also comprise a plasma source 504 proximate to the chamber 502, inside or outside of the chamber 502. Although only one plasma source 504 is shown, the present disclosure does not preclude the system 500 with multiple plasma sources. In some embodiments, the plasma source 504 may be a remote plasma source 504 that is spatially removed from the chamber 502. The plasma source 504 may be an inductively coupled plasma source 502.

However, those of ordinary skill in the art will recognize that in the present disclosure, the plasma source 504 is not limited to a particular plasma source. For example, the plasma source 504 may be a capacitively coupled plasma source, helicon plasma source, or microwave plasma source. As illustrated in the figure, the plasma source 504 is electrically coupled to and powered by a second power supply 506. The second power supply 506 may provide continuous or pulsed, RF or DC power. In some embodiments, the platen 514 and/or the substrate 512 powered by the first plasma source 516 may act as the plasma source.

In operation, one or more gases/vapors containing desired species may be contained in the chamber 502. Thereafter, the plasma source 504 may be powered to convert the gases/vapors into plasma 522 containing, among others, ions, electrons, neutrals, and other radicals of desired species. In the present embodiment, the power applied to the plasma source 504 may be constant or varied. A detailed description of the plasma source being applied with varied RF or DC power may be found in U.S. Patent Application Serial No.: 12/105,761, which is incorporated in its entirety by reference.

As illustrated in the figure, the plasma 522 may be generated near the substrate 512. While the plasma is near the substrate 512, the first power supply 516 may provide continuous or pulsed, positive or negative, RF or DC bias to the substrate 512. The ions in the plasma 522 may be attracted and implanted into the substrate 512 in response to the provided bias. In the present embodiment, a pulsed, DC bias with uniform bias level may be provided to the substrate 512. Alternatively, the bias provided to the substrate 512 may be a pulsed DC bias; but the bias level may ramp upward or downward at a constant or varied rate. A detailed description of the bias ramping is provided in U.S. Patent No.: U.S. Patent No.: 7,528,389, which is incorporated in its entirety by reference.

Herein, several process parameters of the process for implanting particles to form the etch stop layer 340 are provided. As noted above, one of the process parameters that may be controlled during the implantation process may be the dose rate. For example, the rate by which the particles 322 are implanted may range from about 1×10^{15} to about 5×10^{15} . A dose rate of about 1×10^{15} may result in an etch stop layer of about 2nm thickness. Meanwhile, a dose rate of about 5×10^{15} may result in an etch stop layer of about 10nm thickness. By controlling, among

others, the dose rate, the etch stop layer 340 with desired thickness may be achieved.

In addition to the dose rate, the movements of the particle beam 40 and/or the substrate 412 (e.g. scan rate) may be controlled to provide uniform or non-uniform particle implantation. As noted above, either the particle beam 40 or the substrate 412, or both, may move (e.g. scan) relative to one another at a non-uniform rate to induce non-uniform particle implantation. Such a non-uniform implantation may be useful to compensate one or more non-uniform processes that may be performed after the implantation process. For example, the annealing process that may be performed after the implantation process may be a non-uniform process. Accordingly, the rate by which the particle beam 40 or the substrate 412, or both, may move (e.g. scan) relative to one another may be varied across the substrate 412. For example, the rate may be varied from the center of the substrate 412 to the edge of the substrate 412. Such a non-uniform movements may induce a more uniform etch stop layer 340 after the annealing process.

If a plasma based particle implantation system 500 is used, the bias provided to the substrate 512 may be varied. For example, the bias provided from the first power supply 516 may ramp up or down at a constant rate or varied rates (e.g. in steps). Such a variation may enhance the box-like profile of the etch stop layer 340 formed on the substrate 302.

Although only a limited number of the process parameters are discussed, those of ordinary skill in the art will recognize that other parameters may also be adjusted to optimize the formation of the etch stop layer 340.

Several embodiments of techniques for forming 3D structures are disclosed. Those of the art will recognize that the present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Thus, such other embodiments and modifications are intended to fall within the scope of the present disclosure. Further, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

What is claimed is:

1. A method for forming FinFET structure, the method comprising:
providing a substrate comprising at least two vertically extending fins that are spaced
5 apart from one another to define a trench;
depositing a dielectric material in the trench between the at least two vertically extending
fins;
providing an etch stop layer within the dielectric material, the etch stop layer having a
first side and a second opposite side; and
10 removing the dielectric material near the first side of the etch stop layer.

2. The method according to claim 1, wherein the dielectric material near the second side
of the etch stop layer is not removed while the dielectric material near the first side of the etch
stop layer is removed.
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3. The method according to claim 2, further comprising:
exposing a portion of the at least two vertically extending fins.

4. The method according to claim 1, wherein the providing the etch stop layer comprises
20 implanting etch stop layer forming particles into the dielectric material.

5. The method according to claim 4, wherein species of the particles comprises at least
one of Si and Ge.

25 6. The method according to claim 4, wherein species of the particles comprises at least
one of N and C.

7. The method according to claim 4, wherein species of the particles comprises at least
one of H, He, Ne, Ar, Kr, and Xe.
30

8. The method according to claim 4, wherein the providing the etch stop layer further
comprises annealing the substrate.

9. The method according to claim 1, wherein the etch stop layer extends horizontally,
35

10. The method according to claim 1, wherein the etch stop layer extends vertically.

11. A method of forming FinFET structure, the method comprising:

providing an etch stop layer within a dielectric layer deposited on the substrate, the substrate comprising at least one vertically extending fin.

5

12. The method according to claim 11, wherein the providing an etch stop layer comprises implanting ions into the dielectric layer.

13. The method according to claim 12, wherein the ions comprises at least one of Si containing ions and Ge containing ions.

10

14. The method according to claim 12, wherein the ions comprises comprises at least one of N containing ions and C containing ions.

15. The method according to claim 12, wherein the ions comprises at least one of H containing ions, He containing ions, Ne containing ions, Ar containing ions, Kr containing ions, and Xe containing ions.

15

16. The method according to claim 12, wherein the providing the etch stop layer further comprises annealing the substrate after implanting ions into the dielectric material.

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17. The method according to claim 12, wherein the ions are implanted at a temperature ranging between about 25° C to about 750° C.

18. The method according to claim 11, wherein the etch stop layer has a first side and a second opposite side/

25

19. The method according to claim 18, further comprising:
removing the dielectric material disposed on the first side of the etch stop layer without removing the dielectric material disposed on the second side of the etch stop layer.

30

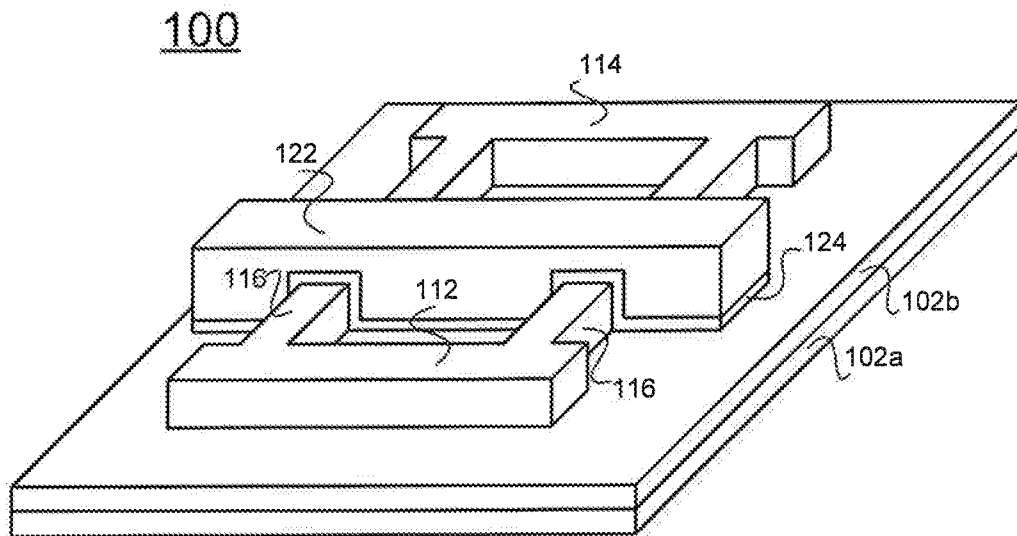


FIG. 1a
(Prior Art)

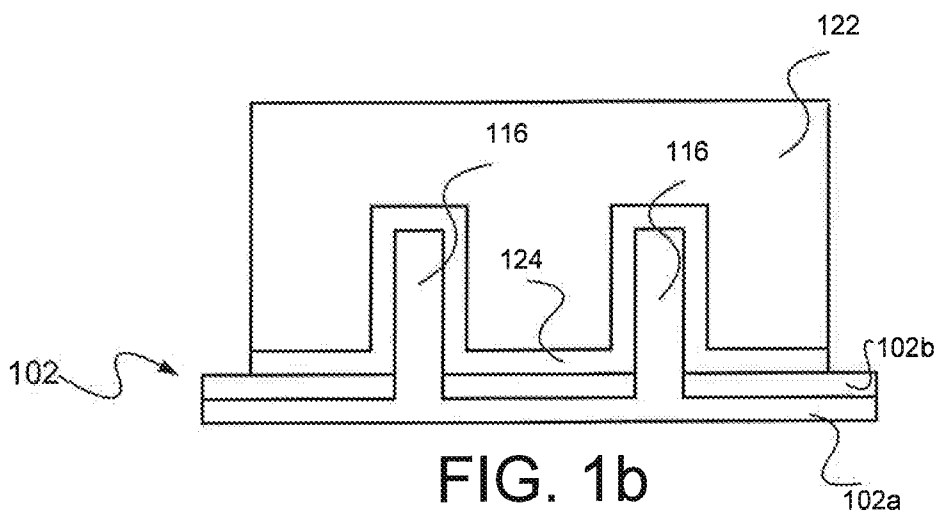


FIG. 1b
(Prior Art)

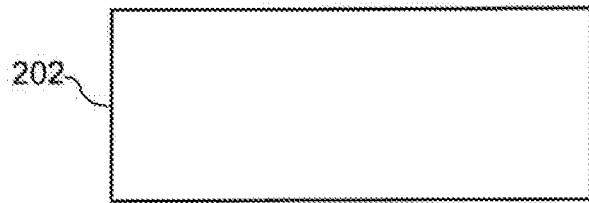


FIG. 2a
(Prior Art)

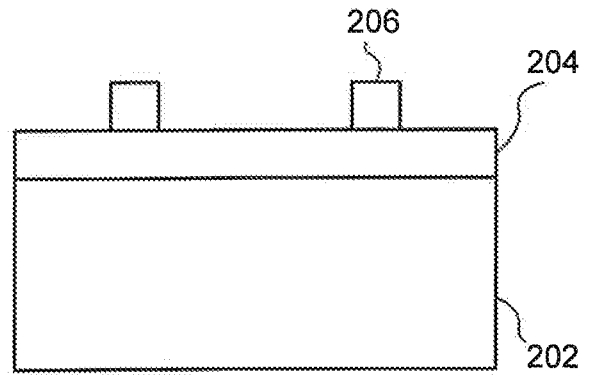


FIG. 2b
(Prior Art)

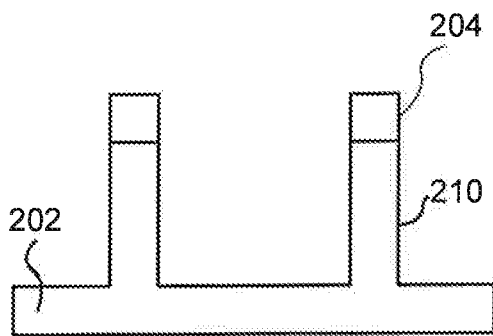


FIG. 2c
(Prior Art)

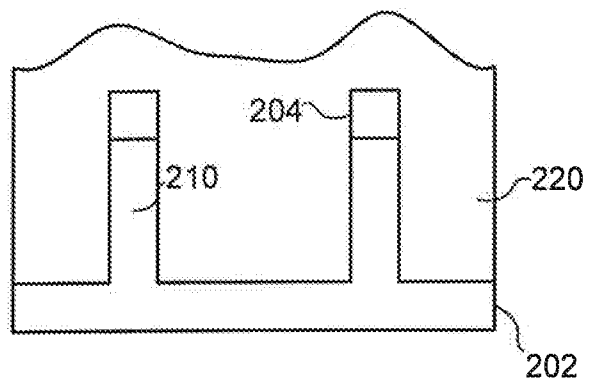


FIG. 2d
(Prior Art)

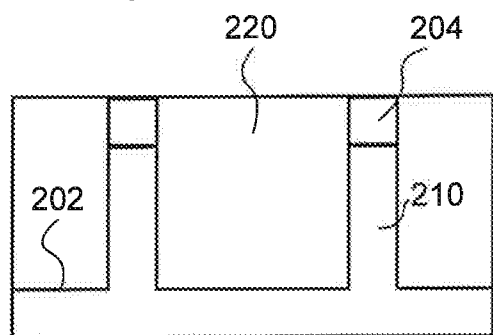


FIG. 2e
(Prior Art)

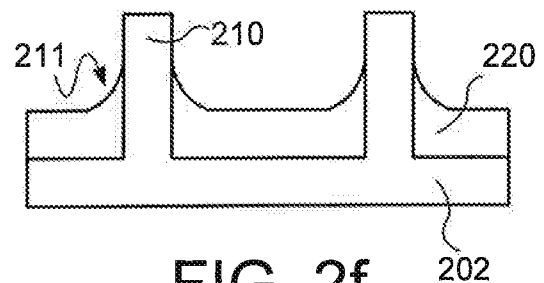


FIG. 2f
(Prior Art)



FIG. 3a

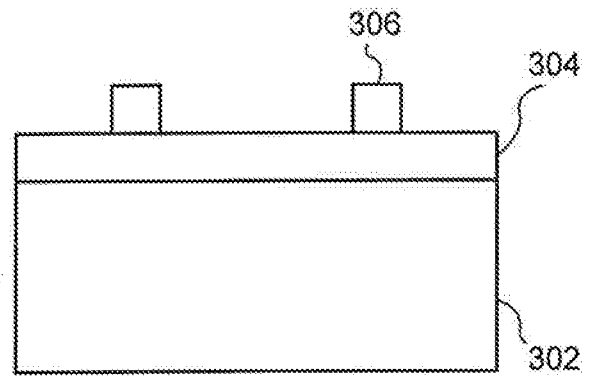


FIG. 3b

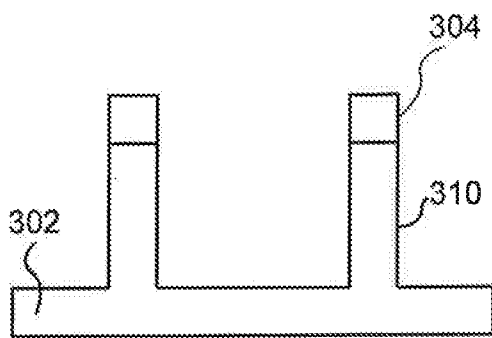


FIG. 3c

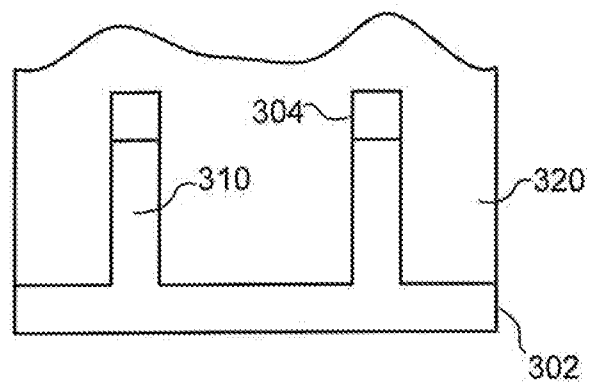


FIG. 3d

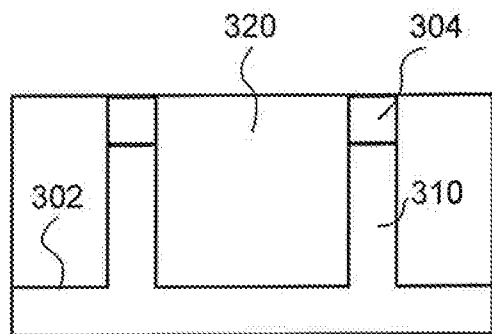


FIG. 3e

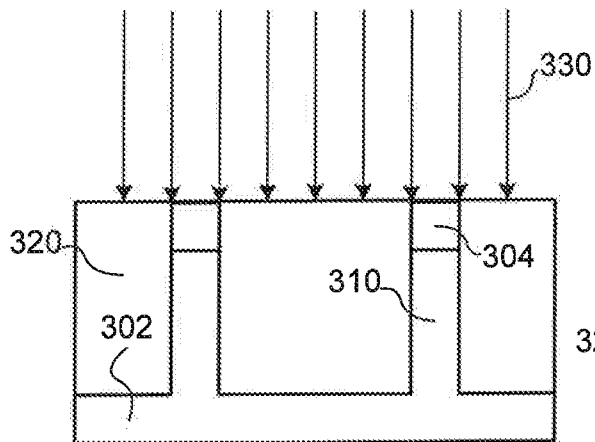


FIG. 3f

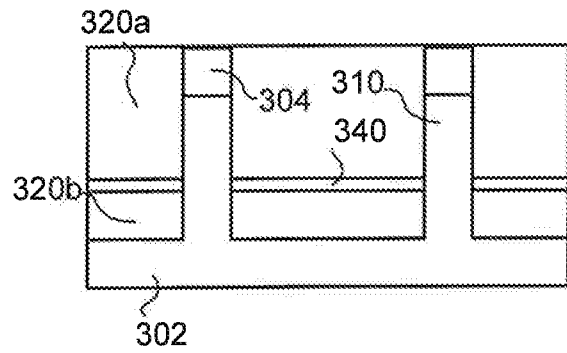


FIG. 3g

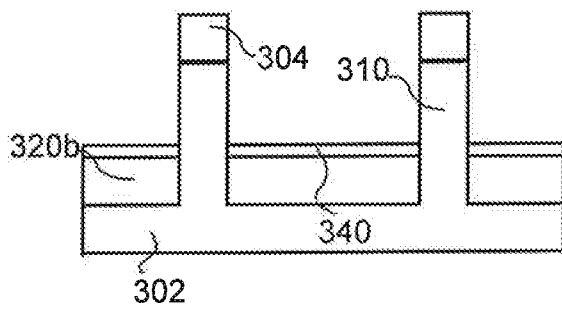


FIG. 3h

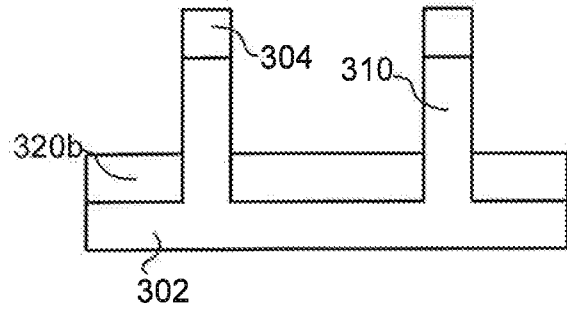


FIG. 3i

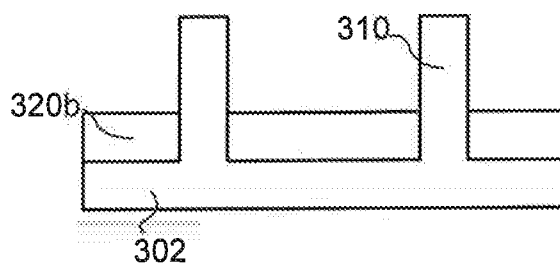
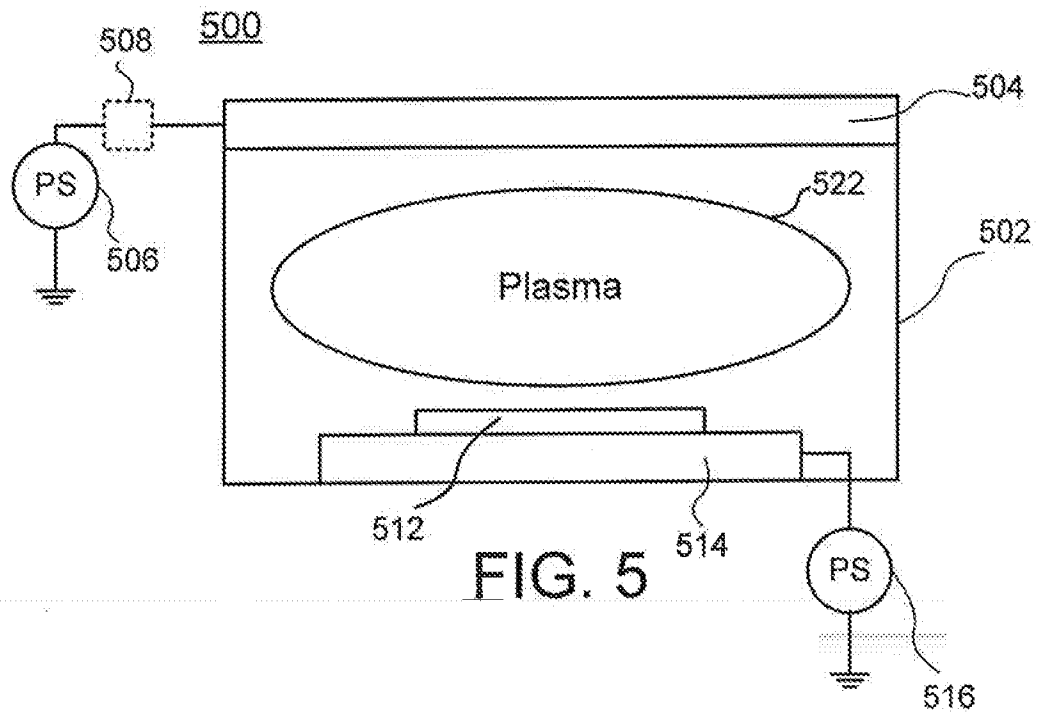
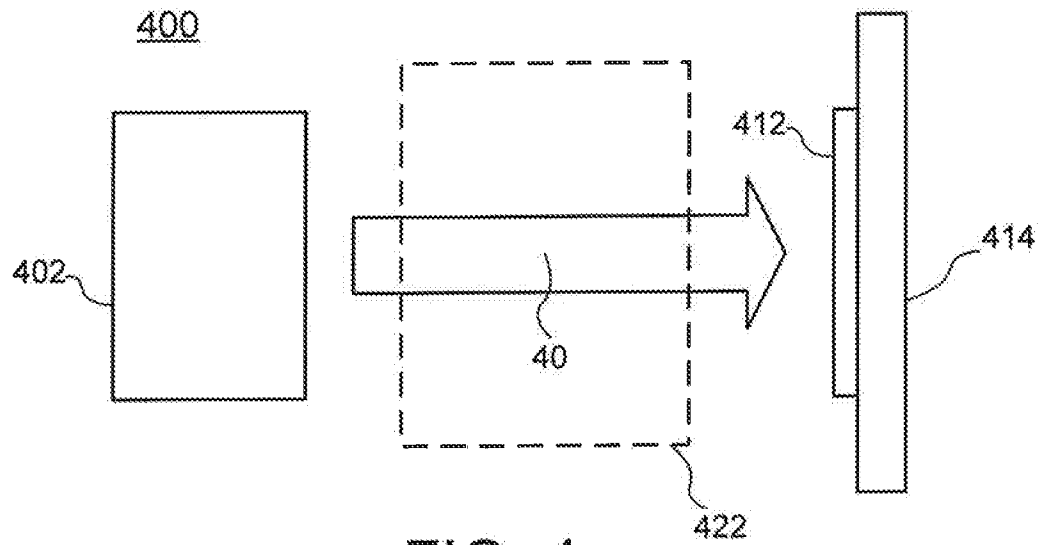


FIG. 3j



INTERNATIONAL SEARCH REPORT

International application No

PCT/US2012/038140

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H01L21/8234 H01L21/265
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	abstract; claims; figures 2e-2g paragraph [0028] - paragraph [0029] -----	5-7,10, 13-15,17
X	US 2009/057780 A1 (WONG ROBERT C [US] ET AL) 5 March 2009 (2009-03-05)	11,18,19
Y	abstract; claims; figures 4-9 -----	13-15,17
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Y	abstract; claims; figures 6c-6h paragraph [0078] - paragraph [0079] -----	10, 13-15,17
	-/-	



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

11 July 2012

Date of mailing of the international search report

18/07/2012

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Authorized officer

Wirner, Christoph

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/038140

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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Information on patent family members

International application No

PCT/US2012/038140

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