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(54) IMPROVEMENTS IN ELECTRON BEAM DEFLECTION CONTROL SYSTEM

(71) We, HITACHI, LTD., of 1—5—1, Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, and NIPPON TELEGRAPH and TELEPHONE PUBLIC CORPORATION of 1—16, 1-chome, Uchasiawai-cho, Chiyada-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an electron beam deflection control system which is suitable for use in an electron beam exposure system, or a graphic display system.

The electron beam exposure system functions to form a minute pattern of a semiconductor device or circuit on a mask or a semiconductor wafer with an electron beam. In order to draw the necessary pattern with the electron beam, it employs an electron beam deflection control system which deflects the electron beam linearly at a uniform speed and which, upon completion of the drawing of one pattern, cuts off the electron beam and moves it to the starting point of the next pattern.

The electron beam deflection control system of this type includes a digital system and an analog system.

A known electron beam deflection control system beased on the digital system is one wherein coordinate data corresponding to respective points of a line pattern are sequentially generated in accordance with data fed from a digital computer, and are then converted into an analog signal in a stepped shape by a digital-to-analog converter, the electron beam being deflected stepwise.

With such a known system, however, the settling time of the digital-to-analog converter, which determines each step width of the stepped signal, is long. Disadvantageously, therefore, as the line pattern becomes longer, the drawing time becomes longer.

A known electron beam deflection control system based on the analog system is one wherein a closed loop circuit consisting of a differential amplifier with limiter function and an integrator is provided, start point and end point levels of a drawing pattern generated by a digital-to-analog converter being sequentially impressed on the closed loop circuit, and the outputs of the integrator converge to the end point level, thereby producing a triangular deflection signal.

With such analog system, however, the outputs of the integrator become inaccurate thus degrading the precision of the drawing pattern. Besides, the convergence time of the first-order lag system constructed of the differential amplifier and the integrator increases as a dead time. Therefore, in cases where the drawing pattern is short, the dead time is no longer negligible compared with the drawing time. Since the triangular deflection signal is used also for the movement of the beam between the patterns, the dead time increases still more.

It is an object of the present invention to provide an electron beam deflection control system which makes it possible to execute drawing at a very high speed, and also to enhance the precision of a drawing pattern.

According to the present invention there is provided an electron beam deflection control system including: generation means to selectively generate either a ramp wave signal varying at a comparatively low speed or a stepped wave signal varying at a comparatively high speed; change-over means to control said generation means so as to generate either the ramp wave signal or the stepped wave signal in response to the required deflection length of an electron beam; and, deflection means to deflect the

electron beam with the signal from said generation means.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

Fig. 1 is a block diagram of a known charged beam deflection control system based on the digital system;

Fig. 2 is a block diagram of a known charged beam deflection control system based on the analog system;

Fig. 3 is a block diagram which shows a first preferred embodiment of a charged beam deflection control system;

Fig. 4 is a graph explaining the operation of the embodiment shown in Fig. 3 as the analog system;

Fig. 5 is a graph explaining the operation of the embodiment of Fig. 3 as the digital system;

Figs. 6(a) and 6(b) are a block diagram and a graph, respectively, which illustrate a second preferred embodiment of the charged beam deflection control system; and

Fig. 7 shows an example of a pattern drawn by the second embodiment shown in Figs. 6(a) and 6(b).

Referring first to the known beam deflection control system based on the digital system shown in Fig. 1, the system comprises a digital computer 1, a logical circuit 2 for producing a control signal, digital-to-analog converters 3 and 4, amplifiers 5 and 6, for deflection signals, a deflector 7, and a beam blanker 8. In operation, coordinate data corresponding to respective points of a pattern are sequentially produced by the logical circuit 2 in accordance with data fed from the digital computer 1. The resultant data are converted into analog signals (voltages or currents) by the digital-to-analog converters 3 and 4. The converter 3 and the amplifier 5 correspond to the x-direction, and the converter 4 and the amplifier 6 to the y-direction. Since the analog signals are in a stepped shape, a beam is deflected stepwise. In this system, the time at which the step is advanced is controlled by a signal of a clock generator contained within the logical circuit 2. A beam blanking signal can be digitally generated by the logical circuit 2. In the case where the movement of the beam is done in the beam blanking state, the digital-to-analog converter 3 or 4 is controlled by the logical circuit 2 so that the beam may arrive at a target point in one block. In the case of this system, the precision of the drawing pattern is excellent. On the other hand the system has the following disadvantage. Each step width of the stepped signal is determined by the settling time of the digital-to-analog converter. In general, the setting time is long. Therefore, as the drawing pattern becomes longer, the drawing time becomes longer proportionally. The system is accordingly very inconvenient for drawing a long pattern.

Referring next to the known beam deflection control system based on the analog system shown in Fig. 2, the system includes the same components 1 to 8 as in the known system shown in Fig. 1. The system additionally includes differential amplifiers 9 and 10 with voltage limiters, a logical circuit 11 for beam blanking signal generation and containing a voltage comparator therein, and integrators 12 and 13. In operation, when the x-directional deflection is considered, an analog signal level corresponding to the start point of line drawing is generated by the digital-to-analog converter 3. Subsequently, an analog signal level corresponding to the end point of the line drawing is generated by the converter 3. Then, owing to the closed loop constructed of the differential amplifier 9 and the integrator 12, when the difference between the output of the converter 3 and an output of the integrator 12 is great and an output of the differential amplifier 9 is limited, the output of the integrator 12 varies at a fixed rate. At this time, a line is drawn whilst providing a beam ON signal at an output of the logical circuit 11 under the control of the logical circuit 2. When the output of the integrator 12 approaches the output of the converter 3, the output of the differential amplifier 9 enters a linear region, and the first-order lag circuit composed of the differential amplifier 9 and the integrator 12 converges to a point at which the output of the converter 3 and that of the differential amplifier 9 coincide. At this time the output of the differential amplifier 9 becomes zero. It is detected by the voltage comparator contained in the logical circuit 11, and a beam OFF signal is provided at the output of the logical circuit 11 so as to blank the beam. This process is repeated, and the scanning and drawing are done by triangular waves. The y-directional deflection is similarly executed by the converter 4, the operational amplifier 10 and the integrator 13.

The disadvantages of this system are that the output of the integrator 12 becomes inaccurate in the vicinities of the start and end points of the line thus degrading the quality of the drawing pattern, and that the convergence time of the first-order lag system constituted of the differential amplifier 9 and the integrator 12 increases as a dead time. This is particularly the case, when the length of the drawing line becomes less than about 10 μm, the dead time is no longer negligible in comparison

with the drawing time. Furthermore it leads to an increase of the dead time to carry out the beam movement under the beam blanking state by the use of the triangular wave signal.

Referring now to the first preferred embodiment of an electron beam deflection control system shown in Fig. 3, the components 1, 2, 3, 5, 7, 8 and 12 correspond to the components of the systems shown in Figs. 1 and 2.

The system further includes a voltage generator 14 for determining the line speed, polarity change-over circuit 15 for changing-over the polarity of an output from the voltage generator 14, an analog switch 16, a logical circuit 17 for beam blanking signal generation, a differential amplifier 18, a zero detector 19, and a sampling and holding circuit 20. Except for the digital computer 1, the logical circuit and and the beam blanker 8, the components corresponding to one axis (x-axis or y-axis) are illustrated in Fig. 3. An identical construction applies to the other axis.

The operation of this system will now be explained. First of all, in case of drawing a comparatively long line by the analog system, an analog output signal 31 corresponding to the start point of the line is generated by the digital computer 1, the logical circuit 2 and the converter 3. The sampling and holding circuit 20 is set at a sampling mode in advance, and the output signal therefrom is applied to a first input terminal of the differential amplifier 18. Since an output signal 121 from the integrator 12 is applied to a second input terminal of the differential amplifier 18, an output 181 from the differential amplifier 18 becomes equal to the gain thereof times a voltage which is equal to the difference between the output signals 31 and 121. When a control signal 23 is previously given so as to energize the analog switch 16 so as to pick-up the output from the differential amplifier 18, then the analog switch 16, the integrator 12 and the differential amplifier 18 form a first-order lag closed loop. Therefore, the circuitry operates so as to bring the output signals 121 and 31 into coincidence, and the start point of the line is set. The subsequent operation will be explained in conjunction with the graphs shown in Fig. 4. At a time t_0, data of the end point of the line are compared with data of the start point and the decision of the magnitudes is made by means of the logical circuit 2. A signal 21 for controlling the polarity of the polarity change-over circuit 15 so as to direct the output signal 121 towards the end point is obtained, with which the polarity of the polarity change-over circuit 15 is set to non-inversion or inversion. At a time t_1, the sampling and holding circuit 20 is placed into a holding mode by a control signal 22 from the logical circuit 2. At a time t_2 slightly later than t_1, the data of the end point are placed in the converter 3, and an output signal 31 of an analog voltage corresponding to the end point is generated. At a time t_3 slightly after the time t_2, the analog switch 16 is changed-over from being connected to the differential amplifier 18 to being connected to the polarity change-over circuit 15, by means of a control signal 23 from the logical circuit 2. Then, the integrating operation of the integrator 12 is initiated in conformity with the line speed set by the voltage generator 14 and the polarity set by the polarity change-over circuit 15, and the output signal 121 varies linearly with respect to time. Simultaneously therefore, the logical circuit 17 is rendered operative by a control signal 24, and an output signal in the form of a beam blanking signal 171 energizes the beam blanker 8 in order to start the drawing. At the time t_3, the sampling and holding circuit 20 is changed-over from the holding mode to the sampling mode by the control signal 22 from the logical circuit 2, and the output signal 31 is applied to the differential amplifier 18. When, at a time t_4, the output signal 121 coincides with the output signal 31, the output 181 becomes zero, the zero detector 19 operates, providing an output signal 191. The coincidence between the output signal 191 and the beam blanking signal 191 in the logical circuit 17 causes the beam blanking signal to be switched off, so that the drawing is stopped. Simultaneously, a control signal 24′ from the logical circuit 17 is fed to the logical circuit 2, the analog switch 16 is changed-over to being connected to the differential amplifier 18 by means of the control signal 23, and a closed loop consisting of the analog switch 16, the logical circuit 17 and the differential amplifier 18 is established so as to settle the output signal 121 to the same level as that of the output signal 31. As will be described in detail later, the output signal 121 is settled to the next start point level between a time t_5 and a time t_6. The output signal 121 is amplified by the deflection amplifier 6 and then applied to the deflector 7, to deflect the beam. By repeating this process, the pattern can be drawn as a set of lines. In this manner, the triangular wave signal is used for drawing the long line, whereby a higher speed than in the digital system is achieved.

Secondly, there will be explained a case of performing the beam movement between patterns by the digital system. For this purpose it will be assumed that at the time t_5 in Fig. 4 the drawing of the first pattern is

completed, and the beam is shifted to the second pattern. At this time, the sampling and holding circuit 20 remains in the sampling mode, to supply the converter 3 with data of the start point of the second pattern and to generate an output signal 31 of an analog voltage corresponding thereto. In this case, the analog switch 16 receives an output from the differential amplifier 18, and the closed loop consisting of the analog switch 16, the integrator 12 and the differential amplifier 18 is established to bring the output signal 121 into coincidence with the output signal 31 at the time t_6. At this time, the time in which the output signal 121 follows up the output signal 31 is determined by the time-constant of the integrator 12 divided by the gain of the differential amplifier 18, and the speed of drawing is high. Meanwhile, the logical circuit 17 is inhibited by a control signal 24 so as not to operate, and the output signal 171 remains "off".

Next, the system will be described in the case of drawing a short line by the digital system. The sampling and holding circuit 20 is set at the sampling mode by a control signal 22, while the analog switch 16 is connected to receive the output from the differential amplifier 18 by the control signal 23. Accordingly, the output signal 121 follows up the output signal 31 very quickly as shown in Fig. 5.

Digital data corresponding to the start point of the line are fed from the digital computer 1 through the logical circuit 2 to the converter 3. At a time t_1, the output signal 31 has settled to a level corresponding to the start point. The output signal 171 of the locial circuit 17 is switched on by a control signal 24, and the drawing of a first dot is initiated. At the time t_2, the clock generator and the counter contained in the logical circuit 2 are started, data corresponding to a second dot are fed from the logical circuit 2 to the converter 3, and the output signal 31 of the converter 3 is shifted and settles to a level corresponding to the position of the second dot. At the time t_3, the output signal 31 is similarly shifted and settles to a level corkesponding to the position of a third dot. In the case, $\Delta t=t_2-t_1=t_3-t_2$ needs to be greater than the settling time of the digital-to-analog converter, and the interval between the first and second dots needs to be smaller than the diameter of the dot. By this process, the line is drawn as a row of dots. When the dot reaches the end point of the line at the time t_4, the output signal 171 of the logical circuit 17 is switched off by the control signal 24 at a time $t_5=t_4+\Delta t$, and the line drawing is completed.

Whether the digital system or the analog system is to be used may be determined by operating the logical circuits contained in the block 2 in conformity with the data fed from the digital computer 1 and this controlling the control signals 22, 23 and 24 as well as the input signal of the digital-to-analog converter 3.

Referring now to the second embodiment of the electron beam deflection control system shown in Figs. 6(a) and 6(b), there is shown the principal portions of a deflection signal generator circuit for the X-axis or Y-axis. For the sake of convenience, the illustrated circuit will hereinafter be referred to as the circuit for the X-axis. First, an analog switch 16 is switched on. Then, a difference e_ϵ between an output signal 31 from a digital-to-analog converter 3 and an output signal 121 from an integrator 12 are fed to the two inputs of a differential amplifier 9 provided with a voltage limiter. An output e_L from the differential amplifier 9 is applied via the analog switch 16 to an integration resistor 122 of the integrator 12. It is assumed here that a switch 16' is held in the off position. A current of a value obtained by dividing the output e_L of the amplifier 9 by the sum of the internal resistance of the switch 16 and the resistance of the integration resistor 122 flows through the integration resistor 122. Under the action of an operational amplifier 123, it is integrated by an integration capacitor 124 and produces an integrator output signal 121. The input-output characteristic of the differential amplifier 9 is as illustrated in Fig. 6(b). This circuit provides a constant value of e_{LO} for $|e_\epsilon|>\Delta e$. As a result, the integration capacitor 124 integrates a fixed current, so that the output current 121 is constituted by a signal which varies at a fixed rate with respect to time. Since the output signal 121 always varies so as to bring e_ϵ near to zero, $|e_\epsilon|=\Delta e$ is subsequently established. The differential amplifier 9 performs a linear operation with further lapse of time, so that e_L decreases and the varying rate of the output signal 121 also decreases. When the output signal 121 has become equal to the absolute value of the output signal 31, $e_\epsilon=0$ holds, that is, the current to be integrated becomes zero, so that the output signal 121 settles at this value. Accordingly, by prescribing to below a predetermined error the value Δe at which the limiting characteristic of the differential amplifier 9 begins, the deflection signal has satisfactory linearity. Although not shown in Fig. 6(a), an appropriate voltage comparator may be used for monitoring the output e_1 of the differential amplifier 9 so as to control the electron beam intensity upon detection of the state $|e_L|<e_{LO}$. Thus, in an electron beam exposure system, the excessive exposure of the electron beam to a photo resist film or a

fluorescent film as attributed to the lowering of the beam deflecting speed at the end point can be effectively avoided. Subsequently, the switch 16 is turned off. This does not change the output signal 121 because the integration current is zero under the present state. Thereafter, the X-coordinate of the next target point is fed to the digital-to-analog converter to slightly shift a Y-axial deflection signal (refer to ΔY in Fig. 7). After a sufficient period of time which allows the output voltage of the digital-to-analog converter to settle, the switch 16 is turned on, whereby the output e_0 of the integrator 12 initiates the deflection at uniform speed. At this time, accordingly, the electron beam is switched on to execute the exposure. By repeating such procedure, smearing exposure as illustrated in Fig. 7 is carried out. Supposing that the exposure of an area A in Fig. 7 has been begun at a point P_{10} and finished at a point P_{1n} by the procedure described above the operation of high-speed deflection to a start point P_{20} for the smearing operation of the next area B will be stated below. When the output signal 121 has settled at the final point P_{1n} of the area A, the switch 16 is turned off, and the X-coordinate of the point P_{20} is fed to the digital-to-analog converter, the digital-to-analog converter of the Y-axial deflection circuit being fed with the Y-coordinate at the point P_{20}. When the switch 16' is subsequently turned on, the output signals 31 and 121 are added through resistors 41 and 42 respectively and the sum is amplified by a coefficient multiplier 40. The current obtained by dividing an output voltage of the coefficient multiplier 40 by the sum between the internal resistance of the switch 16' and the resistance of a resistor 125 is integrated by the integration capacitor 124. Here, a path which extends from the input point of the operational amplifier 123 via the operational amplifier 123, resistor 42, coefficient multiplier 40, switch 16' and resistor 125 back to the above referred to input point constitutes a negative feedback loop. Therefore, the operation after turning the switch 16' "on" is controlled so as to establish $e_0+e_{DA}=0$, where e_0 and e_{DA} denote the output voltages of the integrator 12 and the converter 3, respectively. The settling takes place under the state in which the above equation is fulfilled. The time constant T of the circuit at this high-speed deflection operation is given by:

$$T \simeq 2\ c.r./k$$

on condition that the resistors 41 and 42 have equal values of resistance. In the above formula, *c*, *r* and *k* represent the capacitance of the integration capacitor, the sum of the resistance of the resistor 125 and the internal resistance of the switch 16', and the coefficient of the coefficient multiplier 40, respectively. By properly selecting r/k to a small value, therefore, the output signal 121 can be settled to the target point in a much shorter time than in the foregoing operation of the low-speed mode, it being comparatively easy to shorten the settling time to several tenths of a second. After the start point has been reached in this way, the smearing operation for the area B is executed by the low-speed mode employing the switch 16'.

As set forth above, the scanning and drawing in the analog system and the digital system can be easily accomplished by the block arrangements in Fig. 3 and Fig. 6(a). Therefore, by drawing a long pattern with the analog system very quickly and executing the beam movement between lines or between patterns with the digital system very quickly, a high-speed system can be provided. It is also possible to draw a short pattern or a pattern requiring an especially high precision by the use of the digital system.

It is also possible that, whilst drawing a pattern along the first axis with the analog system, the second axis is moved to draw oblique lines with the digital system by means of the clock generator and the counter which are contained in the logical circuit 2. Further, it is possible to compensate for a deflection distortion or a sample rotation error.

Owing to the system of this invention, there can be realized an electron beam exposure system which skillfully exploits the high drawing speed of the analog system in the case of drawing a long pattern and the high speed and high precision of the digital system in the case of drawing a short pattern and the case of moving a beam between patterns. It should be particularly noted that the above described systems are not limited by the conversion speed of the digital-to-analog converter. Therefore, the good results can be achieved with a converter of low speed, and a system of high cost performance can be provided.

WHAT WE CLAIM IS:—

1. An electron beam deflection control system including: generation means to selectively generate either a ramp wave signal varying at a comparatively low speed or a stepped wave signal varying at a comparatively high speed; change-over means to control said generation means so as to generate either the ramp wave signal or the stepped wave signal in response to the required deflection length of an electron beam; and, deflection means to deflect the

electron beam with the signal from said generation means.

2. An electron beam deflection control system according to Claim 1, wherein said change-over means comprises means to control said generation means so as to generate the ramp wave signal when a relatively long line pattern is to be drawn by the electron beam, and so as to generate the stepped wave signal during either a time when the electron beam is to be moved between patterns or a time when a relatively short line pattern is to be drawn by the electron beam.

3. An electron beam deflection control system according to Claim 1 or 2, wherein said generation means comprises digital-to-analog conversion means to generate an analog signal corresponding to coordinate data of a pattern to be drawn, differential amplification means receiving an output of said conversion means as one input thereof, voltage generation means to generate a predetermined voltage and integration means to integrate one of outputs of said differential amplification means and said voltage generation means, selectively applied through said change-over means and to deliver the integrated output as the other input of said differential amplification means, the integrated output being applied to said deflection means, and said change-over means comprises a switch means to selectively apply one of the outputs of said differential amplification means and said voltage generation means of said integration means.

4. An electron beam deflection control system according to Claim 3, further including a computer which generates the coordinate data for said conversion means.

5. An electron beam deflection control system according to Claim 3 or 4, further including detector means to detect that the output of said differential amplification means has become substantially zero, and means to perform blanking of the electron beam with a detection output of said detection means.

6. An electron beam deflection control system according to any one of the preceding Claims 3 to 5, further including means to sample or hold the output signal of said conversion means, said sampling or holding means being connected between said conversion means and said differential amplification means.

7. An electron beam deflection control system according to Claim 4, wherein said switch means comprises: first switch means to conduct or cut off the output of said amplification means; and second switch means to conduct or cut off a sum between the outputs of said digital-to-analog conversion means and said integration means and to deliver the conducted output to said integration means.

8. An electron beam deflection control system constructed and arranged to operate substantially as herein described with reference to and as illustrated in Fig. 3 or Fig. 6(a) of the accompanying drawings.

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1594476 COMPLETE SPECIFICATION
5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

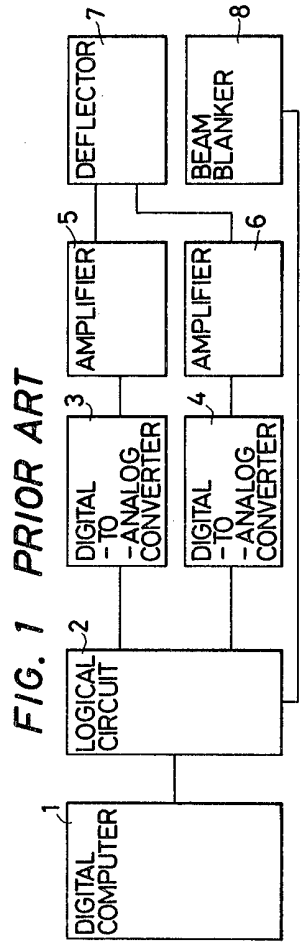


FIG. 1 PRIOR ART

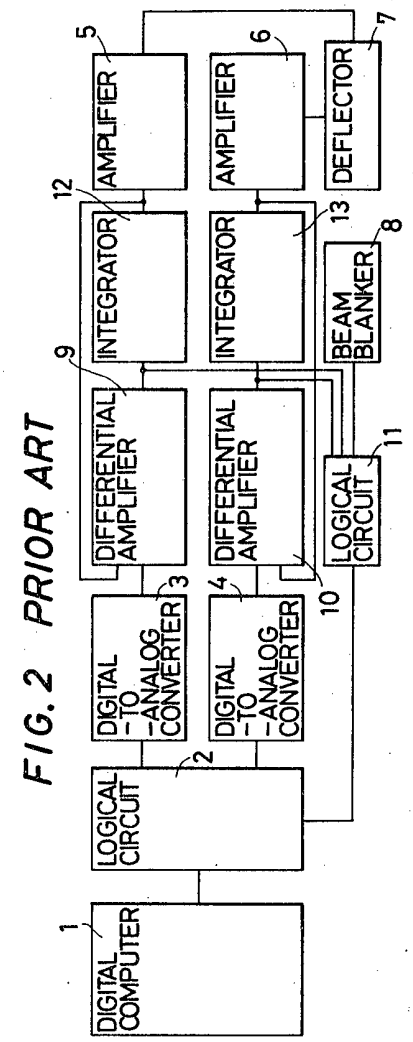


FIG. 2 PRIOR ART

FIG. 3

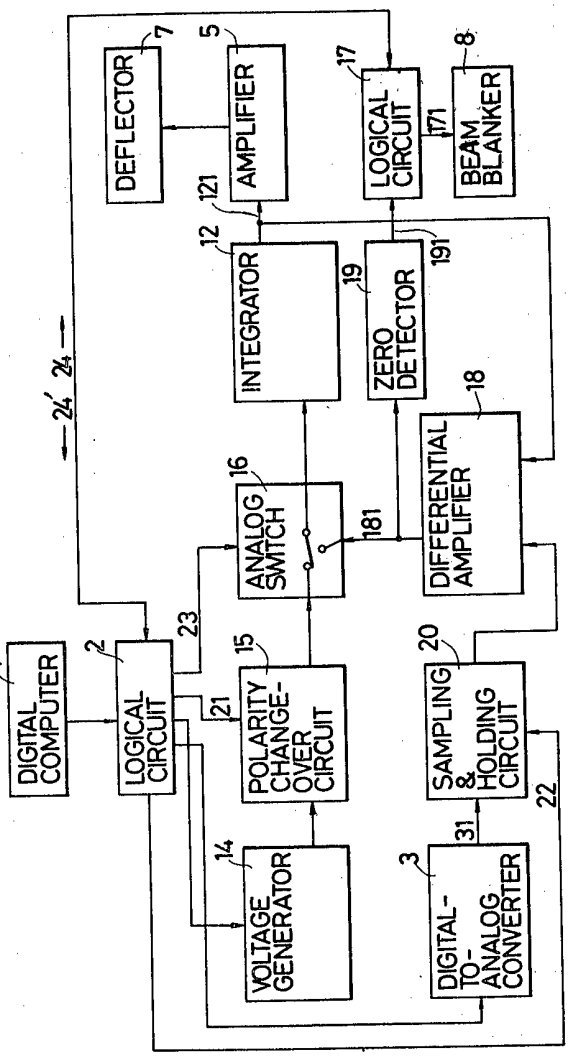

DIGITAL COMPUTER
LOGICAL CIRCUIT
POLARITY CHANGE-OVER CIRCUIT
VOLTAGE GENERATOR
ANALOG SWITCH
INTEGRATOR
DEFLECTOR
AMPLIFIER
ZERO DETECTOR
LOGICAL CIRCUIT
BEAM BLANKER
DIFFERENTIAL AMPLIFIER
SAMPLING & HOLDING CIRCUIT
DIGITAL-TO-ANALOG CONVERTER
1
2
3
5
7
8
12
14
15
16
17
18
19
20
21
22
23
24
24'
31
121
171
181
191

FIG. 4

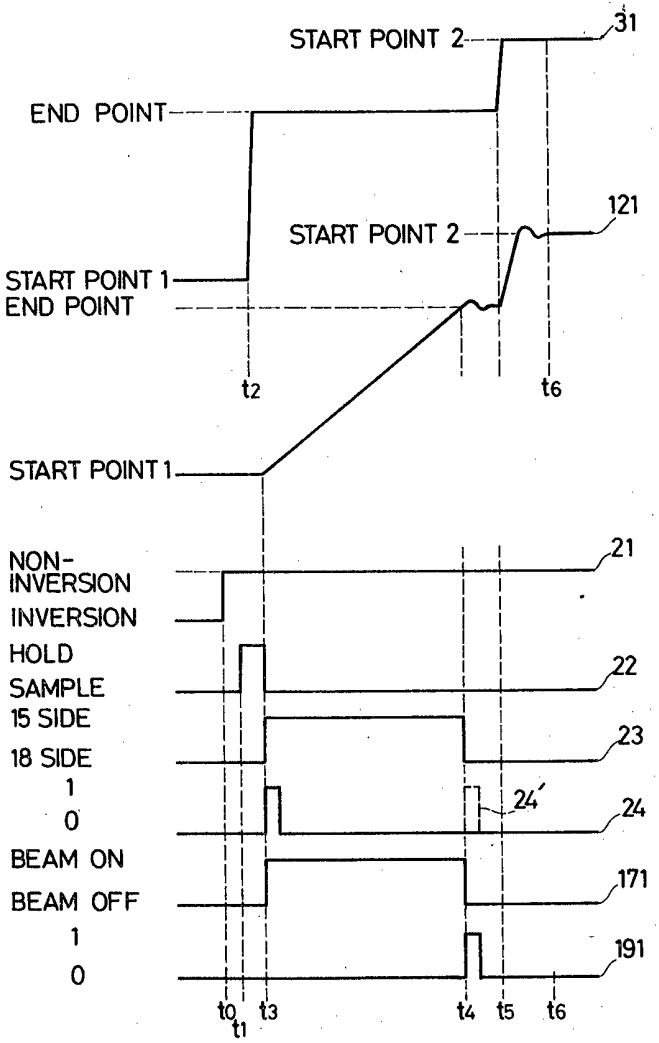

START POINT 2
31
END POINT
121
START POINT 2
START POINT 1
END POINT
t2
t6
START POINT 1
NON-INVERSION
21
INVERSION
HOLD
22
SAMPLE
15 SIDE
23
18 SIDE
1
24'
0
24
BEAM ON
171
BEAM OFF
1
191
0
t0
t1
t3
t4
t5
t6

FIG. 5

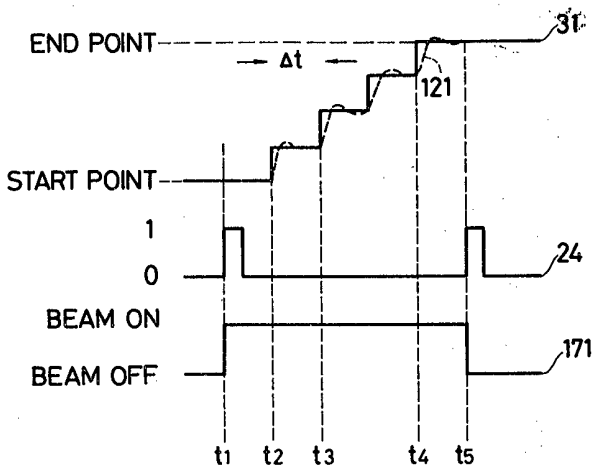

END POINT
Δt
31
121
START POINT
1
0
24
BEAM ON
BEAM OFF
171
t1
t2
t3
t4
t5

FIG. 7

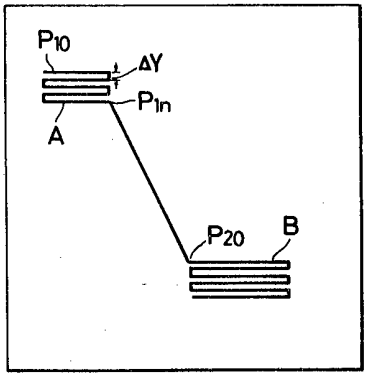
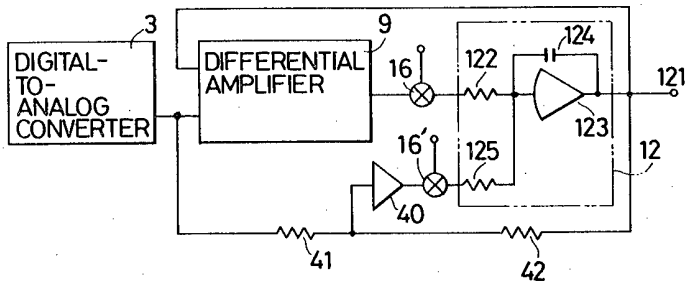
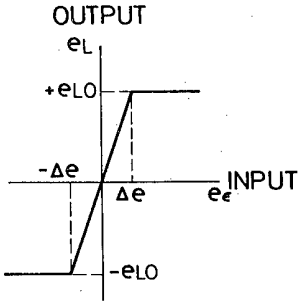

P10
ΔY
P1n
A
P20
B

FIG. 6

(a)


3
DIGITAL-TO-ANALOG CONVERTER
9
DIFFERENTIAL AMPLIFIER
16
16'
122
124
121
123
125
12
40
41
42

(b)


OUTPUT
eL
+eLO
-Δe
Δe
eε
INPUT
-eLO