US008502070B2

(12) **United States Patent**
Horan et al.

(10) **Patent No.: US 8,502,070 B2**
(45) **Date of Patent: Aug. 6, 2013**

(54) **REDUCED WIRE COUNT HIGH SPEED DATA CABLE**

(76) Inventors: **John Martin Horan**, Blackrock (IE); **Gerald Donal Murphy**, Ovens (IE); **David William Mc Gowan**, Rostellan (IE); **John Anthony Keane**, Douglas (IE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 411 days.

(21) Appl. No.: **12/805,103**

(22) Filed: **Jul. 13, 2010**

(65) **Prior Publication Data**

US 2012/0012388 A1 Jan. 19, 2012

(51) **Int. Cl.**
H01B 7/00 (2006.01)

(52) **U.S. Cl.**
USPC **174/36**

(58) **Field of Classification Search**
USPC ..... 174/28, 29, 36, 102 R, 106 R, 110 R, 174/113 R, 74 R, 78
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,940,477	B2 *	9/2005	Moon et al.	345/87
7,118,411	B2 *	10/2006	Huang et al.	439/502
7,423,218	B2 *	9/2008	Konda	174/74 R
7,762,727	B2 *	7/2010	Aronson	385/89
2003/0064625	A1 *	4/2003	Ozai	439/579
2004/0158662	A1 *	8/2004	Konda et al.	710/72
2006/0239310	A1 *	10/2006	Salz	372/29.021
2007/0164802	A1 *	7/2007	Rea et al.	327/266
2008/0106306	A1 *	5/2008	Keady et al.	327/100
2008/0106313	A1	5/2008	Keaoy	
2009/0083825	A1 *	3/2009	Miller et al.	725/151
2009/0260869	A1 *	10/2009	Wang	174/350
2010/0051318	A1	3/2010	Wang	
2010/0236814	A1 *	9/2010	Wang	174/115

FOREIGN PATENT DOCUMENTS

CN	201 170976 Y	12/2008
EP	1434318	6/2004
JP	2004 119060 A	4/2004

OTHER PUBLICATIONS

Deirdre Mathelin, "HDMI version 1.4 provides opportunities for active cables", Electronic Engineering Times Europe, vol. 12, No. 1, pp. 40-41,XP00 Sep. 2009.
Sanjiv Kumar, SuperSpeed USB 3.0 Specification Revolutionizes An Established Standard Nov. 2008.
Universal Serial Bus 3.0 Specification Revision 1.0 Nov. 12, 2008 Hewlett-Packard Company, Intel Corporation and others.
High-Definition Multimedia Interface (HDMI) Specification version 1.4a, dated Mar. 4, 2010.
Video Electronics Standards Association (VESA) DisplayPort Specification v1.2, dated Jan. 5, 2010.

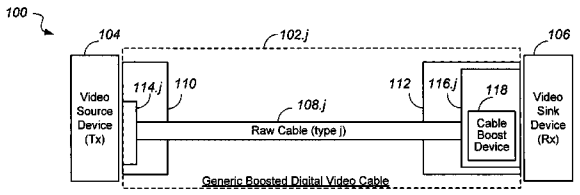
* cited by examiner

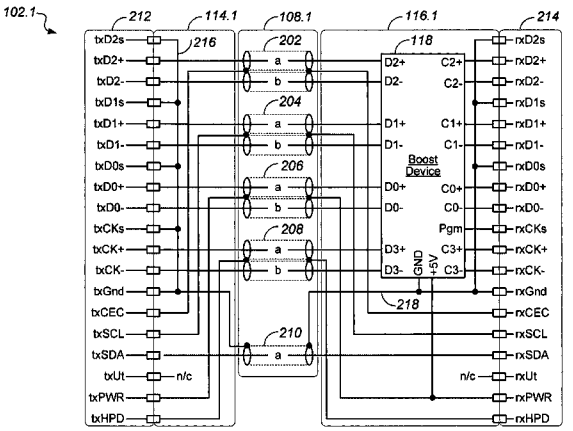
Primary Examiner — William H Mayo, III
(74) *Attorney, Agent, or Firm* — Trellis IP Law Group, PC

(57) **ABSTRACT**

A high speed video cable carries signals according to the High-Definition Multimedia Interface (HDMI) or DisplayPort standards, and includes a raw cable and a boost device. The raw cable is exclusively constructed with either Shielded Twisted Pairs (STP) or coaxial lines which carry all signals on either shielded wires or their shields. The high speed signals are carried on the shielded wires to the boost device where any common mode noise induced by the signals on the shields is removed. Some auxiliary signals including power are carried on ungrounded shields.

24 Claims, 11 Drawing Sheets





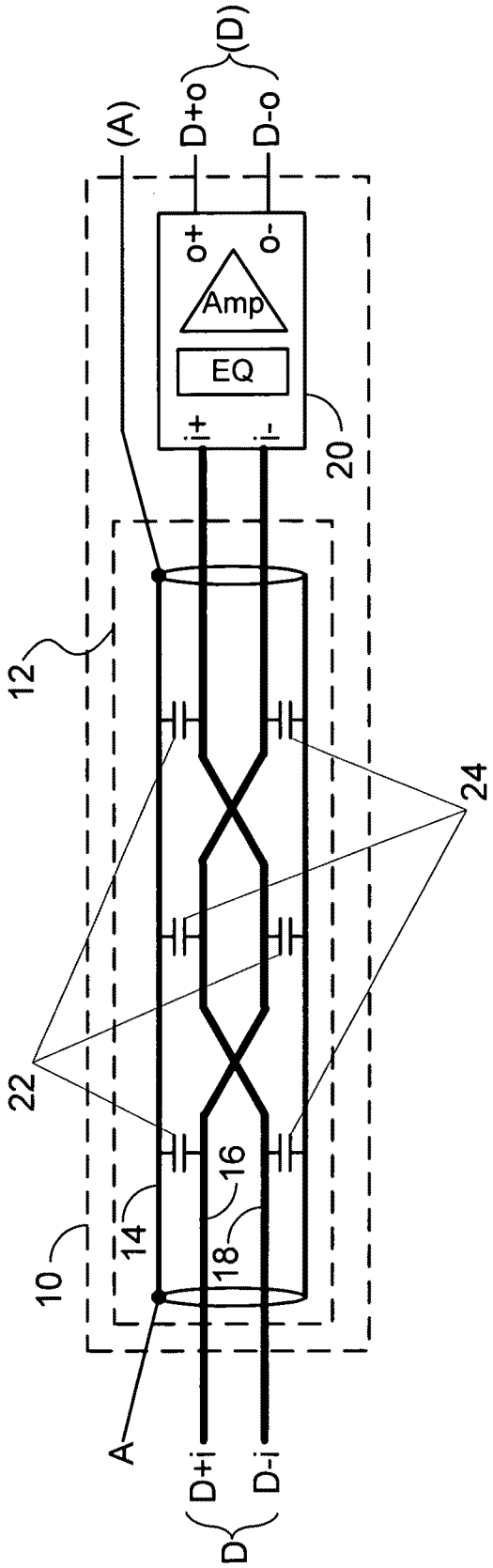


FIG. 1A

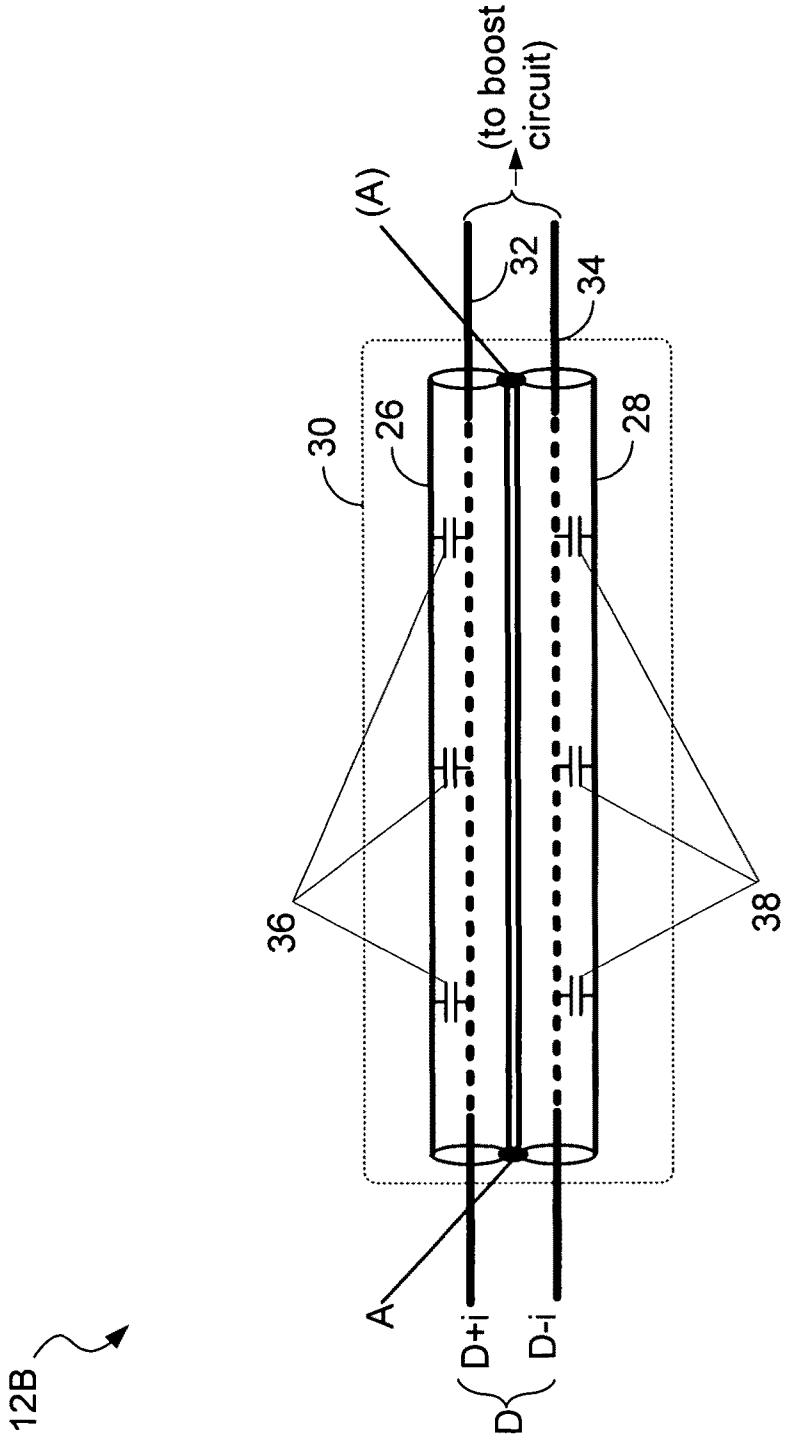


FIG. 1B

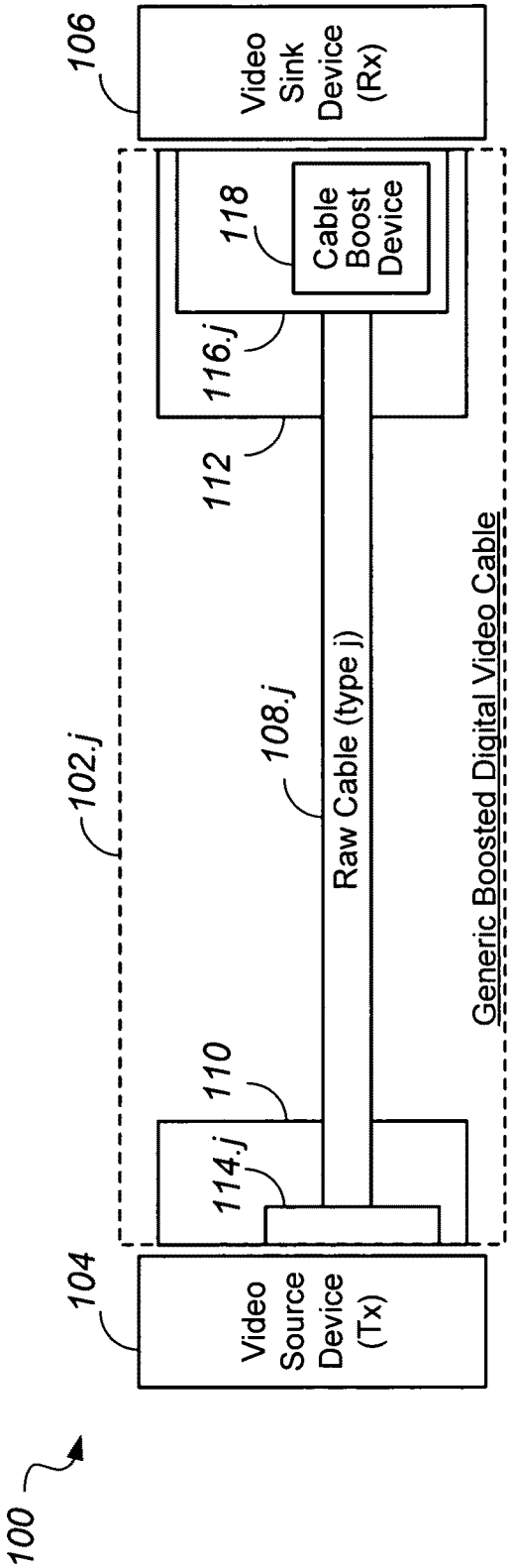

100
104
Video Source Device (Tx)
114.j
110
102.j
108.j
Raw Cable (type j)
Generic Boosted Digital Video Cable
112
116.j
118
Cable Boost Device
106
Video Sink Device (Rx)

FIG. 2

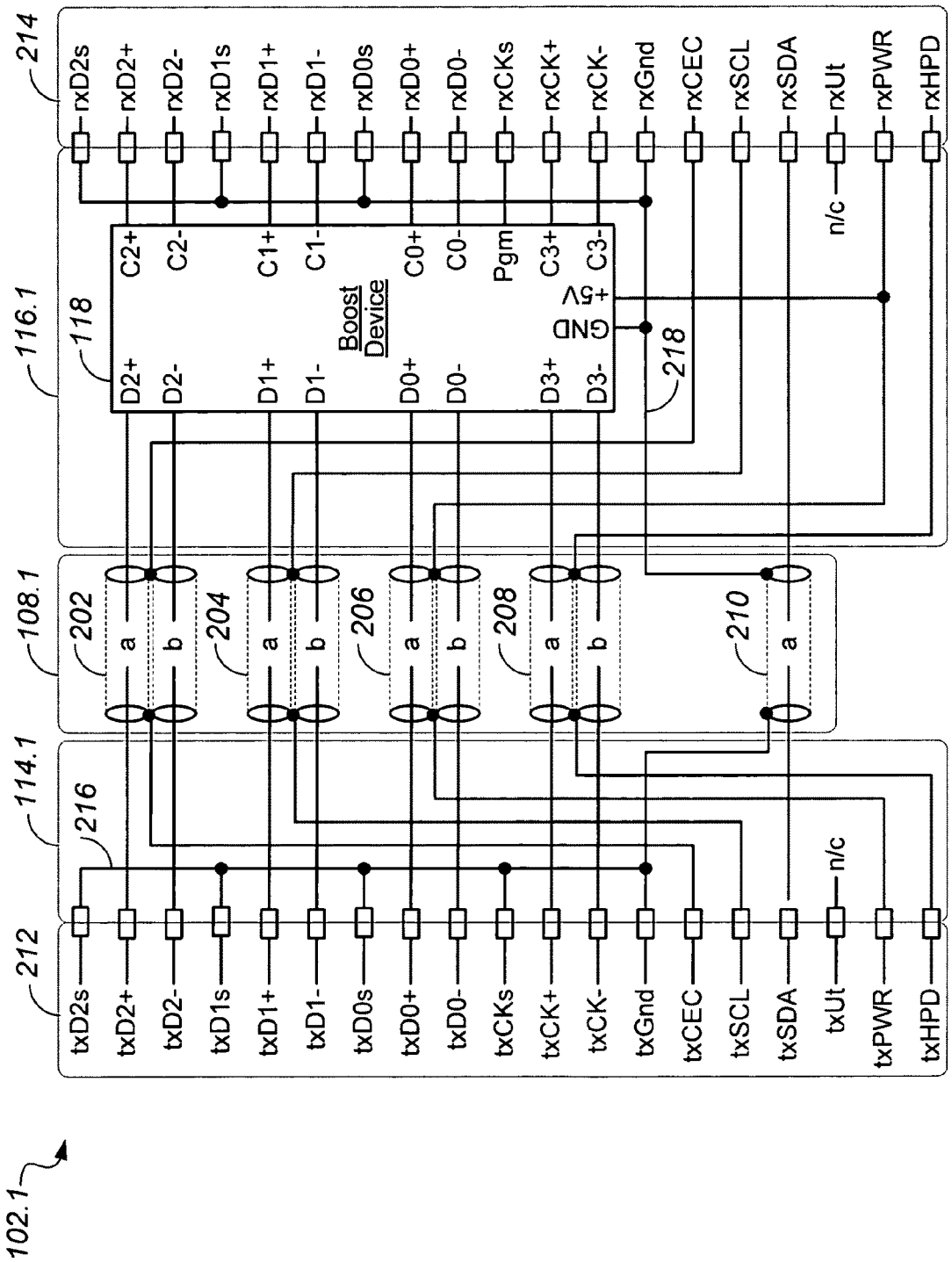

214
rxD2s
rxD2+
rxD2-
rxD1s
rxD1+
rxD1-
rxD0s
rxD0+
rxD0-
rxCKs
rxCK+
rxCK-
rxGnd
rxCEC
rxSCL
rxSDA
rxUt
rxPWR
rxHPD
n/c
116.1
118
C2+
C2-
C1+
C1-
C0+
C0-
Pgm
C3+
C3-
+5V
GND
Boost Device
D2+
D2-
D1+
D1-
D0+
D0-
D3+
D3-
218
108.1
202
204
206
208
210
a
b
114.1
216
212
txD2s
txD2+
txD2-
txD1s
txD1+
txD1-
txD0s
txD0+
txD0-
txCKs
txCK+
txCK-
txGnd
txCEC
txSCL
txSDA
txUt
txPWR
txHPD
n/c
102.1

FIG. 3

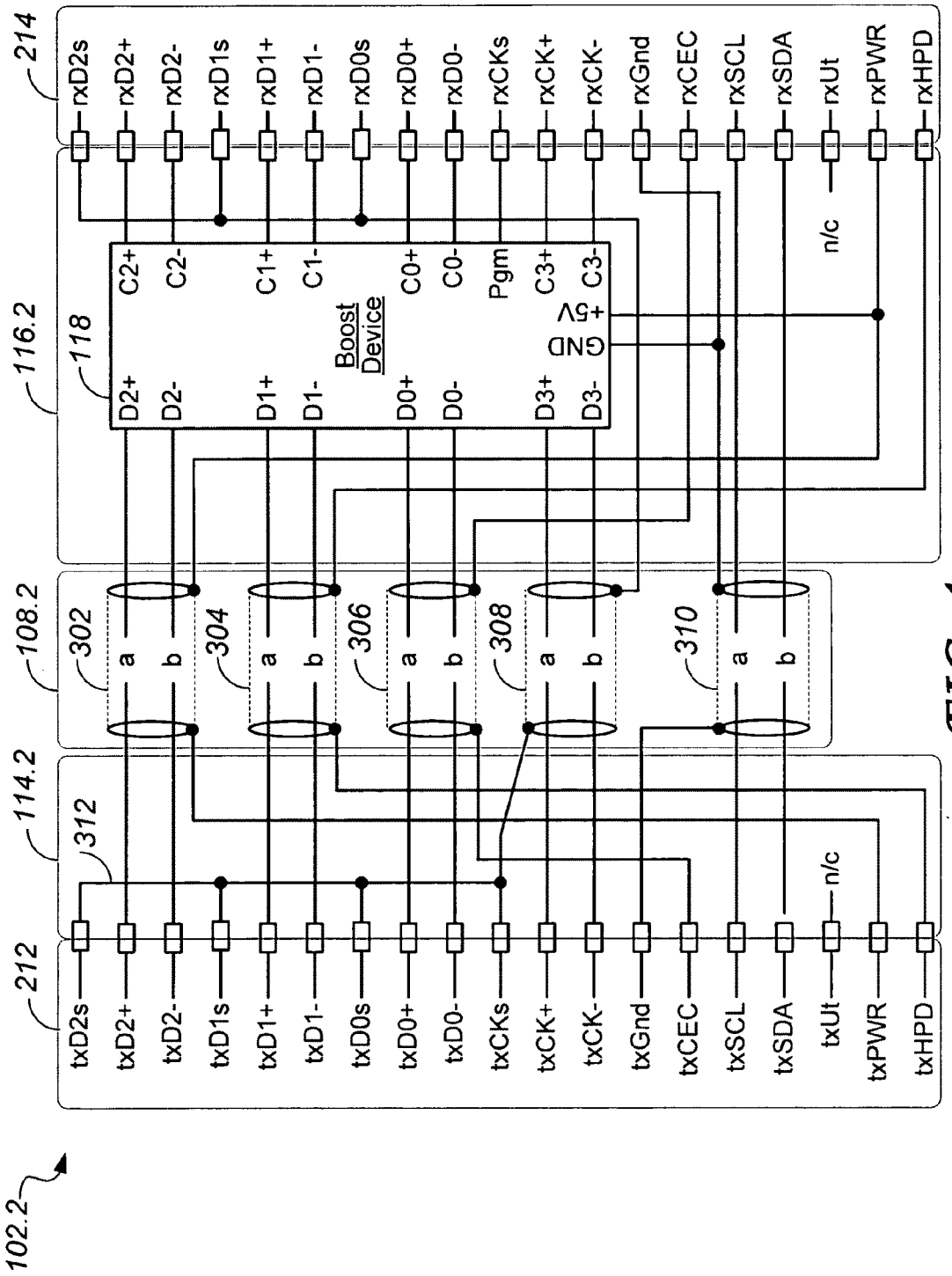

214
rxD2s
rxD2+
rxD2-
rxD1s
rxD1+
rxD1-
rxD0s
rxD0+
rxD0-
rxCKs
rxCK+
rxCK-
rxGnd
rxCEC
rxSCL
rxSDA
rxUt
rxPWR
rxHPD
116.2
118
D2+
D2-
D1+
D1-
D0+
D0-
D3+
D3-
C2+
C2-
C1+
C1-
C0+
C0-
Pgm
C3+
C3-
+5V
GND
Boost Device
n/c
108.2
302
304
306
308
310
a
b
114.2
312
212
txD2s
txD2+
txD2-
txD1s
txD1+
txD1-
txD0s
txD0+
txD0-
txCKs
txCK+
txCK-
txGnd
txCEC
txSCL
txSDA
txUt
txPWR
txHPD
n/c
102.2

FIG. 4

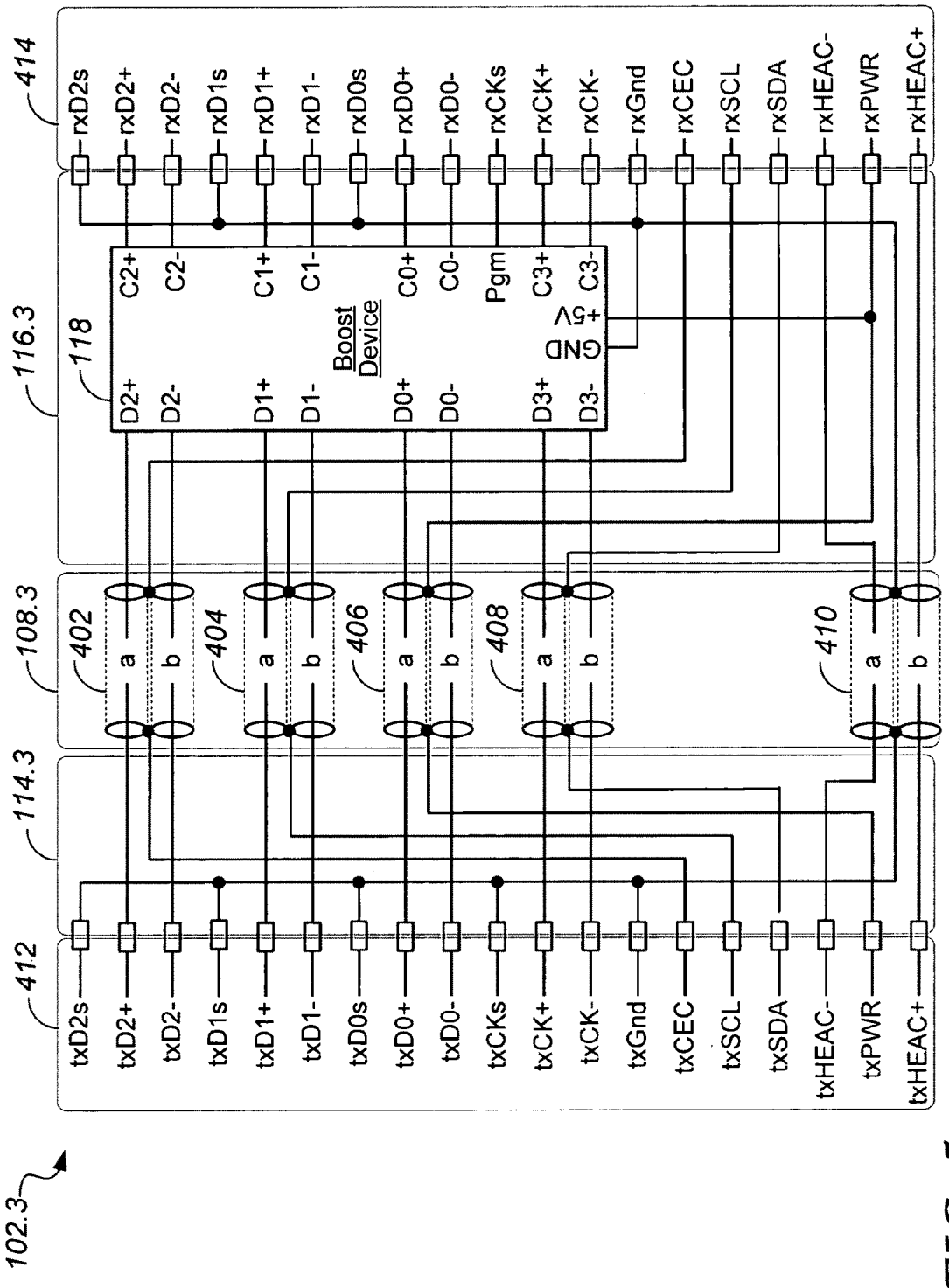

102.3
412
114.3
108.3
116.3
414
118
Boost Device
402
404
406
408
410
txD2s
txD2+
txD2-
txD1s
txD1+
txD1-
txD0s
txD0+
txD0-
txCKs
txCK+
txCK-
txGnd
txCEC
txSCL
txSDA
txHEAC-
txPWR
txHEAC+
D2+
D2-
D1+
D1-
D0+
D0-
D3+
D3-
C2+
C2-
C1+
C1-
C0+
C0-
Pgm
C3+
C3-
+5V
GND
a
b
rxD2s
rxD2+
rxD2-
rxD1s
rxD1+
rxD1-
rxD0s
rxD0+
rxD0-
rxCKs
rxCK+
rxCK-
rxGnd
rxCEC
rxSCL
rxSDA
rxHEAC-
rxPWR
rxHEAC+

FIG. 5

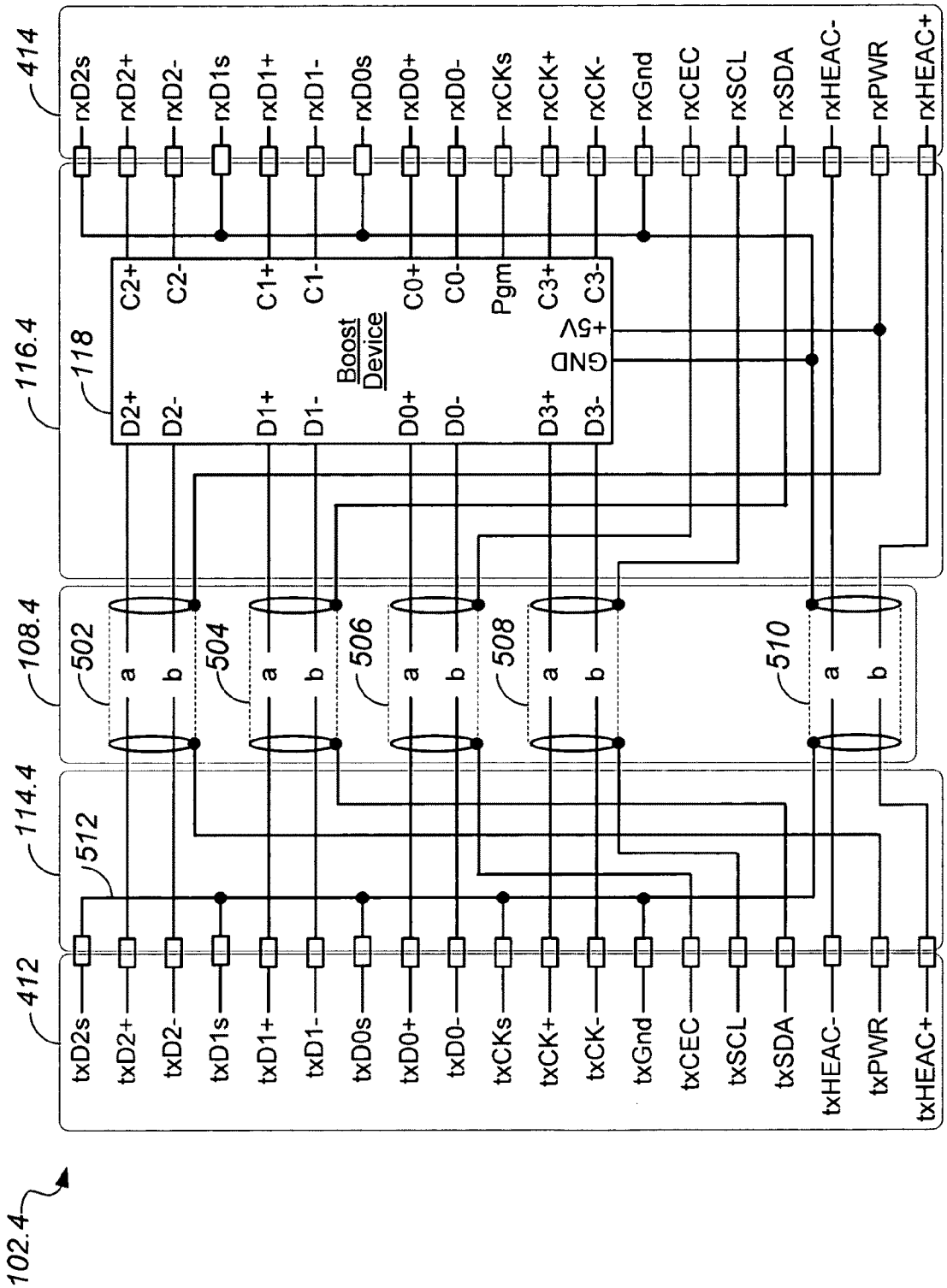

414
rxD2s
rxD2+
rxD2-
rxD1s
rxD1+
rxD1-
rxD0s
rxD0+
rxD0-
rxCKs
rxCK+
rxCK-
rxGnd
rxCEC
rxSCL
rxSDA
rxHEAC-
rxPWR
rxHEAC+
116.4
118
C2+
C2-
C1+
C1-
C0+
C0-
Pgm
C3+
C3-
+5V
GND
Boost Device
D2+
D2-
D1+
D1-
D0+
D0-
D3+
D3-
108.4
502
504
506
508
510
a
b
114.4
512
412
txD2s
txD2+
txD2-
txD1s
txD1+
txD1-
txD0s
txD0+
txD0-
txCKs
txCK+
txCK-
txGnd
txCEC
txSCL
txSDA
txHEAC-
txPWR
txHEAC+
102.4

FIG. 6

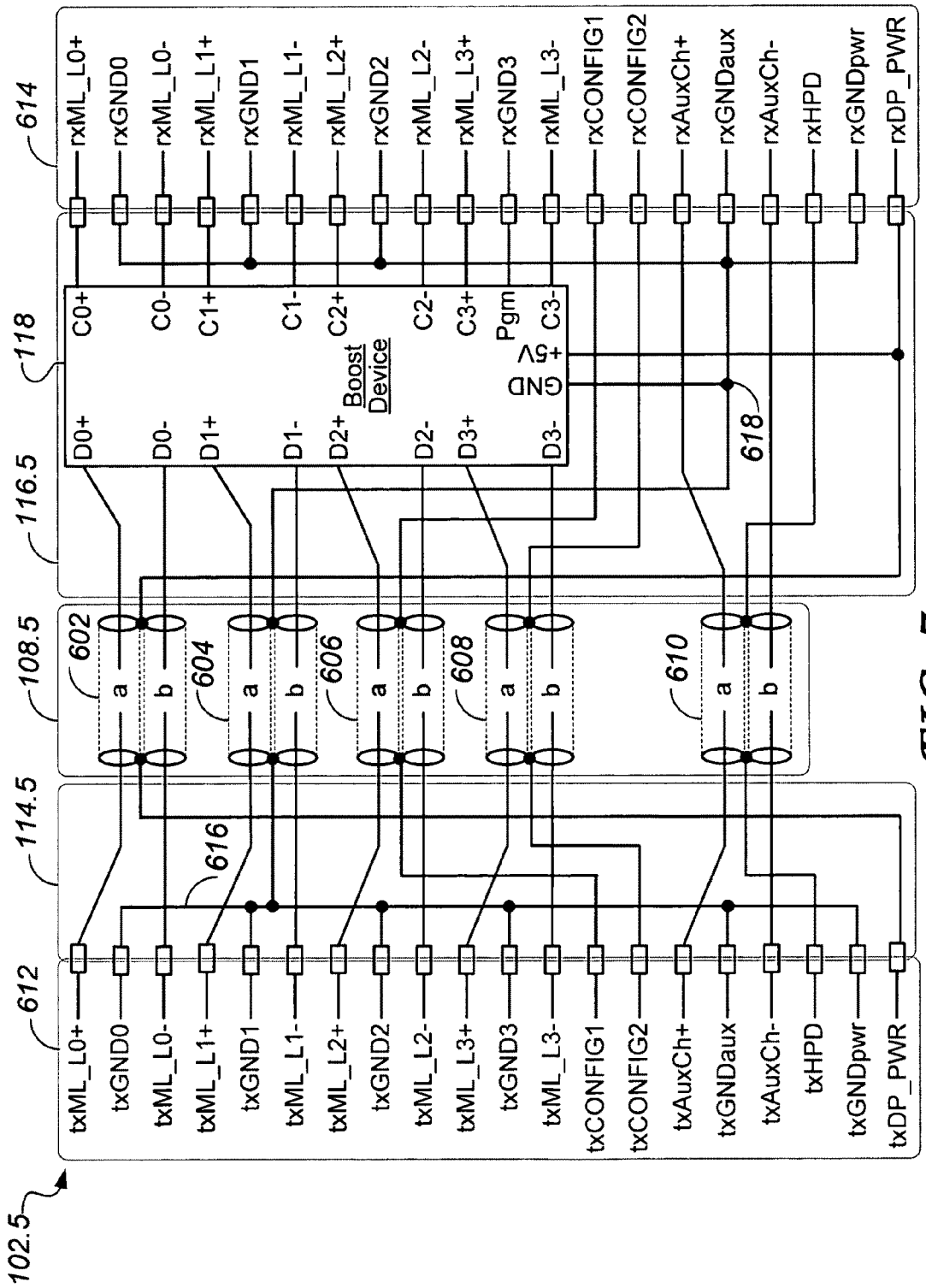

614
rxML_L0+
rxGND0
rxML_L0-
rxML_L1+
rxGND1
rxML_L1-
rxML_L2+
rxGND2
rxML_L2-
rxML_L3+
rxGND3
rxML_L3-
rxCONFIG1
rxCONFIG2
rxAuxCh+
rxGNDaux
rxAuxCh-
rxHPD
rxGNDpwr
rxDP_PWR
118
C0+
C0-
C1+
C1-
C2+
C2-
C3+
Pgm
C3-
+5V
GND
Boost Device
D0+
D0-
D1+
D1-
D2+
D2-
D3+
D3-
618
116.5
108.5
602
604
606
608
610
a
b
114.5
616
612
txML_L0+
txGND0
txML_L0-
txML_L1+
txGND1
txML_L1-
txML_L2+
txGND2
txML_L2-
txML_L3+
txGND3
txML_L3-
txCONFIG1
txCONFIG2
txAuxCh+
txGNDaux
txAuxCh-
txHPD
txGNDpwr
txDP_PWR
102.5

FIG. 7

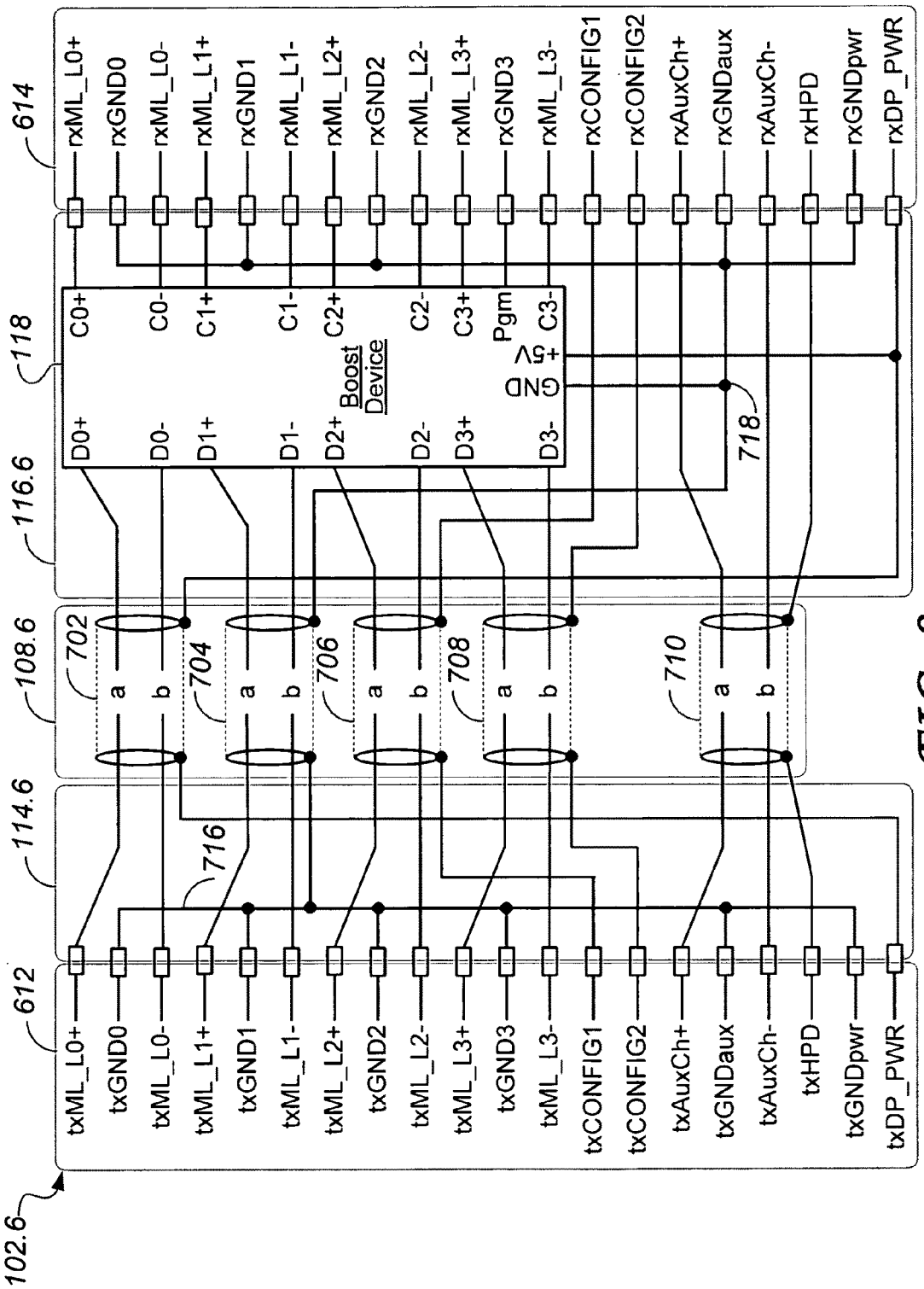

614
rxML_L0+
rxGND0
rxML_L0-
rxML_L1+
rxGND1
rxML_L1-
rxML_L2+
rxGND2
rxML_L2-
rxML_L3+
rxGND3
rxML_L3-
rxCONFIG1
rxCONFIG2
rxAuxCh+
rxGNDaux
rxAuxCh-
rxHPD
rxGNDpwr
rxDP_PWR
118
C0+
C0-
C1+
C1-
C2+
C2-
C3+
Pgm
C3-
+5V
GND
Boost Device
D0+
D0-
D1+
D1-
D2+
D2-
D3+
D3-
718
116.6
108.6
702
704
706
708
710
a
b
114.6
716
612
txML_L0+
txGND0
txML_L0-
txML_L1+
txGND1
txML_L1-
txML_L2+
txGND2
txML_L2-
txML_L3+
txGND3
txML_L3-
txCONFIG1
txCONFIG2
txAuxCh+
txGNDaux
txAuxCh-
txHPD
txGNDpwr
txDP_PWR
102.6

FIG. 8

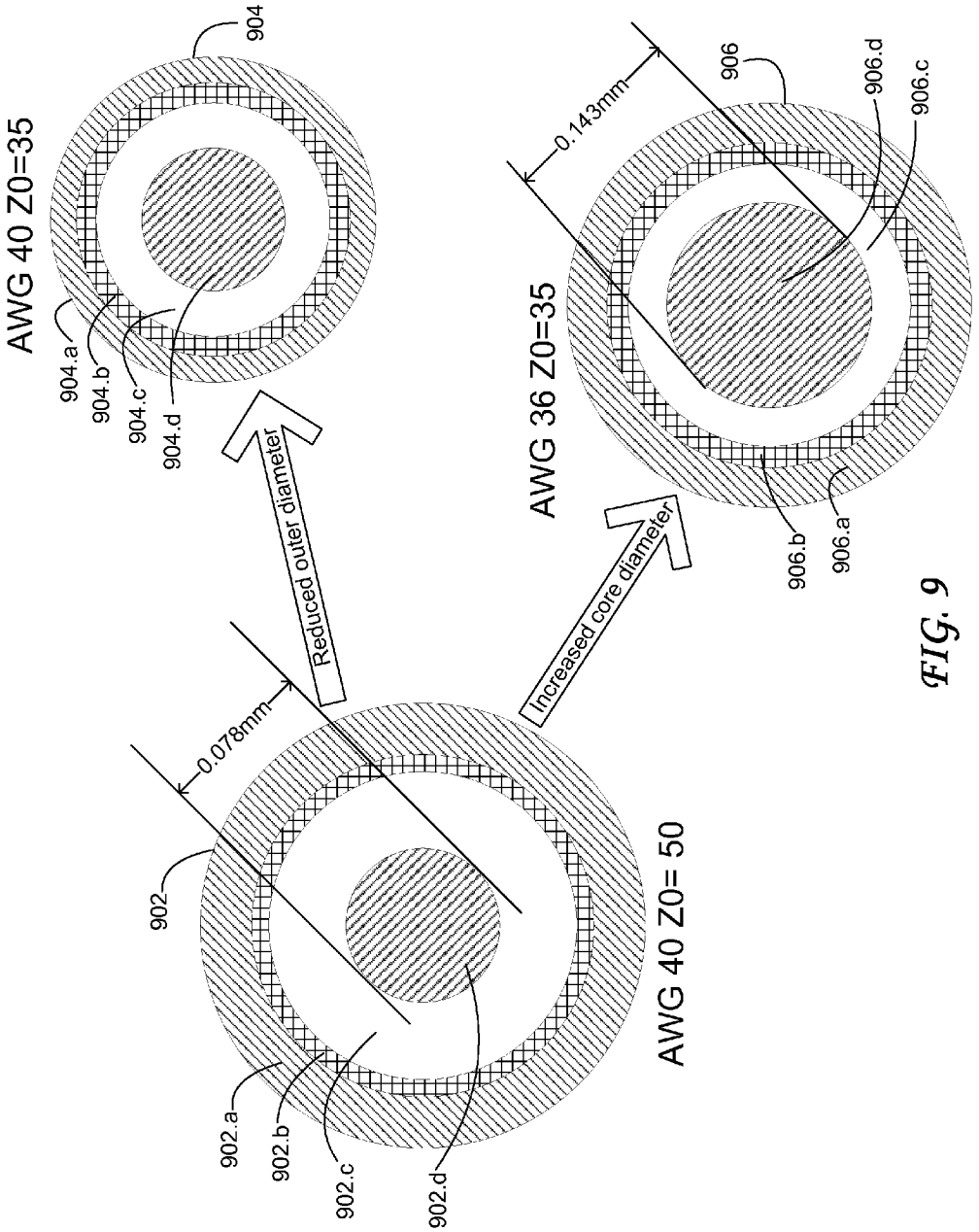

AWG 40 Z0=35
904
904.a
904.b
904.c
904.d
Reduced outer diameter
0.078mm
902
902.a
902.b
902.c
902.d
AWG 40 Z0= 50
Increased core diameter
AWG 36 Z0=35
0.143mm
906
906.a
906.b
906.c
906.d

FIG. 9

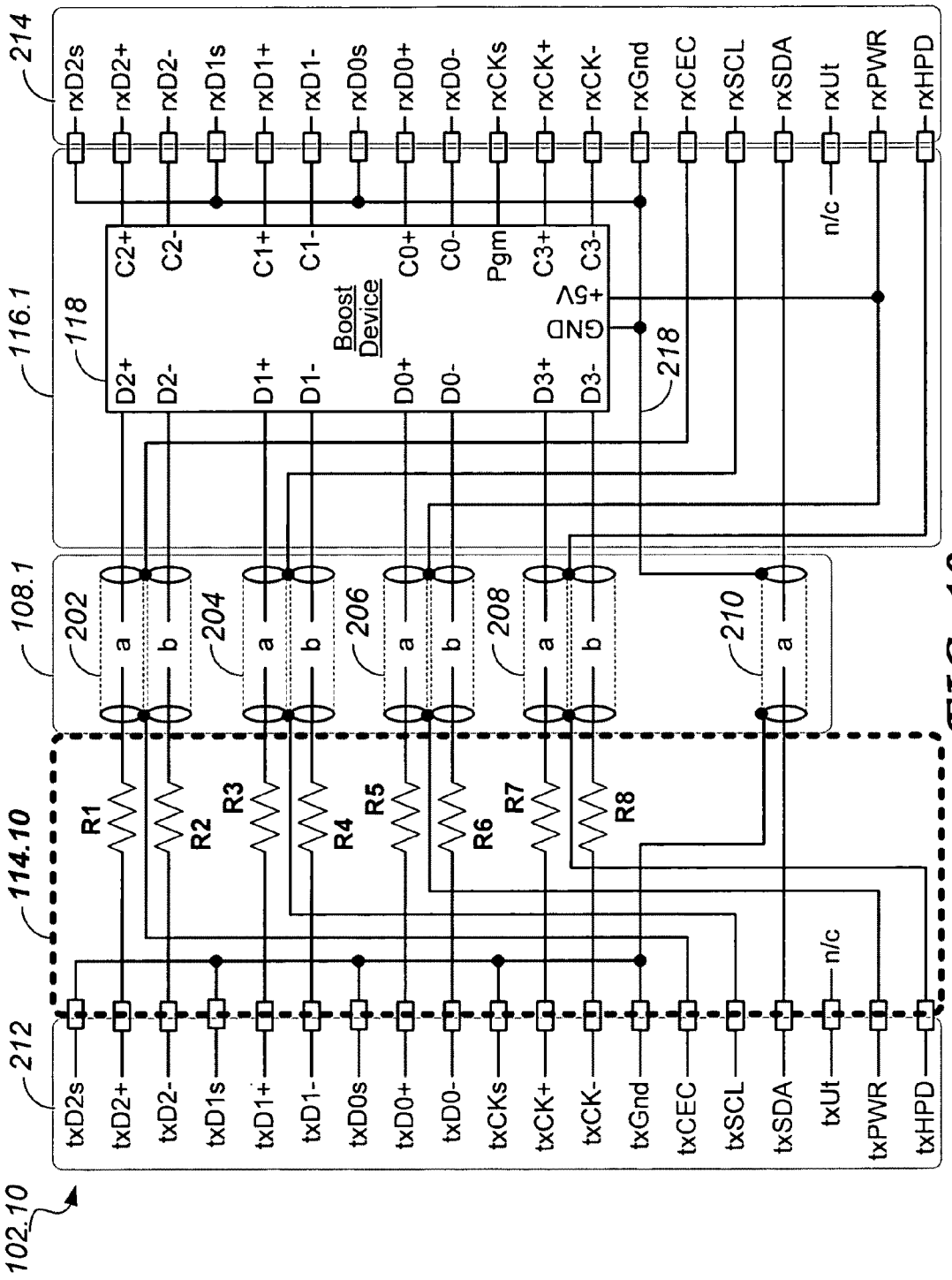

102.10
212
114.10
108.1
116.1
214
118
202
204
206
208
210
218
txD2s
txD2+
txD2-
txD1s
txD1+
txD1-
txD0s
txD0+
txD0-
txCKs
txCK+
txCK-
txGnd
txCEC
txSCL
txSDA
txUt
txPWR
txHPD
R1
R2
R3
R4
R5
R6
R7
R8
a
b
n/c
D2+
D2-
D1+
D1-
D0+
D0-
D3+
D3-
C2+
C2-
C1+
C1-
C0+
C0-
Pgm
C3+
C3-
+5V
GND
Boost Device
rxD2s
rxD2+
rxD2-
rxD1s
rxD1+
rxD1-
rxD0s
rxD0+
rxD0-
rxCKs
rxCK+
rxCK-
rxGnd
rxCEC
rxSCL
rxSDA
rxUt
rxPWR
rxHPD

FIG. 10

REDUCED WIRE COUNT HIGH SPEED DATA CABLE

FIELD OF THE INVENTION

The present invention relates to the construction of boosted high speed data cables, which carry high speed signal lines.

BACKGROUND OF THE INVENTION

The distribution of television signals has increasingly become based on digital methods and digitally encoded forms of video and audio signals. At the same time, higher resolution (high definition TV) has become available in the market place, commensurate with larger and higher definition displays. To meet the requirement of interconnecting such high definition displays with digital signal sources such as Digital Versatile Disc (DVD) players and receivers/decoders for digital satellite and digital cable distribution of video material, a digital interface standard has evolved, known as the High-Definition Multimedia Interface (HDMI). A detailed specification for HDMI can be obtained from the "hdmi.org" website. The HDMI specification currently available and used in this application is HDMI specification version 1.4a dated Mar. 4, 2010, which is incorporated herein by reference.

HDMI cables of various construction may be used for transmitting high speed digital signals from digital signal sources, including, but not limited to, the examples listed above, to digital displays or other equipment designed to receive signals according to the HDMI specification.

A HDMI cable carries not only four high speed differential signals which are shielded, but also a number of lower speed signals, power and ground, the whole being further shielded by an outer braid. The resulting complex cable configuration with numerous wires, some of which are individually shielded, is expensive to manufacture and terminate.

Another standard for connecting video source to a video sink, is published as the DisplayPort standard by the Video Electronics Standards Association (VESA). The latest DisplayPort specification used in this application is DisplayPort v1.2, dated Jan. 5, 2010, a copy of which may be obtained from www.vesa.org. The DisplayPort standard specifies a high speed data cable that is intended primarily to be used between a computer and its display monitor or a home-theater system. A cable meeting the DisplayPort standard is very similar to an HDMI cable, the main difference being in the respective physical connectors.

Therefore there is a need in the industry for developing an improved and easier to manufacture high speed cable, which would avoid or mitigate the shortcomings of the prior art and provides significant economies at the same time.

SUMMARY OF THE INVENTION

Therefore there is an object of the invention to provide an improved high speed cable with reduced wire count, which would have superior properties over existing prior art cables.

According to one aspect of the invention, there is provided a digital video cable for carrying one or more high speed differential digital data signals and one or more auxiliary signals between a video source device and a video sink device according to a cable specification, the cable comprising: a boost device; a raw cable having one or more dual shielded cable elements, each dual shielded cable element comprising two shielded conductors and a shield; the shielded conductors of at least one dual shielded cable element extending between the video source device and the boost device; the shields of said one or more dual shielded cable elements extending between the video source device and the video sink device; wherein the shield of the at least one dual shielded cable element is adapted to carry an auxiliary signal; and wherein the shielded conductors of said at least one dual shielded cable element are adapted to carry a high speed differential digital data signal.

In the cable described above, said one or more dual shielded cable elements are dual coaxial elements, each comprising two coaxial lines whose shields are joined, and each coaxial line enclosing one shielded conductor. Alternatively, only some of said one or more dual shielded cable elements may bedual coaxial elements, each comprising two coaxial lines whose shields are joined, and each coaxial line enclosing one shielded conductor.

In a modification to the cable design, the raw cable may further include a coaxial line having a shield enclosing one shielded conductor, the coaxial line extending between the video source device and the video sink device; the shield is adapted to carry another auxiliary signal, and the shielded conductor is adapted to carry yet another auxiliary signal.

Alternatively, in the cable described above, said one or more dual shielded cable elements are Shielded Twisted Pairs (STP), each comprising a shield enclosing the two shielded conductors. Yet alternatively, only some of said one or more dual shielded cable elements may be Shielded Twisted Pairs (STP), each comprising a shield enclosing the two shielded conductors.

Yet alternatively, the raw cable comprises said one or more dual shielded cable elements only, i.e. excluding any other wires between the video source device and the video sink device, each dual shielded element comprising one of the following:

(i) a dual coaxial element, comprising two coaxial lines whose shields are joined, each coaxial line enclosing one shielded conductor; or

(ii) a Shielded Twisted Pair (STP), comprising a shield enclosing the two shielded conductors.

In one embodiment of the invention, the cable specification is the High-Definition Multimedia Interface (HDMI) standard. In another embodiment of the invention, the cable specification is the DisplayPort standard.

The cable further comprises a first circuit carrier for connecting the video source device to the raw cable, wherein the first circuit carrier further comprises terminals for connecting the high speed differential digital data signal from the video source device to the shielded conductors of said at least one dual shielded cable element. The first circuit carrier further comprises terminals for connecting at least one auxiliary signal from the video source device to the shield of said at least one dual shielded cable element.

The cable may also comprise a second circuit carrier for connecting the raw cable to the video sink device, wherein the second circuit carrier comprises the boost device.

The cable of the embodiment of the invention according to the HDMI specification is suitable for transmitting high speed differential digital data signals, which are Transition Minimized Differential Signaling (TMDS) signals; and auxiliary signals, which are Consumer Electronics Control (CEC), Serial Clock (SCL), Hot Plug Detect (HPD), and +5V Power signals.

The HDMI cable of the embodiments of the invention comprises: the shielded conductors of four dual shielded cable elements are extended between the video source device and the boost device; the shielded conductors of the four dual shielded cable elements are adapted to carry respective four high speed differential digital data signals, which are Transi-

tion Minimized Differential Signaling (TMDS) signals; the shielded conductors of one other dual shielded cable element, extending between the video source device and the video sink device, are adapted to carry an auxiliary signal, which is a HDMI Ethernet and Audio Return Channel (HEAC) differential signal; and the shields of the four dual shielded cable elements and said one other dual shielded cable element are adapted to carry auxiliary signals, which are Consumer Electronics Control (CEC), Serial Clock (SCL), Serial Data (SDA), Digital Data Channel (DDC)/CEC Ground, and +5V Power signals.

In the HDMI cable, the boost device may also comprises an equalizer and an amplifier for equalizing and boosting the TMDS signals respectively.

The cable of the embodiment of the invention according to the DisplayPort specification has been designed as follows: the shielded conductors of four dual shielded cable elements are extended between the video source device and the boost device; the shielded conductors of the four dual shielded cable elements are adapted to carry respective four high speed differential digital data signals, which are Main Line lanes; the shielded conductors of one other dual shielded cable element, extending between the video source device and the video sink device, are adapted to carry an auxiliary signal, which is an Auxiliary Channel (AUX CH) differential signal; and the shields of the four dual shielded cable elements and said one other dual shielded cable element are adapted to carry auxiliary signals, which are CONFIG**1**, CONFIG**2**, Ground, Hot Plug Detect (HPD), and DisplayPort power (DP_PWR) signals.

The Display Port cable of the embodiments of the present invention, the boost device may also comprise an equalizer and an amplifier for equalizing and boosting the Main Line lanes respectively.

In the cable described above, an impedance of said at least one dual shielded cable element may be lower than a nominal impedance of the cable specified in the cable specification. In this case, the cable further comprises: a first circuit carrier connecting the video source device to the raw cable, the first circuit carrier including two padding resistors, each padding resistor being in series with a respective shielded conductor of said at least one dual shielded cable element; and a second circuit carrier connecting the raw cable to the video sink device, the boost device being mounted on the second circuit carrier for terminating said at least one dual shielded cable element, and for boosting the high speed differential digital data signal.

According to another aspect of the invention, there is provided a method for transmitting one or more high speed differential digital data signals and a one or more auxiliary signals from a video source device to a video sink device over a digital video cable having a raw cable and a boost device, the method comprising: carrying at least one high speed differential digital data signal from the video sink device to a boost device in a pair of shielded conductors of the raw cable; boosting the at least one high speed differential digital data signal in the boost device to produce a boosted signal, and transmitting the boosted signal to the video sink device; and carrying at least one auxiliary signal on a shield of the pair of the shielded conductors.

The method further includes equalizing the at least one high speed differential digital data signal in the boost device.

In the method described above, the transmitting comprises transmitting over the digital video cable, which is one of the following: a High-Definition Multimedia Interface (HDMI) cable; a DisplayPort cable. In the embodiments of the invention, the cable specification may be the High-Definition Multimedia Interface (HDMI) standard, or alternatively, it may be the DisplayPort standard.

Thus, an improved reduced wire count high speed data cable and a method of transmitting digital signals over the cable have been provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

FIG. **1**A shows a simplified boosted cable **10** to illustrate the principle of transmitting a single-ended signal and a differential signal over a shielded cable comprising a dual shielded cable element **12**, which is a Shielded Twisted Pair (STP), and a boost circuit **20**;

FIG. **1**B shows a dual coaxial element **12**B that may be used instead of the dual shielded cable element **12** of FIG. **1**A;

FIG. **2** shows a configuration **100** of a generic Boosted Digital Video Cable **102**.*j* which may be of any one "j" of a number of types according to embodiments of the invention, interconnecting a Video Source Device (Tx) **104** and a Video Sink Device (Rx) **106**;

FIG. **3** shows a Basic Coax HDMI Cable **102.1** based on coax technology according to a first embodiment of the invention;

FIG. **4** shows a Basic STP HDMI Cable **102.2** based on Shielded Twisted Pair (STP) technology according to a second embodiment of the invention;

FIG. **5** shows a HEAC-Capable Coax HDMI Cable **102.3** based on coax technology according to a third embodiment of the invention;

FIG. **6** shows a HEAC-Capable STP HDMI Cable **102.4** based on Shielded Twisted Pair (STP) technology according to a fourth embodiment of the invention;

FIG. **7** shows a Coax DisplayPort Cable **102.5** based on coax technology according to a fifth embodiment of the invention;

FIG. **8** shows a STP DisplayPort Cable **102.6** based on Shielded Twisted Pair (STP) technology according to a sixth embodiment of the invention;

FIG. **9** shows a three coax line cross sections, to illustrate a comparison between exemplary design choices, including a standard coax **902**; a reduced-outer-diameter coax **904**; and an increased-core-diameter coax **906**; and

FIG. **10** shows a Low-Impedance (Low Z**0**) Coax HDMI Cable **102.10** which is identical to the Basic Coax HDMI Cable **102.1** of FIG. **1** except for a Low-Impedance Input Paddle Board **114.10** which replaces the first Input Paddle Board **114.1**.

DETAILED DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

Embodiments of the present invention describe a boosted high speed cable comprising shielded high speed signal lines and carrying other signals of lower speed as well as power and ground, in which the shields of the shielded high speed signal lines are used in carrying the lower speed signals and power and ground.

The inherent characteristics and manufacturing imperfections of high-speed differential signaling cables such as may be used to carry HDMI signals have an adverse effect on the high-speed signals carried by the cable. To mitigate these effects, various boosted high speed data cables have been proposed by the industry. For example, in the previously filed

US application of the same assignee, Ser. No. 11/826,713 filed on Jul. 18, 2007, a boost device is embedded in the cable, the contents of the patent application being incorporated herein by reference.

The inventors have discovered that the boost device may not only be used to equalize and boost the signal, as described in the U.S. application Ser. No. 11/826,713 cited above, but may also be used to advantage in other ways, specifically to allow the individual shields of the differential high speed signals to be used for carrying other signals.

In a cable of the prior art, the shields are all tied to ground in an effort to reduce electro-magnetic interference (EMI). In a cable according to any of the embodiments of the invention, EMI shielding is still provided, but instead of tying the shields of the high-speed HDMI signals to ground, the lower speed signals as well as power and ground, are sent over the shields.

FIG. **1**A shows a simplified boosted cable **10** to illustrate the principle of transmitting a single-ended signal and a differential signal over a shielded cable. The simplified boosted cable **10** comprises a dual shielded cable element **12** which is a Shielded Twisted Pair (STP) including a single shield **14** enclosing first and second signal wires (two shielded conductors) **16** and **18** respectively, and a boost circuit **20** having inputs i+ and i− and outputs o+ and o−. The inputs i+ and i− of the boost circuit **20** are a differential input pair and the outputs o+ and o− of the boost circuit **20** are a differential output pair.

The simplified boosted cable **10** receives a single-ended signal "A" and a differential signal "D" comprising polarities D+i and D−i at the input of the simplified boosted cable **10**, and is designed to deliver these signals substantially undistorted at its output. The boost circuit **20** includes an equalizer circuit (EQ) and a differential amplifier (Amp) for equalizing and boosting the differential signal "D".

The signal wires **16** and **18** carry the differential signal "D", comprising polarities D+i and D−i respectively from the input of the simplified boosted cable **10** through the dual shielded cable element **12** to the inputs i+ and i− of the boost circuit **20**. The outputs o+ and o− of the boost circuit **20** deliver a processed differential signal comprising polarities D+o and D−o to the output of the simplified boosted cable **10**, which represent the differential signal "D".

The single shield **14** carries a single-ended signal "A" directly from the input of the simplified boosted cable **10** to its output.

The processing functions of the boost circuit **20** include: receiving the differential input signal; removing any common mode component of the differential input signal; equalizing the signal to compensate for signal impairments introduced by the dual shielded cable element **12**; and outputting a boosted version of the equalized differential signal "D".

To summarize, the differential signal is a high-speed data signal "D", which may benefit from equalization and boosting while the single-ended signal "A" may be a ground signal, a power supply signal, or any low speed signal which does not require equalization or boosting.

Along the length of the STP raw cable **12**, a small fraction of the single-ended signal "A" is unavoidably coupled as undesirable noise through distributed capacitances **22** and **24** into the signal wires **16** and **18** respectively, thus affecting the differential signal "D". Given that, by the construction of the dual shielded cable element **12**, the capacitances **22** and **24** are essentially equal, the polarities D+i and D−i respectively are equally affected, and the coupled noise manifests itself as common mode noise.

At the receiving end of the dual shielded cable element **12**, the boost circuit **20** receiving the differential signal "D", provides sufficient common-mode rejection such that the common mode noise is not converted into a differential signal. The outputs o+ and o− of the boost circuit **20**, that produces a boosted signal, is then a clean differential signal which is delivered at the output of the simplified boosted cable **10**.

Alternatively, as shown in FIG. **1**B, a dual coaxial element **12**B may be used instead of the dual shielded cable element **12**. The dual coaxial element **12**B is comprised of two coaxial lines **26** and **28** forming a coax pair **30** whose outer conductors (shields) are joined together, the joined shields providing the connection for the single-ended signal "A". The coaxial line **26** carries the polarity D+i of the differential signal "D" on its inner conductor **32**, while the coaxial line **28** carries the polarity D−i of the differential signal "D" on its inner conductor **34**. Coupling between the single-ended signal "A" and the inner conductors **32** and **34** which are also referred to as shielded conductors, through distributed capacitances **36** and **38** respectively is analogous to the case of the dual shielded cable element **12**, resulting in common mode noise only which is rejected by the boost circuit **20**.

In the following figures, various boosted HDMI cable configurations are shown which are embodiments of the invention that are based on the cable elements described in FIGS. **1**A and **1**B.

FIG. **2** shows a configuration **100** of a generic Boosted Digital Video Cable **102**.*j* which may be of any of a number of types to be described below, connecting a Video Source Device (Tx) **104** to a Video Sink Device (Rx) **106**. The Boosted Digital Video Cable **102**.*j* comprises a Raw Cable **108**.*j*, and Input and Output Connectors **110** and **112** respectively.

The Input Connector **110** connects the Raw Cable **108**.*j* to the Video Source Device (Tx) **104**, and comprises an Input Paddle Board **114**.*j* for providing connectivity between signals from the Video Source Device (Tx) **104** and facilities (wires, shields) of the Raw Cable **108**.*j*.

The Raw Cable **108**.*j* includes dual shielded cable elements and optionally a single coaxial line, for carrying the video signals which are high speed differential data signals as well as auxiliary signals as defined by cable specifications. Alternatively, the raw cable may include dual shielded cable elements only, i.e. excluding any other wires between the video source device and the video sink device.

Various embodiments of the Raw Cable **108**.*j* are described below, covering HDMI and DisplayPort specifications and using either coaxial or shielded twisted pair (STP) technology.

The Output Connector **112** connects the Raw Cable **108** to the Video Sink Device (Rx) **106**, and comprises an Output Paddle Board **116**.*j* including a Cable Boost Device **118**, for providing connectivity between the facilities (wires, shields) of the Raw Cable **108**.*j* and the Video Sink Device (Rx) **106**. The Cable Boost Device **118** is connected between some of the wires of the cable and the input of the Video Sink Device (Rx) **106**. The Cable Boost Device **118** includes a number of Boost Circuits **20**, one Boost Circuit **20** for terminating the dual shielded cable elements of the Raw Cable **108** which carry the high speed differential digital data signals that arrive from the Video Source Device (Tx) **104** over the Raw Cable **108**.

The Input Paddle Board **114**.*j* and the Output Paddle Board **116**.*j* constitute first and second circuit carriers which are conveniently constructed as small printed circuit boards (PCB) and may be configured to provide the mechanical

support for connector contacts according to the cable specification, for example according to the HDMI or DisplayPort standards.

FIG. **3** shows a Basic Coax HDMI Cable **102.1** based on coax technology, including a circuit carrier in the form of a first Input Paddle Board **114.1**, a first Raw Cable **108.1**, and a first Output Paddle Board **116.1** according to an embodiment of the invention. The first Raw Cable **108.1** includes a total of nine individual coaxial lines arranged as four dual shielded cable elements, that is coax pairs **202**, **204**, **206** and **208**, and a single coaxial line **210**. Each coax pair **202** to **208** comprises two coaxial lines with inner signal wires labeled as "a" and "b", and two shields which are joined together such that the joined shields form a single conductive path. Thus, each of the coax pairs **202** to **208** provides three electrical connections, i.e. one differential connection (wires "a" and "b") and one single-ended connection (the joined shields), as described earlier (see FIG. **1**B). The single coaxial line **210** provides only two conductive paths, the inner signal wire "a" and the shield.

The Cable Boost Device **118** is comprised within the first Output Paddle Board **116.1**, and has high speed differential signal inputs D**2**+, D**2**−), D**1** (D**1**+, D−), D**0** (D**0**+, D**0**−), a D**3** (D**3**+, D**3**−) and corresponding boosted outputs C**2** (polarities C**2**+, C**2**−), C**1** (C**1**+, C**1**−), C**0** (C**0**+, C**0**−), and C**3** (C**3**+, C**3**−). In addition, the Cable Boost Device **118** has ground and power inputs (GND, +5V), and a programming input (Pgm). The programming input is used to program parameters of the Cable Boost Device **118** in manufacturing. In normal operation this input is not active, and is effectively grounded (connected to GND) through a low resistance within the Cable Boost Device **118**.

HDMI signals may be classified as either high speed differential data signals or auxiliary signals. The high speed differential data signals include Transition Minimized Differential Signaling (TMDS) Data **0**, TMDS Data **1**, TMDS Data **2**, and TMDS Clock. The auxiliary signals are the following single ended signals: Consumer Electronics Control (CEC), Serial Clock (SCL), Serial Data (SDA), Utility, and Hot Plug Detect (HPD). A +5V Power and a Digital Data Channel (DDC)/CEC Ground connection is also provided through the cable. The +5V Power and the DDC/CEC Ground connections are included in the auxiliary signals for simplicity here.

The signals from the Video Source Device (Tx) **104** are connected to terminals in an Input Connection Field **212** of the Basic Coax HDMI Cable **102.1**, and recovered at the opposite end of the cable with terminals of an Output Connection Field **214** for transmission to the Video Sink Device (Rx) **106**. Standard HDMI signal names and corresponding terminal labels of the Input and Output Connection Fields **212** and **214** are listed in Table 1, which shows the preferred connection arrangement, or signal allocation scheme, for the Basic Coax HDMI Cable **102.1**.

Referring to FIG. **3** and Table 1, each of the four HDMI high speed differential data signals, TMDS Data **0**, TMDS Data **1**, TMDS Data **2**, and TMDS Clock, are routed through the Basic Coax HDMI Cable **102.1** as described in the following:

The TMDS Data **2** differential signal, comprising TMDS Data**2**+ and TMDS Data**2**− is:

- connected from the Video Source Device (Tx) **104** to txD**2**+ and txD**2**− terminals in the Input Connection Field **212**;
- routed in the first Input Paddle Board **114.1** to the input of the raw cable, namely the inner signal wires "a" and "b" of the coax pair **202**;
- routed through the inner signal wires "a" and "b" of the coax pair **202** of the first Raw Cable **108.1**;
- coupled from the end of the first Raw Cable **108.1** to D**2**+ and D**2**− inputs of the Cable Boost Device **118** in the first Output Paddle Board **116.1**; and
- coupled from the C**2**+ and C**2**− outputs of the Cable Boost Device **118** to rxD**2**+ and rxD**2**− terminals in the Output Connection Field **214**.

The other three HDMI high speed differential data signals (TMDS Data **0**, TMDS Data **1**, and TMDS Clock) are similarly connected, see Table 1.

The shields of the HDMI high speed data signals (TMDS Data**0** Shield, TMDS Data**1** Shield, TMDS Data**2** Shield, and TMDS Clock Shield), as well as the DDC/CEC Ground signal from the Video Source Device (Tx) **104** are connected to terminals txD**0***s*, txD**1***s*, txD**2***s*, txCKs, and txGnd of the Input Connection Field **212**, and tied to an input common ground node **216** in the first Input Paddle Board **114.1** whence the input common ground node **216** is connected to the shield of the single coaxial line **210**.

In the first Output Paddle Board **116.1**, the shield of the single coaxial line **210** is connected to an output common ground node **218** which is further connected to the ground (GND) input of the Cable Boost Device **118**, and to shield and ground connections of the Video Sink Device (Rx) **106**, namely terminals rxD**0***s*, rxD**1***s*, rxD**2***s*, and rxGnd. The TMDS Clock Shield of the Video Sink Device (Rx) **106** is connected through a terminal rxCKs to the programming (Pgm) input of the Cable Boost Device **118**, and so is indirectly grounded through the small resistance within the Cable Boost Device **118**. This allows the Cable Boost Device **118** to be programmed from the HDMI connector after the boosted cable is assembled without requiring any additional wire to access it. Alternatively, the rxCKs terminal may be grounded directly at the output common ground node **218** along with the other shield connections.

The remaining auxiliary signals (CEC, SCL, SDA, Utility, +5V Power, and HPD), are connected in the first Input Paddle Board **114.1** to terminals txCEC, txSCL, txSDA, txUt, txPWR, and txHPD respectively. In the first Output Paddle Board **116.1**, they are connected to terminals rxCEC, rxSCL, rxSDA, rxUt, rxPWR, and rxHPD respectively. Compared to the HDMI high speed data signals which are boosted by the Boost Device **118**, these auxiliary HDMI signals are at a lower speed, bypass the Cable Boost Device **118**, and may be carried on the inner wires or over the shields of the coaxial lines as may be convenient. The "Utility" signal in this case is unused. However if it is necessary to include it, it may be carried on an additional inner wire or over the shield of a coaxial wire as way be convenient.

While four of the auxiliary signals CEC, SCL, +5V Power and HPD are carried over the shields of the coax pairs **202** to **208**, another auxiliary signal (DDC/CEC Ground), to which also the shields of the TMDS signals are tied) is carried over the shield of single coaxial line **210**, and yet another auxiliary signal (SDA), is carried over the inner signal wire "a" of the single coaxial line **210**.

In the Basic Coax HDMI Cable **102.1**, these remaining HDMI signals (except the Utility signal) are carried over the cable as follows:

- CEC from the terminal txCEC, over the combined shields of the coax pair **202**, to the terminal rxCEC;
- SCL from the terminal txSCL, over the combined shields of the coax pair **204**, to the terminal rxSCL;
- SDA from the terminal txSDA, over the inner wire "a" of the coax **210**, to the terminal rxSDA;

+5V Power from the terminal txPWR, over the combined shields of the coax pair **206**, to the terminal rxPWR; and

Hot Plug Detect from the terminal txHPD, over the combined shields of the coax pair **208**, to the terminal rxHPD.

In the first Output Paddle Board **116.1** the +5V Power is also connected to the power input (+5V) of the Boost Device **218**.

TABLE 1

Preferred Signal Routing in Basic Coax HDMI Cable 102.1

HDMI Signal Name	Input Connection 212	Raw Cable 108.1	Boost Device Input	Boost Device Output	Output Connection 214
TMDS Data2 Shield	txD2s	210.shield	-->	-->	rxD2s
TMDS Data2+	txD2+	202.a	D2+	C2+	rxD2+
TMDS Data2−	txD2−	202.b	D2−	C2−	rxD2−
TMDS Data1 Shield	txD1s	210.shield	-->	-->	rxD1s
TMDS Data1+	txD1+	204.a	D1+	C1+	rxD1+
TMDS Data1−	txD1−	204.b	D1−	C1−	rxD1−
TMDS Data0 Shield	txD0s	210.shield	-->	-->	rxD0s
TMDS Data0+	txD0+	206.a	D0+	C0+	rxD0+
TMDS Data0−	txD0−	206.b	D0−	C0−	rxD0−
TMDS Clock Shield	txCKs	210.shield	—	—	—
			Pgm	-->	rxCKs
TMDS Clock+	txCK+	208.a	D3+	C3+	rxCK+
TMDS Clock−	txCK−	208.b	D3−	C3−	rxCK−
DDC/CEC Ground	txGnd	210.shield	GND	-->	rxGnd
CEC	txCEC	202.shield	-->	-->	rxCEC
SCL	txSCL	204.shield	-->	-->	rxSCL
SDA	txSDA	210	-->	-->	rxSDA
Utility	txUt	n/c	—	—	rxUt
+5 V Power	txPWR	206.shield	+5 V	-->	rxPWR
Hot Plug Detect	txHPD	208.shield	-->	-->	rxHPD

FIG. **4** shows a Basic STP HDMI Cable **102.2** based on Shielded Twisted Pair (STP) technology, including a second Input Paddle Board **114.2**, a second Raw Cable **108.2**, and a second Output Paddle Board **116.2** according to another embodiment of the invention.

The Input and Output Connection Fields **212** and **214**, including the respective terminals remain unchanged from the Basic Coax HDMI Cable **102.2**. The second Raw Cable **108.2** comprises five Shielded Twisted Pairs (STPs) **302**, **304**, **306**, **308**, and **310**, each comprising a shield and two signal wires "a" and "b" as described in FIG. **1**A. The allocation of the standard HDMI signals to connections through the second Raw Cable **108.2** is provided by configurations of the second Input and Output Paddle Boards **114.2** and **116.2** respectively.

The STPs **302**, **304**, **306**, **308**, and **310** of the second Raw Cable **108.2** provide 15 (3×5) distinct conductive paths, compared to the 14 paths (3×4+1) of the first Raw Cable **108.1**. Hence an additional path is available which is advantageously used in a modification of the signal assignments. This is illustrated in FIG. **4** as well as in Table 2 which lists the preferred arrangement for the Basic STP HDMI Cable **102.2**.

Because of the additional line available in the second Raw Cable **108.2**, compared to the first Raw Cable **108.1**, it is possible to use a shield connection (a common node **312** connected to the shield of the STP **308**) to connect the shields of all high speed signals (D**0**, D**1**, D**2**, and CK), and use a separate shield connection (the shield of the STP **310**) for the ground connection.

The preferred assignments shown in Tables 1 and 2 are to some extent arbitrary, and may be adapted to best utilize the space on the paddle boards and the configurations of the respective connectors.

TABLE 2

Preferred Signal Routing in Basic STP HDMI Cable 102.2

HDMI Signal Name	Input Connection 212	Raw Cable 108.2	Boost Device Input	Boost Device Output	Output Connection 214
TMDS Data2 Shield	txD2s	308.shield	-->	-->	rxD2s
TMDS Data2+	txD2+	302.a	D2+	C2+	rxD2+
TMDS Data2−	txD2−	302.b	D2−	C2−	rxD2−
TMDS Data1 Shield	txD1s	308.shield	-->	-->	rxD1s
TMDS Data1+	txD1+	304.a	D1+	C1+	rxD1+
TMDS Data1−	txD1−	304.b	D1−	C1−	rxD1−
TMDS Data0 Shield	txD0s	308.shield	-->	-->	rxD0s
TMDS Data0+	txD0+	306.a	D0+	C0+	rxD0+
TMDS Data0−	txD0−	306.b	D0−	C0−	rxD0−
TMDS Clock Shield	txCKs	308.shield	—	—	—
			Pgm	-->	rxCKs
TMDS Clock+	txCK+	308.a	D3+	C3+	rxCK+
TMDS Clock−	txCK−	308.b	D3−	C3−	rxCK−
DDC/CEC Ground	txGnd	310.shield	GND	-->	rxGnd
CEC	txCEC	306.shield	-->	-->	rxCEC
SCL	txSCL	310	-->	-->	rxSCL
SDA	txSDA	310.b	-->	-->	rxSDA
Utility	txUt	n/c	—	—	rxUt
+5 V Power	txPWR	302.shield	+5 V	-->	rxPWR
Hot Plug Detect	txHPD	304.shield	-->	-->	rxHPD

In this embodiment of the invention, the raw cable includes STPs only, i.e. excluding any other wires between the video source device and the video sink device.

HEAC Capability

In a Supplement 2 to the HDMI specification version 1.4. dated Jun. 5, 2009 cited above, a "HDMI Ethernet and Audio Return Channel" (HEAC) is specified. The HEAC channel is carried in a HEAC-capable HDMI cable as a differential data signal, i.e. negative and positive polarity signals HEAC− and a HEAC+ respectively, which replace the Hot Plug Detect (HPD) signal and the previously unused "Utility" signal respectively of the standard HDMI signal set. The HEAC channel is a passive channel which does not require boosting by the Cable Boost Device **118**. However, it does require careful control of its impedance and should therefore be enclosed in a shield, either by running each polarity in a coaxial line, or both polarities over a shielded twisted pair (STP). Accordingly, only modified connectivity (adding the HEAC channel, with controlled impedance lines, replacing HPD and "Utility" signals) in the paddle boards and in the raw cable are required to convert the basic HDMI, Cables (**102.1** and **102.2**) to accommodate the HEAC channel.

FIG. **5** shows a HEAC−Capable Coax HDMI Cable **102.3** based on coax technology, and capable of carrying an HEAC channel: including a third Input Paddle Board **114.3**, a third Raw Cable **108.3**, and a third Output Paddle Board **116.3** according to yet another embodiment of the invention.

The signals of the HEAC-capable HDMI signal set from the Video Source Device (Tx) **104**, are connected to a HEAC-capable Input Connection Field **412** of the HEAC−Capable Coax HDMI Cable **102.3**, and recovered at the opposite end of the cable with a HEAC-capable Output Connection Field **414** for transmission to the Video Sink Device (Rx) **106**. The modifications of the HEAC-capable Input and Output Fields **412** and **414** relate to name changes compared to the Input and Output Fields **212** and **214**, and reflect name changes of the terminals concerned: txUt, rxUt, txHPD, and rxHPD of the Input and Output Fields **212** and **214**, become txHEAC−, rxHEAC−, txHEAC+, and rxHEAC+ of the HEAC-capable Input and Output Fields **412** and **414**.

The third Raw Cable **108.3** comprises a total of ten individual coaxial lines arranged in four dual shielded cable elements, that is coax pairs **402**, **404**, **406**, and **408**, for carrying high speed digital data signals, and another dual shielded cable element, that is a coax pair **410**, for carrying a differential auxiliary signal. Each coax pair **402** to **410** includes two coaxial lines with inner signal wires labeled as "a" and "b", and two shields which are joined together such that the joined shields of each coax pair form a single conductive path. Thus, each of the coax pairs **402** to **410** provides three electrical connections, i.e. one differential connection (wires "a" and "b") and and one single-ended connection (the joined shields), as described earlier (see FIG. **1**B).

The assignments of the HDMI signals to the available cable connections in the third Input Paddle Board **114.3** and the third Output Paddle Board **116.3** are similar compared to the assignments used in the first Input and Output Paddle Boards **114.1** and **116.1** respectively. Unchanged connections are those for the differential HDMI high-speed data channels TMDS D**2**, D**1**, D**0**, and Clock, incoming from the Video Source Device **104**, which are connected through the coax pairs **402**, **404**, **406**, and **408** respectively to corresponding inputs of the Cable Boost Device **118**.

The differential HEAC channel is connected through the coax pair **410**, and bypasses the Cable Boost Device **118**. The shields of the coax pairs **402**, **404**, **406**, **408**, and **410** serve as conductors for the HDMI signals CEC, SCL, +5V Power, SDA, and DDC/CEC Ground respectively.

TABLE 3

Preferred Signal Routing in HEAC-capable Coax HDMI Cable 102.3

HDMI Signal Name	Input Connection 212	Raw Cable 108.2	Boost Device Input	Boost Device Output	Output Connection 214
TMDS Data2 Shield	txD2s	410.shield	-->	-->	rxD2s
TMDS Data2+	txD2+	402.a	D2+	C2+	rxD2+
TMDS Data2−	txD2−	402.b	D2−	C2−	rxD2−
TMDS Data1 Shield	txD1s	410.shield	-->	-->	rxD1s
TMDS Data1+	txD1+	404.a	D1+	C1+	rxD1+
TMDS Data1−	txD1−	404.b	D1−	C1−	rxD1−
TMDS Data0 Shield	txD0s	410.shield	-->	-->	rxD0s
TMDS Data0+	txD0+	406.a	D0+	C0+	rxD0+
TMDS Data0−	txD0−	406.b	D0−	C0−	rxD0−
TMDS Clock Shield	txCKs	410.shield	—	—	—
			Pgm	-->	rxCKs
TMDS Clock+	txCK+	408.a	D3+	C3+	rxCK+
TMDS Clock−	txCK−	408.b	D3−	C3−	rxCK−
DDC/CEC Ground	txGnd	410.shield	GND	-->	rxGnd
CEC	txCEC	402.shield	-->	-->	rxCEC
SCL	txSCL	404.shield	-->	-->	rxSCL
SDA	txSDA	408.shield	-->	-->	rxSDA
HEAC−	txHEAC+	410	-->	-->	rxHEAC−
+5 V Power	txPWR	406.shield	+5 V	-->	rxPWR
HEAC+	txHEAC+	410.b	-->	-->	rxHEAC+

The incoming shields of the HDMI high-speed data channels TMDS D**2**, D**1**, D**0**, and the TMDS Clock, are tied to the DDC/CEC Ground connection through the shield of the coax pair **410** of the cable, thus providing a connection to the outgoing shields of the HDMI high-speed data channels TMDS D**2**, D**1**, and D**0**. The outgoing shield of the TMDS Clock (rxCKs) is connected to the programming pin (Pgm) of the Cable Boost Device **118** as described above with reference to the Basic Coax HDMI Cable **102.1**.

The preferred HDMI signal routing of the HEAC−Capable Coax HDMI Cable **102.3** is listed in Table 3.

FIG. **6** shows a HEAC−Capable STP HDMI Cable **102.4**, based on Shielded Twisted Pair (STP) technology and capable of carrying an HEAC channel, including a fourth Input Paddle Board **114.4**, a fourth Raw Cable **108.4**, and a fourth Output Paddle Board **116.4** according to a fourth embodiment of the invention.

The HEAC-capable Input and Output Connection Fields **412** and **414** of the HEAC−Capable STP HDMI Cable **102.4**, including the respective terminals remain unchanged from the HEAC−Capable Coax HDMI Cable **102.3**. The fourth Raw Cable **108.4** comprises five Shielded Twisted Pairs (STPs) **502**, **504**, **506**, **508**, and **510**, each comprising a shield and two signal wires "a" and "b" as described in FIG. **1**A. The allocation of the HDMI signals to connections through the fourth Raw Cable **108.4** is provided by configurations of the fourth Input and Output Paddle Boards **114.4** and **116.4** respectively.

The STPs **502**, **504**, **506**, **508**, and **510** of the fourth Raw Cable **108.4** provide 15 (3×5) distinct conductive paths, the same number as provided in the third Raw Cable **108.3**. Accordingly, an analogous allocation of the individual signals to the Shielded Twisted Pairs including their shields, could be made. Similarly, part of the allocation scheme could also be "borrowed" from the other STP based embodiment (the Basic STP HDMI Cable **102.2**) and suitably modified to accommodate the HEAC signal.

A different connection allocation scheme is proposed here to illustrate the considerable latitude available in choosing configurations. The preferred assignments for the HEAC−Capable STP HDMI Cable **102.4** are illustrated in FIG. **6** as well as in Table 4.

As indicated earlier, the preferred assignments of signal leads in the cables are shown in the Tables 1, 2, 3, and 4. These are to some extent arbitrary. The "+5V Power" and the "DDC/CEC Ground" connections are preferably carried on a shield; the HDMI high speed data signals (TMDS D**0**, D**1**, D**2**, and Clock) should always be carried on shielded conductors, i.e. the inner conductors of coax lines or the twisted signal wires of STPs, depending on wire type; and the lower speed connections (CEC, SCL, SDA, Utility, and HPD) may be carried on inner/signal wires or shields in an arrangement that may be adapted to best utilize the space on the paddle boards and the configuration of the respective connectors.

The use of the TMDS Clock Shield connection on the receive side (rxCKs) to access the programming pin (Pgm) of the Cable Boost Device **118** is a convenience for programming the device in the fully assembled boosted HDMI cable. If this feature is not required, the TMDS Clock Shield should be grounded along with the other TDMS signal shields at both ends of the cable.

TABLE 4

Preferred Signal Routing in HEAC-capable STP HDMI Cable 102.4

HDMI Signal Name	Input Connection 212	Raw Cable 108.2	Boost Device Input	Boost Device Output	Output Connection 214
TMDS Data2 Shield	txD2s	510.shield	-->	-->	rxD2s
TMDS Data2+	txD2+	502.a	D2+	C2+	rxD2+
TMDS Data2−	txD2−	502.b	D2−	C2−	rxD2−
TMDS Data1 Shield	txD1s	510.shield	-->	-->	rxD1s
TMDS Data1 +	txD1+	504.a	D1+	C1 +	rxD1+
TMDS Data1−	txD1−	504.b	D1−	C1−	rxD1−
TMDS Data0 Shield	txD0s	510.shield	-->	-->	rxD0s

TABLE 4-continued

Preferred Signal Routing in HEAC-capable STP HDMI Cable 102.4

HDMI Signal Name	Input Connection 212	Raw Cable 108.2	Boost Device Input	Boost Device Output	Output Connection 214
TMDS Data0+	txD0+	506.a	D0+	C0+	rxD0+
TMDS Data0−	txD0−	506.b	D0−	C0−	rxD0−
TMDS Clock Shield	txCKs	510.shield	—	—	—
			Pgm	-->	rxCKs
TMDS Clock+	txCK+	508.a	D3+	C3+	rxCK+
TMDS Clock−	txCK−	508.b	D3−	C3−	rxCK−
DDC/CEC Ground	txGnd	510.shield	GND	-->	rxGnd
CEC	txCEC	506.shield	-->	-->	rxCEC
SCL	txSCL	508.shield	-->	-->	rxSCL
SDA	txSDA	504.shield	-->	-->	rxSDA
HEAC−	txHEAC-->	510	-->	-->	rxHEAC−
+5 V Power	txPWR	502.shield	+5 V	-->	rxPWR
HEAC+	txHEAC+	510.b	-->	-->	rxHEAC+

DisplayPort Cables

FIG. **7** shows a Coax DisplayPort Cable **102.5** based on coax technology, including a fifth Input Paddle Board **114.5**, a fifth Raw Cable **108.5**, and a fifth Output Paddle Board **116.5** according to an embodiment of the invention. The fifth Raw Cable **108.5** includes a total of ten individual coaxial lines arranged in five coax pairs **602**, **604**, **606**, **608**, and **610**. Each coax pair **602** to **610** comprises two coaxial lines with inner signal wires labeled as "a" and "b", and two shields which are joined together such that the joined shields form a single conductive path. Thus, each of the coax pairs **602** to **608** provides three electrical connections, i.e. one differential connection (wires "a" and "b") and one single-ended connection (the joined shields), as described earlier (see FIG. **1**B).

The same Cable Boost Device **118** as in the boosted HDMI cables described above, is comprised within the fifth Output Paddle Board **116.5**.

Standard DisplayPort signals from the Video Source Device (Tx) **104**, are connected to terminals in a DisplayPort Input Connection Field **612** of the Coax DisplayPort Cable **102.5**, and recovered at the opposite end of the cable at terminals of a DisplayPort Output Connection Field **614** for transmission to the Video Sink Device (Rx) **106**. The DisplayPort signal names and corresponding terminal labels of the DisplayPort Input and Output Connection Fields **612** and **614** are listed in Table 5, which shows the preferred connection arrangement, or signal allocation scheme, for the Coax DisplayPort Cable **102.5**.

Referring to FIG. **7** and Table 5, each of the four DisplayPort high speed differential data lanes ML-L**0**, ML-L**1**, ML-L**2**, and ML-L**3**, is routed through the Coax DisplayPort Cable **102.5** as described in the following:

The Main Line Lane**0** differential signal, comprising positive (p) and negative (n) polarities is:

- connected from the Video Source Device (Tx) **104** to txML_L**0+** and txML_L**0−** terminals in the DisplayPort Input Connection Field **612**;
- routed in the fifth Input Paddle Board **114.5** to the inner signal wires "a" and "b" of the coax pair **602**;
- routed through the fifth Raw Cable **108.5** on the inner signal wires "a" and "b" of the coax pair **602** of the fifth Raw Cable **108.5**;
- coupled from the end of the fifth Raw Cable **108.5** to D**0+** and D**0−** inputs of the Cable Boost Device **118** in the fifth Output Paddle Board **116.5**; and
- coupled from the C**0+** and C**0−** outputs of the Cable Boost Device **118** to rxML_L**0+** and rxML_L**0−** terminals in the DisplayPort Output Connection Field **614**.

The other three main-line differential data signals (Main Line Lane**1**, Lane**2**, and Lane **3**) are similarly connected, see Table 5.

All ground connections of the incoming DisplayPort connector which are labeled txGND**0**, txGND**1**, txGND**2**, txGND**3**, txGNDaux as well as the "Return" (txGNDpwr), i.e. the power return terminal, are tied together to an input common ground node **616** in the fifth Input Paddle Board **114.5**, and connected to the shield of the coax pair **604**.

In the fifth Output Paddle Board **116.5**, the shield of the coax pair **604** is connected to an output common ground node **618** which is also connected to the ground (GND) input of the Cable Boost Device **118**, and to shield and ground connections of the Video Sink Device (Rx) **106**, namely terminals rxGND**0**, rxGND**1**, rxGND**2**, rxGNDaux, and txGNDpwr. An exception is the fourth ground pin of the receive side which is connected through a terminal rxGND**3** to the programming (Pgm) input of the Cable Boost Device **118**, and so is only indirectly grounded. This allows the Cable Boost Device **118** to be programmed from the connector after the boosted cable is assembled without requiring any additional wire to access it. Alternatively, the rxGND**3** terminal may also be grounded at the output common ground node **618** along with the other ground connections.

Other DisplayPort signals CONFIG**1**, CONFIG**2**, AUX Channel (p) and (n), Hot Plug, and DP_PWR, are respectively connected in the fifth Input Paddle Board **114.5** to terminals txCONFIG**1**, txCONFIG**2**, txAuxCh+ and txAuxCh−, txHPD, and txDP_PWR. In the fifth Output Paddle Board **116.5**. they are respectively connected to terminals rxCONFIG**1**, rxCONFIG**2**, rxAuxCh+ and rxAuxCh−, rxHPD, and rxDP_PWR. Compared to the main line high speed signals which are boosted by the Boost Device **118**, these other DisplayPort signals are at a lower speed, bypass the Cable Boost Device **118**, and may be carried on the inner wires or over the shields of the coaxial lines as may be convenient. The AUX Channel signal however is of moderately high speed and is required to be carried in a controlled impedance wire, for which the coax pair **610** is chosen in this embodiment of the invention.

In the Coax DisplayPort Cable **102.5**, the remaining signals are carried over the cable as follows:

- CONFIG**1** from the terminal txCONFIG**1**, over the combined shields of the coax pair **606**, to the terminal rxCONFIG**1**;
- CONFIG**2** from the terminal txCONFIG**2**, over the combined shields of the coax pair **608**, to the terminal rxCONFIG**2**;
- Hot Plug from the terminal txHPD, over the combined shields of the coax pair **610**, to the terminal rxHPD; and
- DP_PWR from the terminal txDP_PWR, over the combined shields of the coax pair **602**, to the terminal rxDP_PWR.

In the fifth Output Paddle Board **116.5** the DP_PWR is also connected to the power input (+5V) of the Cable Boost Device **218**. Even though the voltage of DP_PWR will be lower than the HDMI +5V Power, the same Cable Boost Device **218** may be designed or programmed to run at both the HDMI and the DisplayPort voltages. Alternatively, a DisplayPort specific version of the Cable Boost Device **218** may be developed.

TABLE 5

Preferred Signal Routing in Coax DisplayPort Cable 102.5

DisplayPort Signal Name	Input Connection 212	Raw Cable 108.1	Boost Device Input	Boost Device Output	Output Connection 214
Main Line Lane0 (p)	txML_L0+	602	D0+	C0+	rxML_L0+
Ground (pin 2)	txGND0	604.shield	-->	-->	rxGND0
Main Line Lane0 (n)	txML_L0−	602.b	D0−	C0−	rxML_L0−
Main Line Lane1 (p)	txML_L1+	604	D1+	C1+	rxML_L1+
Ground (pin 5)	txGND1	604.shield	-->	-->	rxGND1
Main Line Lane1 (n)	txML_L1−	604.b	D1−	C1−	rxML_L1−
Main Line Lane2 (p)	txML_L2+	606	D2+	C2+	rxML_L2+
Ground (pin 8)	txGND2	604.shield	-->	-->	rxGND2
Main Line Lane2 (n)	txML_L2−	606.b	D2−	C2−	rxML_L2−
Main Line Lane3 (p)	txML_L3+	608	D3+	C3+	rxML_L3+
Ground (pin 11)	txGND3	604.shield	Pgm	-->	rxGND3
Main Line Lane0 (n)	txML_L3−	608.b	D3−	C3−	rxML_L3−
CONFIG1	txCONFIG1	606.shield	-->	-->	rxCONFIG1
CONFIG2	txCONFIG2	608.shield	-->	-->	rxCONFIG2
AUX Channel (p)	txAuxCh+	610	-->	-->	rxAuxCh+
Ground (pin 16)	txGNDaux	604.shield	-->	-->	rxGNDaux
AUX Channel (n)	txAuxCh−	610.b	-->	-->	rxAuxCh−
Hot Plug	txHPD	610.shield	-->	-->	rxHPD
Return	txGNDpwr	604.shield	GND	-->	rxGNDpwr
DP_PWR	txDP_PWR	602.shield	+5 V	-->	rxDP_PWR

FIG. **8** shows a STP DisplayPort Cable **102.6** based on Shielded Twisted Pair (STP) technology, including a sixth Input Paddle Board **114.6**, a sixth Raw Cable **108.6**, and a sixth Output Paddle Board **116.6** according to an embodiment of the invention. The sixth Raw Cable **108.6** includes a total of five STPs **702**, **704**, **706**, **708**, and **710**, each comprising a shield and two signal wires "a" and "b" as described in FIG. **1**A.

The allocation of the DisplayPort signals to connections through the sixth Raw Cable **108.6** is provided by configurations of the sixth Input and Output Paddle Boards **114.6** and **116.6** respectively, and is analogous to the allocation in the Coax DisplayPort Cable **102.5**, FIG. **7**. The STP signal assignments are illustrated in FIG. **8** which is identical to FIG. **7** except for showing Shielded Twisted Pairs (STPs) **702**, **704**, **706**, **708**, and **710** instead of coax pairs **602**-**610**. While the sixth Input and Output Paddle Boards **114.6** and **116.6** have similar connectivity to the corresponding fifth Input and Output Paddle Boards **114.5** and **116.5**, their mechanical properties would differ in order to accommodate the different termination geometries of the STPs versus the coax pairs on the paddle boards.

All auxiliary signals, CONFIG**1**, CONFIG**2**, Hot Plug, Ground and DP_PWR, may be placed over any shields of coaxial or STP lines as may be convenient or for an arrangement that may be adapted to best utilize the space on the paddle boards and the configuration of the respective connectors.

Low Wire Count Summary

The number of wires in a boosted high speed digital video cable such as an HDMI or DisplayPort cable, has been reduced from fourteen or more in prior art cables to nine or ten by using the shields to individually carry active signals as well as power and ground. This reduction is enabled by the boost device which guarantees the removal of potentially harmful common mode interference on the high speed data lines. The reduction in the number of wires simplifies their alignment for termination in the connectors. The original high speed cables use a mix of coaxial lines or shielded twisted pairs and standard wires. The invention provides a reduction in the construction cost of high speed cables by the use of only a single type of wire, either coaxial or STP, to carry all signals. This significantly simplifies cable assembly and allows a single step termination process, ultimately reducing cost.

Low Impedance Cables

In addition to the advantages obtained through the low wire count technique described above, a further cost advantage may be achieved by using coaxial lines or Shielded Twisted Pairs (STP) of a lower impedance than the nominal line impedance implied in the standards, for carrying the high speed data signals in any of the Boosted Digital Video Cables **102** described here.

FIG. **9** shows a three coax line cross sections, to illustrate a comparison between exemplary design choices, including a standard coax **902**; a reduced-outer-diameter coax **904**; and an increased-core-diameter coax **906**. The standard coax **902** comprises an outer insulating sheath **902**.*a*, a shield **902**.*b*, an inner insulator **902**.*c*, and a core wire (core) **902**.*d*.

The reduced-outer-diameter coax **904** comprises an outer insulating sheath **904**.*a*, a shield **904**.*b*, an inner insulator **904**.*c*, and a core wire (core) **904**.*d*. The increased-core-diameter coax **906** comprises an outer insulating sheath **906**.*a*, a shield **906**.*b*, an inner insulator **906**.*c*, and a core wire (core) **906**.*d*.

The characteristic impedance Z**0** of a coaxial line is determined by dimensions of the cable, more precisely, by the ratio of the diameter of the core wire to the inner diameter of the shield, and by the dielectric constant of the inner isolator material.

The core **902**.*d* of the thin standard coax **902** with a characteristic impedance of 50 ohms is an American Wire Gauge (AWG) wire of about 78 μm diameter, resulting in an overall diameter of the standard coax **902** of about 210 μm.

By allowing the coax to have a lower, "non-standard" characteristic impedance it is possible for example, and without changing the insulator material, to either reduce the outer diameter of the coax without having to use a finer core wire, or to increase the core diameter while keeping the outer diameter constant.

The core **904**.*d* of the reduced-outer-diameter coax **904** is the same wire gauge as the core **902**.*d* of the standard coax **902**, but the shield **904**.*c* is shrunk such that a characteristic impedance of 35 ohms is obtained for the reduced-outer-diameter coax **904**. This results in an overall diameter of the reduced-outer-diameter coax **902** of about 145 μm, a savings of about 30% compared to the standard coax **902** with 50 ohm characteristic impedance.

If the outer diameter is not changed, a thicker core wire may be used. The shield **906**.*b*, hence the overall diameter of the increased-core-diameter coax **906**, corresponds to that of the standard coax **902**. However, the thickness of the core **906**.*d* is increased such that a characteristic impedance of 35 ohms is obtained for the increased-core-diameter coax **906**, resulting in a wire size of AWG **40** for the core **906**.*d* of the increased-core-diameter coax **906**. AWG **35** corresponds to a wire diameter of about 143 μm, an almost 80% increase in thickness.

The inventors have considered the impact of deviating from the standard 50 ohm coax for implementing the HDMI and DisplayPort cables described above, that is the Basic Coax HDMI Cable **102.1**, the HEAC−Capable Coax HDMI

Cable **102.3**, and the Coax DisplayPort Cable **102.5**, as well as other boosted digital video cables. To recapitulate, the Video Source Device **104** transmits high speed differential signals through coax pairs to the Cable Boost Device **118** which equalizes and boosts the signals before transmitting them to the Video Sink Device **106**.

The Video Source Device **104** is designed to transmit these high speed differential signals over cables presenting a characteristic impedance of 100 ohms differentially, that is 2 times 50 ohms in the case of dual coaxial lines (coax pairs). An input circuit in the Video Sink Device **106** similarly presents matching 100 ohms differential terminations to the cable.

In the case of the boosted cables with a reduced impedance coax, the Cable Boost Device **118** provides a proper output circuit for transmission of the boosted signals to the Video Sink Device **106**. An input termination in the Cable Boost Device **118** can be tuned to terminate a reduced impedance cable with the correct impedance, for example 35 ohms, or 70 ohms differentially.

The Video Source Device **104** is designed as a current source and would be able to directly transmit into any cable impedance; no undesired signal reflections would result as long as the cable is correctly terminated at the receiving end, that is at the Cable Boost Device **118**. However, compliance testing of HDMI and DisplayPort cables requires the cable to present a nominal 100 ohm differential impedance at source end for a unidirectional active cable and both ends for a passive cable.

FIG. **10** shows a Low-Impedance (Low Z**0**) Coax HDMI Cable **102.10** which is identical to the Basic Coax HDMI Cable **102.1** of FIG. **3** except for a Low-Impedance Input Paddle Board **114.10** which replaces the first Input Paddle Board **114.1**. The Low-Impedance Input Paddle Board **114.10** has the same connectivity as the first Input Paddle Board **114.1**, except for eight padding resistors R**1** to R**8** which are inserted between the high speed signal terminals txD**2**+, txD**2**−, txD**1**+, txD**1**−, txD**0**+, txD**02**−, txCK+, and txCK− of the Input Connection Field **212**, and the inner signal wires "a" and "b" of the corresponding coax pairs **202** to **208** of the first Raw Cable **108.1**.

One pair of padding resistors is required to be inserted in series with each of the inner signal wires "a" and "b" of the TMDS signals. The resistance of each padding resistor is derived such that the combined resistance of two padding resistors in series with the inner signal wires (the shielded conductors) of each coax pair (dual shielded cable element) **202** to **208** is equal to the difference between the specified nominal cable impedance and the impedance of the coax pair, for example a 100 ohm nominal impedance is achieved by using two coax lines of 35 ohm impedance, each with 15 ohm padding resistors, as a coax pair.

The padding resistors R**1**-R**8** could be omitted without loss of functionality, but they are provided in order to meet the specified differential input impedance of 100 ohms for the Low-Impedance Coax HDMI Cable **102.10**.

If the coax pairs **202** to **208** of the first Raw Cable **108.1** are made of low-impedance coaxial lines, such as the reduced-outer-diameter coax **904** or the increased-core-diameter coax **906** which each have an exemplary characteristic impedance of 35 ohms, the values of each of the padding resistors R**1** to R**8** should be 50−35=15 ohms, such that each coax pair, combined with the padding resistors, presents a 2×50=100 ohm impedance to the differential terminals of the Input Connection Field **212**. In general, the resistance of each padding resistor R**1** to R**8** should be X ohms, where X is equal to the difference between one half of the specified nominal impedance (e.g. 100 Ohms for HDMI) and the actual characteristic impedance of the coax.

Similarly, other coax based high speed video cables such as the HEAC−Capable Coax HDMI Cable **102.3** (FIG. **5**) and the Coax DisplayPort Cable **102.5** (FIG. **7**) are easily modified by the addition of the padding resistors R**1** to R**8** on their respective input paddle boards, to accommodate low-impedance coax cables.

It is worth noting that signals other than the high speed differential data signals, for example the HEAC channel of HDMI and the AUX channel of DisplayPort, are not boosted by the Cable Boost Device **118**. The coax pairs transporting these signals (coax pair **410** for HEAC, and coax pair **610** for the AUX channel) can not be of the low-impedance type, but must be regular 50 ohm coaxes.

The same techniques for using reduced impedance coax cables also applies for boosted HDMI and DisplayPort cables that use Shielded Twisted Pairs (STP) for transmitting the high speed differential data signals. The characteristic impedance of STPs is determined by the ratio of the insulated wire diameter to the diameter of the bare wire, and the dielectric properties of the insulation material.

Low-impedance STPs are easily made by reducing the thickness of the insulation compared to the diameter of the bare wire. This of course also affects the size of the shield. A reduction in the thickness of STP wire insulation by about 30% without changing the bare wire thickness will reduce the (differential) impedance of the STP from a nominal 100 ohms to 70 ohms. Instead of reducing the size of the STP cable in this way, it is also possible to maintain the original overall size and increase the bare wire thickness.

When a low impedance STP is employed in any of the boosted video cables based on STP technology, such as the Basic STP HDMI Cable **102.2** (FIG. **4**), the HEAC−Capable STP HDMI Cable **102.4** (FIG. **6**), and the STP DisplayPort Cable **102.6**, the same considerations as with the coax based cables apply: the input circuit of the Cable Boost Device **118** should be programmed to match the STP impedance, and the input paddle board should be modified to include padding resistors. Similar to the rule that applies in the coax case, the resistance of each padding resistor R**1** to R**8** in the STP case should be Y ohms, where Y is equal to one half of the difference between the specified nominal impedance (e.g. 100 Ohms for HDMI) and the actual differential impedance of the STP.

The lowering of the characteristic impedance in coax or STP based cables which include boost devices has a number of advantages which may be exploited, either to reduce the size of the cable for material savings, improved flexibility, etc., or to increase the wire size without reducing the overall size of the cable for improved handling, and lower material cost. Note that thicker wire may actually cost less to produce than very fine wire.

Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the true scope of the invention.

A person understanding this invention may now conceive of alternative structures and embodiments or variations of the above all of which are intended to fall within the scope of the invention as defined in the claims that follow.

What is claimed is:

1. A digital video cable for carrying one or more high speed differential digital data signals and one or more auxiliary signals between a video source device and a video sink device according to a cable specification, the cable comprising:

a boost device;

a raw cable having one or more dual shielded cable elements, each dual shielded cable element comprising two shielded conductors and a shield;

the shielded conductors of at least one dual shielded cable element extending between the video source device and the boost device;

the shields of said one or more dual shielded cable elements extending between the video source device and the video sink device;

wherein the shield of the at least one dual shielded cable element is electrically connected with an auxiliary signal input and an auxiliary signal output, such that the shield is adapted to carry an auxiliary signal between the auxiliary signal input and the auxiliary signal output; and

wherein the shielded conductors of said at least one dual shielded cable element are adapted to carry a high speed differential digital data signal.

2. The cable of claim **1**, wherein said one or more dual shielded cable elements are dual coaxial elements, each comprising two coaxial lines whose shields are joined, and each coaxial line enclosing one shielded conductor.

3. The cable of claim **1**, wherein some of said one or more dual shielded cable elements are dual coaxial elements, each comprising two coaxial lines whose shields are joined, and each coaxial line enclosing one shielded conductor.

4. The cable of claim **1**, wherein the raw cable further includes a coaxial line having a shield enclosing one shielded conductor, the coaxial line extending between the video source device and the video sink device; the shield is adapted to carry another auxiliary signal, and the shielded conductor is adapted to carry yet another auxiliary signal.

5. The cable of claim **1**, wherein said one or more dual shielded cable elements are Shielded Twisted Pairs (STP), each comprising a shield enclosing the two shielded conductors.

6. The cable of claim **1**, wherein some of said one or more dual shielded cable elements are Shielded Twisted Pairs (STP), each comprising a shield enclosing the two shielded conductors.

7. The cable of claim **1**, wherein the raw cable comprises said one or more dual shielded cable elements only, each dual shielded element comprising a dual coaxial element, comprising two coaxial lines whose shields are joined, each coaxial line enclosing one shielded conductor.

8. The cable of claim **1**, wherein the raw cable comprises said one or more dual shielded cable elements only, each dual shielded element comprising a Shielded Twisted Pair (STP), comprising a shield enclosing the two shielded conductors.

9. The cable of claim **1**, wherein the cable specification is the High-Definition Multimedia Interface (HDMI) standard.

10. The cable of claim **9**, wherein said one or more high speed differential digital data signals comprise Transition Minimized Differential Signaling (TMDS) signals; and said one or more auxiliary signals comprise Consumer Electronics Control (CEC), Serial Clock (SCL), Hot Plug Detect (HPD), and +5V Power signals.

11. The cable of described in claim **10**, wherein the boost device comprises an equalizer and an amplifier for equalizing and boosting the TMDS signals respectively.

12. The cable of claim **9**, wherein:

the shielded conductors of four dual shielded cable elements extending between the video source device and the boost device;

the shielded conductors of the four dual shielded cable elements are adapted to carry respective four high speed differential digital data signals, which are Transition Minimized Differential Signaling (TMDS) signals;

the shielded conductors of one other dual shielded cable element, extending between the video source device and the video sink device, are adapted to carry an auxiliary signal, which is a HDMI Ethernet and Audio Return Channel (HEAC) differential signal; and

the shields of the four dual shielded cable elements and said one other dual shielded cable element are adapted to carry auxiliary signals, which are Consumer Electronics Control (CEC), Serial Clock (SCL), Serial Data (SDA), Digital Data Channel (DDC)/CEC Ground, and +5V Power signals.

13. The cable of claim **1**, wherein the cable specification is the Displayport standard.

14. The cable of claim **13**, wherein:

the shielded conductors of four dual shielded cable elements extending between the video source device and the boost device;

the shielded conductors of the four dual shielded cable elements are adapted to carry respective four high speed differential digital data signals, which are Main Line lanes;

the shielded conductors of one other dual shielded cable element, extending between the video source device and the video sink device, are adapted to carry an auxiliary signal, which is an Auxiliary Channel (AUX CH) differential signal; and

the shields of the four dual shielded cable elements and said one other dual shielded cable element are adapted to carry auxiliary signals, which are CONFIG**1**, CONFIG**2**, Ground, Hot Plug Detect (HPD), and DisplayPort power (DP-PWR) signals.

15. The cable of claim **14**, wherein the boost device comprises an equalizer and an amplifier for equalizing and boosting the Main Line lanes respectively.

16. The cable of claim **1**, further comprising a first circuit carrier for connecting the video source device to the raw cable.

17. The cable of claim **16**, wherein the first circuit carrier further comprises terminals for connecting the high speed differential digital data signal from the video source device to the shielded conductors of said at least one dual shielded cable element.

18. The cable of claim **17**, wherein the first circuit carrier further comprises terminals for connecting at least one auxiliary signal from the video source device to the shield of said at least one dual shielded cable element.

19. The cable of claim **16**, further comprising a second circuit carrier for connecting the raw cable to the video sink device.

20. The cable of claim **19**, wherein the second circuit carrier comprises the boost device.

21. The cable of claim **1**, wherein an impedance of said at least one dual shielded cable element is lower than a nominal impedance of the cable specified in the cable specification, the cable further comprising:

a first circuit carrier connecting the video source device to the raw cable, the first circuit carrier including two padding resistors, each padding resistor being in series with a respective shielded conductor of said at least one dual shielded cable element; and

a second circuit carrier connecting the raw cable to the video sink device, the boost device being mounted on the second circuit carrier for terminating said at least one dual shielded cable element, and for boosting the high speed differential digital data signal.

22. A method for transmitting one or more high speed differential digital data signals and a one or more auxiliary signals from a video source device to a video sink device over a digital video cable having a raw cable and a boost device, the method comprising:

carrying at least one high speed differential digital data signal from the video sink device to a boost device in a pair of shielded conductors of the raw cable;

boosting the at least one high speed differential digital data signal in the boost device to produce a boosted signal, and transmitting the boosted signal to the video sink device; and

carrying at least one auxiliary signal from the video source device to the video sink device on a shield of the pair of the shielded conductors.

23. The method of claim **22**, further including equalizing the at least one high speed differential digital data signal in the boost device.

24. The method of claim **22**, wherein the transmitting comprises transmitting over the digital video cable, which is one of the following:

a High-Definition Multimedia Interface (HDMI) cable;

a Displayport cable.

* * * * *