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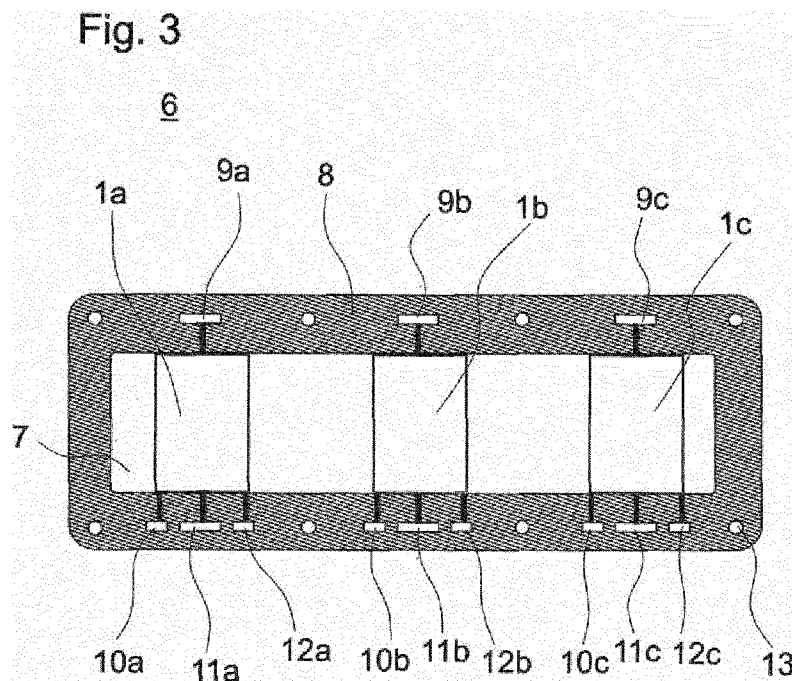
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(57) Abstract: The present invention relates to a 3-level power module (6) comprising a baseplate (8), a 3-level inverter circuit (1a), the 3-level inverter circuit (1a) being arranged on the baseplate (8), and a phase output connector (9a). The object of the invention is to provide a compact 3-level multi-phase power module (6). The object is solved when the 3-level power module (6) further comprises one or more further 3-level inverter circuits, each being arranged on the baseplate and each being connected to a corresponding further phase output connector (9b, 9c) of the 3-level power module (6).



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3-level power module

The present invention relates to a 3-level power module comprising a baseplate, a 3-level inverter circuit, the 3-level inverter circuit being arranged on the baseplate, and a phase output connector.

5 Multi-phase power modules are well known, and are used extensively where the conversion of a DC voltage into an AC voltage is required. Examples include the use as an inverter to convert DC supplied by a solar panel into an AC supply suitable for feeding into a supply grid. Multi-phase inverters are also used in motor controllers, wind generators, and active filters, and each
10 of these cases inverter circuits are used for converting power from DC stages into AC, or vice versa. 3-phase systems are particularly common in connection with power distribution grids, and systems with more than three phases are also known in specialized areas such as motor control. Inverters which convert +/- DC voltages into AC, known as 2-level inverters, are also
15 well known in the art. Both, 2-level and 3-level inverters, function by switching the voltage occurring at the input in a controlled manner to create an AC power supply at the output which has the required waveform. A 3-level inverter is able to recreate the required waveform in a more efficient way than a 2-level inverter.

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The 3-level power module as described above may generate, for example, a single phase AC voltage from three DC voltage levels. If a multi-phase system is intended to be constructed, two or more of such single phase circuits are required. For example, for a 3-phase inverter three single-phase
25 power modules are required.

In general, it is normal to supply multiple separate power modules, each of which is fed by 3-level DC inputs and gives a single phase output. For multi-phase inverter applications, two or more of these separate modules need to
30 be used. This requires space, since each of the individual power modules

-2-

has packaging and fixing features which will take space. It is therefore impossible to mount such separate power modules very close together. In addition, the fact that the need to be separately cooled is liable to lead to overly complex cooling systems and/or two or more separately cooled areas with consequentially long sealed perimeters. Since such sealed perimeters are prone to leakage of coolant, the minimizing of the sealed perimeter length is of great advantage.

It is therefore the object of the invention to provide a compact 3-level multi-phase power module.

The object of the invention is solved by the 3-level power module as described above in which the 3-level power module further comprises one or more further 3-level inverter circuits, each being arranged on the baseplate and each being connected to a corresponding further phase output connector of the 3-level power module.

In other words, the inventive solution comprises use of a single baseplate construction for a 3-level, multi-phase power module. This means that all circuitry, thus all electrical circuit elements of the 3-level inverter circuits of the multi-phase power module, is built into a single package comprising a single monolithic baseplate, suitable for being cooled. In this way, the space used in the prior art for packaging of individual phase modules and for fixing holes etc. is reduced and the 3-level multi-phase power module can be manufactured in a more compact manner. This may be of great advantage where size and/or weight considerations are important.

In embodiments, the 3-level power module comprises one or more substrates arranged on the baseplate, each substrate carrying electrical circuit elements of one or more of the 3-level inverter circuits. In embodiments, there is exactly one substrate. In other embodiments, the number of substrates equals the number of 3-level inverter circuits. In yet other embodiments, the

-3-

number of substrates equals twice the number of 3-level inverter circuits. In embodiments, the substrate is a direct bonded copper (DBC) substrate. The substrate may comprise a ceramic core with copper layers on each side of the ceramic core. One of the copper layers may be affixed to the baseplate.

5 The other copper layer on the surface opposite to that affixed to the baseplate may be divided into separate tracks to comprise the circuitry required for the components mounted on the surface. Such components, also known as electrical circuit elements, may comprise power semiconductors used for switching and ancillary components such as resistors, capacitors,

10 control electronics and conductors for linking these individual components and the tracks. However, other substrates may be used in further embodiments. In embodiments, the baseplate is a solid copper baseplate. This gives rigidity to the 3-level multi-phase power module. However, in some embodiments, the baseplate may comprise or consist of aluminium or

15 another metal with good thermal conductivity. Alternatively, a non-metallic baseplate can be used such as the baseplate constructed from ceramic materials or laminates. It should be noted, however, that the electrical circuit elements, like controlled semiconductors, used in the circuits described here, are liable to generate heat when in service. Therefore, it is important that the

20 baseplate has high thermal conductivity to enable that heat to be conducted away from the electrical circuit elements, especially from the controlled semiconductors. In some embodiments, there are two or more substrates, each substrate carrying electrical circuit elements of two or more of the 3-level inverter circuits.

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In embodiments, electrical circuit elements of two or more of the 3-level inverter circuits are arranged on the same substrate. Thus, all the 3-level inverter circuits may be placed on a single substrate which in turn is affixed to the single baseplate. The packaging in this embodiment may be very

30 compact.

-4-

In embodiments, electrical circuit elements of one or more of the 3-level inverter circuits are distributed over two or more substrates. In embodiments, this means that some controlled semiconductors of the 3-level inverter circuit may be arranged on one substrate while the remaining electrical circuit elements of the 3-level inverter circuit are arranged on one or two further substrates. This may improve the quality of the phase output signal. For example, inductance may be reduced. In embodiments, each of the 3-level inverter circuits is distributed over two substrates, respectively. Thus, in these embodiments, the number of substrates may be twice the number of 3-level inverter circuits.

In embodiments, the 3-level inverter circuits are arranged side by side in a linear array, the 3-level power module providing three phase output connectors. This may lead to a very compact 3-level power module. In embodiments, there are exactly three 3-level inverter circuits, each of the three 3-level inverter circuits being electrically connected to one corresponding phase output connector of the module respectively. 3-level inverter circuits may be of NPC1 topology or NPC2 topology. The 3-level power module may comprise a positive input voltage connector, a negative input voltage connector and an intermediate voltage connector per 3-level inverter circuit. The intermediate voltage connector is adapted to receive a voltage of a value between a positive input voltage and a negative input voltage. In some embodiments, the intermediate input voltage connector, also known as centre tap or zero point, may be adapted to receive a zero voltage. The AC voltage to be provided at each phase output connector may be then be generated by controlled switching of control semiconductor elements electrically connected between said corresponding input voltage connectors and the phase output connector. In embodiments, there are two, three, four, five, six, or more 3-level inverter circuits, each connected to a corresponding further phase output connector, respectively. Thus, the number of phase output connectors of the module may be equal to the

number of 3-level inverter circuits present in the 3-level power module. Therefore, depending on the number of phase output connectors, a corresponding number of phases may be provided on the output side by the 3-level power module.

5

In embodiments, the phase output connectors are arranged on one side of the baseplate and DC input connectors are arranged on an opposing side of the baseplate. Each DC input connector may be connected to exactly one of the 3-level inverter circuits. The 3-level power module may provide three DC
10 input connectors per 3-level inverter circuit. Thus, the number of DC input connections may be three times the number of phase output connectors. The baseplate may be a rectangular baseplate. The phase output connectors may be arranged on one long side of the baseplate and the DC input
15 connectors of each of the 3-level inverter circuits may be arranged on the opposing long side of the baseplate. However, in embodiments the phase output connectors are arranged on one short side of the baseplate and the DC input connectors are arranged on the opposing short side of the
20 baseplate. In either way, being arranged on one side of the baseplate means being arranged close to the same edge of the baseplate. In general, the phase output connectors and the DC input connectors extend to the same
25 direction away from the baseplate, in embodiments perpendicularly away from the baseplate.

In embodiments, the phase output connectors and the DC input connectors
25 are arranged in a linear array and/or in a grouped configuration, respectively. Thus, in embodiments the phase output connectors, each of the phase output connectors being connected to a corresponding of the 3-level inverter
30 circuits, are arranged in a linear array and/or in a grouped configuration. In embodiments, the DC input connectors, each of the DC input connectors being connected to a corresponding of the 3-level inverter circuits are
30 arranged in a linear array and/or in a grouped configuration. In embodiments,

the DC input connectors of the 3-level power module are arranged in the linear array, thus forming a single row of connectors. Lining up either type of connectors may allow a compact connector design. Grouping the connectors may allow easy identification of connectors of the same 3-level inverter

5 circuit. Grouping may mean that DC input connectors connected to one of the 3-level inverter circuits have a smaller distance from each other than the DC input connectors of the same 3-level inverter circuit from a DC input connector of a further 3-level inverter circuit have. The phase output connector connected to the 3-level inverter circuit may be arranged on the

10 opposite side of the baseplate compared to the DC input connectors of the same 3-level inverter circuit.

In embodiments one or more of the 3-level inverter circuits comprise an upper bridge branch, which is arranged between a positive input connection and a centre tap, and a lower bridge branch, which is arranged between the

15 negative input connection and the centre tap, wherein the upper bridge branch comprises two or more controlled upper semiconductor elements and the lower bridge branch comprises two or more controlled lower semiconductor elements. This may be realized by using NPC1 topology or

20 NPC2 topology, in embodiments.

In embodiments, the upper bridge branch comprises two or more groups of controlled upper semiconductor elements connected in parallel to each other and the lower bridge branch comprises two or more groups of controlled

25 lower semiconductor elements connected in parallel to each other.

According to some embodiments, at least two groups of each bridge branch are distributed over two or more substrates. As discussed before, this may have positive effects on the electrical characteristics of the 3-level power

30 module, more specifically the quality of the phase output.

In the following, the invention is described by means of exemplary embodiments referring to the attached drawings, in which:

5 Fig. 1a to 1c show a first topography of a 3-level inverter circuit used in embodiments of the invention;

Fig. 2a to 2c show a second topography of a 3-level inverter circuit used in embodiments of the invention;

10 Fig. 3 shows a first embodiment of the invention in a top view;

Fig. 4 shows details of the first embodiment of the invention in a perspective view;

15 Fig. 5 shows a second embodiment of the invention in a top view;

Fig. 6 shows a third embodiment of the invention in a top view;

Fig. 7 shows a bottom view of the first embodiment of the invention;

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Fig. 8 shows three 3-level power modules forming a 3-phase output according to prior art;

25 Fig. 9 shows a perspective view of the third embodiment of the invention and;

Fig. 10 shows a cross-section through the embodiment depicted in fig. 9.

30 In the following detailed description, reference numerals have been added to improve readability. They are in no way meant to be limiting. Furthermore, it should be noted that the invention is not limited to the depicted exemplary embodiments. Additionally, any combination of features described above or

-8-

in the following is possible and may be of importance to the present invention as long as the features combined are not in conflict with each other.

Fig. 1 schematically shows a first topology, thus a circuit arrangement of a 3-level inverter circuit 1, which is used in an embodiment of the 3-level power module according to the invention. This circuit arrangement illustrated in fig. 1a to 1c is known as NPC1 topology. Other designations are "I-Type" or "NPC". The circuit arrangement comprises an upper bridge branch 2, which is arranged between a positive input connection + and a centre tap 0, and a lower bridge branch 3, which is arranged between a negative input connection - and the centre tap 0.

As shown in fig. 1, the upper bridge branch 2 has a first controlled upper semiconductor element T1 and a second controlled upper semiconductor element T2. The lower bridge branch 3 has a first control lower semiconductor element T4 and a second controlled semiconductor element T3. The controlled semiconductor element T1 to T4 can be embodied as transistors, as IGBTs, as MOSFETs or the like. The controlled semiconductor elements T1 to T4 should be able to handle currents having an order of magnitude of 100 A or more.

According to the first topology, a diode D1 is arranged in an antiparallel configuration with the first controlled upper semiconductor element T1 and a diode D2 is arranged in an antiparallel configuration with the second controlled upper semiconductor element D2. A diode D5 is arranged between the centre tap 0 and a point 4 between the two upper controlled semiconductor elements T1, T2, the forward direction of said diode pointing away from the centre tap 0. In the lower bridge branch 5, a first controlled lower semiconductor element T4 and a second controlled lower semiconductor element T3 are arranged between the AC output AC and the negative input connection -. A diode T4 is connected in an antiparallel

configuration with the first lower controlled semiconductor element T4. A diode D3 is connected in an antiparallel configuration with a second lower controlled semiconductor element T3. A diode D6 is arranged between a point 5 between the two controlled lower semiconductor elements T3, T4 and the centre tap 0, the forward direction of said diode D6 being directed towards the centre tap 0.

The controlled semiconductor elements T1 to T4 shown in the first topology are operated as electronic switches. Provision is made for separating the upper bridge branch 2 and the lower bridge branch 3 from one another and for also arranging the respective semiconductor elements of the two bridge branches 2, 3 physically separated, as will be described further below. This division is illustrated in fig. 1b and 1c. Fig. 1b depicts the lower bridge branch 3 while fig. 1c depicts the upper bridge branch 2. The upper bridge branch 2 and the lower bridge branch 3 share the centre tap 0 and the AC output AC, also known as phase output. In other words, it becomes clear that the upper bridge branch 2 comprises two or more groups of controlled upper semiconductor elements connected in parallel to each other and the lower bridge branch 3 comprises two or more groups of controlled lower semiconductor elements connected in parallel to each other. At least two groups of each bridge branch may be distributed over two or more substrates, as will become more clear in view of embodiments of the invention to be described later.

Fig. 2 shows a different topology which may be used in embodiments of the invention, which is referred to as "NPC2" topology. Other designations for this topology, or circuit arrangement, are T-Type, MPC, "mixed voltage NPC" or "bi-directional switch NPC". This topology comprises an upper bridge branch 2, in which a first upper controlled semiconductor element T1 and a second controlled semiconductor element T2 are connected in series between a positive input connection + and an AC output AC. In the upper bridge branch

-10-

2, a diode D1 is arranged in an antiparallel configuration with the first controlled upper semiconductor element T1. A diode D2 is arranged in series with the second controlled lower semiconductor element T2. In a similar manner, in the lower bridge branch 3, a diode D4 is arranged in an antiparallel configuration with a first controlled lower semiconductor element T4 and a diode D3 is arranged in series with the second lower controlled semiconductor element T3. According to his second topology, a division into the lower bridge branch (fig. 2b) and into the upper bride branch (fig. 2c) can be performed and the two bridge branches can also be physically separated from one another, as in the first topology depicted in fig.1.

Fig. 3 now shows a first embodiment of a 3-level multi-phase power module 6 according to the invention in which all components of the circuit, thus the electrical circuit elements, of the 3-level 3-phase power module are placed on a single substrate 7. The 3-level power module 6 comprises a baseplate 8 and a 3-level inverter circuit 1a, the 3-level inverter circuit being arranged on the baseplate 8 and being connected to a phase output connector 9a of the module 6. The 3-level power module 6 further comprises two further 3-level inverter circuits 1b and 1c, each being arranged on the same baseplate 8 and each being connected to a corresponding further phase output connector, 9b and 9c, respectively. The phase output connector 9a as well as the further phase output connectors 9b, 9c may be mounted directly on the baseplate 8 and/or to the substrate 7. The three 3-level inverter circuits 1a to 1c may be of the NPC1 type as shown in fig. 1 or of the NPC2 type as shown in fig. 2. Accordingly, each of the three 3-level inverter circuits 1a to 1c is connected to a DC positive input connector 10a to 10c, a centre tap 11a to 11c and a DC negative input connector 12a to 12c of the module 6, respectively. Thus, the 3-level power module 6 comprises three DC input connectors 10a to 12e per 3-level inverter circuit 1a-1e, respectively. Accordingly, the 3-level power module 6 provides nine DC input connectors 10a to 12e and three phase output connectors 9a to 9c in total. The electrical

-11-

circuit elements of the circuits 1a to 1c connecting the DC input connectors 10a to 12e to the phase output connectors 9a to 9c, respectively, are omitted in this drawing for reason of simplification.

- 5 As shown in fig. 3, the single substrate 7 carries the electrical circuit elements of all of the three 3-level inverter circuits 1a to 1c. Accordingly, the electrical circuit elements of all three of the 3-level inverter circuits 1a to 1c are arranged on the same substrate 7. Thus, the substrate 7 is arranged interposed between the three 3-level inverter circuits 1a to 1c, mounting the
- 10 three 3-level inverter circuits 1a to 1c to the same baseplate 8. As shown, the 3-level inverter circuits are arranged side by side in a linear array. Similarly, the phase output connectors 9a to 9c of each of the 3-level inverter circuits 1a to 1c are arranged in a linear array. Likewise, the DC input connectors of each of the 3-level inverter circuits 1a to 1c are arranged in a linear array.
- 15 Furthermore, the DC input connectors 10a to 12c are arranged in a grouped configuration. As shown, the phase output connectors 9a to 9c are arranged on one side of the baseplate and the DC input connectors 10a to 12c are arranged on an opposing side of the baseplate 8. More specifically, as the baseplate 8 is a rectangular solid copper baseplate, the phase output
- 20 connectors 9a to 9c are arranged along an edge of the base plate 8 opposing the edge along which the DC input connectors 10a to 12c are arranged. In this embodiment, the substrate 7 is a direct bonded copper (DBC) substrate comprising a ceramic core with copper layers on each side of the ceramic core. The copper layer on one side of the ceramic is fixed to the baseplate 8
- 25 of the module 6 and the copper layer on the surface opposite to that facing the baseplate 8 may be divided into separate tracks to comprise the circuitry required for electrical circuit elements mounted on this surface. Mounting holes 13 are arranged along the edges of the baseplate 8. There are eight mounting holes 13 in the present embodiment, four on each long side of the
- 30 baseplate 8. Between each two neighboring mounting holes 13 along one edge, one of the phase output connectors 9a to 9c each is arranged. Along

-12-

the opposite edge, between two neighboring of the mounting holes 13, the three DC input connectors leading to a corresponding 3-level inverter circuit 1a to 1c are arranged in a grouped manner. Thus, the three respective DC input connectors 10a to 12c of each 3-level inverter circuit 1a to 1c are
5 arranged in a grouped manner between two neighboring mounting holes 13.

Fig. 4 shows a perspective view of the finished power module 6 according to the embodiment schematically shown in fig. 3. The power module 6 comprises a frame 14 having recesses for the mounting holes 13. Therefore,
10 the frame 14 partially surrounds each mounting hole 13 radially. The frame 14 is formed from a plastic material. The phase output connectors 9a to 9c and the DC input connectors 10a to 12c are encapsulated in the frame 14. A lid 15 covers the three 3-level inverter circuits 1a to 1c. Connectors 16a to 16c for controlling and monitoring extend from each 3-level inverter circuit 1a
15 to 1c through the lid 15. The mounting holes 13 may be used to enable the baseplate 8 to be fixed to other equipment. Such other equipment may comprise a cooling system (not shown) which cools the bottom of the baseplate 8 (not seen in fig. 4) by the circulation, for example, of a coolant fluid such as air or water.

20

Fig. 5 shows a variation of the embodiment illustrated in fig. 3 and 4. In this embodiment, the individual phase sections, thus the 3-level inverter circuits 1a to 1c, of the module 6 are built on separate substrates 7a to 7c. Accordingly, each substrate 7a to 7c carries electrical circuit elements of one
25 of the 3-level inverter circuits 1a to 1c, respectively. Specifically, each of the three 3-level inverter circuits 1a to 1c is mounted on a separate substrate 7a to 7c, respectively. Each of the substrates 7a to 7c is mounted to the same baseplate 8. Again, the substrate 7a to 7c may be formed from DBC structures. It is sometimes an advantage to use multiple substrates 7a to 7c
30 as shown, instead of a single substrate 7 as in the embodiment of fig. 3 and 4, because temperature induced stresses are more readily dissipated in

smaller substrates 7a to 7c. In the given embodiment, the complete circuit 1 shown in fig. 1a or in fig. 2a may be built on each of the three substrates 7a to 7c. Details regarding the mounting holes 13 and the arrangement of the phase output connectors 9a to 9c and the DC input connectors 10a to 12c are the same as in the first embodiment shown in fig. 3 and 4.

Fig. 6 shows a further variation of the embodiment illustrated in fig. 3 and 4. In this embodiment, each of the individual phase sections, thus the 3-level inverter circuits 1a to 1c, is formed on two separate substrates 7a to 7f. Thus, six substrates in total are used for this 3-phase inverter module 6. Each of the substrates 7a to 7f in this embodiment comprises either a part circuit 2, 3 of fig. 1b or fig. 1c (for the case of the NPC1 topology) or part circuit as shown in fig. 2b or fig. 2c (for the case of the NPC2 topology). Therefore, as an example, the 3-level inverter circuit 1a may comprise the upper bridge branch 2 on substrate 7a and the lower bridge branch 3 on substrate 7b. The two further 3-level inverter circuits 1b, 1c may be designed likewise.

Fig. 7 shows an area on the back side of the baseplate 8. Thus, in this embodiment the three 3-level inverter circuits 1a to 1c are, due to the viewing direction, covered by the baseplate 8. The cross-hatched area will require cooling during use. A known method for cooling is to apply a circulating coolant to the back surface of the baseplate 8. Such coolant may be fluids such as water, which may cause additional problems with they are not retained within the cooling system. Such problems may include unwanted shorting due to the electrically conducting coolant being present in unsuitable portions of the module or longer-term corrosion effects. For this reason, a seal 17 is often used to limit the area of coolant contact with the baseplate 8. This is illustrated by the thick line around the shaded area in fig. 7. Such a seal 17 may be an O-ring structure comprising a rubber or some other elastic material which makes a good seal with a flat baseplate 8.

-14-

Fig. 8 shows prior art power modules 18a to 18c. Three separate power modules 18a to 18c are used to form the 3-level 3-phase inverter. For example, each of the prior art power modules 18a to 18c may comprise a single 3-level inverter circuit 1. Thus, each of the prior art 3-level power modules 18a to 18c comprises a phase output connector (not shown in fig. 8). As shown in this illustration, the total area used for mounting the inverter is substantially larger than the single baseplate 8 solution of the current invention, as may be seen when comparing fig. 8 to fig. 7. Also illustrated here is the fact that the three separate prior art modules 18a to 18c require three separate cooling areas and three separate peripheral seals 17a to 17c. The total length of the peripheral seal 17a to 17c, for example an O-ring structure, is substantially greater than that needed in fig. 7.

Fig. 9 shows a perspective view of the inventive power module 6 in which the substrates 7a to 7f of the embodiment shown in fig. 6 are seen. The broken lines show the extent of each of the six substrates 7a to 7f. Thus, at least two groups of each bridge branch 2, 3 are distributed over two substrates 7a to 7f. Thus, for example, the upper bridge branch 2, as depicted in fig. 1c or fig. 2c may be arranged on substrate 7a while the lower bridge branch 3, shown in fig. 1b or fig. 2b, may be arranged on substrate 7b, the two branches 2, 3 together forming the 3-level inverter circuit 1a. As comes clear from fig. 9, all three 3-level inverter circuits 1a to 1c are arranged side by side in a linear array. Three phase output connectors 9a to 9c are provided by the 3-level power module 6, each connected to one corresponding of the inverter circuits 1a to 1c.

Finally, fig. 10 is a cross-section through the inventive module 6 shown in fig. 9. The cross-section is visualized the plane X-X in fig. 9. Fig. 10 illustrates how the module 6 is built up. In addition to the baseplate 8 and the DBC substrate 7 which is attached to the baseplate 8, the phase output connector 9c and the DC input connectors 11c, 12c are shown. Connectors 16a to 16c

-15-

for control and/or monitoring are shown extending from the upper surface of the DBC substrate 7e to the outside of the module 6. The top of the module 6 is closed with the lid 15.

- 5 As described above, the 3-level power module 6 comprising the baseplate 8, the 3-level inverter circuit 1a, the 3-level inverter circuit 1a being arranged on the baseplate 8, and a phase output connector 9a becomes very compact when the 3-level power module 6 further comprises one or more further 3-level inverter circuits 1b, 1c, each being arranged on the baseplate 8 and
- 10 connected to a corresponding further phase output connector 9b, 9c of the module 6.

Claims

1. A 3-level power module comprising a baseplate, a 3-level inverter circuit, the 3-level inverter circuit being arranged on the baseplate, and a phase output connector, the 3-level power module further comprising one or more further 3-level inverter circuits, each being arranged on the baseplate and each being connected to a corresponding further phase output connector of the 3-level power module.
2. The 3-level power module according to claim 1, comprising one or more substrates arranged on the baseplate, each substrate carrying electrical circuit elements of one or more of the 3-level inverter circuits.
3. The 3-level power module according to claim 2, wherein electrical circuit elements of two or more of the 3-level inverter circuits are arranged on the same substrate.
4. The 3-level power module according to claim 2 or 3, wherein electrical circuit elements of one or more of the 3-level inverter circuits are distributed over two or more substrates.
5. The 3-level power module according to any of the claims 1 to 4, wherein the 3-level inverter circuits are arranged side by side in a linear array, the 3-level power module providing three phase output connectors.
6. The 3-level power module according to any of the claims 1 to 5, wherein the phase output connectors are arranged on one side of the baseplate and DC input connectors are arranged on an opposing side of the baseplate.
7. The 3-level power module according to any of the claims 1 to 6, wherein the phase output connectors and DC input connectors are arranged in a linear array and/or in a grouped configuration, respectively.

8. The 3-level power module according to any of the claims 1 to 7, wherein one or more of the 3-level inverter circuits comprise an upper bridge branch, which is arranged between a positive input connection and a centre tap, and a lower bridge branch, which is arranged between a negative input connection and the centre tap, wherein the upper bridge branch comprises two or more controlled upper semiconductor elements and the lower bridge branch comprises two or more controlled lower semiconductor elements.
9. The 3-level power module according to claim 8, wherein the upper bridge branch comprises two or more groups of controlled upper semiconductor elements connected in parallel to each other and the lower bridge branch comprises two or more groups of controlled lower semiconductor elements connected in parallel to each other.
10. The 3-level power module according to claim 9, wherein at least two groups of each bridge branch are distributed over two or more substrates.

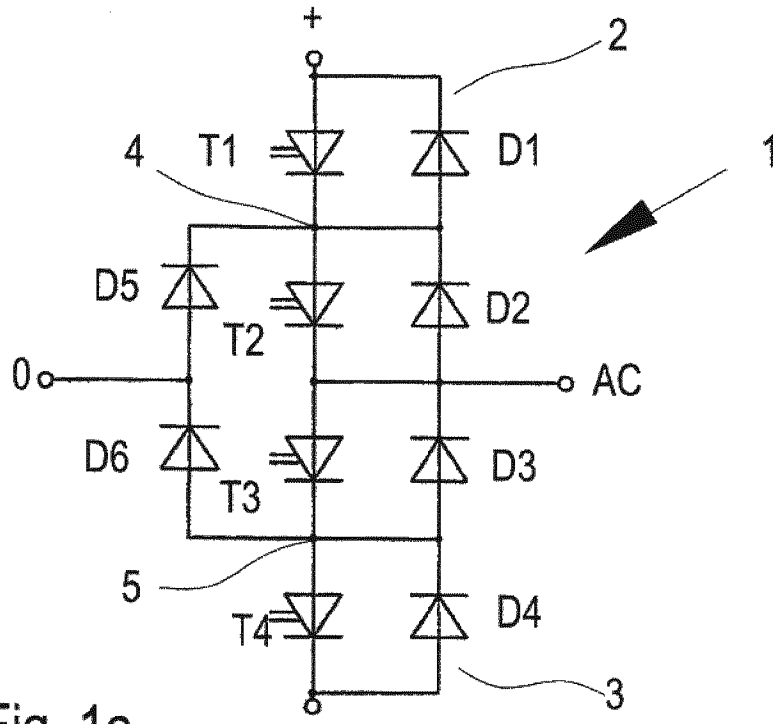


Fig. 1a

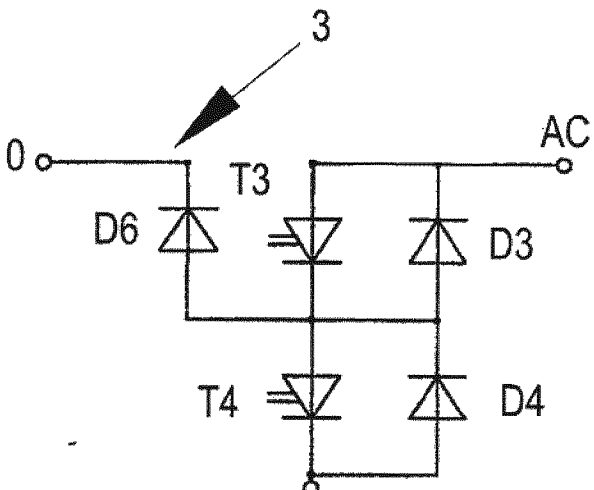


Fig. 1b

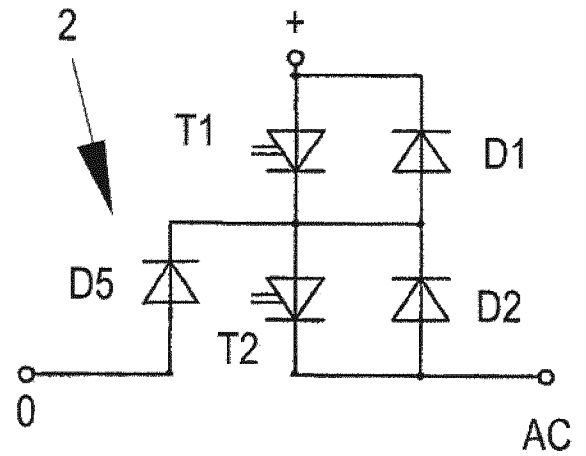


Fig. 1c

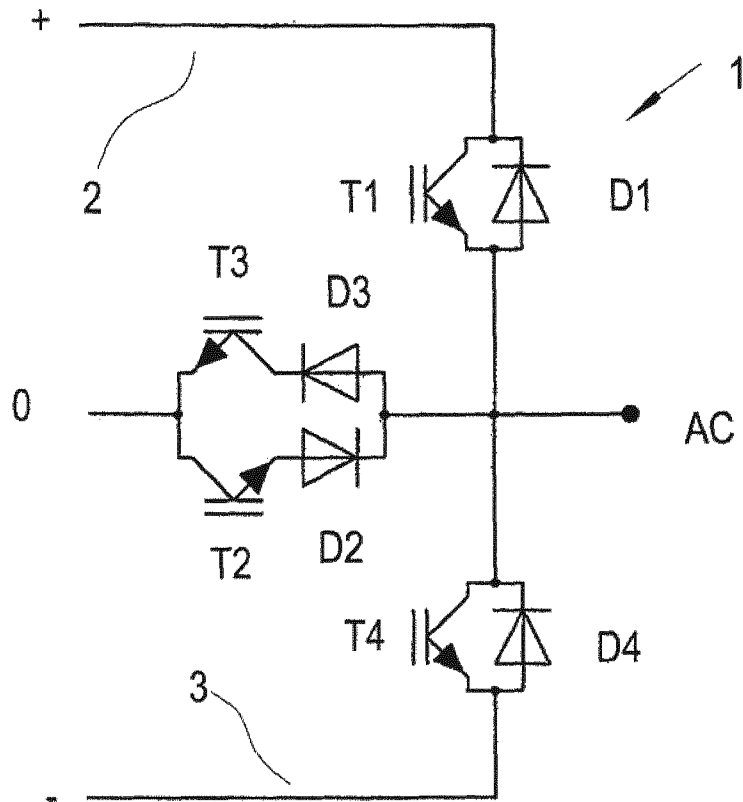


Fig. 2a

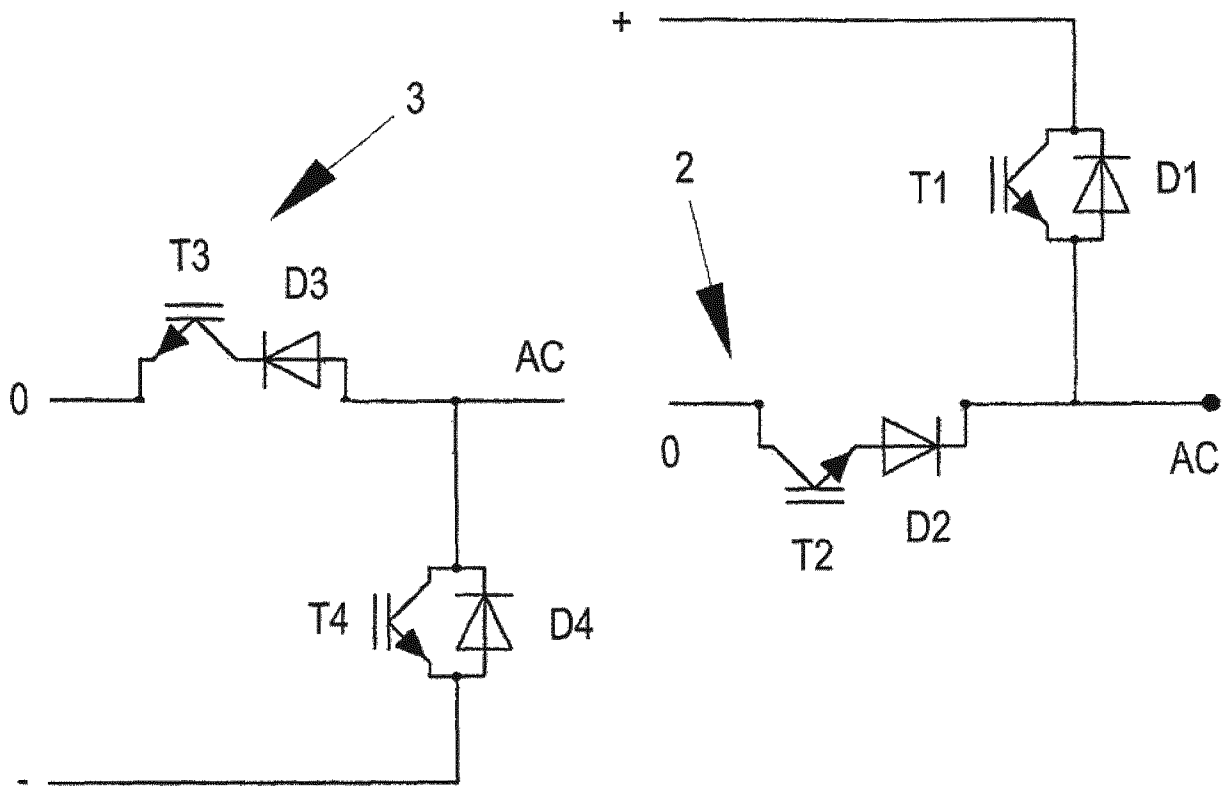


Fig. 2b

Fig. 2c

Fig. 3

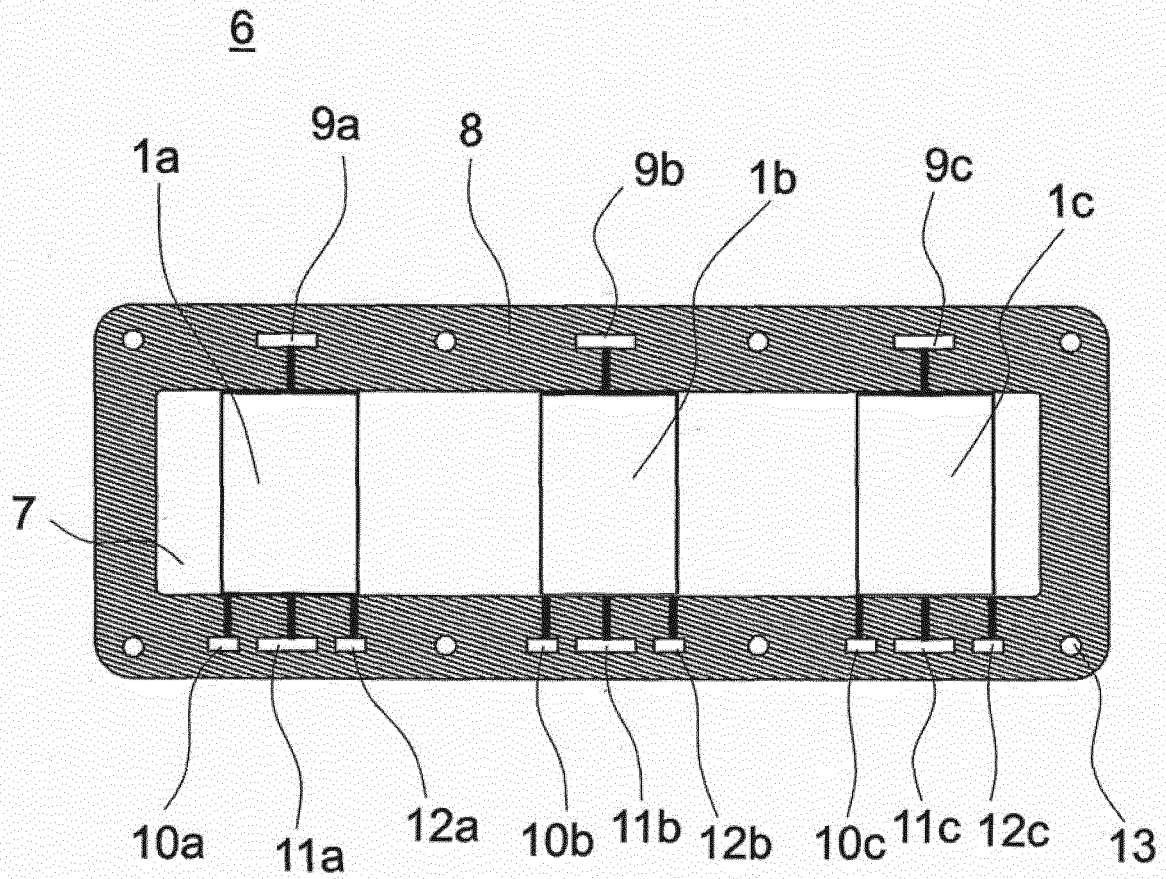


Fig. 4

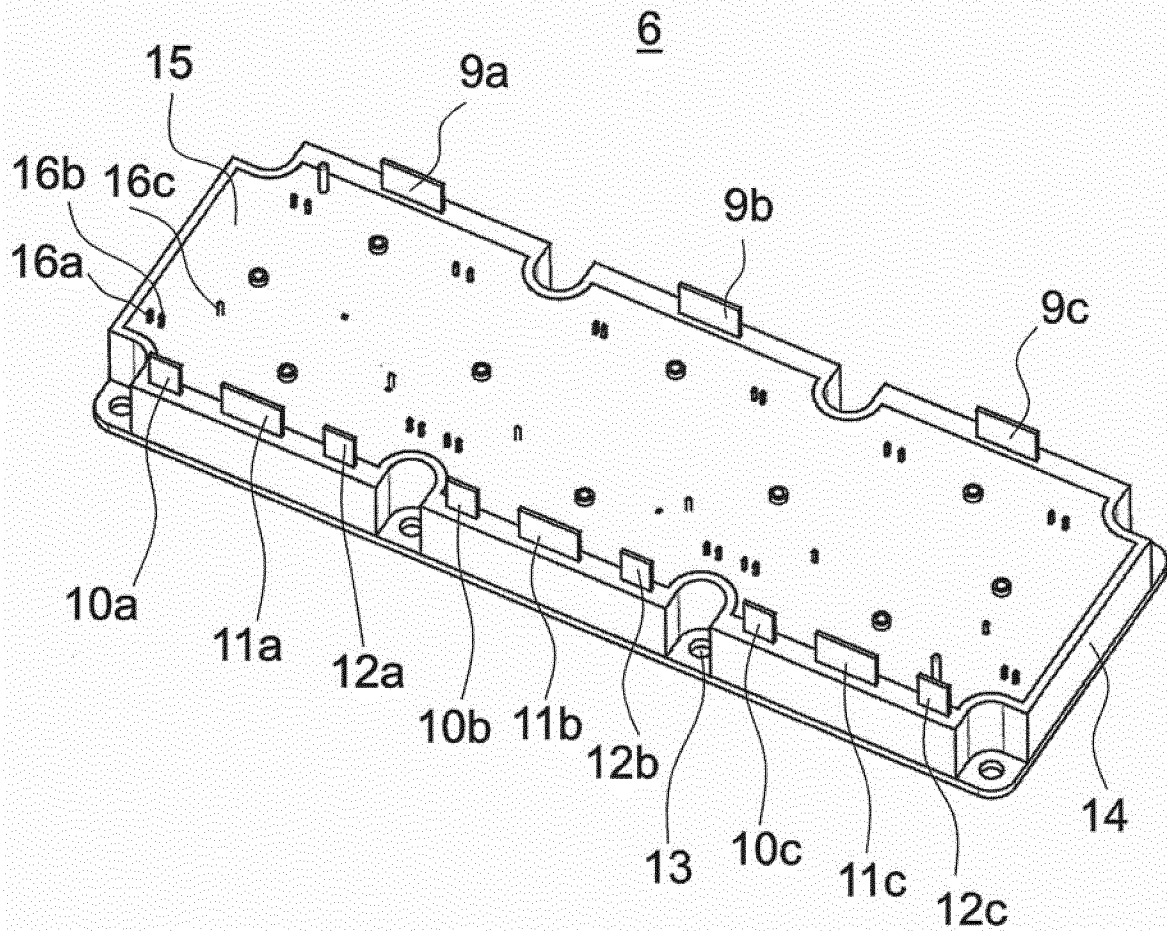


Fig. 5

6

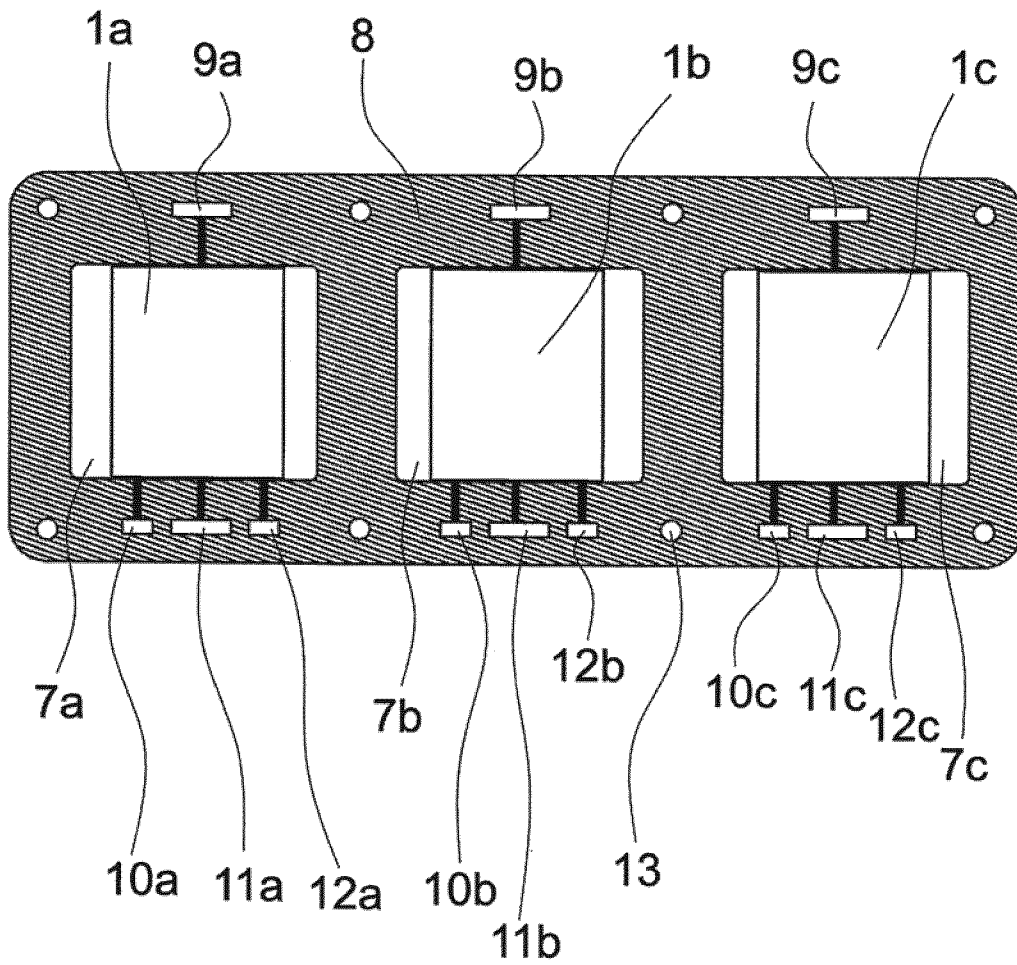


Fig. 6

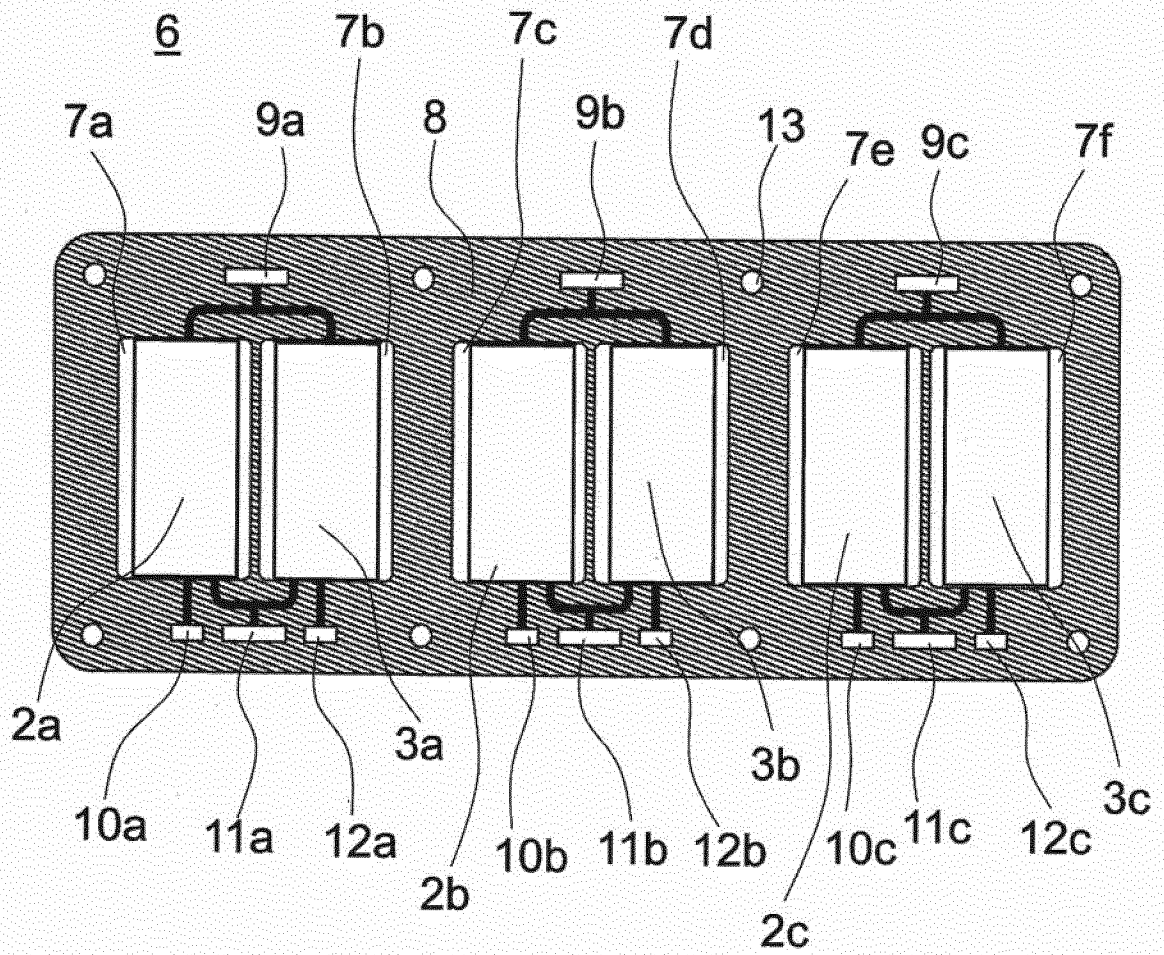


Fig. 7

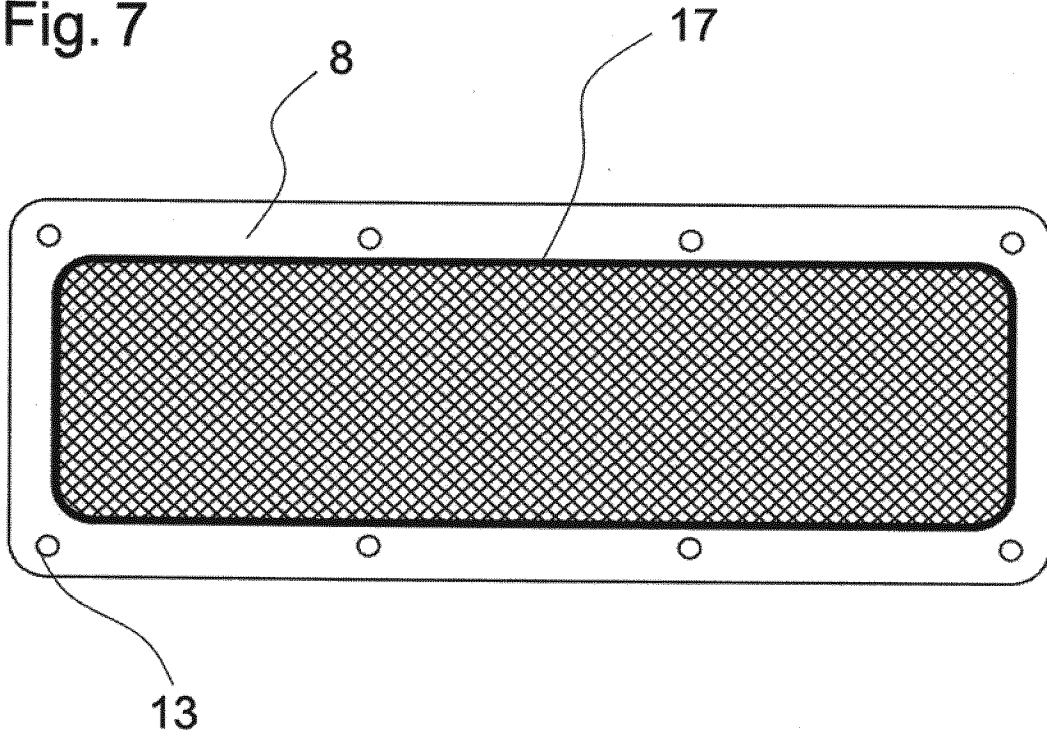


Fig. 8

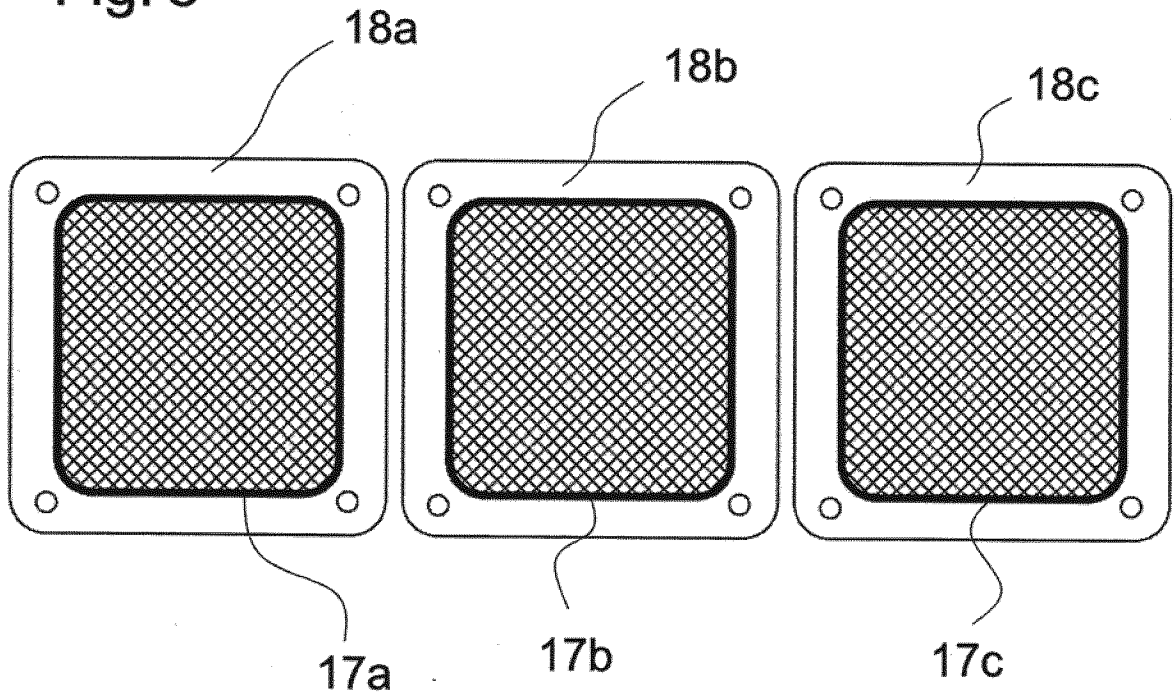
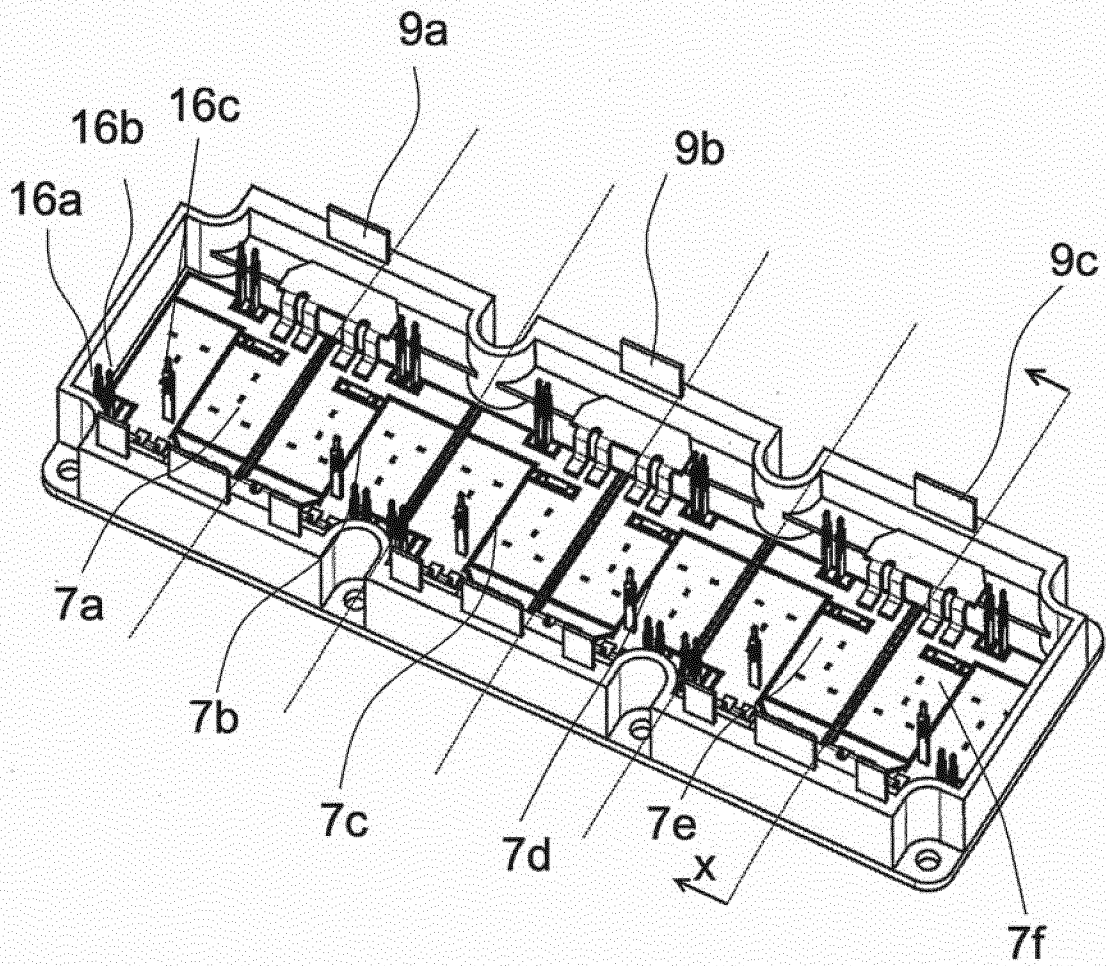
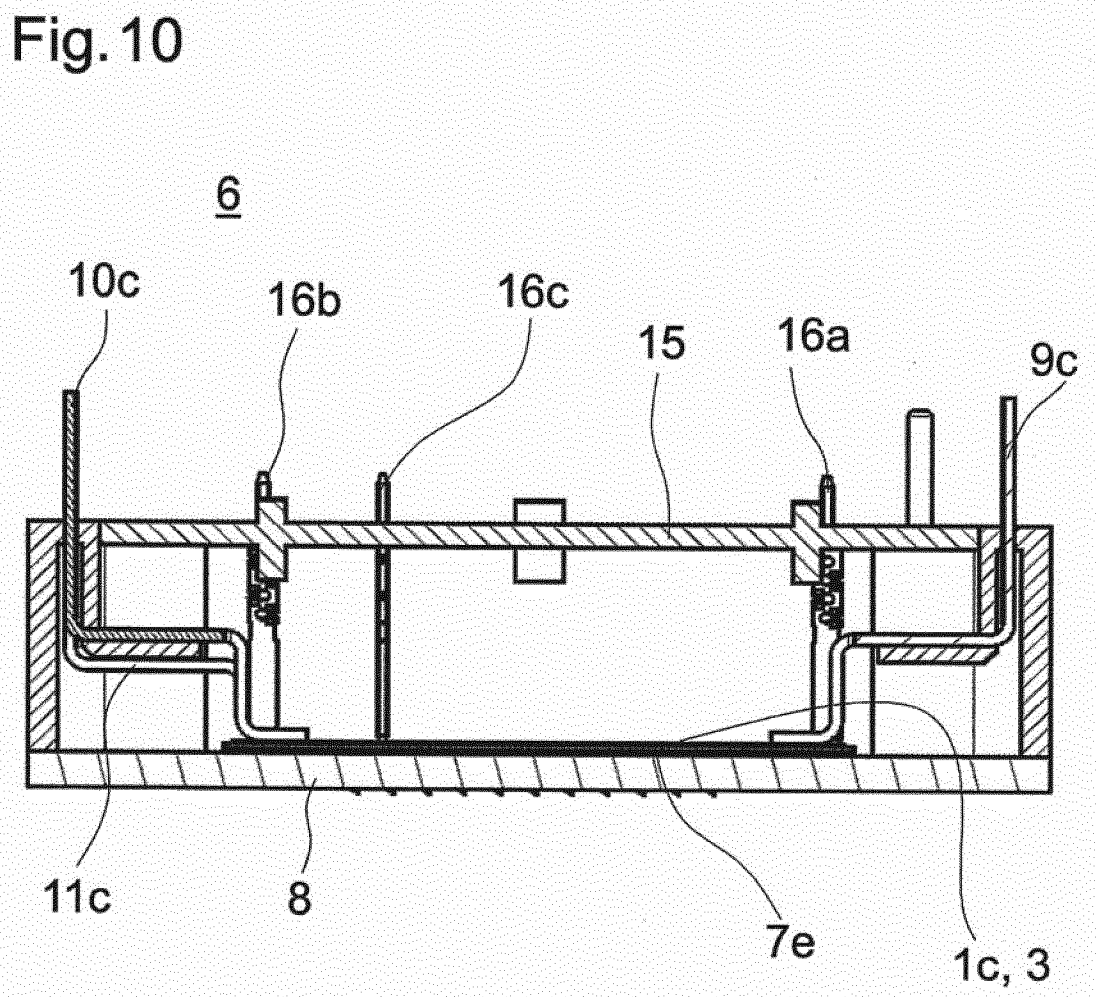


Fig. 9





INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/056093

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H02M7/00
 ADD. H02P27/14 H02M7/483 H02M7/487

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H02M H02P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2014/111959 A1 (LI YAN [TW] ET AL) 24 April 2014 (2014-04-24) the whole document in particular: paragraph [0091]; figure 9B paragraphs [0103] - [0106]; figures 11A,11B	1-10
A	----- WO 2016/140008 A1 (FUJI ELECTRIC CO LTD [JP]) 9 September 2016 (2016-09-09) abstract & US 2017/179095 A1 (AMI HIDEO [JP]) 22 June 2017 (2017-06-22) Cited for language reasons only. paragraphs [0077], [0078], [0108] figures 5,6 claims 1,11,12 ----- -/--	3

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See patent family annex.

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Date of the actual completion of the international search 18 May 2018	Date of mailing of the international search report 01/06/2018
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Standaert, Frans

INTERNATIONAL SEARCH REPORT

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