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(54) Title: METHODS TO FORM WIDE HEATER TRENCHES AND TO FORM MEMORY CELLS TO ENGAGE HEATERS

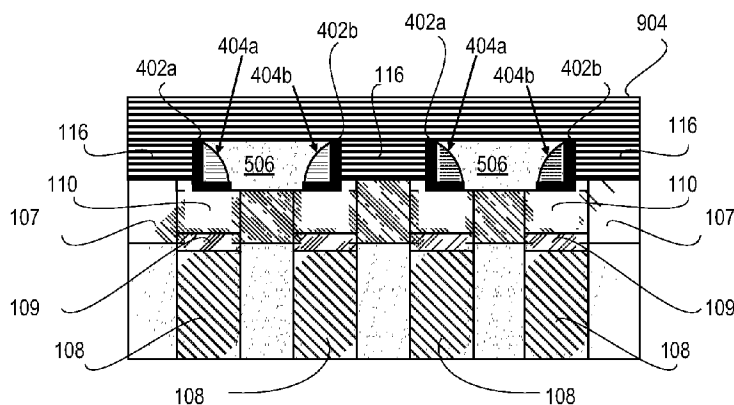


Figure 8

(57) Abstract: Embodiments of the present invention, provide a method that includes providing a wafer including multiple cells, each cell including at least one emitter (108), and performing a lithographic operation on the wafer. The lithographic operation comprises forming heater trenches adjacent the emitters, each heater trench having a width that extends over at least respective portions of two cells. Embodiments of the present invention also provide a method that includes providing wafer including multiple cells, each cell including at least one emitter. The method further includes performing a lithographic operation in a word line direction of the wafer across the cells to form pre-heater element arrangements, performing a lithographic operation in a bit line direction of the wafer across the pre-heater element arrangements to form a pre-heater element adjacent each emitter, and performing a lithographic operation in the word line direction across a portion of the pre-heater elements to form a heater element (402a, 402b) adjacent each emitter. Other embodiments are also described.



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METHODS TO FORM WIDE HEATER TRENCHES AND TO FORM MEMORY CELLS TO ENGAGE HEATERS

Cross Reference to Related Applications

5 The present application claims priority to U.S. Patent Application No. 60/910,240, filed April 5, 2007, entitled "Wide Trench PCM to Heater Contact dx dy," U.S. Patent Application No. 60/910,389, filed April 5, 2007, entitled "Wide Trench PCM Heater dx dy," and U.S. Patent Application No. 60/909,813, filed April 3, 2007, entitled "Method to Form High Efficiency GST Cell with Double
10 Heater Cut," the entire specifications of which are hereby incorporated by reference in their entirety for all purposes, except for those sections, if any, that are inconsistent with this specification.

Technical Field

15 Embodiments of the present invention relate to the field of electronic memory devices, and more particularly, to phase change material (PCM) memory devices and methods for fabricating thereof.

Background

20 Memory cells of electronic memory devices such as dynamic random access memory typically employ a number of electronic components in order to save data. For instance, in order to store data, a combination of electronic components such as transistors, diodes, and/or capacitors are typically employed in such memory cells to store or not store electrical charges. If a charge is stored
25 in such a memory cell, that may indicate a logic "1," and if no charge is stored in such a memory cell that may indicate a logic "0."

 An alternative approach for storing data is to use memory cells made of phase change material (PCM). A PCM is a material that can be placed into at least two physical states, a crystalline state and an amorphous state, by
30 increasing or decreasing temperature. By changing the physical state of the PCM, certain characteristics of the material, such as electrical resistance, may also change. Such properties may be exploited in order to form memory cells made of PCM (herein "PCM cells").

Such memory cells are generally intricate and expensive to manufacture. Thus, it is important to manufacture them in such a way to ensure accuracy and reliability such that few memory cells are wasted. One concern involves the contact between a heater element and the PCM. Since it is undesirable to heat
5 up the PCM, it is desirable to have a small contact between the PCM and the heater element. It is also desirable to manufacture the cells in such a way that ensures quality but that is also efficient and economical.

Summary

10 In accordance with various embodiments of the present invention, a method includes providing a wafer including multiple cells, each cell including at least one emitter, and performing a lithographic operation on the wafer. The lithographic operation comprises forming heater trenches adjacent the emitters, each heater trench having a width that extends over at least respective portions
15 of two cells.

In accordance with various embodiments, the lithographic operation is performed in a word-line direction across the wafer. In accordance with other embodiments, the lithographic operation is performed in a bit-line direction across the wafer.

20 In accordance with various embodiments, the lithographic operation further comprises depositing a heater alloy layer within each heater trench and depositing a nitride layer over the heater alloy layer. The lithographic operation also includes performing an anisotropic etching of the nitride layer and the heater alloy layer and depositing an oxide layer over the nitride layer to form a pre-
25 heater element arrangement within each heater trench.

In accordance with various embodiments, the method further includes performing another lithographic operation across the wafer across the pre-heater arrangements to form two heater elements within each heater trench.

30 In accordance with various embodiments, the method further comprises performing a third lithographic operation comprising depositing a nitride layer over the heater elements and etching trenches within the second nitride layer, depositing germanium antimony tellurium (GST) material within the trenches and performing an anisotropic etching of the GST material.

In accordance with various embodiments, each trench has a width that extends over at least a portion of one cell. In accordance with other embodiments, each trench has a width that extends over at least a portion of two cells.

5 In accordance with various embodiments, the method further comprises forming a top emitter interface on the GST material for at least one emitter.

In accordance with various embodiments, the method further comprises performing a metallization such that a metal protective layer is provided on a top surface of the top emitter interface. In accordance with such embodiments, the
10 metallization may be performed with tungsten.

In accordance with various embodiments, each heater element comprises one of TiN or TaN.

In accordance with various embodiments of the present invention, a method comprises providing a wafer comprising multiple cells, where each cell
15 comprises a heater element and a nitride layer over the heater element. The method further comprises forming a trench within the nitride layer, where the trench has a depth such that a portion of the heater element is exposed. The method further comprises depositing GST material within the trench and performing an anisotropic etch of the GST material to form a memory cell
20 adjacent to the portion.

In accordance with various embodiments, the trench has a width that extends over at least a portion of one cell. In accordance with other embodiments, the trench has a width that extends over at least respective portions of two cells and has a depth such that the portion of the respective
25 heater element of the two cells is exposed.

In accordance with various embodiments of the present invention, an apparatus comprises a substrate comprising multiple cells, where each cell comprises at least one emitter within an emitter layer. The apparatus further comprises a heater trench adjacent to the emitter layer. The heater trench has a
30 width that extends over at least respective portions of two cells.

In accordance with various embodiments, the apparatus further comprises heater elements within the heater trench. A heater element is adjacent the at least one emitter and has a substantially L-shape.

In accordance with various embodiments of the present invention, each heater element comprises one of TiN or TaN.

In accordance with various embodiments, a top emitter interface is included on a memory cell. In accordance with various embodiments, the top emitter interface comprises tungsten. In accordance with further embodiments, the memory cell comprises GST. In accordance with various embodiments of the present invention, a method includes providing wafer including multiple cells, each cell including at least one emitter. The method further includes performing a lithographic operation in a first direction of the wafer across the cells to form pre-heater element arrangements, performing a lithographic operation in a second direction of the wafer across the pre-heater element arrangements to form a pre-heater element adjacent each emitter, and performing a lithographic operation in the first direction across a portion of each pre-heater elements to form a heater element adjacent each emitter.

In accordance with various embodiments, each heater element may comprise one of titanium nitride (TiN) or tantalum nitride (TaN).

In accordance with various embodiments, the method further includes depositing a heater seal layer adjacent to the heater elements.

In accordance with various embodiments, the method further includes performing a lithographic operation in the second direction to create a micro trench across each cell such that each heater element is exposed.

In accordance with various embodiments, the method further includes depositing germanium antimony tellurium (GST) material within each micro trench.

In accordance with various embodiments, the method further includes forming a top emitter interface on the GST material for at least one emitter.

In accordance with various embodiments, the method further includes performing a metallization such that a metal protective layer is provided on a top surface of at least one top emitter interface. In accordance with such embodiments, the metallization may be performed with tungsten.

In accordance with various embodiments, the first direction is a word line direction and the second direction is a bit line direction.

The present invention also provides an apparatus including a substrate comprising an emitter layer and at least one emitter within the emitter layer, and a

heater element adjacent each emitter and having a substantially squared U-shape, wherein a first portion of the U-shape is shorter than a second portion of the U-shape.

5 In accordance with various embodiments, the first portion is substantially flush with a bottom portion of the substantially squared U-shape.

In accordance with various embodiments, each heater element may comprise one of TiN or TaN.

In accordance with various embodiments, the apparatus further includes a memory cell adjacent the second portion.

10 In accordance with various embodiments, the apparatus may further include a top emitter interface on the memory cell. In accordance with such embodiments, a top surface of the top emitter interface may comprise tungsten.

In accordance with various embodiments, the memory cell may comprise GST.

15

Brief Description of the Drawings

Embodiments of the present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments of the invention are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

20 Figures 1 and 2 are cross sectional schematic views of a substrate after various operations, in accordance with various embodiments of the present invention;

25 Figure 3 is a top schematic view of the substrate illustrating a lithographic operation, in accordance with various embodiments of the present invention;

Figure 4 is cross sectional schematic view of the substrate after the lithographic operation of Figure 3, as seen along the line A-A' of Figure 3, in accordance with various embodiments of the present invention;

30 Figure 5 is a top schematic view of the substrate illustrating lithographic operations, in accordance with various embodiments of the present invention;

Figures 6-8 are cross sectional schematic views of the substrate after the lithographic operations of Figures 3 and 5, as seen along the line A-A' of Figure 6, in accordance with various embodiments of the present invention;

Figures 9-14 are cross sectional schematic views of the substrate, as seen along the line C-C' of Figure 5, in accordance with various embodiments of the present invention;

Figure 15 is a top schematic view of the substrate illustrating a lithographic operation, in accordance with various embodiments of the present invention;

Figure 16 is cross sectional schematic view of the substrate after the lithographic operation of Figure 15, as seen along the line A-A' of Figure 15, in accordance with various embodiments of the present invention;

Figures 17 and 18 are top schematic views of the substrate illustrating lithographic operations, in accordance with various embodiments of the present invention;

Figure 19 and 20 are cross sectional schematic views of the substrate after the lithographic operations of Figures 17 and 18, as seen along the line A-A' of Figure 6, in accordance with various embodiments of the present invention;

Figure 21 is a top schematic view of the substrate illustrating a lithographic operation, in accordance with various embodiments of the present invention;

Figures 22 and 23 are cross sectional schematic views of the substrate after the lithographic operation of Figure 21, as seen along the line C-C' of Figure 21, in accordance with various embodiments of the present invention; and

Figure 24 a top schematic view of the substrate after at least some of the lithographic operation of Figure 21, in accordance with various embodiments of the present invention.

Detailed Description of Embodiments of the Invention

In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments in accordance with the present invention is defined by the appended claims and their equivalents.

Various operations may be described as multiple discrete operations in turn, in a manner that may be helpful in understanding embodiments of the present invention; however, the order of description should not be construed to imply that these operations are order dependent.

5 The description may use perspective-based descriptions such as up/down, back/front, and top/bottom. Such descriptions are merely used to facilitate the discussion and are not intended to restrict the application of embodiments of the present invention.

 For the purposes of the present invention, the phrase "A/B" means A or B.
10 For the purposes of the present invention, the phrase "A and/or B" means "(A), (B), or (A and B)". For the purposes of the present invention, the phrase "at least one of A, B, and C" means "(A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C)". For the purposes of the present invention, the phrase "(A)B" means "(B or (AB))" that is, A is an optional element.

15 The description may use the phrases "in an embodiment," or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present invention, are synonymous.

20 Embodiments of the present invention provide an ultra high density (UHD) phase change memory (PCM) apparatus and methods for fabricating the same.

 Referring to Figure 1, a memory cell area may be formed beginning with a memory cell area lithograph operation (Clear Tone Mask) that is performed on a silicon vapor substrate 101. A collector doping operation is performed to create a
25 P+ collector region 102, followed by a base doping operation to create an N base region 104. Next, a shallow trench isolation (STI) lithographic operation is performed including etching and filling trenches 106 with oxide. This generally completes the memory cell area and thus, a chemical mechanical planarization (CMP) operation may be performed to smooth the various areas of the substrate
30 101.

 Referring to Figure 2, an interlayer dielectric deposition (ILD) may then be performed with, for example, oxide, followed by an emitter lithographic formation. The area 100 may then be etched in order to open emitter areas (where the emitters 108 will subsequently be formed) and form ILD regions 107. High

temperature silicon germanium (SiGe) is Epi (epitaxial) formed in the emitter areas in order to fill up the emitter areas with P+ SiGe and thereby form the emitters. If needed, a CMP operation may be performed to smooth the surface. In accordance with various embodiments, this Epi step may be skipped if desired
5 and emitters 108 may simply be silicon.

A base lithographic operation may then be performed for memory area opening and ion metal plasma (IMP) is provided to the base 104. It is desirable to insure that the IMP N+ covers the base pick-up. This may be followed by another emitter lithographic operation and IMP to the emitters 108. This is done
10 to help ensure that the base 104 and emitters 108 maintain the proper level of doping after the SiGe Epi formation.

In accordance with various embodiments of the present invention, a silicidation may be performed in order to deposit silicide at regions 109. The silicidation may include depositing a layer of, for example, nickel or cobalt. The
15 layer is then etched resulting in regions 109. This may be skipped if emitters 108 are silicon as opposed to Epi grown SiGe. A metallization may be performed to place a protective layer 110 of metal, for example tungsten, on the silicide regions 109 or directly on emitters 108 if the silicidation is skipped.

In accordance with various embodiments of the present invention, an
20 interlayer dielectric layer 112 may then be deposited. This layer 112 is then etched over the emitters 108 until the silicide layer 109 is reached (if included) or until the emitter 108 is reached (if the silicide layer is not included). A metallization step may then be performed to fill the etched trenches with a protective layer 110 of tungsten. A CMP may then be performed to smooth and
25 flatten the tungsten and ILD layers 110, 112. A layer 116 of nitride (Si_3N_4) may be deposited and a CMP may be performed if needed.

Referring to Figures 3 and 4, a lithographic operation 300 may be performed in order to form a heater trench 400, in accordance with various embodiments of the present invention. Figure 13 is a top view of a wafer that
30 includes multiple cells 100 that have been previously described. Figure 14 is a cross-sectional view through four cells as seen along the line A-A'.

The lithographic operation 300 includes etching heater trench 400 through the nitride layer 116. As may be seen in Figures 13 and 14, the heater trench 1400 extends across at least a portion of two cells. The heater trench 1400 is

etched such that it has a depth that extends into tungsten and ILD layers 110, 112.

A layer of heater alloy, for example, TiN or TaN, may then be conformally deposited within the heater trenches. A layer of nitride is then deposited over the heater alloy layer.

As may be seen in Figure 3, the lithographic operation 300 is illustrated as being performed in a word-line direction W across the wafer. Those skilled in the art will understand that the operation 300 may be performed in a bit-line direction B if desired.

Referring to Figures 5-8, an anisotropic etch of the heater trenches 400 is then performed. This removes portions of both the nitride and heater alloy layers that are planar, thus separating the heater alloy layer into two pieces 402a, 402b, as may be seen in Figure 6. Thus, the heater alloy layer is now divided into two pre-heater element arrangements, where the pre-heater element arrangements also include nitride spacers 404a, 404b. In accordance with various embodiments, a layer 506 of oxide is deposited within the heater trenches 400. A CMP operation may then be performed to smooth the nitride and oxide layers 116, 506. The CMP process is performed until the vertical leg 403 of the heater alloy pieces 402a, 402b are exposed.

In accordance with various embodiments of the present invention, a lithographic operation is performed in the bit-line direction in order to cut across the pre-heater element arrangements to thereby form the heater alloy layers into heater elements. As may be seen in Figures 6-8, the heater elements 402a, 402b are substantially L-shaped. If the lithographic operation 300 was performed in the bit-line direction, then this second lithographic operation would be performed in the word-line direction across the wafer. A layer 904 of nitride may then be deposited.

Figures 9-11, in accordance with various embodiments of the present invention, a lithographic operation in the bit-line direction B may be performed on the layer 904 of nitride in order to create a trench 900 and to expose the vertical leg of the heater elements 402a, 402b for contact with a PCM portion, which will serve as a memory cell. The resulting exposure of heating elements 402a, 402b within trench 900 is relatively small. Thus, contact of heating elements 402a,

402b with GST material 902 will be small. In accordance with various embodiments, the trench side walls 900a, 900b may be sloped.

In accordance with various embodiments, the PCM material is germanium antimony tellurium (GST) material that is conformally deposited within the trench 900. in accordance with various embodiments, a top electrode layer 908 may be deposited on top of the GST material. Examples of material for the top electrode layer 908 include Ti, Ta, TiN and TaN. An anisotropic etch is then performed, leaving a thin layer 902a of GST material on the side wall 900a of the trench 900. Nitride 906 may then be deposited into the trench to fill it up. Alternatively, an
10 ILD may be performed in order to fill up the trench. A CMP is then performed to smooth the surface and to expose the GST material. If desired, the CMP process may be performed until a desired width of the GST material is exposed.

In accordance with various embodiments, a lithographic operation may be performed in the bit-line direction B on layers 902 and 908 in order to create GST
15 columns. An anisotropic etch is then performed, leaving a thin layer 902a and 902b of GST material on the surface and inside the trench 900. A metallization may also be performed if desired to provide a protective layer of metal such as, for example, tungsten, over the top electrode 908. The protective layer may serve as a top emitter interface.

Referring to Figures 12-14, the trench 900 may be etched such that it extends across a portion of two cells and thus, exposes two adjacent heater element legs. A layer of GST material may then be conformally deposited within the trench and an anisotropic etch is performed leaving a thin layer 902a, 902b of GST material on each side wall 900a, 900b of the trench 900. As may be seen,
25 each side wall 900a, 900b is adjacent an exposed leg of the heater elements 402a, 402b. A nitride layer 906 may then be deposited to fill up the trench between the two thin layers of the GST material or alternatively, an ILD may be performed in order to fill up the trench 900. A CMP process may then be performed to smooth the layers and expose the GST material 902a, 902b. A top
30 electrode and protective layer may be provided on each GST portion if desired.

Referring to Figures 15 and 16, in accordance with various embodiments of the present invention, other processes of creating heater elements may be presented. Figure 15 schematically illustrates a wafer 1300 including multiple cells 100 as previously described. Each cell includes at least one emitter. As an

example, four emitters are labeled as 1302, 1304, 1306 and 1308. The word line direction is indicated by W. A column trench lithograph operation 1301 may be performed in a word line direction. Figure 16 is a cross sectional view of emitter 1302 as seen along the line A-A'.

5 In accordance with various embodiments, prior to the column trench lithograph operation, a layer of oxide 1400 is deposited. The column trench is then etched, stopping at the silicided region 109 of the emitter 108. While not illustrated, a metal layer, such as Tungsten layer 110, may be included over silicided region 109 if desired and as previously described. A thin layer of silicon
10 nitride (Si_3N_4) may then be deposited and an anisotropic etch of the Si_3N_4 layer is then performed in order to remove a portion of the Si_3N_4 layer, but preserve the side wall Si_3N_4 in the heater trench in order to provide a heater seal 1402.

A heater alloy layer 1404, for example, titanium nitride (TiN) or tantalum nitride (TaN) may then be deposited. A thin layer 1406 of Si_3N_4 is then deposited
15 over the heater alloy layer 404 in order to provide a second heater seal. A layer 1408 of oxide is then deposited. Isotropic etching of the Si_3N_4 layer 406 may then be performed. A CMP operation may be performed in order to remove oxide until Si_3N_4 layer 1406 is exposed. The layers 1404, 1406 and 1408 thus form a pre-heater element arrangement. As may be seen in Figure 16, the heater alloy
20 layer 1404 has a substantially squared U shape.

Referring to Figure 17, a lithographic operation 1500 may then be performed in a bit line direction B across the wafer 1300. This lithographic operation cuts across cells 100 and the pre-heater element arrangements in the bit line direction to form pre-heater elements. The pre-heater elements still have
25 the same shape and appearance as the pre-heater element arrangement of layers 1404, 1406 and 1408 as seen in Figure 16.

Referring to Figures 18 and 19, in accordance with various embodiments, a lithographic operation 1600 is performed across the wafer 1300 in a word line direction W in order to complete formation of heater elements 1700. As may be
30 seen in Figure 18, this operation is performed "offset" with respect to the emitters. Thus, a first portion or leg 1702 of heater alloy layer is etched such that it is shorter than a second portion or leg 1704. Ideally, the leg 1702 will be etched such that it is substantially flush with a bottom portion 1706 of the heater alloy

layer 1704. Figure 19 is a cross sectional view of emitter 1302 as seen along the line A-A'.

Referring to Figure 20, a layer 1802 of Si_3N_4 may now be deposited in order to replace the removed portion of heater alloy layer 404 and any portions of Si_3N_4 1406 and the Si_3N_4 heater seal 1402 that were removed. A CMP process may then be performed in order to smooth layer 1802.

In accordance with various embodiments, referring to Figures 21, 22 and 23, a lithographic operation 1900 in the bit line direction B may be performed on the layer 1802 of Si_3N_4 in order to expose the leg 1604 for contact with GST material portion 1902. In accordance with the various embodiments, the lithographic operation 1900 is performed in order to create a micro trench 1904 having a reasonable slope on the sides of the trenches 1904a, 1904b of approximately 30 to 40 degrees relative to a vertical line. Figures 22 and 23 are cross sectional views of emitter 1302 as seen along the line C-C'.

As may be seen in Figure 22, the resulting exposure of the leg 1604 of heating element 1700 within micro trench 1904 is relatively small. Thus, contact of heating element 1700 with GST material 1902 will be small.

Referring again to Figure 23, GST material 1902 may then be deposited within the micro trenches. If the surface of the GST material 1902 is not flat, a CMP operation may be performed. A top electrode 1906 may then be deposited for the GST material 1902. Examples of material for the top electrode include Ti, Ta, TiN and TaN. Finally, a lithograph and etching operation is performed for the GST material 1902 and top electrode 1906 within the micro trenches. In accordance with the various embodiments, a thin layer of Si_3N_4 is deposited and then etched in order to provide a GST seal 1908. A deposition of oxide 1910 is provided in order to provide over-GST dielectric. If the surface of oxide 1910 is not as flat as desired, a CMP operation may be performed. A lithographic and etching operation is performed in order to provide the top emitter contact 1912 on the GST material 1902. In accordance with various embodiments, this operation is a metallization and the top contacts are formed from Tungsten.

Although certain embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent embodiments or implementations calculated to achieve the same purposes may

be substituted for the embodiments illustrated and described without departing from the scope of the present invention. Those with skill in the art will readily appreciate that embodiments in accordance with the present invention may be implemented in a very wide variety of ways. This application is intended to cover
5 any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that embodiments in accordance with the present invention be limited only by the claims and the equivalents thereof.

Claims

What is claimed is:

1. A method comprising:
providing a wafer including multiple cells, each cell including at least one emitter; and
5 performing a lithographic operation on the wafer to form heater trenches adjacent the emitters, each heater trench having a width that extends over at least respective portions of two cells.
2. The method of claim 1, wherein the lithographic operation is performed in
10 a word line direction across the wafer.
3. The method of claim 1, wherein the lithographic operation is performed in a bit line direction across the wafer.
- 15 4. The method of claim 1, wherein performing the lithographic operation further comprises depositing a heater alloy layer within each heater trench and depositing a nitride layer over the heater alloy layer, performing an anisotropic etching of the nitride layer and the heater alloy layer, and depositing an oxide layer over the nitride layer to form a pre-heater element arrangement within each
20 heater trench.
5. The method of claim 4, further comprising:
performing another lithographic operation on the wafer across the pre-heater arrangements to form two heater elements within each heater trench.
25
6. The method of claim 5, further comprising performing a third lithographic operation comprising depositing a nitride layer over the heater elements and etching trenches within the second nitride layer, depositing germanium antimony tellurium (GST) material within the trenches and performing an anisotropic
30 etching of the GST material.

7. The method of claim 6, wherein each trench has a width that extends over at least a portion of one cell.
8. The method of claim 6, wherein each trench has a width that extends over at least respective portions of two cells.
9. The method of claim 6, further comprising forming a top emitter interface on the GST material for at least one emitter.
10. The method of claim 9, further comprising performing a metallization such that a metal protective layer is provided on a top surface of the top emitter interface.
11. The method of claim 10, wherein the metallization is performed with tungsten.
12. The method of claim 5, wherein each heater element comprises one of TiN or TaN.
13. A method comprising:
providing a wafer comprising multiple cells, each cell comprising a heater element and a nitride layer over the heater element;
forming a trench within the nitride layer, the trench having a depth such that a portion of the heater element is exposed;
depositing GST material within the trench; and
performing an anisotropic etch of the GST material to form a memory cell adjacent the portion.
14. The method of claim 13, wherein the trench has a width that extends over at least a portion of one cell.
15. The method of claim 13, wherein the trench has a width that extends over at least respective portions of two cells and has a depth such that the portion of the respective heater elements of the two cells is exposed.

16. The method of claim 13, further comprising forming a top emitter interface on each memory cell.

17. The method of claim 16, further comprising performing a metallization
5 such that a metal protective layer is provided on a top surface of the top emitter interface.

18. The method of claim 17, wherein the metallization is performed with tungsten.

10

19. The method of claim 13, wherein each heater element comprises one of TiN or TaN.

20. An apparatus comprising:

15 a substrate comprising multiple cells, each cell comprising at least one emitter within an emitter layer; and

a heater trench adjacent to the emitter layer, the heater trench having a width that extends over at least respective portions of two cells.

20 21. The apparatus of claim 20, further comprising heater elements within the heater trench, a heater element being adjacent the at least one emitter, each heater element having a substantially L-shape.

22. The apparatus of claim 21, wherein each heater element comprises one of
25 TiN or TaN.

23. The apparatus of claim 21, further comprising a memory cell adjacent a vertical portion of each heater element.

30 24. The apparatus of claim 23, further comprising a top emitter interface on the memory cell.

25. The apparatus of claim 24, wherein the top emitter interface comprises tungsten.

26. The apparatus of claim 25, wherein the memory cell comprises GST.

27. A method comprising:

5 providing wafer including multiple cells, each cell including at least one emitter;

performing a lithographic operation in a first direction of the wafer across the cells to form pre-heater element arrangements;

10 performing a lithographic operation in a second direction of the wafer across the pre-heater element arrangements to form a pre-heater element adjacent each emitter; and

performing a lithographic operation in the first direction across a portion of each pre-heater element to form a heater element adjacent each emitter.

15 28. The method of claim 27, wherein each heater element comprises one of titanium nitride (TiN) or tantalum nitride (TaN).

29. The method of claim 27, further comprising depositing a heater seal layer adjacent to the heater elements.

20 30. The method of claim 29, further comprising performing a lithographic operation in the second direction to create a micro trench across each cell such that each heater element is exposed.

25 31. The method of claim 30, further comprising depositing germanium antimony tellurium (GST) within each micro trench.

32. The method of claim 31, further comprising forming a top emitter interface on the GST for at least one emitter.

30 33. The method of claim 32, further comprising performing a metallization such that a metal protective layer is provided on a top surface of at least one top emitter interface.

34. The method of claim 33, wherein the metallization is performed with tungsten.

35. The method of claim 27, wherein the first direction is a word line direction
5 and the second direction is a bit line direction.

36. An apparatus comprising:

a substrate comprising an emitter layer including at least one emitter within the emitter layer; and

10 a heater element adjacent each emitter and having a substantially squared U-shape, wherein first portion of the U-shape is shorter than a second portion of the U-shape.

37. The apparatus of claim 36, wherein the first portion is substantially flush
15 with a bottom portion of the substantially squared U-shape.

38. The apparatus of claim 36, wherein each heater element comprises one of TiN or TaN.

20 39. The apparatus of claim 38, further comprising a memory cell adjacent the second portion.

40. The apparatus of claim 38, further comprising a top emitter interface on the memory cell.

25

41. The apparatus of claim 40, wherein a top surface of the top emitter interface comprises tungsten.

42. The apparatus of claim 41, wherein the memory cell comprises GST.

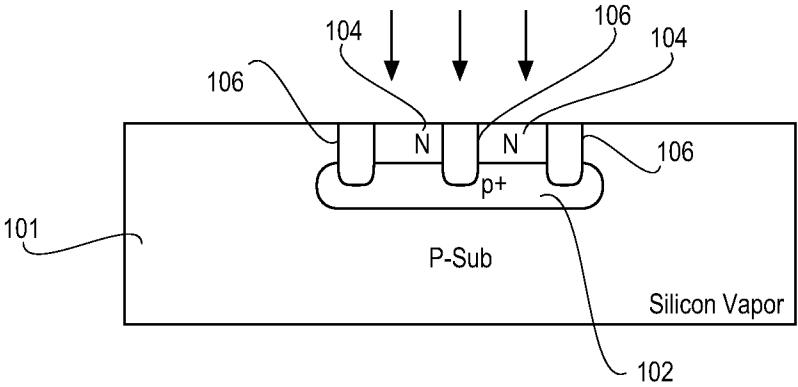


Figure 1

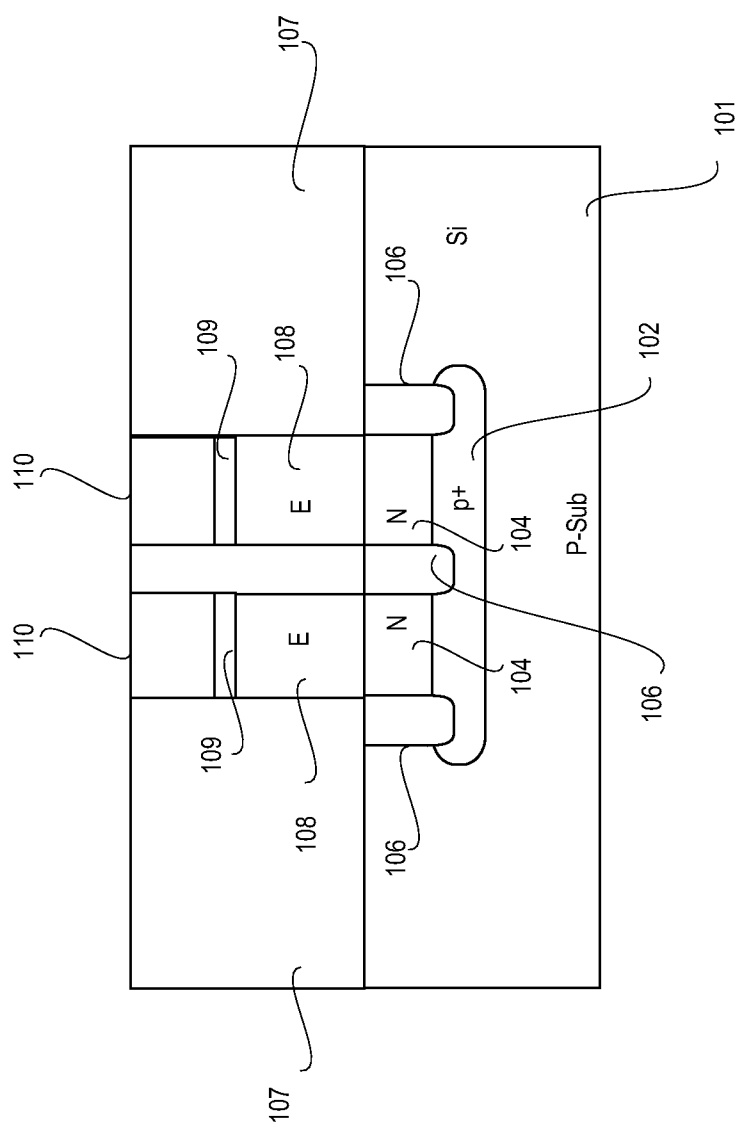


Figure 2

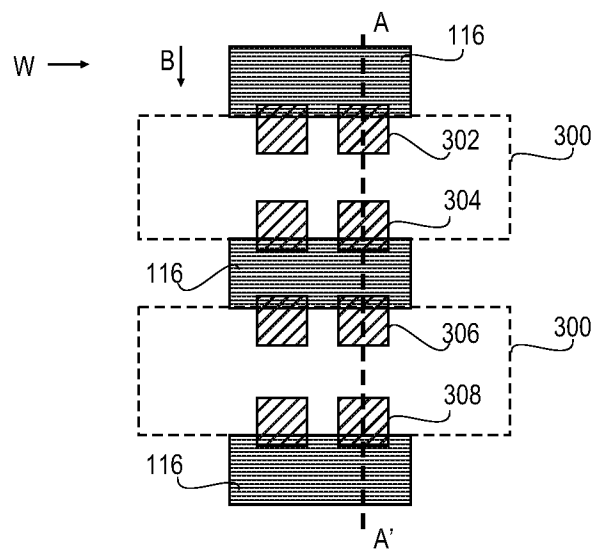


Figure 3

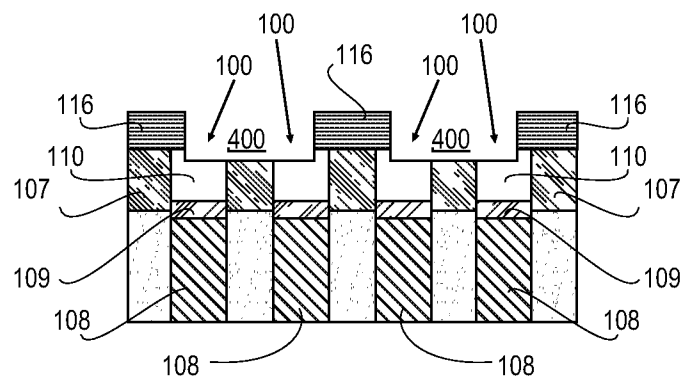


Figure 4

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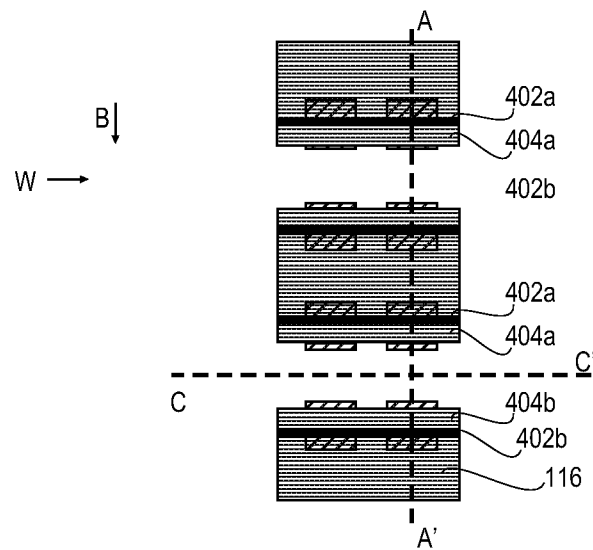


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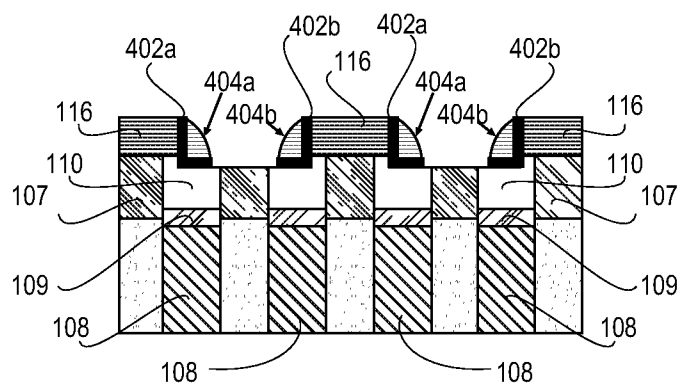


Figure 6

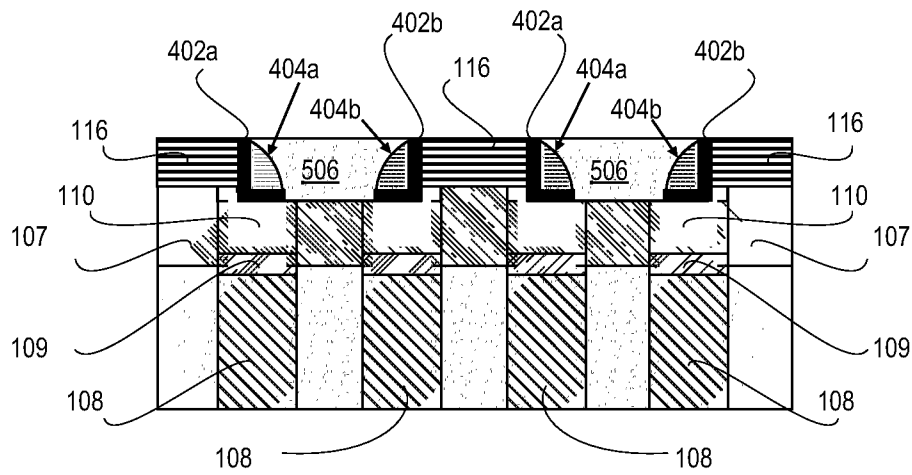


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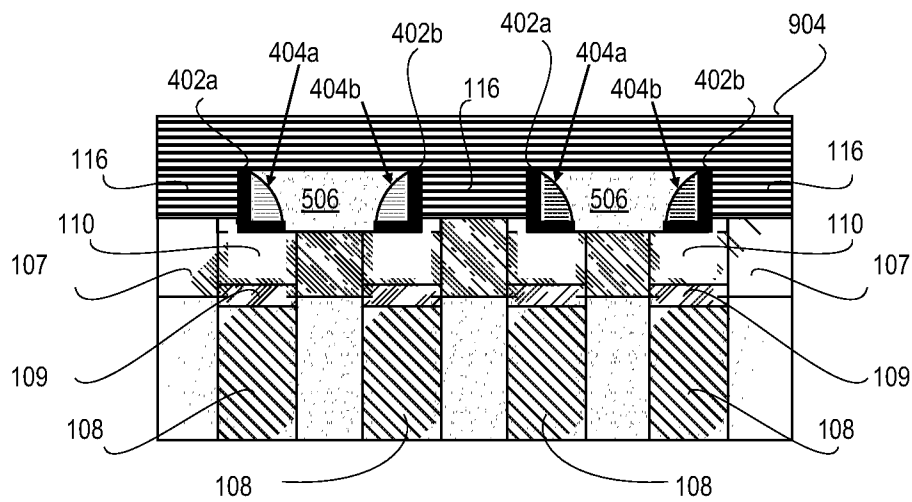


Figure 8

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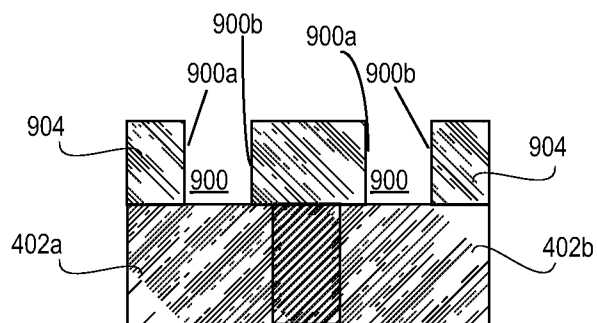


FIG. 9

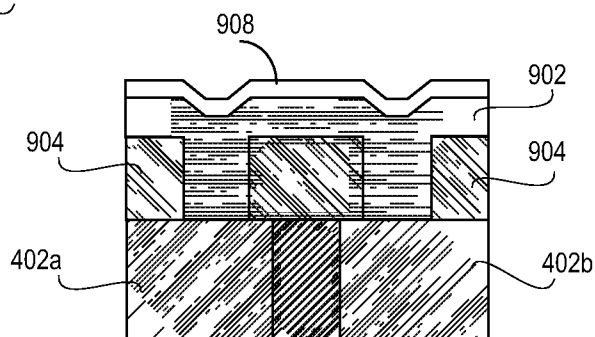


FIG. 10

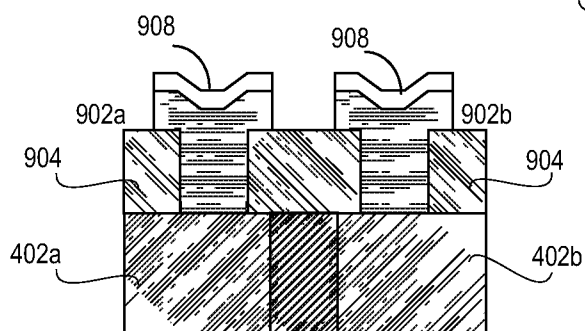


FIG. 11

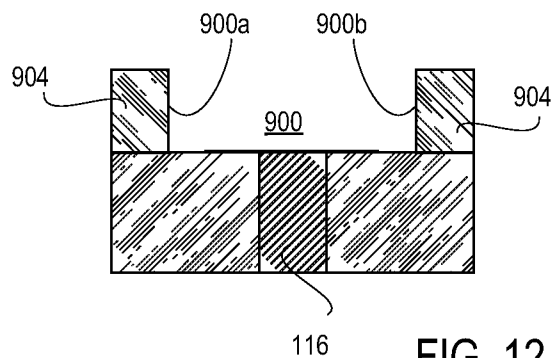


FIG. 12

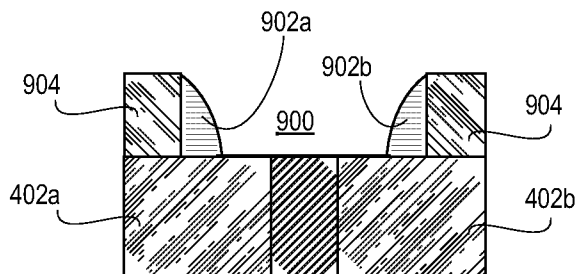


FIG. 13

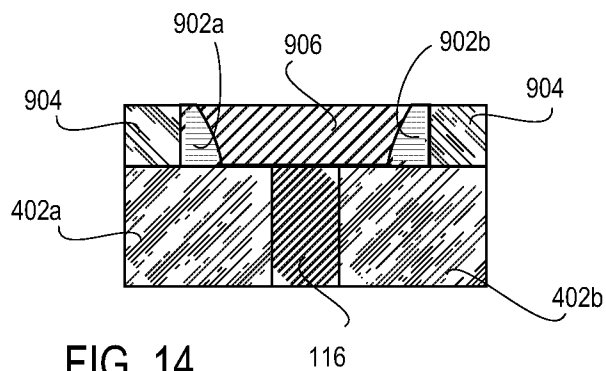


FIG. 14

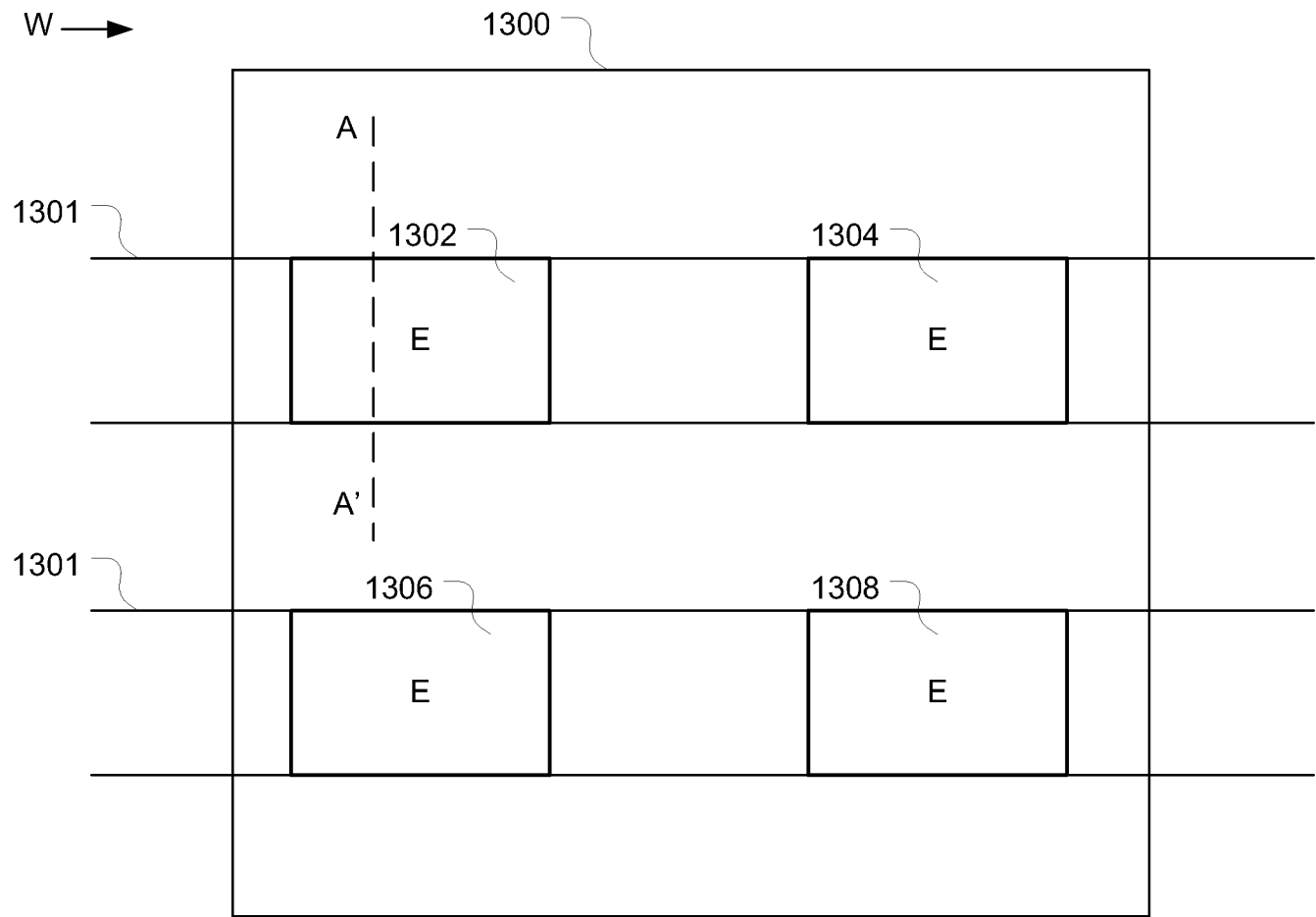
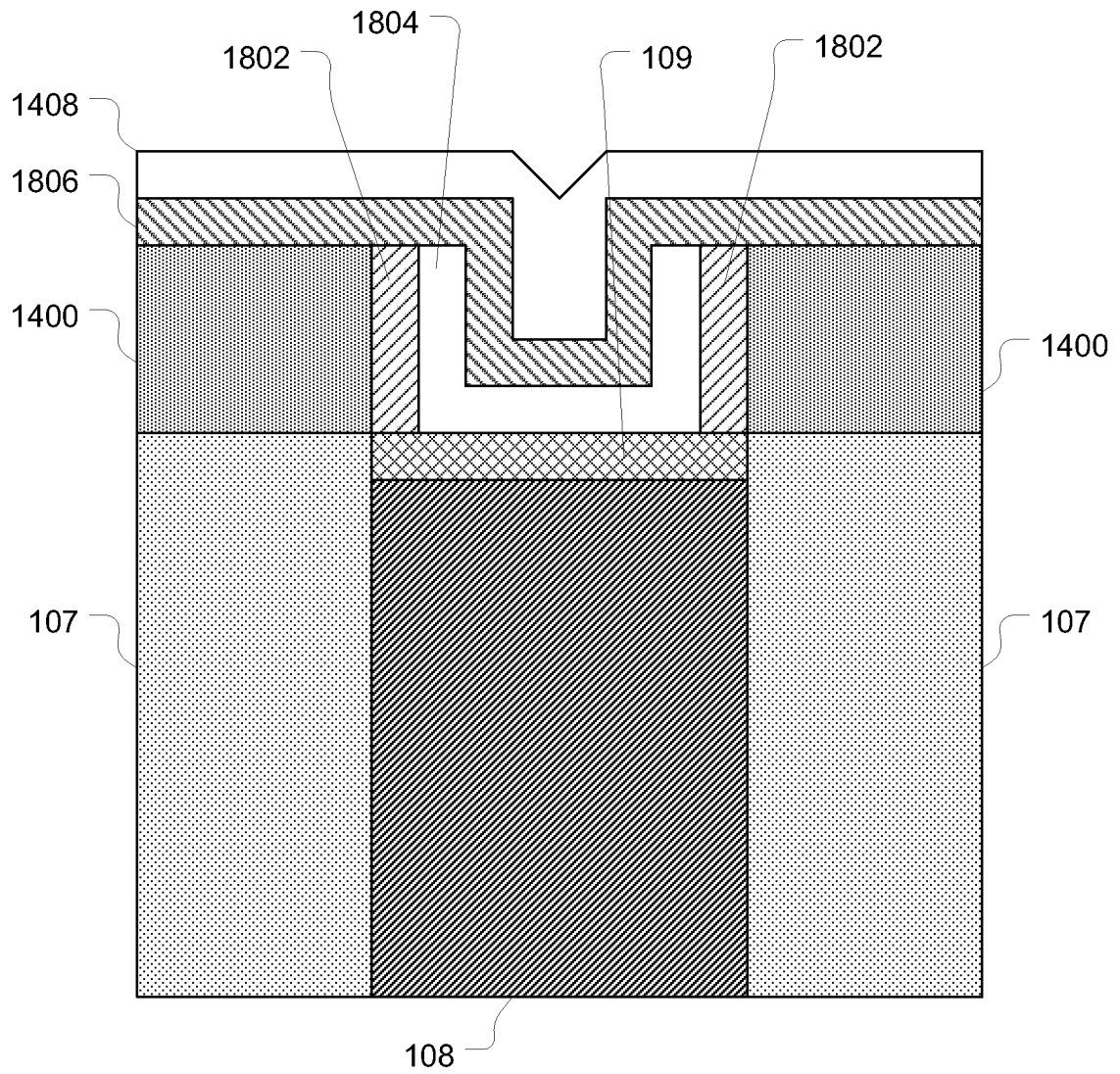


Figure 15

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**Figure 16**

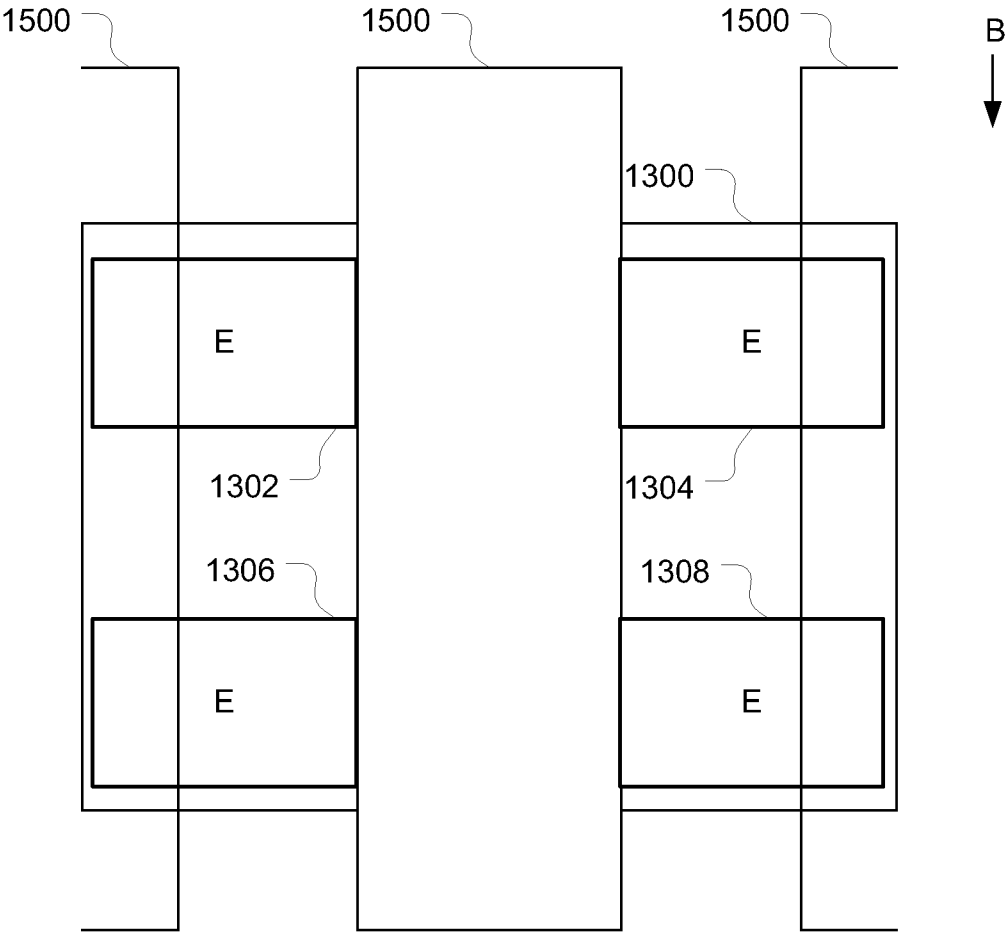


Figure 17

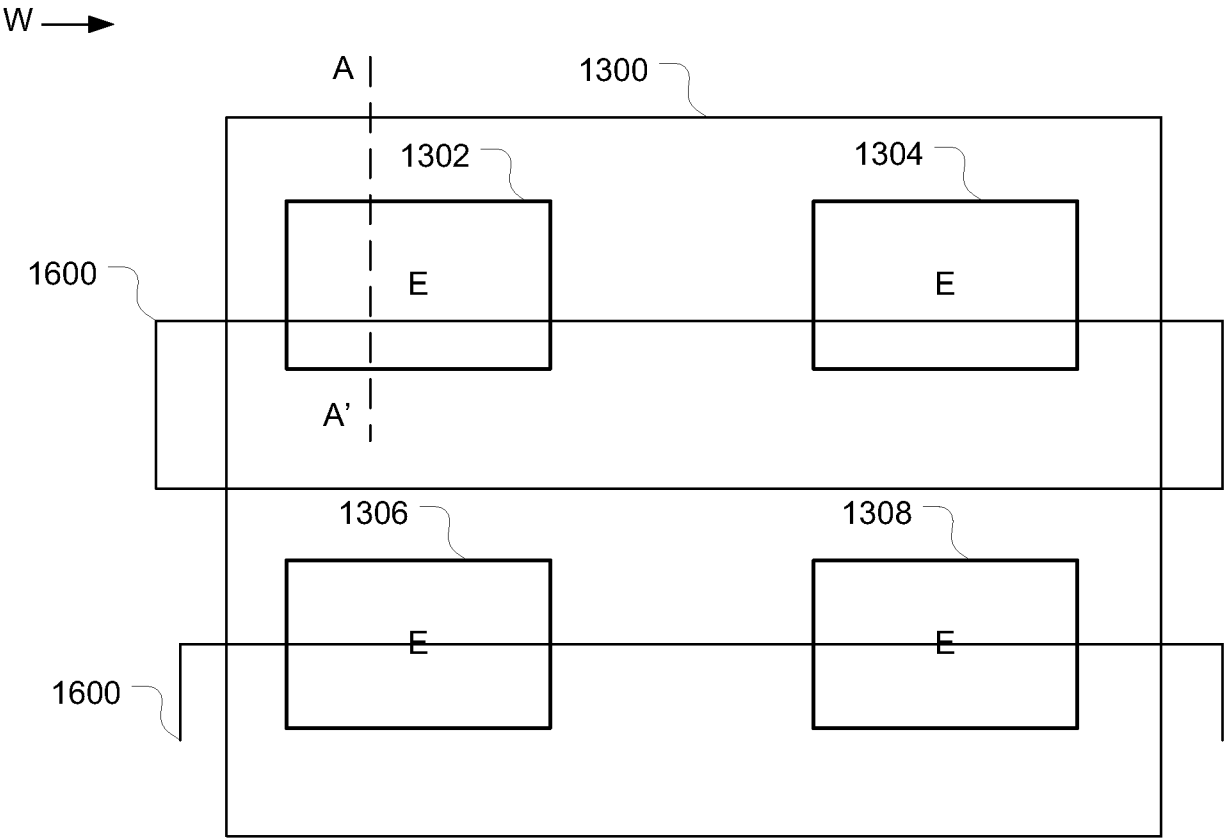
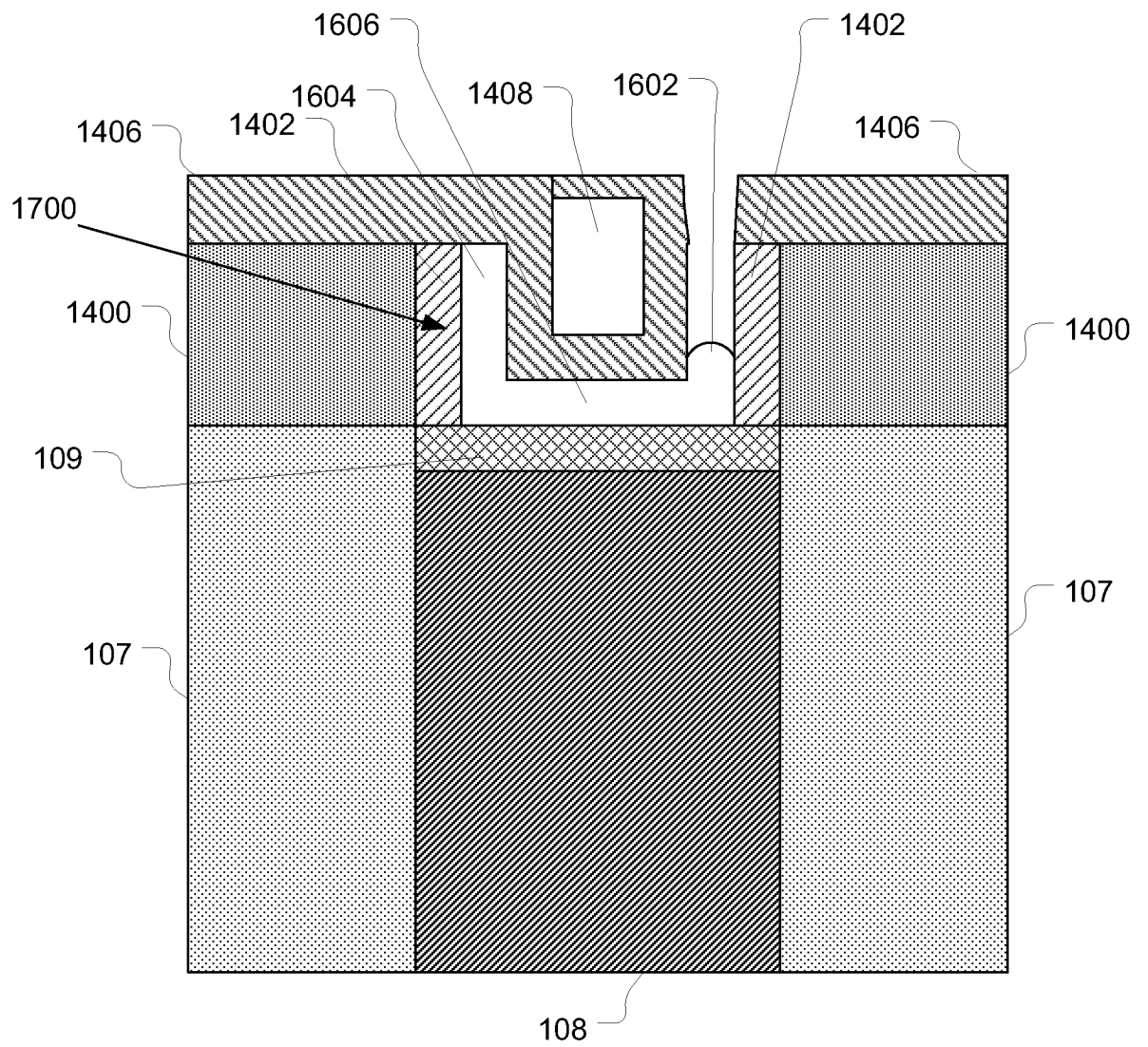
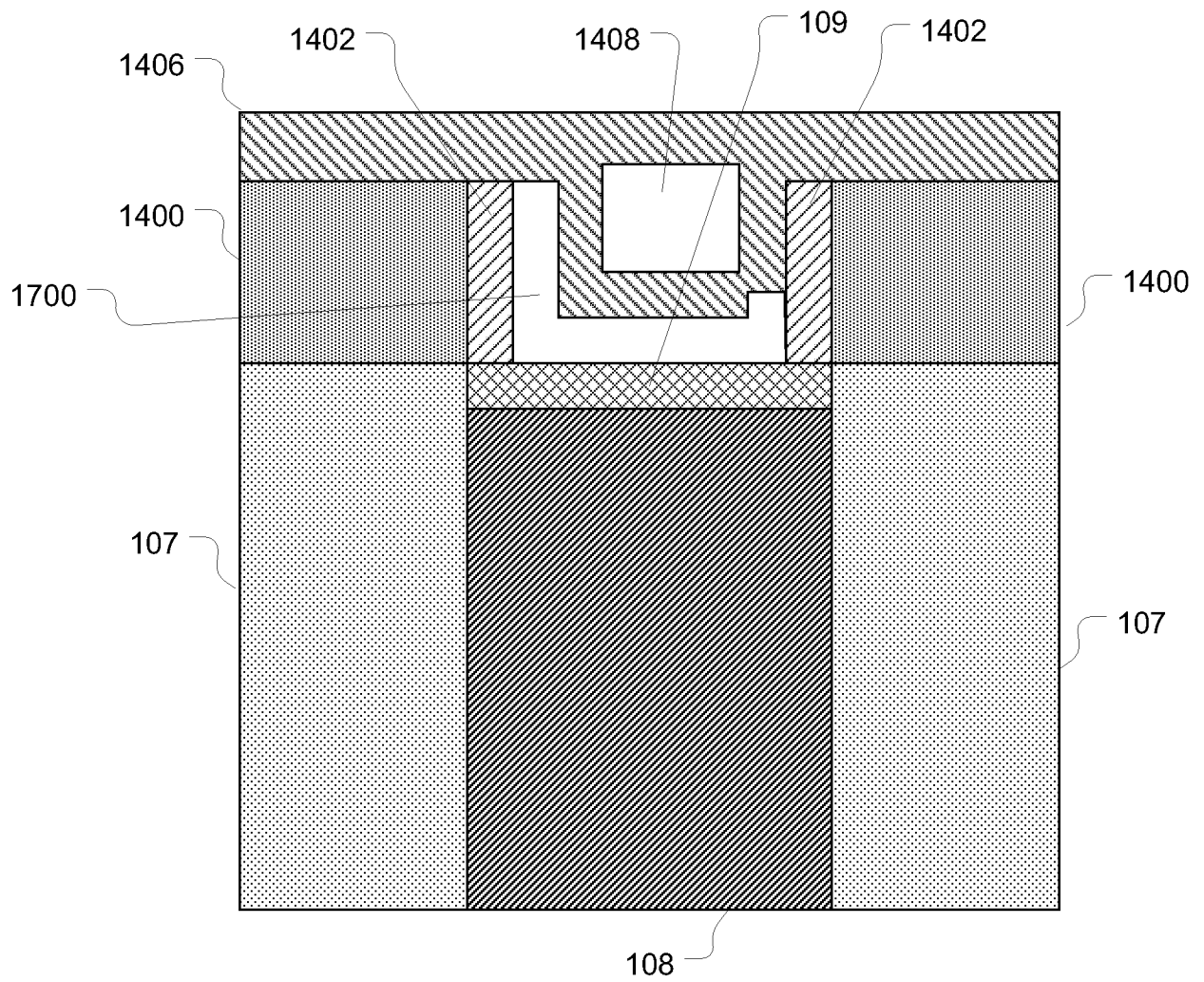
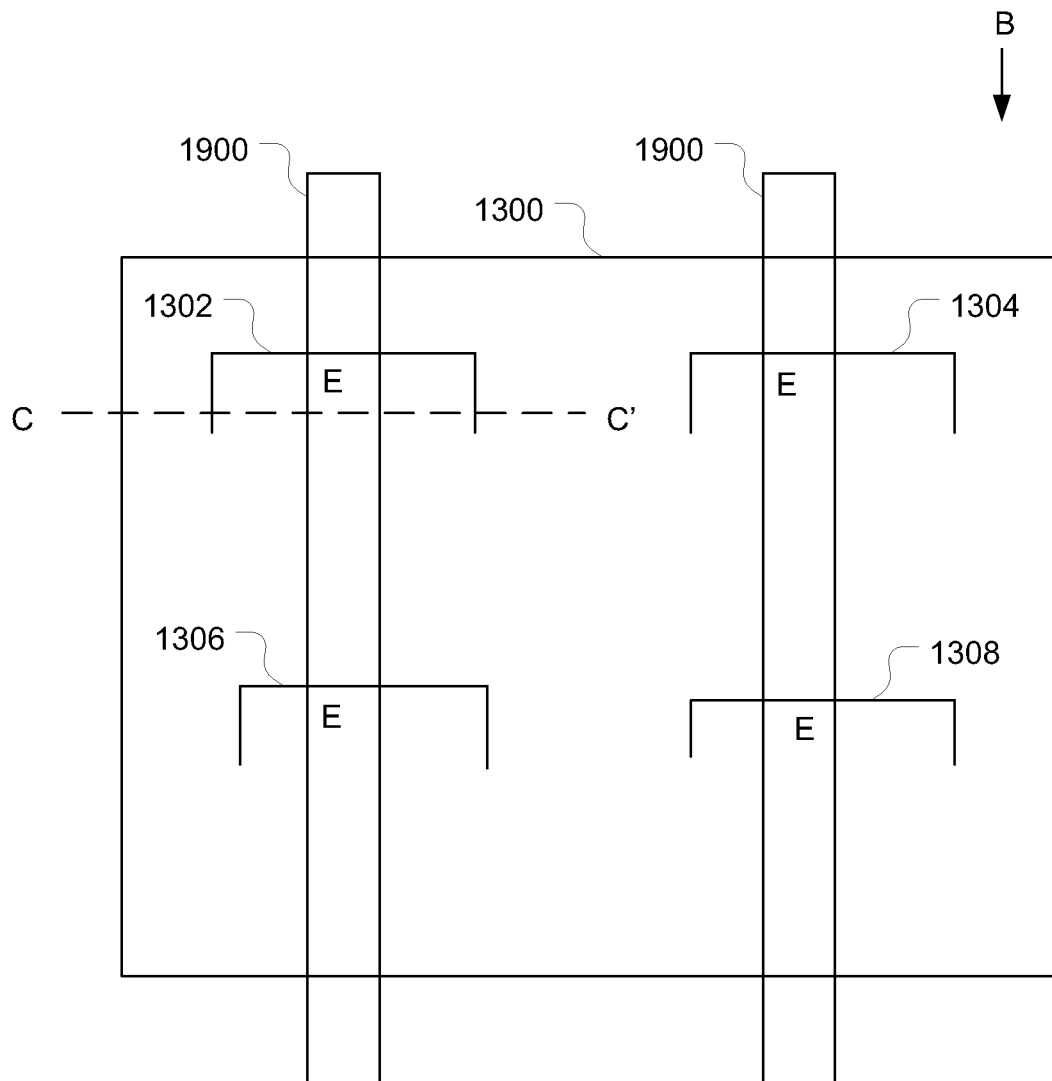


Figure 18

**Figure 19**

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**Figure 20**

**Figure 21**

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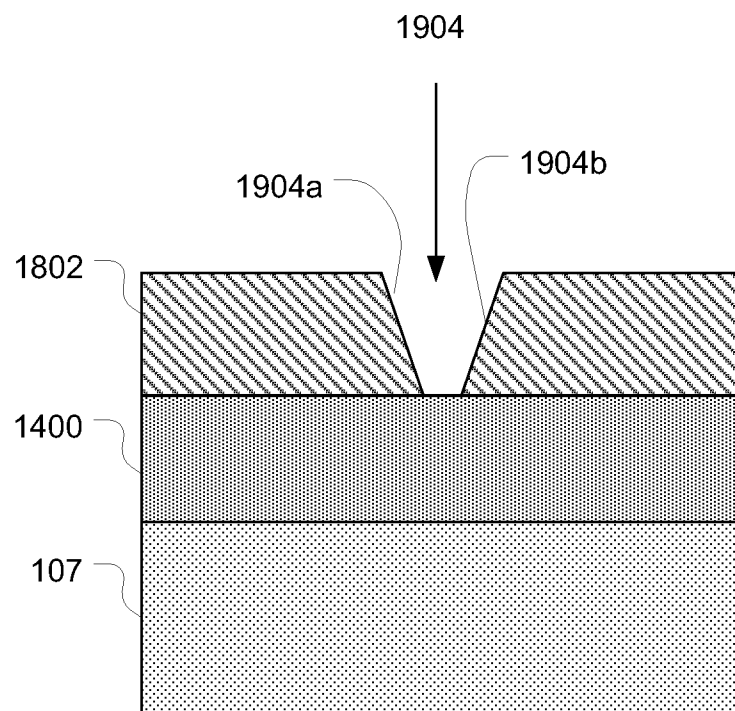


Figure 22

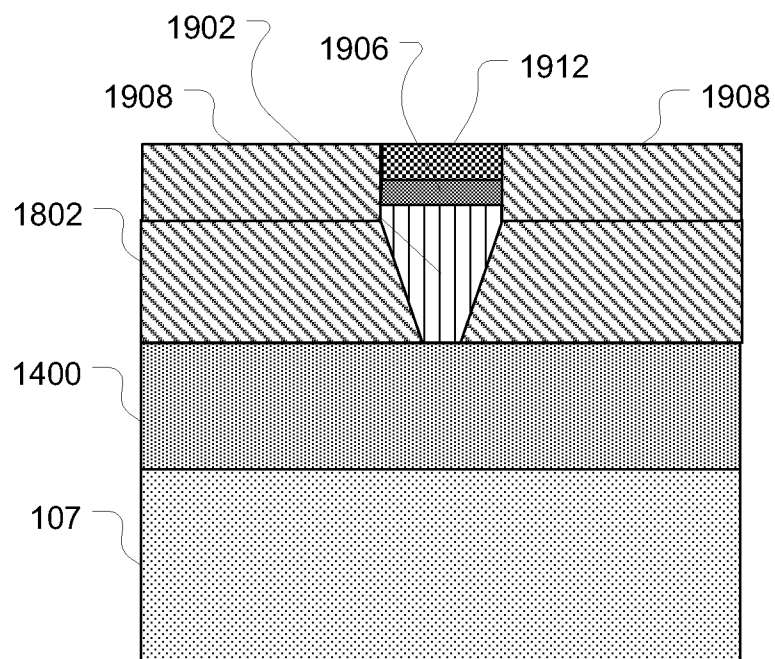


Figure 23

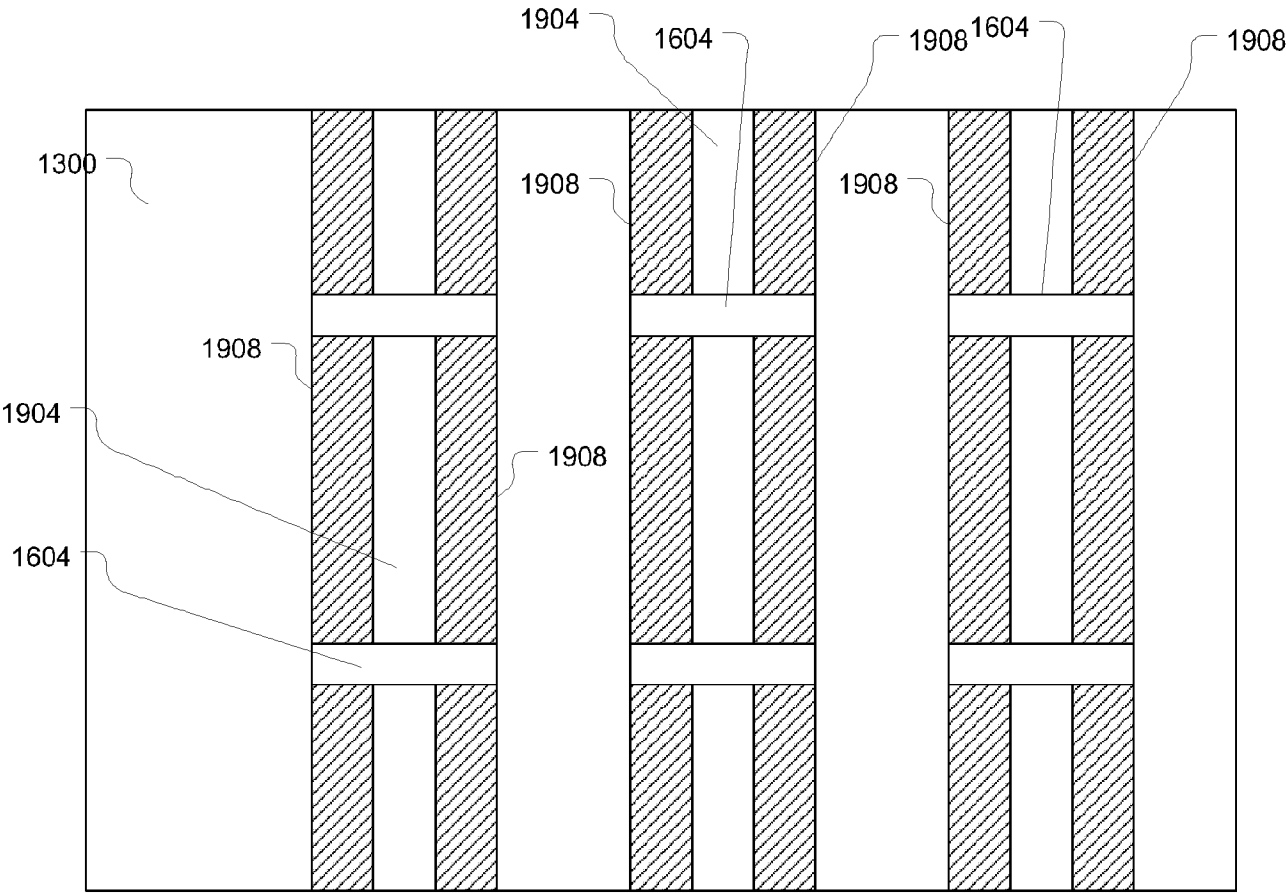


Figure 24

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/059148

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 729 355 A (ST MICROELECTRONICS SRL [IT]) 6 December 2006 (2006-12-06)	1-12, 20-22, 24-42
Y	paragraph [0031] - paragraph [0040]; figures 18-31	15
X	US 2005/006681 A1 (OKUNO YASUTOSHI [JP]) 13 January 2005 (2005-01-13)	13,14, 16-19
Y	paragraph [0046] - paragraph [0056]	15
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

Z document member of the same patent family

Date of the actual completion of the international search

16 July 2008

Date of mailing of the international search report

25/07/2008

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
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Gröger, Andreas

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/059148

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	OTTOGALLI F ET AL: "Phase-change memory technology for embedded applications" SOLID-STATE DEVICE RESEARCH CONFERENCE, 2004. ESSDERC 2004. PROCEEDING OF THE 34TH EUROPEAN LEUVEN, BELGIUM 21-23 SEPT. 2004, PISCATAWAY, NJ, USA, IEEE, US, 21 September 2004 (2004-09-21), pages 293-296, XP010738434 ISBN: 978-0-7803-8478-1 the whole document	1-42
A	PIROVANO A ET AL: "/spl mu/Trench phase-change memory cell engineering and optimization" SOLID-STATE DEVICE RESEARCH CONFERENCE, 2005. ESSDERC 2005. PROCEEDING S OF 35TH EUROPEAN 12-16 SEPT. 2005, PISCATAWAY, NJ, USA, IEEE, 12 September 2005 (2005-09-12), pages 313-316, XP010858778 ISBN: 978-0-7803-9203-8 the whole document	1-42

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/059148

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
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US 2005006681	A1	13-01-2005	JP	2005032855 A	03-02-2005
			US	2007158635 A1	12-07-2007