

May 5, 1959

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2,885,662

ANALOG-TO-DIFUNCTION CONVERTERS

Filed Oct. 17, 1955

4 Sheets-Sheet 1

FIG. 1.

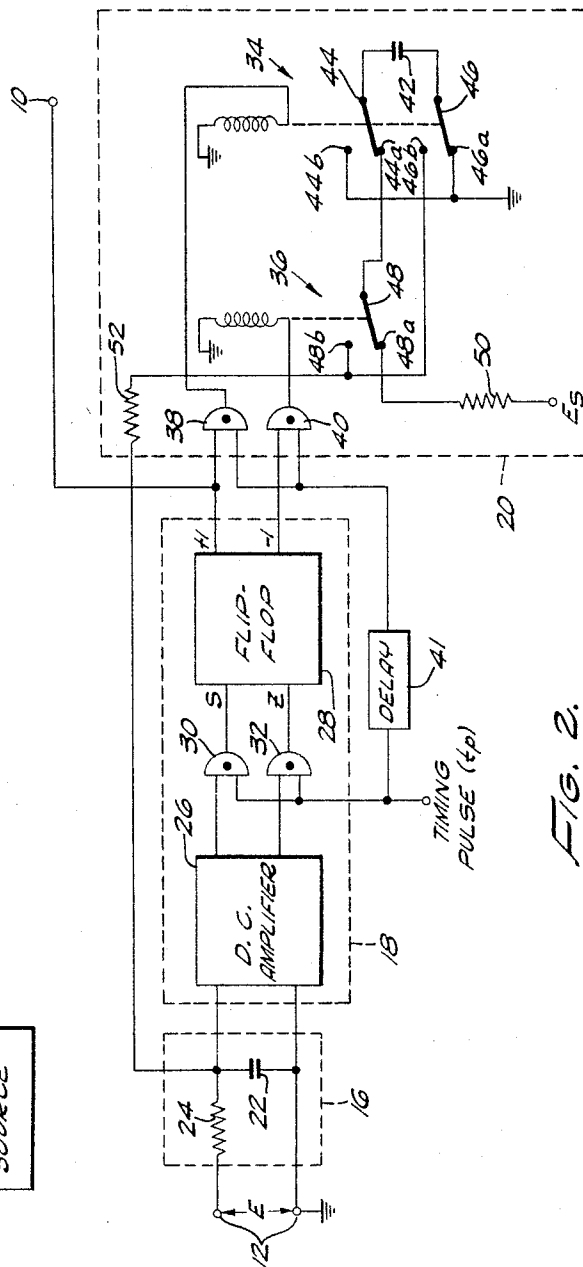
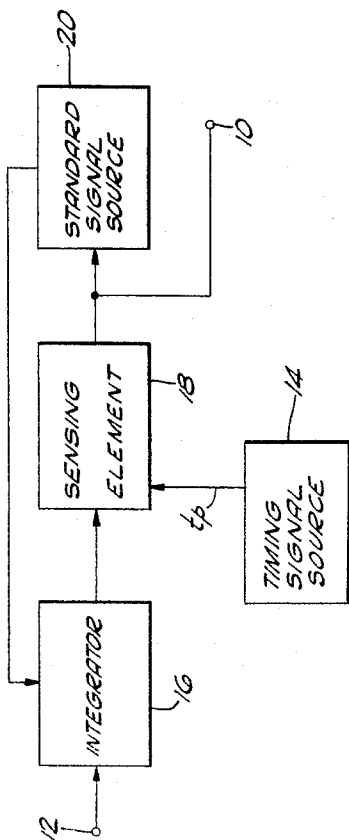


FIG. 2.

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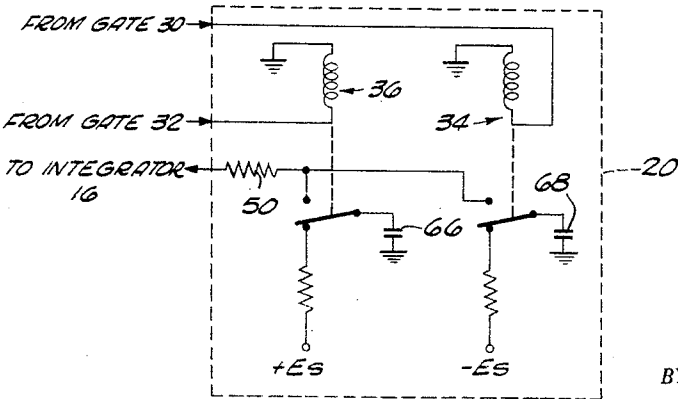
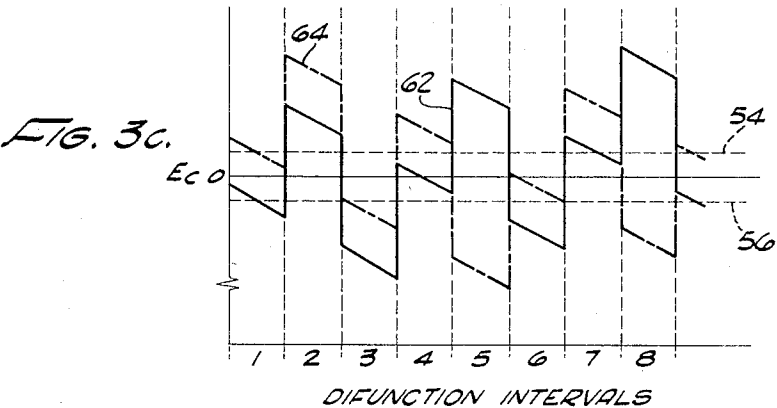
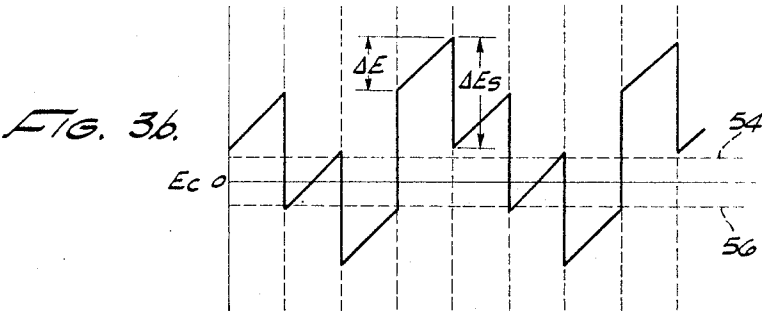
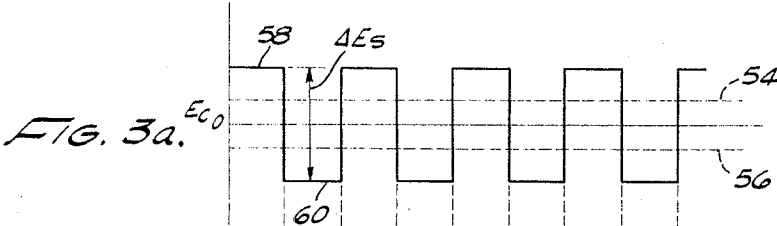
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4 Sheets-Sheet 2



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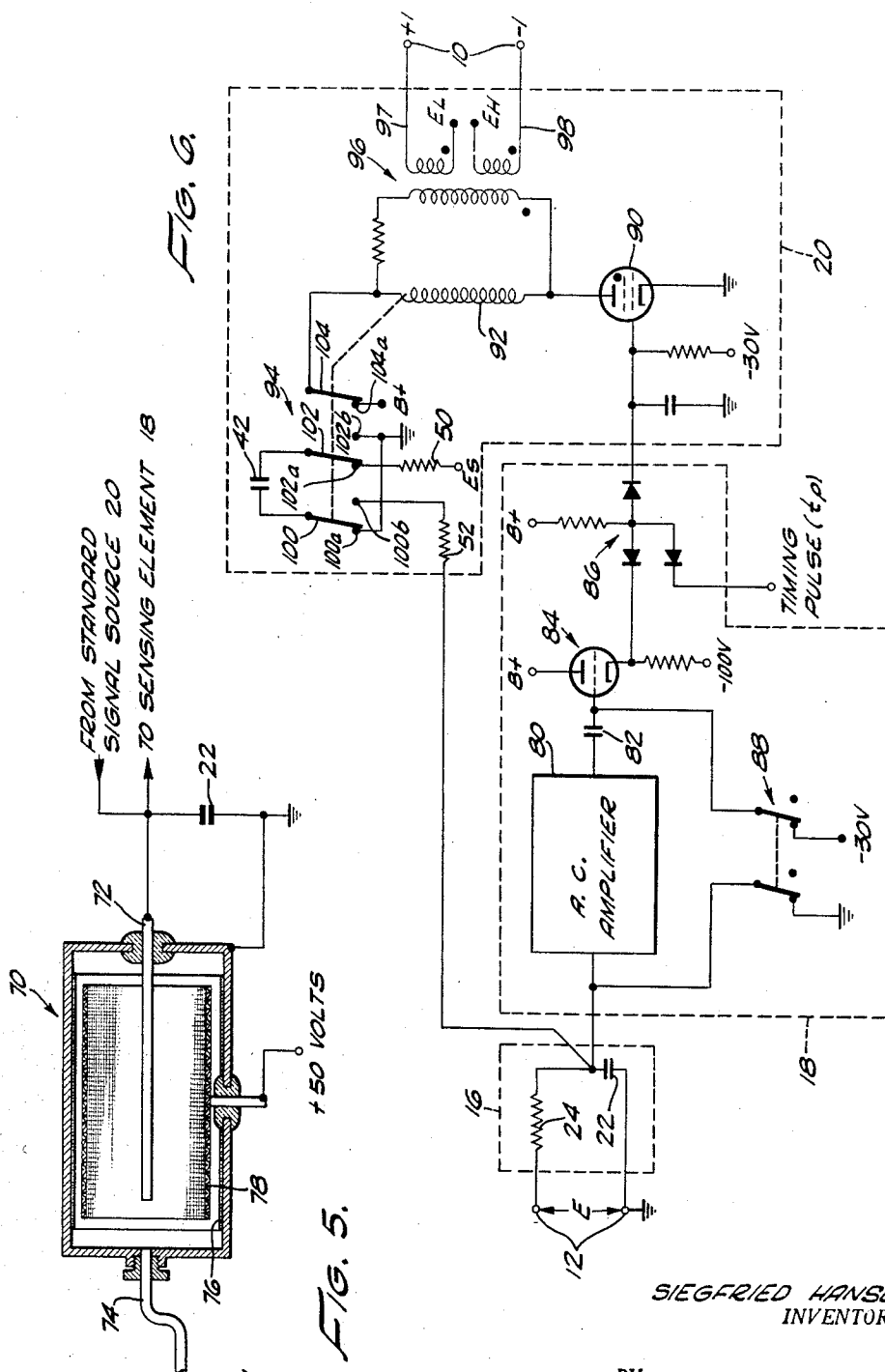
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4 Sheets-Sheet 3



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ANALOG-TO-DIFUNCTION CONVERTERS

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4 Sheets-Sheet 4

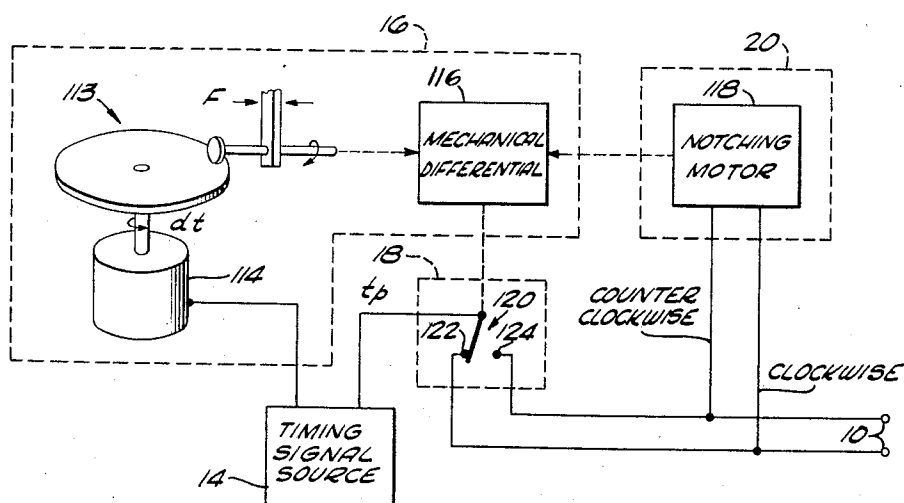
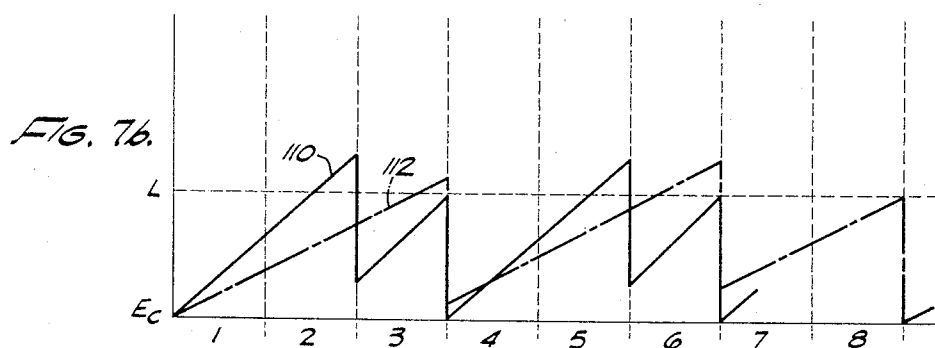
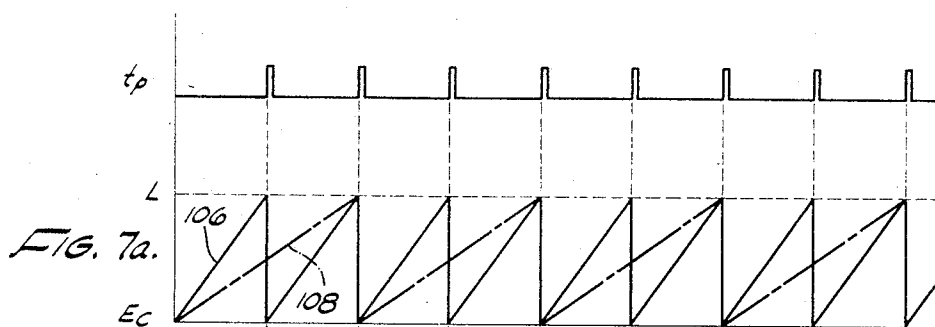


FIG. 8.

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ANALOG-TO-DIFUNCTION CONVERTERS

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Application October 17, 1955, Serial No. 540,699

14 Claims. (Cl. 340—347)

This invention relates to analog-to-difunction converters and more particularly to converters which are operative to convert to a difunction output signal train an applied analog signal by integrating the signal, generating periodic difunction signals corresponding to the value of the integral with respect to a reference level, and decreasing the integral by a fixed amount each time the integral exceeds the reference level.

Relatively recent developments in the field of digital computation have brought forth a new class of electronic digital computing elements in which operations are performed on and in response to what has come to be termed difunction signal trains, as contrasted with the conventional digital computing machines which operate upon signals representing weighted binary digits. As will be disclosed in more detail hereinafter, the term difunction signal train refers to a train of signals each having either a first value representing a first number or a second value representing a second number, and is readily distinguished from signal trains conventional in prior art computer systems in that all of the signals in the difunction signal train having the same value represent identical numbers.

For example, if it is assumed that the algebraic numbers in a difunction signal train are plus one and minus one, then each of the signals in the train individually represents either a plus one or a minus one, depending on the value of the signal. Stated differently, in a difunction signal train the individual signals are unweighted, each signal having equal significance with every other signal. Accordingly, a difunction signal train may be termed a non-numerical representation of the quantity which the train represents, since the signals are not weighted according to any number system, or in other words, have no radix as this term is customarily employed. For purposes of simplicity, it will be assumed hereinafter that the difunction signals generated by the converters of the invention have a value of either a plus one or a minus one, although it will be later shown that the output signals from the identical converters may be considered as representing either a plus one or zero by merely changing the difunction notation.

The representation of physical or mathematical quantities by difunction signal trains has been found to be extremely useful both in the solution of mathematical equations and in the field of automatic control. Some examples of the application of difunction representation of the solution of mathematical equations may be found in copending U.S. patent application Serial No. 388,780, filed by Floyd G. Steele on October 28, 1953, for "Electronic Digital Differential Analyzer," wherein difunction signal trains are employed for communicating between the integrators of a digital differential analyzer, and in copending U.S. patent application Serial No. 510,673, filed May 24, 1955 by Floyd G. Steele for "Difunction Computing Elements." Similarly, copending U.S. patent application Serial No. 311,609, filed September 26, 1952 by Floyd G. Steele, for "Computer and Indicator

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System," discloses the application of difunction representation to the field of process control and also discloses electronic computing circuits which operate directly to perform mathematical operations by combining difunction signals.

The foregoing patent applications disclose structures for adding, subtracting, multiplying, dividing, and integrating difunction signal trains. However, there has remained a need for new and improved forms of analog-to-difunction converters in order to fully realize the potential of difunction computing techniques, especially as applied to the field of process control and to the solution of real time problems.

In the past a number of analog-to-difunction converters have been proposed and constructed for converting to difunction form analog signals of various types. For example, U. S. Patent 2,733,430, issued January 31, 1956 to Floyd G. Steele for an "Angular Quantizer," discloses an angular quantizer which is operative to generate an output difunction signal representative of the rotational rate of an associated shaft. Still other forms of analog-to-difunction converters are disclosed in copending U. S. patent application Serial No. 510,736, filed May 24, 1955 by Floyd G. Steele for "Electronic Digital Computing Systems," which discloses devices for converting analog signals first to related time intervals, and then to corresponding difunction signal trains. Although each of the foregoing conversion devices has been utilized successfully in numerous instances, there still remains a need for a relatively simple circuit which is capable of directly converting analog voltages or currents into their equivalent difunction form representative of the magnitude and polarity of the analog signals.

The present invention fulfills the aforementioned void in the art by providing an analog-to-difunction converter which is operable to directly convert an applied analog signal to an equivalent difunction signal train. According to the basic concept of the invention, each of the analog-to-difunction converters herein set forth includes an integrator for integrating the analog quantity with respect to time over each difunction signal period, a comparator or sensing element operative to sample the integral developed for generating a plus one representing difunction signal if the value of the integral exceeds a predetermined reference level and a minus one representing difunction signal if the value of the integral is less than the reference level, and a standard signal source operable in response to each plus one difunction signal for subtracting from the integral a unit quantity representative of the difunction signal generated.

According to several specific embodiments of the invention, the integrator utilized for integrating the applied analog signal includes a capacitor which is charged during each difunction signal period at a rate and in a sense corresponding to the magnitude and polarity of an applied variable voltage analog signal. The integral signal thus developed is then sampled at the end of each difunction signal period by an associated electronic sensing circuit which in turn generates a control signal, corresponding to a plus one representing difunction signal, each time the integral exceeds a predetermined reference potential. Each control signal generated is then employed to control the actuation of a standard charge storage circuit which when actuated functions to discharge the integrator capacitor by a fixed amount and in a sense opposite to the polarity of the capacitor voltage when last sensed by the sensing element.

It should be pointed out that the term "capacitor discharge" as herein employed does not imply that the capacitor thus operated is driven to ground potential, but instead implies that the voltage on the capacitor is driven in a sense opposite to the polarity of the capacitor voltage

when last sampled. Thus for example, a capacitor which has charged to a voltage of plus one volt may be discharged to a minus two volts, even though the final charge on the capacitor is thereby increased over its initial value if it is assumed that the other terminal of the capacitor is at ground potential.

In accordance with different embodiments of the invention there are provided an electronic analog-to-difunction converter which is operative to convert a bipolar variable voltage analog signal to its difunction equivalent, and a modified form of electronic converter which functions to convert a unipolar analog signal to an equivalent difunction signal train. In still another embodiment of the invention there is provided an electromechanical analog-to-difunction converter for converting to a difunction output signal train an applied mechanical analog signal, the basic concept and mode of operation of the invention being generic to both this latter embodiment and the electronic embodiments previously described.

It is, therefore, an object of the invention to provide analog-to-difunction converters which are operative to directly convert an applied analog signal to an equivalent difunction signal train non-numerically representative of the quantity represented by the applied analog signal.

Another object of the invention is to provide analog-to-difunction converters which function to convert an applied analog signal to an equivalent difunction signal train by integrating the applied signal, periodically sampling the applied signal to generate difunction signals corresponding to the value of the integral with respect to a predetermined reference level, and decreasing the integral by a predetermined fixed quantity corresponding to value of the difunction signal each time the signal exceeds the reference level.

A further object of the invention is to provide electronic analog-to-difunction converters which function to convert an applied variable voltage analog signal to its equivalent difunction form by integrating the signal with respect to time during each successive difunction signal period, sampling the integral signal at the end of each period to generate a difunction signal having one value each time the integral signal exceeds a predetermined reference voltage, and decreasing the integral signal by a fixed amount each time a difunction signal having said one value is generated.

Still another object of the invention is to provide electronic analog-to-difunction converters for converting an applied electrical analog signal to an equivalent difunction signal train, the converters including a capacitor for developing a charge corresponding to the integral with respect to time of the analog signal, and being operative to generate a difunction signal representative of a predetermined numerical value each time the capacitor charges above a predetermined value and to discharge the capacitor with a predetermined standard charge each time a difunction signal having said predetermined value is generated.

The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages thereof, will be better understood from the following description considered in connection with the accompanying drawings in which several embodiments of the invention are illustrated by way of example. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only, and are not intended as a definition of the limits of the invention.

Fig. 1 is a block diagram illustrating the basic elements of the analog-to-difunction converters of the invention;

Fig. 2 is a circuit diagram, partly in schematic form, of an electronic analog-to-difunction converter, according to the invention;

Figs. 3a, 3b and 3c are waveforms illustrating the operation of the circuit of Fig. 2;

Fig. 4 is a schematic diagram of a modified standard signal source which may be employed in the embodiment of Fig. 2;

Fig. 5 is a schematic diagram of a combined integrator and instrument circuit which may be employed in the circuit of Fig. 2 for generating a difunction output signal train representative of an analog input current;

Fig. 6 is a circuit diagram, partly in schematic form, of a modified electronic analog-to-difunction converter, according to the invention;

Figs. 7a and 7b are waveforms illustrating the operation of the circuit of Fig. 5; and

Fig. 8 is a block diagram, partly in schematic form, of an electromechanical analog-to-difunction converter in accordance with the invention.

With reference now to the drawings, wherein like or corresponding parts are designated by the same reference characters throughout the several views, there is shown in Fig. 1 a block diagram of the basic analog-to-difunction converter of the invention which is operative to produce at an output terminal 10 a difunction output signal train non-numerically representative of the magnitude and polarity of an analog input signal applied to an input terminal 12. As shown in Fig. 1 the converter is operated in synchronism with a timing signal source 14 which generates a periodically recurring clock or timing signal (*tp*) which delimits or marks off successive difunction signal periods, and includes three basic elements, namely, an integrator 16 which integrates the applied analog signal with respect to time over each difunction signal period, a sensing element 18 coupled to the integrator and operative to sample the integral developed during each difunction interval for generating a plus one representing difunction signal whenever the integral exceeds a predetermined reference level, and a standard signal source 20 coupled to the sensing element and operative in response to each plus one representing difunction signal for subtracting a predetermined fixed quantity, representative of a plus one difunction signal, from the integral developed by integrator 16.

Consider now the basic mode of operation of the analog-to-difunction converter of Fig. 1. It will be assumed that initially integrator 16 has an initial remainder (R_0) stored therein, and that the analog input signal is thereafter integrated through a difunction signal period, after which sensing element 18 compares the integral developed with a reference level (L) to determine whether a plus one or minus one difunction signal should be generated. Thus the sign of the difunction signal may be expressed as:

$$\text{sign of } (R_0 + \Delta Q_0) - L = \text{sign of} \\ \text{difunction signal No. 1} \quad (1)$$

where ΔQ_0 is the integral developed by integrating the analog signal over the initial difunction signal period.

If now the difunction signal generated represents a plus one, standard signal source 20 is actuated to reduce the integral stored in integrator 16 by a fixed amount Q_s representing the plus one difunction signal generated, and thereby leaves a new remainder R_1 in the integrator. This operation may be expressed by the equation:

$$(R_0 + \Delta Q_0) - X_1 Q_s = R_1 \quad (2)$$

where X_1 takes the value of the difunction signal generated, namely plus one.

During the succeeding difunction signal period the integration process is again carried out and an incremental integral ΔQ_1 is added to the remainder R_1 . Consequently the

$$\text{sign of } (R_1 + \Delta Q_1) - L = \text{sign of} \\ \text{difunction signal No. 2} \quad (3)$$

Assume now that the second difunction signal has a negative sign. The operation of the analog-to-difunction converter now may follow either of two courses, depend-

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ing upon whether the converter is constructed to convert bipolar analog signals or unipolar analog signals. If it is assumed that the converter is to convert only unipolar analog signals, the new remainder R_2 is merely:

$$(R_1 + \Delta Q_1) = R_2 \quad (4)$$

and integrator 16 continues to integrate the applied signal through the third difunction signal interval, after which the interval is again sampled to see if it exceeds level (L). In other words, if the converter is for converting unipolar analog signals to their difunction equivalents, the value of the integral developed is set back or decreased when a plus one difunction signal is generated, but is permitted to increase if the level (L) is not exceeded, in which instances minus one representing difunction signals are generated. Thus the sign of the third difunction signal may be expressed as:

$$\text{sign of } (R_2 + \Delta Q_2) = \text{sign of difunction signal No. 3} \quad (5)$$

If, on the other hand, the analog to difunction converter is to be capable of converting bipolar signals to difunction form, the fixed quantity Q_s is added to the integral developed at the end of each difunction interval during which the value of the integral remains less than the reference level L. Consequently the remainder R_2 in the bipolar system is:

$$(R_1 + \Delta Q_1 - X_2 Q_s) = R_2 \quad (6)$$

where X_2 takes the value of the difunction signal generated, namely minus one.

Generalizing the foregoing equations for converters of both bipolar and unipolar analog signals, the sign of the n th difunction signal generated is given by:

$$\text{sign of } (R_{n-1} + \Delta Q_{n-1}) - L = \text{sign of } n\text{th difunction signal} \quad (7)$$

and the remainder may be expressed as:

$$R_n = (R_{n-1} + \Delta Q_{n-1}) - X_n Q_s \quad (8)$$

where X in the case of a converter of bipolar signals takes the value of the last difunctional signal generated, and in the case of a converter of unipolar analog signals is either a plus one or a zero, depending upon whether a plus one or minus one difunction signal was last generated.

If now the terms of Equation 8 are summed over all of the difunction intervals from the first to the n th, there is obtained:

$$\sum_{i=1}^n R_i = \sum_{i=1}^{n-1} R_i + \sum_{i=1}^{n-1} \Delta Q_i - Q_s \sum_{i=1}^n X_i \quad (9)$$

which simplifies to

$$R_n - R_0 = \sum_{i=1}^{n-1} \Delta Q_i - Q_s \sum_{i=1}^n X_i \quad (10)$$

Since Q_s is a standard signal representing unity, the following expression may be obtained by transposing terms and dividing all terms by n

$$\frac{\sum_{i=1}^n X_i}{n} = \frac{\sum_{i=1}^{n-1} \Delta Q_i}{n} + \frac{R_n - R_0}{n} \quad (11)$$

Consider now the significance of this equation. It may be shown that the term

$$\frac{\sum_{i=1}^n X_i}{n}$$

is the average value of the difunction train from the first through n th difunction signal periods, since the average value of a difunction train over a given interval is obtained by subtracting from the number of plus one signals occurring within the interval the number of minus one signals occurring within the interval, and dividing the

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difference by the total number of signals occurring within the interval. In a similar manner, the term

$$\frac{\sum_{i=1}^{n-1} \Delta Q_i}{n}$$

may be shown to be the integral of the analog divided by the number of difunction signal periods, or in other words, to be the average value of the analog input function over the total interval. Finally, the term

$$\frac{R_n - R_0}{n}$$

merely represents the difference between the final remainder (R_n) and the initial remainder (R_0) divided by the number of difunction signals, and is representative of the conversion error. Thus it may be seen that the average value of the difunction signal generated very closely approximates the average value of the analog input, the error term becoming smaller as the interval over which the signals are averaged is increased. In fact it may be shown that the maximum error which can result is

$$\pm \frac{2}{n}$$

It will be recognized that regardless of whether the analog-to-difunction converter of the invention is employed for converting either a bipolar or unipolar analog signal, if the analog signal is to be representable over its entire range by an equivalent difunction signal train then the maximum incremental integral which may be generated during any difunctional signal period should not exceed the standard unit quantity Q_s by which the integral stored in integrator 16 is modifiable. More specifically, in constructing an analog-to-difunction converter in accordance with the teachings herein set forth, the standard signal source is preferably designed to provide a standard signal equal to the incremental integral signal which is generated when the analog signal is at its maximum value.

With reference now to Fig. 2, there is shown one embodiment of an electronic analog-to-difunction converter, according to the invention, which is operative to present at output terminal 10 a difunction signal train representative of the value of a bipolar analog signal E which is applied to a pair of input terminals 12, one of which is grounded. As shown in Fig. 2, integrator 16 here includes a capacitor 22 and a charging resistor 24 in series therewith, while sensing element 18 comprises a direct current amplifier 26, which may be chopper stabilized if desired, a bistable multivibrator or flip-flop 28, and a pair of two input terminal "and" gates 30 and 32 which are operative under the control of amplifier 26 and in response to the timing signal (t_p) for controlling the conduction state of flip-flop 28.

Before continuing further with the description of the invention, consideration will be given to the designation of the input and output conductors of flip-flop 28. The flip-flop indicates a pair of input conductors which are designated the S input conductor and Z input conductor respectively and a pair of output conductors one of which is designated +1 conductor while the other is designated -1 conductor.

In operation flip-flop 28 will be assumed to be responsive to the application of an input signal to its S input conductor for setting to a conduction state corresponding to the difunction value of +1, and to the application of an input signal to its Z input conductor for setting to the opposite conduction state, which corresponds to the difunction value of -1. In addition it will be assumed that when the flip-flop is in its +1 representing state the voltage presented on its correspondingly designated output conductor has a relatively high level value while the voltage presented on its -1 conductor has a relatively

low level value. Conversely, when the flip-flop is in its -1 representing state the voltage presented on the correspondingly designated output conductor has a relatively high level value whereas the voltage presented on the +1 conductor has a relatively low level value.

Each "and" gate is represented in the drawings by a semicircular hood with a dot (.) in the center thereof and may utilize either vacuum tubes or crystal rectifiers, the gates preferably being structurally similar to the gating circuits illustrated in the article entitled "How an Electronic Brain Works" by Berkeley and Jensen, found on page 45 of the September 1951 issue of Radio-Electronics magazine. Briefly stated, each "and" gate herein disclosed includes two input terminals and a single output terminal and is responsive to the voltage levels of the signals applied to its input terminals for presenting at its output terminal the timing pulse applied to one of its input terminals only when the signal applied to the other input terminal is at its high level value.

Continuing with the description of Fig. 2, standard signal source 20 in this particular embodiment of the invention comprises a pair of relays generally designated 34 and 36, respectively, a pair of "and" gates 38 and 40 operative under the control of flip-flop 28 and in response to a delayed timing pulse signal received from a delay unit 41 for controlling the actuation of the relays, and a standard charge storage capacitor 42 which is employed in conjunction with relays 34 and 36 for periodically discharging integrator capacitor 22 under the control of sensing circuit 18. Referring now with particularity to the circuit of standard signal source 20, relay 34 includes a pair of armatures 44 and 46 across which capacitor 42 is connected, each of these armatures having an associated back contact correspondingly designated with the reference letter *a* and an associated front contact designated with the reference letter *b*. In a similar manner, relay 36 includes a single armature 48 having an associated back contact 48*a* and an associated front contact 48*b*. As shown in Fig. 2, contacts 44*b* and 46*a* of relay 34 are grounded, while contacts 44*a* and 46*b* of relay 34 are respectively connected to armature 48 and contact 48*b* of relay 36. Front contact 48*a* of relay 36, on the other hand, is connected to one terminal *E_s* of a standard voltage source, not shown, through a current limiting resistor 50. The circuit of standard signal source 20 is completed through a feedback connection including a current limiting resistor 52 which interconnects relay contacts 46*a* and 48*b* with the junction of capacitor 22 and resistor 24 in integrator circuit 16.

It will be noted that when relays 34 and 36 are in their normal positions as shown in the drawing, standard charge storage capacitor 42 is connected across the standard voltage *E_s*. Consequently, if it is assumed that the value of limiting resistor is relatively small and that the standard voltage *E_s* is positive, it will be recognized that a positive standard charge *Q_s* is stored in capacitor 42 during each difunction signal period, the charge being given by

$$Q_s = E_s C_s \quad (12)$$

where *C_s* is the capacitance of capacitor 42.

If it is now assumed that integrator capacitor 22 is very large compared to standard charge storage capacitor 42, and that the voltage standard *E_s* is correspondingly large relative to the normal peak signal voltage across capacitor 22, it is clear that operation of relay 36 will function to discharge integrator capacitor 22 in a positive direction by virtue of a transfer of substantially all of the standard charge on capacitor 42. Conversely, if relay 36 remains normal and relay 34 is actuated, the polarity of the charge on capacitor 42 is reversed with respect to ground potential and integrator capacitor 22 will be discharged in a negative direction by a transfer of the charge on capacitor 42.

Consider now the interaction of integrator circuit 16

and standard signal source 20. It will be recalled that the maximum incremental integral (ΔQ) which may be developed by the integrator during any one difunction signal period cannot exceed the standard integral *Q_s*. Stated in terms of the specific circuit of Fig. 2, therefore, the voltage change across capacitor 22 during any one difunction signal period should be incapable of exceeding the standard correction or neutralization voltage contributed by standard signal source 20 through the aforementioned capacitive charge transfer.

It may be shown that if an accuracy of the order of one part in one thousand is desired for the analog-to-difunction converter of the invention, then the maximum integral signal ΔQ which may be generated in any one difunction period should be limited to approximately one thousandth of the maximum value of the analog input signal. In other words, if the analog signal were to be variable over a range of ± 100 volts, then the maximum integral signal which may be generated over difunction signal period should be .1 volt. This parameter of the system of course, is easily controlled by selecting a sufficiently large charging resistor 24 and capacitor 22. It may be shown that the charging time constant (*RC*) for the above voltage range is

$$RC = T / .00101 \quad (13)$$

where

T is the difunction signal period

R is the resistance of resistor 24 and

C is the capacitance of capacitor 22.

It should also be pointed out that for maximum accuracy the charging transient of capacitor 22 should be substantially linear and of constant slope for a constant amplitude input signal, or in other words, should be dependent only on the magnitude of the analog signal and should be substantially independent of the initial voltage across the capacitor.

This requirement is inherently fulfilled in the present invention by virtue of two facts. Firstly, as set forth hereinabove, the time constant of the charging circuit for capacitor 22 is much larger than the difunction signal period. Secondly, the converter is essentially a null seeking system which tends to keep the capacitor voltage at a predetermined reference level, the level in the embodiment of Fig. 2 being ground potential. Consequently the charging current which is integrated by capacitor 22 is substantially independent of the initial charge on capacitor 22; hence the incremental integral signal ΔQ is dependent only upon the analog signal *E*, and may be expressed by the following equation:

$$\Delta Q = \int_0^T i dt = \frac{E}{R} \int_0^T dt = E \times \frac{T}{R} \quad (14)$$

Since the capacitance (*C*) of capacitor 22 is constant, the incremental integral signal may be considered as the voltage increase ΔE across the capacitor, rather than the net charge increase. Thus the net voltage change from the integration is:

$$\Delta E = \frac{\Delta Q}{C} = E \times \frac{T}{RC} \quad (15)$$

It will be remembered now that standard signal source 20 is operative under the control of sensing element 18 to periodically discharge capacitor 22. The standard voltage change across capacitor 22 which is produced by the transfer of charge from capacitor 42 may be expressed as:

$$\Delta E_s = E_s \frac{C_s}{C + C_s} \quad (16)$$

If now the value of the standard voltage is 100 volts, for example, while the capacitance (*C*) of capacitor 22 is one thousand times larger than the capacitance (*C_s*) of

capacitor 42, then from Equation 16 the standard voltage change ΔE_s which may be effected by a charge transfer between capacitors 42 and 22 is .1 volt; this value will in turn be recognized as the maximum incremental voltage change which is produced across integrator capacitor 22 when the analog input signal E is at the limit of its range, namely plus or minus 100 volts.

Consider now the operation of the analog-to-difunction converter of the invention. With reference now to Figs. 3a, 3b and 3c, there are illustrated the waveforms which appear across capacitor 22 for analog input signals of various magnitudes and polarities. In each of these figures there is shown a pair of dotted lines 54 and 56 which represent the threshold voltages at the input to D.C. amplifier 26 below which the output signals from the amplifier are insufficient to open "and" gates 30 and 32 in Fig. 2.

It will be recalled that for the particular embodiment of Fig. 2, the predetermined reference level about which the voltage across capacitor 22 should vary is ground potential. Ideally, therefore, the threshold levels 54 and 56 should both coincide with ground potential. As a matter of practical circuitry, however, some finite voltages of the order of several millivolts above and below ground potential are required before the D.C. amplifier is operative to open an "and" gate so that flip-flop 28 may be triggered by the timing pulse (tp). For purposes of illustration the threshold voltages are exaggerated in the drawings so that their effect on the operation of the converter can best be described.

Since the actuation of standard signal source 20 is controlled from flip-flop 28, and since the flip-flop will remain in its existing conduction state if no input pulse is received from either gate 30 or gate 32, it will be recognized that the charge transfer which takes place at the end of a selected difunction signal period will be in the same sense as that of the preceding period if at the end of the selected period the voltage across capacitor 22 is within the bounds of threshold levels 54 and 56. Although it may at first appear that a substantial error might thereby be introduced in the analog-to-difunction conversion, it may be shown that the maximum error which may be introduced in the generation of n successive difunction signals is $1/n$. Moreover, it may be shown that as reference levels 54 and 56 are brought closer to ground potential, the statistical probability of this error being produced at all becomes smaller and smaller.

Referring now with particularity to Fig. 3a, there is shown the waveform across capacitor 22 when the analog input signal E is zero volts. As illustrated in Fig. 3a, the voltage across capacitor 22 during the first difunction signal period is at a level designated 58 which is above reference level 54. Consequently, a relatively high level signal is applied to gate 30 in Fig. 2, and at the end of the first interval timing pulse (tp) passes through gate 30 and sets flip-flop 28 to its plus one representing state. Assuming that the delay provided by delay unit 41 in Fig. 2 is merely sufficient to permit the switching transients in flip-flop 28 to take place, the delayed timing pulse is then passed through gate 38 and functions to pulse relay 34. Actuation of the relay then in turn functions in the manner previously described to discharge integrator capacitor 22 in a negative direction and thereby decreases the voltage across the capacitor by the amount ΔE_s , as defined in Equation 16, and drives the capacitor voltage to level 60 shown in Fig. 3a.

During the second difunction interval the voltage across capacitor 22 again remains substantially unchanged owing to the fact that the value of the analog signal is zero. Consequently at the end of the second difunction period flip-flop 28 is set to its minus one representing state, relay 36 is actuated, and the voltage across the integrator capacitor is again restored to level 58. The above described process is then repeated, the integrator capacitor

being alternately discharged positively and negatively by standard signal source 20.

Consider now the signal appearing at output terminal 10. Obviously as flip-flop 28 is alternately switched to its plus one and minus one representing condition states the output signal appearing at output terminal 20 will alternately vary between a plus one representing high level difunction signal and a minus one representing difunction signal. If the difunction signal train thus generated is evaluated by adding together the number of plus one representing signals, subtracting therefrom the number of minus one representing signals, and dividing the difference by the total number of signals, it will be seen that the value of the output train is zero corresponding to the value of the analog input signal.

With reference now to Fig. 3b, there is shown the waveform of the capacitor voltage for an applied analog input signal of +50 volts, which represents half scale voltage in the positive direction. It will be noted that the incremental increase in voltage ΔE during each difunction interval is equal to one-half the voltage change ΔE_s produced at the end of each difunction interval by the standard signal source. From the description set forth hereinabove with respect to the operation of the circuit of Fig. 2, it will be recognized that at the ends of the eight difunction intervals shown flip-flop 28 is sequentially set to its +1, +1, -1, +1, +1, +1, -1, and +1 representing states, while relays 34 and 36 are correspondingly energized in the sequence 34, 34, 36, 34, 34, 34, 36 and 34. Evaluation of the difunction sequence over the eight difunction periods shown then gives

$$\frac{6(+1) + 2(-1)}{8} = +\frac{1}{2}$$

which will be recognized as corresponding to the sense of the applied signal and the ratio of its amplitude to full scale voltage in that sense. It should also be noted that the waveform is cyclically repetitive every four difunction intervals, which is of course consistent with difunction notation since one-half is representable in four difunction intervals by three plus ones and one minus one.

Referring now to Fig. 3c, there are shown two waveforms 62 and 64 representing the capacitor voltage under two different conditions for an applied analog signal of -25 volts. Considering initially waveform 62, it will be noted that at the beginning of the first difunction interval capacitor 22 has a slight negative voltage thereacross. This voltage increases negatively during the first difunction interval, at the end of which the capacitor is discharged positively by a plus one representing difunction signal. Again at the end of the second and third difunction intervals capacitor 22 is respectively discharged negatively and positively, in response to sequential difunction output signals of +1 and -1.

Considering now the operation of the converter at the end of the fourth difunction interval, it will be noted that the voltage across capacitor 22 is within the bounds of threshold levels 54 and 56. Accordingly, flip-flop 28 remains in its existing state since both of gates 30 and 32 are closed, and the flip-flop is operative to again generate a plus one representing difunction signal notwithstanding the fact that the capacitor voltage does not exceed the threshold. The converter then again reverses the conduction state of flip-flop 28 at the ends of the fifth, sixth and eighth difunction intervals and thereby further generates sequentially a +1, -1, -1 and +1 during the fifth to eighth intervals, respectively. Evaluating the difunction output train over the eight intervals thus gives $3(+1) + 5(-1)/8 = -1/4$ which corresponds to the sense and magnitude of the applied signal. It will be noted that at the end of the eighth interval the voltage across capacitor 22 is identical to the voltage existing at the beginning of the first difunction interval. Accordingly, if it is assumed that the analog input signal remains constant

at -25 volts, then waveform 62 will recur every eight difunction intervals.

The purpose of waveform 64 in Fig. 3c is to illustrate that a difunction signal train having the same value over eight difunction signal periods may be generated if the initial voltage across capacitor 22 at the beginning of the first difunction interval is different from the initial voltage which resulted in the generation of waveform 62. Thus the difunction signal sequence which produces waveform 64 is -1, +1, -1, +1, -1, -1, +1 and -1, which again equals $-1/4$. It should again be noted that the voltage remainder at the end of the eighth interval is identical to the capacitor voltage at the beginning of the first interval. In addition, it will be noted that the conduction state of flip-flop 28 is reversed at the ends of the second, third, fourth, fifth, seventh and eighth difunction intervals, but remains the same at the end of the first and sixth intervals owing to the fact that the capacitor voltage is within the threshold boundaries.

Summarizing the operation of the bipolar analog-to-difunction converter of Fig. 2, it will be recognized that the converter functions to integrate the analog signal with respect to time over each difunction signal period, to sample the integral developed at the end of each difunction period for generating a plus one difunction signal if the value of the integral is above a predetermined reference level and a minus one difunction signal if the value of the integral is less than the reference level, and to decrease the magnitude of the integral at the end of each difunction interval by either adding thereto or subtracting therefrom a standard unit quantity, depending upon whether the difunction signal generated was a minus one or a plus one, respectively.

It will be recognized that the analog-to-difunction converter of Fig. 2 may be modified in numerous particulars without departing from the spirit and scope of the invention. For example there is shown in Fig. 4 an alternate form of standard signal source 20 which may be substituted directly in the circuit of Fig. 2. In this particular standard signal source each of relays 34 and 36 includes only one associated set of make and break contacts, while two matched capacitors 66 and 68 are provided for discharging the integrator capacitor by selectively either adding a standard charge or subtracting a standard charge. It will also be noted that the standard signal source of Fig. 4 utilizes two standard voltage sources $+E_s$ and $-E_s$, respectively, both of which have the same magnitude.

In the description of Fig. 2 set forth hereinabove it has been assumed that the applied analog signal was a variable voltage signal E. However, it should be clear that the electronic analog-to-difunction converters of the invention will operate equally well in response to analog signals wherein the forcing function is electrical current. With reference to Fig. 5, for example, there is shown a combined integrator and input instrument which may be substituted in the circuit of Fig. 2 for generating a difunction output signal train representative of air pressure.

As shown in Fig. 5, the combined circuit includes an integrator capacitor 22 which is connected in series with an ion chamber generally designated 70, the ion chamber being operative to produce in a collector rod 72 a current proportional to the density of air introduced to the chamber through a static tube 74. The current is produced by the combined action of a long-life radioactive isotope layer 76 which functions to ionize the gas within the chamber, and a cylindrical accelerating electrode 78 which functions to drive the ions to the lower potential collector rod 72. If it is assumed that the temperature of the chamber is substantially constant and that the radioactive isotope has a reasonably long half-life, it is clear that the current collected and thereafter integrated by capacitor 22 is directly proportional to the molecular density of the air within the ion chamber. Consequently

the output difunction signal train is non-numerically representative of the air pressure being measured by the ion chamber.

It will be noted that the ion chamber of Fig. 5 is essentially a unidirectional device, or in other words, can only charge capacitor 22 in one direction. Consequently the output difunction which is produced by the converter of Fig. 2 can only vary between all plus ones, representing full scale current, and alternate plus ones and minus ones representing zero current. It may be seen, therefore, that the effective bandwidth of the output signal train is halved, since there is no analog input representable by the difunction signal patterns between zero and all minus ones, which normally represents full-scale in the negative direction. This problem may be avoided by the utilization of a unidirectional analog-to-difunction converter, one of which will now be described.

Referring now to Fig. 6, there is shown an analog-to-difunction converter, according to the invention, which is operative to produce at a pair of output terminals 10 a difunction output signal train non-numerically representative of the magnitude of a unipolar analog input signal E applied to input terminals 12. The basic elements of integrator 16 are identical with those shown and described hereinabove with respect to the embodiment of Fig. 2, and are correspondingly designated. However, the component parts of sensing element 18 and standard signal source 20 are here modified to illustrate alternative structures which may be employed in electronic embodiments of the invention.

In the embodiment of Fig. 6 sensing element 18 includes a low-drift A.C. amplifier 80 whose input circuit is connected to integrator 16 and whose output circuit is coupled through a relatively large capacitor 82 to a cathode follower circuit generally designated 84. The cathode follower output signal is then applied to one input terminal of a two terminal "and" gate generally designated 86, the other input terminal of the "and" gate being utilized for receiving the timing signal (tp) while the output circuit of the gate is connected to standard signal source 20.

It should be pointed out that the sensing circuit of Fig. 6 is preferably employed in those applications where an analog signal is available for sampling over only a relative short time of the order of seconds. In such an application the inherent drift of amplifier 80 may be rendered substantially inconsequential by utilizing a switch 88 for clamping the amplifier input and output circuits at predetermined levels before the circuit is actuated to generate a difunction output signal train. At the end of the sampling interval switch 88 is then again closed to re-establish the input and output levels, thereby providing in essence a very low frequency chopper stabilizer in which switch 88 functions as a chopper.

The standard signal source 20 of Fig. 6 includes as its principal elements a thyatron tube 90 whose grid circuit receives pulses passed by gate 86 and whose plate is connected in series with a winding 92 of a relay generally designated 94. Coupled in parallel with winding 92 is an output transformer 96 having two output windings 97 and 98 which are poled as shown and which are interrogated once per difunction signal period to determine whether a plus one or minus one representing difunction signal is being generated.

Relay 94 includes mechanically intercoupled armatures 100, 102 and 104, each having a correspondingly designated back contact identified by the suffix letter a, armatures 100 and 102 also including an associated front contact identified by the suffix letter b. Armature 104 is connected to relay winding 92 and functions when in its normal position to apply the plate voltage B+ to the thyatron circuit and to open the plate voltage supply circuit when the thyatron has been fired to actuate relay 94, thereby permitting the thyatron to deionize.

The functions of armatures 100 and 102, on the other

hand, is to normally connect standard charge capacitor 42 across a standard voltage source E_s through a limiting resistor 50 to thereby permit the storage in the capacitor of a standard charge, in the same manner as previously described for the circuit of Fig. 2. Actuation of the relay then functions to reverse the ground connection to capacitor 42 and to interconnect the capacitor 42 with capacitor 22 in integrator 16 through a current limiting resistor 52, thereby providing a means for discharging capacitor 22 in the negative direction by a fixed amount whenever relay 94 is actuated.

Consider now the operation of the analog-to-difunction converter of Fig. 6. After switch 88 is opened to initiate operation of the converter, amplifier 80 serves to apply to gate 86 an amplified signal corresponding to the voltage across integrator capacitor 22, gate 86 being opened to pass the next occurring timing pulse each time the capacitor voltage exceeds a predetermined reference level. Each timing pulse thus passed functions to trigger the thyatron which in turn actuates relay 94 to both squelch the thyatron and transfer charge to the integrator for discharging capacitor 22.

Assume now that the analog signal is variable over a range from 0 volts to +100 volts; assume also that the reference level at which gate 86 opens is selected so that if integrator capacitor 22 is charged at its maximum rate, or in other words, if the analog signal is +100 volts, the incremental voltage increase across capacitor 22 through one difunction interval is just enough, when amplified by amplifier 80, to open gate 86. Obviously then, if an analog signal of zero volts is applied to the integrator, the capacitor voltage will not increase and gate 86 will not open. Accordingly, thyatron 90 will not fire and interrogation of output windings 97 and 98 with suitable pulse gates, not shown, will result in the generation of a minus one difunction signal during each and every difunction interval.

With reference now to Figs. 7a and 7b, there are shown waveforms of the integrator capacitor voltage for analog input signals of various magnitudes. For example, the waveform 106 in Fig. 7a illustrates the capacitor voltage in response to an input signal of +100 volts, which will be remembered as being the upper range of the input signal. Recalling that a signal of this magnitude charges capacitor 22 at its maximum rate, and that this rate is sufficient to drive the capacitor to the predetermined reference level, here designated as L, it will be recognized that an input signal of +100 volts will function to trigger the thyatron during each difunction time interval. Consequently interrogation of output windings 97 and 98 in Fig. 6 will produce a continuous train of plus one representing difunction signals.

Consider next the application of an analog signal of +50 volts to the integrator circuit. The voltage across capacitor 22 will then follow the waveform designated 108 in Fig. 7a, and will reach the level (L) during every other difunction interval. Accordingly the difunction signals derived by interrogation of output windings 97 and 98 will alternately represent plus ones and minus ones. In a similar manner the waveforms 110 and 112 in Fig. 7b represent the capacitor voltage waveforms in response to analog input signals of +66⅔ volts and +25 volts respectively, the sequential difunction signals thereby generated being -1, +1, +1, -1, +1, +1 representing +⅓ for waveform 110, and -1, -1, +1, -1, -1, +1, -1, +1 representing -¼ for waveform 112.

It should be emphasized that for the foregoing discussion a normalized difunction system has been assumed in which the individual difunction signals represent either a plus one or minus one. Thus analog input signals having values of +100, +50 and 0 volts are represented by difunction signal trains whose values are +1, 0 and -1, respectively. However, if the difunction notation is changed so that the difunction signals represent either a plus one or zero instead of plus one and minus one,

respectively, then the difunction signal trains generated in response to analog input signals of +100, +50 and 0 volts have values of +1, +½, and 0, respectively. It is to be expressly understood that no structural changes in the circuit of Fig. 6 are required to achieve this result, but only a change in the numerical significance attributed to the difunction signals of one level.

It should also be pointed out that although the circuit of Fig. 6 utilizes transformer 96 for deriving its output intelligence information, the same intelligence information is contained in the output signal from "and" gate 86 in sensing circuit 18. More specifically, the appearance of a timing signal (tp) at the output circuit of gate 86 at the beginning of a difunction interval indicates a plus one representing difunction signal for that interval, whereas the absence of a timing signal indicates either a minus one or zero representing signal, depending upon whether the converter is to present its output signal in a normalized +1, -1 difunction system or in a +1, 0 difunction system.

The specific embodiments of the invention thus far described have all been electronic devices; however, it will be recalled that the basic and motivating concept of the invention is equally applicable to mechanical, electro-mechanical or hydraulic analog-to-difunction converters. With reference to Fig. 8, for example, there is shown a bipolar electromechanical analog-to-difunction converter in accordance with the invention which again includes the three basic components set forth in Fig. 1, namely an integrator 16 for receiving a mechanical signal represented by a displacement F, a sensing element 18 for indicating when the integral developed during a difunction interval exceeds a predetermined reference level and for presenting at a pair of output terminals 10 a pair of complementary output signals representative of the equivalent difunction output signal train, and a standard signal source 20 operable under the control of the sensing element whenever the integral exceeds the predetermined reference level.

Integrator 16 includes a conventional wheel-and-disk integrator 113, the disk being driven by a motor 114 at a rate (dt) and in synchronism with timing signal source 14, while the wheel is driven by the disk at a rate proportional to the magnitude of the displacement F which positions the wheel. The wheel shaft is then applied to one input of a conventional mechanical differential 116 through a suitable reduction gear unit, not shown.

The other input shaft of differential 116 is coupled to the shaft of a bidirectional notching motor 118 within standard signal source 20, the notching motor being operative in response to control signals received from sensing element 18 for rotating its shaft through a discrete angle each time the motor is actuated. The output shaft of differential 116, on the other hand, is coupled to sensing element 18 wherein its rotational position is employed for controlling the actuation of a suitable commutator or switching mechanism, such as a toggle switch 120.

As shown in Fig. 8 toggle switch 120 includes an armature connected to timing signal source 14 for receiving the timing signal (tp), and a pair of contacts 122 and 124 which are selectively engageable by the armature in accordance with the rotational position of the output shaft from the differential. These contacts are then connected to notching motor 118 so that the notching motor is operative to rotate a discrete amount in one direction when contact 122 is engaged by its associated armature and a timing pulse is received, and to rotate a discrete amount in the opposite direction when contact 124 is engaged by the toggle switch armature and a timing pulse is received.

In operation, if the magnitude of displacement F is zero, then the wheel of integrator 113 is positioned at the center of the disk and hence differential 116 receives

no rotational input from integrator 113. Accordingly, notching motor 118 will be stepped in one direction during one difunction interval and in the opposite direction during the next under the control of toggle switch 120 which is reversed each time the notching motor is reversed.

Assume now that displacement F drives the integrator wheel to some intermediate point on the associated disk. It will be recognized that the output shaft of the differential will be rotated during each difunction interval at a rate proportional to the magnitude of the displacement, the angular rotation of the output shaft over the difunction interval corresponding to the integral with respect to time of the analog input signal. If the integral exceeds the predetermined reference level, toggle switch 120 is reversed and notching motor 118 is activated to compensate for the integral signal generated by driving the output shaft in the opposite direction through a discrete angle; this operation in turn functions to restore the toggle switch to its original state.

The operation of the converter of Fig. 8 during ensuing difunction intervals is substantially identical with the operation of the bipolar analog-to-difunction converter of Fig. 2, and the waveforms of Figs. 3a, 3b and 3c are equally applicable to the converter of Fig. 8. It should be pointed out that in applying these waveforms to Fig. 8 the ordinate represents the rotational position of the output shaft from mechanical differential 116 rather than the voltage across an integrator capacitor as described for Fig. 2.

It is to be expressively understood, of course, that numerous other modifications and alterations may be made in the analog-to-difunction converters herein disclosed without departing from the invention. For example, it will be recognized that the electromechanical converter of Fig. 8 may be modified to provide a converter of unipolar signals, in which instance the converter would be analogous to the unipolar converter of Fig. 6. Accordingly it is to be expressly understood that the spirit and scope of the invention are to be limited only by the spirit and scope of the appended claims.

What is claimed as new is:

1. An analog-to-difunction converter for converting an applied analog signal to a difunction output signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a first numerical quantity or a second value representing a second numerical quantity, each of the difunction signals in the train having a predetermined period, said analog-to-difunction converter comprising: an integrator; means for applying the analog signal to said integrator, said integrator being responsive to the analog signal for producing an integral signal representing the integral with respect to time of the analog signal; a sensing element coupled to said integrator and operative to periodically sample the magnitude of said integral signal once per difunction signal period, said sensing element including means for generating an output difunction signal representing the first numerical quantity whenever the magnitude of said integral signal exceeds a predetermined reference level and an output difunction signal representing the second numerical quantity whenever the magnitude of said integral signal is less than said predetermined level; and a standard signal source coupled to said integrator and to said sensing element, said standard signal source being operable when said sensing element generates a difunction signal representing the first numerical quantity for applying a standard signal to said integrator to decrease the magnitude of said integral signal by a fixed amount corresponding to said standard signal and in a sense corresponding to the direction of said reference level with respect to said integral signal.

2. The analog-to-difunction converter defined in claim 1 wherein said standard signal source further includes means responsive to each difunction signal representing

the second numerical quantity for applying to said integrator a standard signal to decrease the magnitude of said integral signal by a fixed amount corresponding to said standard signal and in a sense opposite to the first named sense.

3. An analog-to-difunction converter for converting an applied analog signal to a difunction output signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a first numerical quantity or a second value representing a second numerical quantity, each of the difunction signals in the train having a predetermined period, said analog-to-difunction converter comprising: an integrator; means for applying the analog signal to said integrator, said integrator being responsive to the analog signal for producing an integral signal representing the integral with respect to time of the analog signal; a sensing element coupled to said integrator and operative to periodically sample the magnitude of said integral signal once per difunction signal period, said sensing element including means for generating an output difunction signal representing the first numerical quantity whenever said integral signal is positive with respect to a predetermined reference level and an output difunction signal representing the second numerical quantity whenever the magnitude of said integral signal is negative with respect to a predetermined level; and means coupled to said integrator and operable when said sensing element generates a difunction signal representing the first numerical quantity, for decreasing the magnitude of said integral signal by a fixed amount and in a negative sense with respect to said reference level.

4. An analog-to-difunction converter for converting an applied analog signal to a difunction output signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a plus one or a second value representing a minus one, each of the difunction signals in the train having a predetermined period, said analog-to-difunction converter comprising: an integrator; means for applying the analog signal to said integrator, said integrator being responsive to the analog signal for producing an integral signal representing the integral with respect to time of the analog signal; a sensing element coupled to said integrator and operative to periodically sample the magnitude of said integral signal at the end of each difunction signal period for generating a plus one representing difunction signal whenever said integral signal is positive with respect to a predetermined reference level and a minus one representing difunction signal whenever the magnitude of said integral signal is negative with respect to said predetermined level; and a standard signal source coupled to said integrator and to said sensing element, said standard signal source being responsive to each plus one representing difunction signal for decreasing by a fixed amount the magnitude of said integral signal in a sense negative with respect to said reference level, and to a minus one representing signal for decreasing by said fixed amount the magnitude of said integral signal in a sense positive with respect to said reference level.

5. An electronic analog-to-difunction converter for converting an applied analog signal to a difunction signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a first numerical quantity or a second value representing a second numerical quantity, each of the difunction signals in the train having a predetermined signal period, said analog-to-difunction converter comprising: an integrator circuit including a capacitor; means for applying the analog signal to said integrator circuit to vary the charge on said capacitor in accordance with the magnitude of the analog signal and in a sense corresponding to the polarity of the analog signal; a sensing circuit coupled to said capacitor, said sensing circuit being operative to periodically sample the charge on said capacitor at the end of each difunction signal

period to produce a control signal whenever the charge on said capacitor exceeds a predetermined charge in one sense; standard charge storage means; means for establishing a standard charge on said charge storage means during each difunction signal period; means responsive to said control signal for connecting said standard charge means to said capacitor for discharging said capacitor through said charge storage means to decrease the charge on said capacitor in said one sense by substantially said standard charge; and means responsive to said control signal for presenting a difunction signal having said first value during each difunction signal period after the charge on said capacitor has exceeded said predetermined charge and a difunction signal having said second value during the other difunction signal periods.

6. An electronic analog-to-difunction converter for converting an applied analog signal to a difunction signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a first numerical quantity or a second value representing a second numerical quantity, each of the difunction signals in the train having a predetermined signal period, said analog-to-difunction converter comprising: an integrator circuit including an integrator capacitor; means for applying the analog signal to said integrator circuit to vary the charge on said capacitor in accordance with the magnitude of the analog signal and in a sense corresponding to the polarity of the analog signal; a sensing circuit coupled to said capacitor, said sensing circuit being operative to periodically sample the voltage across said capacitor at the end of each difunction signal period to produce a difunction signal representing said first value whenever the voltage is positive with respect to a predetermined voltage, and to produce a difunction signal representing said second value whenever the voltage is negative with respect to said predetermined voltage; standard charge storage means including at least one capacitor; means for establishing a standard charge on said charge storage means during each difunction signal period; and means responsive to difunction signals representing said first value for connecting said standard charge means to said integrator capacitor through said charge storage means to decrease the voltage on said integrator in a negative sense relative to said pre-voltage by a fixed amount corresponding to said standard charge.

7. The electronic analog-to-difunction converter of claim 6 which further includes means responsive to each difunction signal representing said second value for connecting said standard charge storage means to said integrator capacitor for discharging said integrator capacitor through said charge storage means in a positive sense relative to said predetermined voltage to decrease the voltage on said capacitor by said fixed amount corresponding to said standard charge.

8. An electronic analog-to-difunction converter for converting an applied bipolar analog signal to a difunction signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a plus one or a second value representing a minus one, each of the difunction signals in the train having a predetermined signal period, said analog-to-difunction converter comprising: an integrator circuit including a capacitor; means for applying the analog signal to said integrator circuit to vary the charge on said capacitor in accordance with the magnitude of the analog signal and in a sense corresponding to the polarity of the analog signal; a sensing circuit coupled to said capacitor, said sensing circuit being operative to periodically sample the voltage on said capacitor once per difunction signal period to produce a plus one representing difunction signal when the capacitor voltage is positive with respect to a predetermined voltage, and to produce a minus one representing difunction signal when the capacitor voltage is negative with respect to

said predetermined voltage, standard charge storage means; means for establishing a standard charge on said charge storage means during each difunction signal period; and means operable to connect said standard charge means to said capacitor once per difunction period for discharging said capacitor through said charge storage means to decrease the voltage on said capacitor in a sense opposite to the sense of said capacitor voltage with respect to said predetermined voltage when last sampled, and by a fixed voltage corresponding to said standard charge.

9. The electronic analog-to-difunction converter defined in claim 8 wherein said sensing circuit includes a D.C. amplifier coupled to said integrator and operative to amplify the signal appearing across said capacitor, and a flip-flop coupled to said amplifier and being selectively switchable to either a plus one representing conduction state or a minus one representing conduction state, and gating means operable at the end of each difunction signal period and in response to the amplified signal from said amplifier for switching said flip-flop to its plus one representing state when said capacitor voltage exceeds said predetermined voltage and to its minus one representing state when said capacitor voltage is less than said predetermined voltage.

10. An electronic analog-to-difunction converter for converting an applied unipolar analog signal to a difunction signal train, said difunction signal train being composed of a plurality of bivalued difunction signals having either a first value representing a plus one or a second value representing a zero, each of the difunction signals in the train having a predetermined signal period, said analog-to-difunction converters comprising: an integrator circuit including a capacitor; means for applying the analog signal to said integrator circuit to vary the charge on said capacitor in accordance with the magnitude of the analog signal and in a sense corresponding to the polarity of the analog signal; a sensing circuit coupled to said capacitor, said sensing circuit being operative to periodically sample the voltage on said capacitor once per difunction signal period to produce a plus one representing difunction signal when the capacitor voltage is positive with respect to a predetermined reference level, and to produce a zero representing difunction signal when the capacitor voltage is negative with respect to said predetermined reference level; standard charge storage means; means for establishing a standard charge on said charge storage means during each difunction signal period; and means operable when said sensing element produces a plus one representing difunction signal for discharging said capacitor by substantially said standard charge whereby the voltage across said capacitor is decreased by a predetermined amount corresponding to said standard charge.

11. The electronic analog-to-difunction converter defined in claim 10 wherein said sensing element includes a low drift A.C. amplifier coupled to said capacitor for producing an amplified signal corresponding to the voltage appearing across said capacitor, and a gate circuit coupled to said amplifier and responsive to said amplified signal for producing an output signal when said capacitor voltage exceeds said predetermined reference level at the end of a difunction signal period.

12. The method of generating a difunction signal train representative of the magnitude of an analog signal, each difunction signal in the train having a predetermined period and having either a first value representing a first number or a second value representing a second number corresponding in magnitude but opposite in sign to said first number, said method comprising the steps of: generating a first signal corresponding to the integral with respect to time of the analog signal, combining a standard signal with the first signal whenever the first signal exceeds a predetermined value at the end of a difunction signal period to reduce the first signal

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by substantially the value of the standard signal, and generating a difunction signal having said first value during each signal period after the combining step has been performed, and a difunction signal having said second value during all other signal periods.

13. The method of generating a difunction signal train representative of the magnitude of an analog signal, each difunction signal in the train having a predetermined period and having either a first value representing a first number or a second value representing a second number, said method comprising the steps of generating an integral signal corresponding to the integral with respect to time of the analog signal, generating a difunction signal having said first value when the integral signal is positive with respect to a predetermined reference

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level at the end of a difunction signal period, and a difunction signal having said second value when the integral signal is negative with respect to the reference level at the end of a difunction signal period, and reducing the integral signal by a fixed amount and in a sense negative with respect to the reference level each time a difunction signal having said first value is generated.

14. The method defined in claim 13 which includes the additional step of increasing the integral signal by a fixed amount and in a sense positive with respect to the reference level each time a difunction signal having said second value is generated.

No references cited.