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(19) **United States**(12) **Patent Application Publication****Une et al.**(10) **Pub. No.: US 2007/0207618 A1**(43) **Pub. Date: Sep. 6, 2007**(54) **DRY ETCHING METHOD****Publication Classification**

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(57) **ABSTRACT**

The invention provides a dry etching method for performing a wiring process on a semiconductor substrate using a plasma etching apparatus, wherein the wiring process is performed without causing disconnection or deflection of the wiring. The invention provides a dry etching method for performing a wiring process on a semiconductor substrate using a plasma etching apparatus, wherein during a step for etching a material **12** to be etched using a mask pattern composed of a photoresist **15** and inorganic films **14** and **13** made of SiN, SiON, SiO and the like formed on the material **12** to be etched, a mixed gas formed of a halogen-based gas such as chlorine-containing gas or bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF₄, CHF₃, SF₆ and NF₃ is used to reduce the mask pattern and the processing dimension of the material to be etched substantially equally during processing of the material **12** to be etched.

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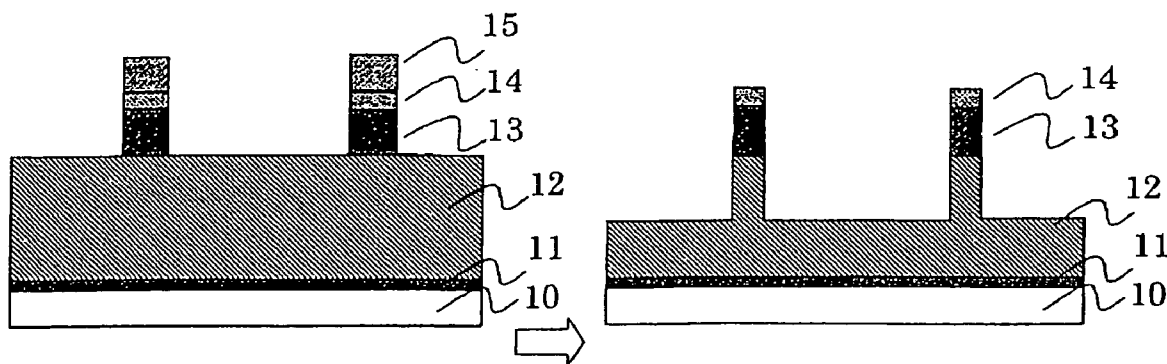


FIG. 1

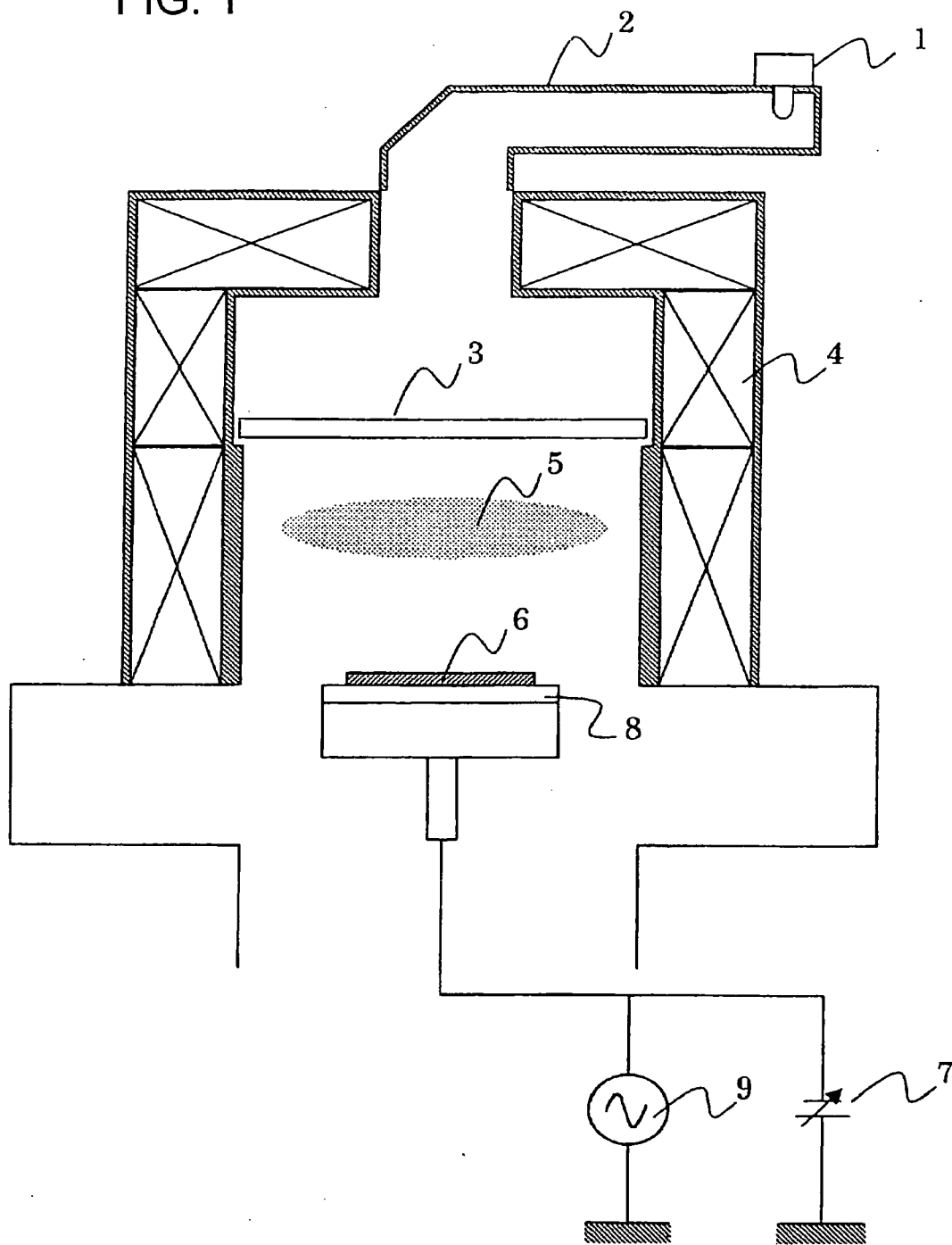


FIG. 2A

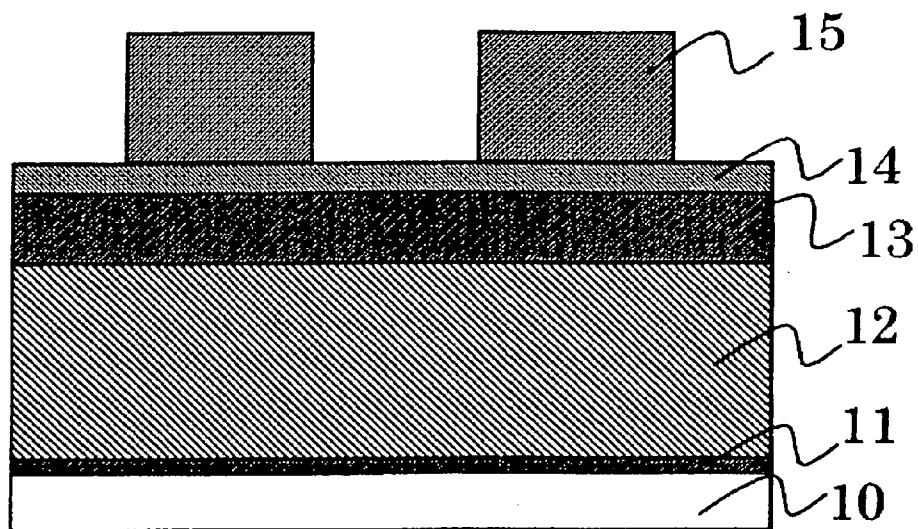


FIG. 2B

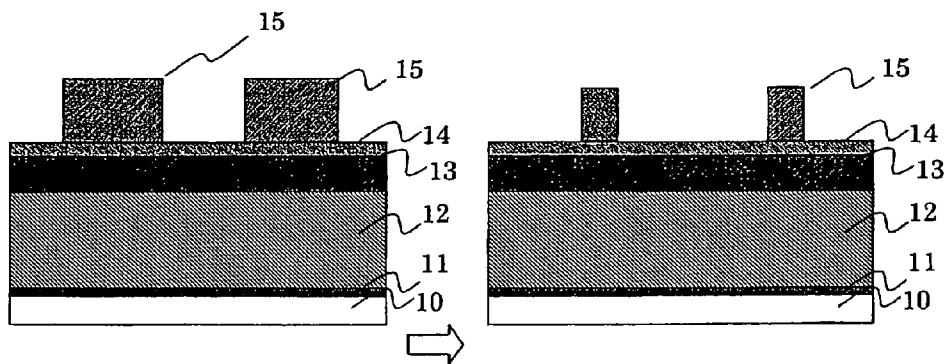


FIG. 2C

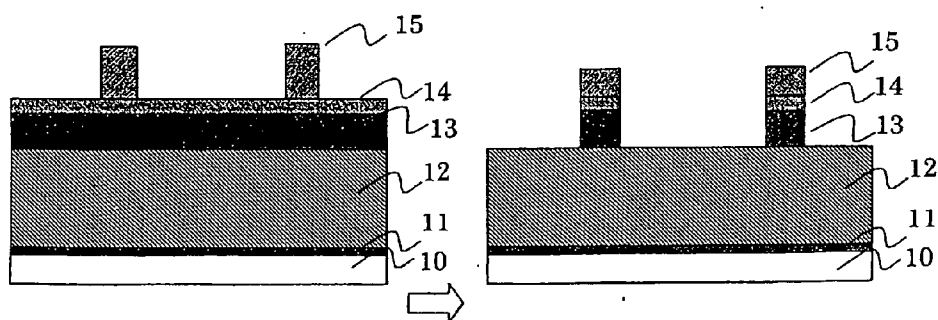


FIG. 2D

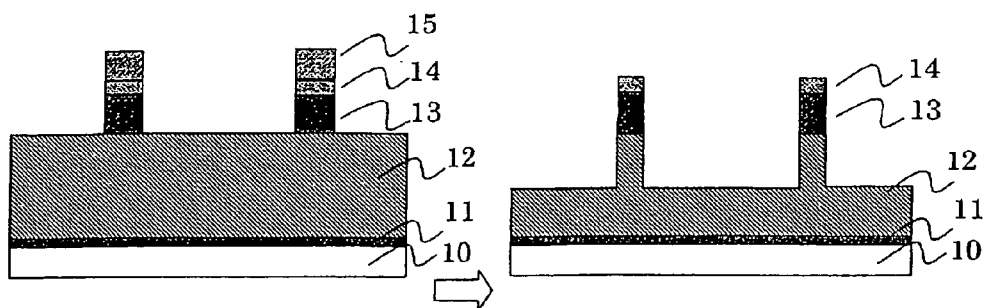


FIG. 2E

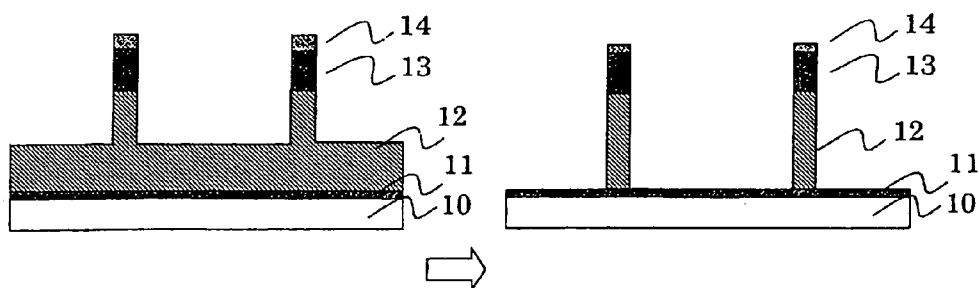


FIG. 3A

RELATIONSHIP BETWEEN RF BIAS
AND REDUCTION RATIO

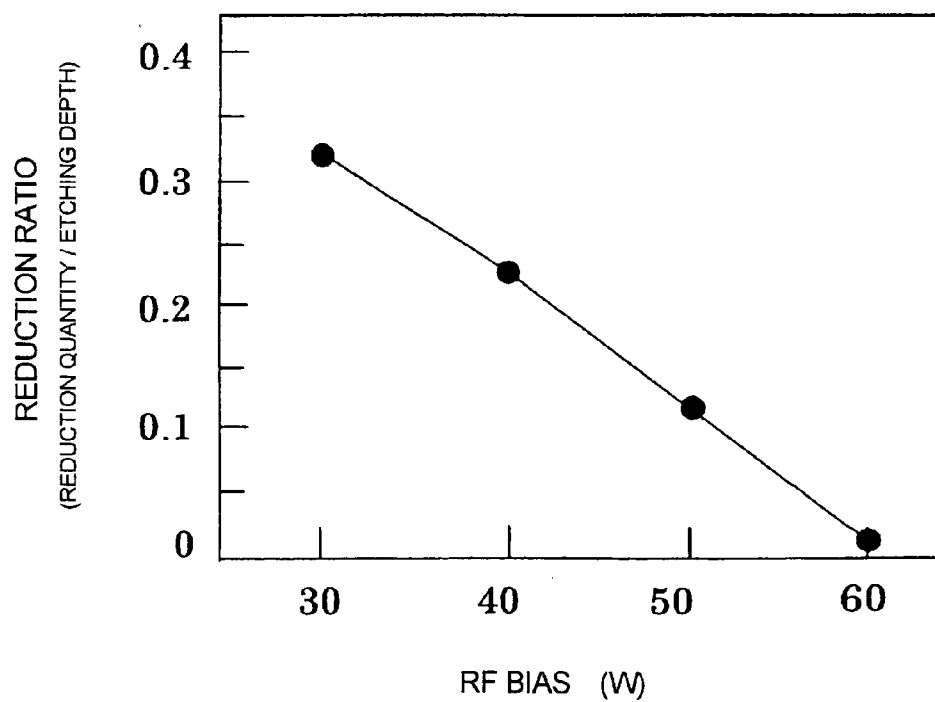
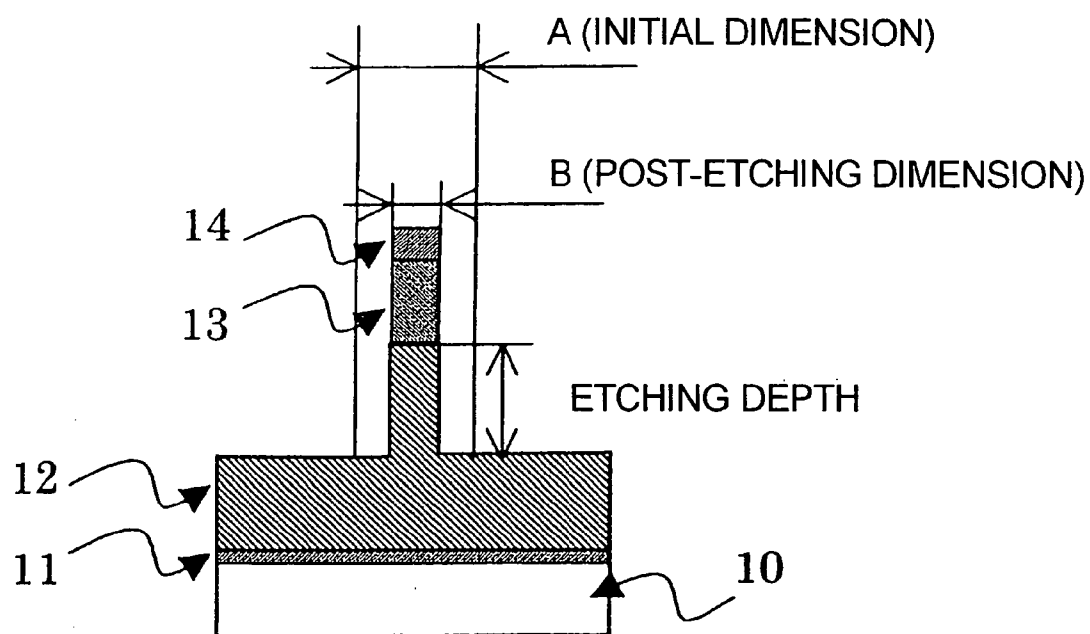


FIG. 3B



REDUCTION QUANTITY

$$= A \text{ (INITIAL DIMENSION)} - B \text{ (POST-ETCHING DIMENSION)}$$

DRY ETCHING METHOD

[0001] The present application is based on and claims priority of Japanese patent application No. 2006-54914 filed on Mar. 1, 2006, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a method for etching semiconductor devices. More specifically, the present invention relates to a dry etching method capable of reducing the wiring dimension without causing defective pattern by reducing the processing dimension simultaneously while processing a material to be etched which is the wiring layer disposed on the semiconductor substrate.

[0004] 2. Description of the Related Art

[0005] Recently, along with the advanced integration technology accompanying the increase in processing speed of semiconductor devices, there are increasing demands for enhancing the miniaturization processes in the field of gate material processing and the like. In the field of dry etching, generally in order to miniaturize the pattern, the photoresist pattern used as the mask is reduced in dimension via dry etching prior to processing the material to be etched, so as to reduce the processing dimension of the material to be etched.

[0006] Along with the further advancement of miniaturization, ArF resist has been adopted as the material for the photoresist mask capable of being exposed via an ArF laser, which is capable of forming a micropattern with higher accuracy. However, since ArF resist cannot be deposited as thick as the conventional mask members, and since ArF has a high etching rate, it has a property vulnerable to etching. Therefore, the ArF resist has a drawback in that the mask is removed during processing of the material to be etched, making it impossible to perform fine wiring process of the material to be etched with high accuracy. In order to overcome this problem, an inorganic film layer composed of SiON, SiN, SiO or the like is disposed between the photoresist mask and the material to be etched, wherein the inorganic film layer is processed via dry etching using a reduced photoresist mask pattern, according to which an inorganic film mask having a slow etching rate is formed to realize stable processing of the material to be etched. This technique is disclosed for example in Japanese patent application laid-open publication No. 9-237777 (patent document 1).

[0007] However, according to the method for reducing the photoresist pattern dimension via dry etching, it is necessary to ensure a photoresist mask thickness required for processing the inorganic film layer, so there is a limitation in the reduction thickness of the processing dimension.

SUMMARY OF THE INVENTION

[0008] The object of the present invention is to provide a dry etching method capable of reducing the processing dimension during processing of the material to be etched, and realizing fine processing without causing drawbacks such as disconnection and deflection of the material to be etched due to mask defection.

[0009] The above object can be realized by using a patterned photoresist as the mask so as to process an inorganic layer via dry etching to form an inorganic film mask, and then simultaneously reducing the inorganic film mask and the material to be etched during the process for etching the material to be etched.

[0010] According to this processing method, since the pattern dimension of the inorganic film mask is reduced after forming the inorganic film mask, drawbacks such as collapse of the photoresist mask do not occur.

[0011] Furthermore, even by adopting the conventional method for reducing the photoresist mask dimension via dry etching together with the present invention, there is no need to perform excessive reduction of the photoresist mask, so the conventional problems such as collapse of pattern or disconnection of the wiring layer by reduction do not occur.

[0012] By the methods described above, the present invention enables to reduce the processing dimension significantly and perform fine wire processing without causing disconnection or deflection of the wiring of the material to be etched which may accompany the reduction of the processing dimension.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a schematic cross-sectional view of a microwave plasma etching apparatus to which the etching method of the present invention is applied;

[0014] FIG. 2A is a cross-sectional view showing the relevant portion of a semiconductor substrate after forming a resist mask according to an embodiment of the present invention;

[0015] FIG. 2B is a cross-sectional view showing the relevant portion of a semiconductor substrate during a resist mask reduction process according to an embodiment of the present invention;

[0016] FIG. 2C is a cross-sectional view showing the relevant portion of a semiconductor substrate during the etching process of SiON film and SiN film according to an embodiment of the present invention;

[0017] FIG. 2D is a cross-sectional view showing the relevant portion of a semiconductor substrate during the etching process for reducing the SiON film and SiN film and reducing the polysilicon film according to an embodiment of the present invention;

[0018] FIG. 2E is a cross-sectional view showing the relevant portion of a semiconductor substrate during the etching process of the polysilicon film according to an embodiment of the present invention;

[0019] FIG. 3A is a graph describing the RF bias dependency of the reduction rate according to the present invention; and

[0020] FIG. 3B is a drawing illustrating the etching depth and the lateral direction etching of the mask according to FIG. 3A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Now, the plasma etching method according to the present invention will be described. FIG. 1 illustrates a plasma etching apparatus to which the dry etching method according to the present invention is applied. The illustrated plasma etching apparatus is an example of a microwave plasma etching apparatus utilizing microwaves and mag-

netic field as means for generating plasma. Microwaves generated by a magnetron **1** travel through a waveguide **2** and a quartz panel **3** to enter a vacuum chamber. Solenoid coils **4** are disposed around the vacuum chamber, which generate a magnetic field that acts together with the microwaves entering the vacuum chamber to cause electron cyclotron resonance (ECR). Thereby, process gases can efficiently be turned into plasma **5** with high density. A processing wafer **6** is held onto the electrode via electrostatic chuck by applying a DC voltage to a substrate stage **8** from an electrostatic chuck power supply **7**. Furthermore, a high-frequency power supply **9** is connected to the electrode, applying high-frequency power (RF bias) so as to provide an accelerating potential in the perpendicular direction with respect to the wafer to the ions in the plasma. The gas used for etching is discharged after etching through an exhaust port disposed on the lower portion of the apparatus via a turbo pump—dry pump (not shown).

[0022] Plasma etching apparatuses such as a microwave plasma etching apparatus, an inductively coupled plasma etching apparatus, a helicon wave plasma etching apparatus and a double-frequency-excited parallel plate plasma etching apparatus are adopted.

[0023] FIGS. 2A through 2E illustrate the manufacturing method of a semiconductor device using the plasma etching apparatus of FIG. 1. FIG. 2A shows the structure of a sample used in the present embodiment, FIG. 2B shows the step of reducing the processing dimension of the photoresist mask, FIG. 2C shows the mask forming process of the SiON film and SiN film, FIG. 2D shows the step of processing the mask and polysilicon film and the step of reducing the processing dimension, and FIG. 2E shows the step of processing the polysilicon film.

[0024] The example of the structure of a sample used according to one preferred embodiment of the present invention is shown in FIG. 2A. A gate oxide film **11** (2 nm), a polysilicon film **12** (film thickness 100 nm), an SiN film **13** (50 nm), an SiON film **14** (25 nm) and a photoresist **15** (250 nm) are sequentially formed on a silicon substrate **10** with a diameter of 12 inches, and thereafter, a mask pattern is formed via photolithography technology.

[0025] FIG. 2B shows the step of reducing the processing dimension of the photoresist mask that has been performed conventionally, and for example, etching is performed using plasma generated from a mixed gas having O₂ gas added to Ar gas, with the processing pressure set to 0.2 Pa and the microwaves set to 600 W. The O₂ gas flow rate determines the reducing rate of the photoresist, and approximately 10% of O₂ gas is added so as to set the reduction rate to approximately 1.5 nm/sec. The reduction rate increases by increasing the amount of O₂ gas. According to the present embodiment, a pattern with an initial photoresist pattern dimension of 100 nm is subjected to processing for 43 seconds, by which the photoresist pattern dimension is narrowed down to 35 nm.

[0026] According to the mask forming process shown in FIG. 2C, the photoresist **15** is used as a mask to etch the SiON film **14** and the SiN film **13**. The etching process is performed while having the interface with the polysilicon film **12** detected via an etching monitor such as an EPD (end point detector). As for processing conditions, for example, etching is performed by applying 100 W of RF bias to plasma generated from a mixed gas composed of CF₄ gas and CHF₃ gas mixed with a ratio of 1:1 and with the

processing pressure set to 0.8 Pa. The etching of the SiN film **13** is ended when the surface of the polysilicon film **12** is detected.

[0027] The step of reducing the processing dimension of the polysilicon film illustrated in FIG. 2D is the characteristic step of the present invention, wherein the pattern dimension is reduced by performing etching in the depth direction and simultaneously performing etching in the lateral direction using the pattern of the SiON film **14** and the SiN film **13** formed in FIG. 2C as the mask. By using CF₄ together with Cl₂, it becomes possible to etch the mask material simultaneously while etching the polysilicon film **12**. As for processing conditions, for example, 30 W of RF bias is applied to plasma generated by applying 900 W of microwaves to a mixed gas composed of Cl₂ gas and CF₄ gas with a ratio of 1:3 and a processing pressure of 0.2 Pa, so as to perform etching both in the depth direction and the lateral direction.

[0028] Now, the etching thickness of the polysilicon in the lateral direction depends on the application thickness of the RF bias, as shown in FIG. 3A, and according to the present embodiment, the processing conditions are optimized so that the reduction ratio in the lateral direction with respect to the depth direction is approximately 0.32. According to the present embodiment, processing is performed under this processing condition until approximately 50 nm which is half the thickness 100 nm of the polysilicon film **12** is etched, and then the pattern reduced to 35 nm via the processing dimension reduction step of the photoresist **14**, the SiON film **14** and the SiN film **13** is further reduced by 16 nm to obtain a pattern with a dimension of 19 nm. According to this processing step, the photoresist **14** is totally etched, and thereafter, the SiON film **14** and the SiN film **13** are used as the mask. According to this step, isotropic etching can be continued until either the photoresist **14** is gone or the mask width reaches a determined size, which for example is 19 nm. The reduction thickness according to FIG. 3A is the value obtained by subtracting dimension B of the mask width after etching from the initial dimension A of the mask width, and the reduction ratio is the value obtained by dividing this reduction thickness by the etching depth of the polysilicon film.

[0029] In the processing step of the polysilicon film **12** shown in FIG. 2E, the processing dimension of the polysilicon subjected to reduction in the former step is maintained while the remaining polysilicon film is etched. As for processing conditions, for example, etching is performed by applying 30 W of RF bias to plasma generated by applying 900 W of microwaves to a mixed gas having O₂ gas added to HBr gas in the amount of approximately 4% of the HBr gas flow rate, with the processing pressure set to 0.4 Pa. According to the etching conditions in this step, the etching of the polysilicon in the lateral direction will not occur, and the etching is performed while maintaining the processing dimension formed in the upper layer.

[0030] Thereby, the present embodiment enables to realize a polysilicon wiring process with a width of 19 nm without causing any disconnection or deflection (side etching) of the material being etched by using a mask pattern having an initial dimension of 100 nm.

[0031] Similarly, the prior art attempt to perform polysilicon processing to realize a 19 nm width polysilicon just by reducing the pattern dimension of the photoresist **15** of FIG. 2B requires the photoresist to be reduced as much as 80 nm,

which caused the photoresist pattern to fall down, causing drawbacks such as disconnection or deflection (side etching) of the polysilicon wiring.

[0032] If the reduction of the pattern dimension of the photoresist **15** is promoted significantly according to the prior art technology, it becomes impossible to maintain a sufficient mask thickness for etching the SiON film **14** and the SiN film **13**. Even when assuming that sufficient mask thickness is ensured, the photoresist pattern has its film thickness reduced, according to which the resistance to plasma is significantly deteriorated, causing drawbacks such as pattern deflection.

[0033] Moreover, the processing conditions of the process of FIG. 2D (wherein the ratio of Cl₂ gas to CF₄ gas is 1:3) is a condition optimized to correspond to the sample of the present embodiment, and the amount of CF₄ to be added should preferably be within the range of 40 to 90% from the viewpoint of shape control. If the amount of CF₄ being added is 40% or smaller, the etching performed by fluorine in the lateral direction will not progress effectively, and it becomes difficult to reduce the pattern dimension. On the other hand, if the amount of CF₄ being added is 90% or greater, the isotropic etching by fluoride becomes intense, by which the side etching is performed intensely and the perpendicular profile will not be maintained. Other than the reduction rate control method shown in FIG. 3, in other words, other than the above-mentioned processing conditions, the reduction rate can also be controlled by adding O₂ gas to the Cl₂ gas and CF₄ gas, or fluorine-containing gas such as CHF₃, SF₆ and NF₃, or by using fluorine-containing gas such as CHF₃, SF₆ and NF₃ instead of the CF₄ gas. Similarly, the reduction rate can also be controlled by using a halogen-based gas such as HBr gas instead of the Cl₂ gas.

[0034] The present embodiment discloses process conditions optimized with respect to the sample of a semiconductor device, and the method for etching the polysilicon film **12**, the SiN film **13**, the SiON film **14** and the photoresist **15** is not restricted to the conditions of the present embodiment.

[0035] Though the present invention is described with reference to the wiring process of polysilicon, it is not restricted thereto, and the present invention can also be applied to wiring processes of materials other than polysilicon in a semiconductor device manufacturing process. For example, the present invention can be applied to the wiring process of an object having tungsten silicide (WSi) film formed on a polysilicon film **12**, and further having an SiN film **13**, an SiON film **14**, a photoresist **15** and the like formed thereon. Since the reduction rate varies according to the material to be processed, it is preferable to seek the appropriate gas or the appropriate processing conditions corresponding to the material.

[0036] A sample having a photoresist mask is used in the present embodiment, but the present invention can be applied to samples using an inorganic film mask such as SiN, SiON and SiO₂, in other words, samples having the photoresist **15** of FIG. 2D removed.

[0037] Further, the present embodiment utilizes a plasma etching apparatus using microwaves and magnetic fields, but the present invention can be applied regardless of how plasma is generated. For example, equivalent effects can be achieved by applying the present invention to a helicon

wave plasma etching apparatus, an inductively-coupled plasma etching apparatus, a capacitively-coupled plasma etching apparatus and so on.

What is claimed is:

1. A dry etching method for performing a wiring process on a semiconductor substrate using a plasma etching apparatus, the method comprising:

a step of etching a material to be etched using a mask pattern composed of an inorganic film made of SiN, SiON, SiO and the like disposed on the material to be etched, wherein during processing of the material to be etched, the mask pattern and the processing dimension of the material to be etched are reduced substantially equally.

2. The dry etching method according to claim 1, wherein the reduction of the processing dimension is performed using a mixed gas composed of a halogen-based gas such as a chlorine-containing gas or a bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF₄, CHF₃, SF₆ and NF₃.

3. The dry etching method according to claim 1, wherein the reduction of the processing dimension is performed using a mixed gas composed of a halogen-based gas such as a chlorine-containing gas or a bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF₄, CHF₃, SF₆ and NF₃, the ratio of the fluorine-containing gas being 40 to 90 percent of the mixed gas.

4. The dry etching method according to claim 1, wherein the reduction of the processing dimension is realized by controlling an RF bias of the plasma etching apparatus, according to which the reduction ratio of the material to be etched is adjusted.

5. The dry etching method according to claim 1, wherein the reduction of the processing dimension is performed using a mixed gas composed of a halogen-based gas such as a chlorine-containing gas or a bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF₄, CHF₃, SF₆ and NF₃, the reduction ratio of the material to be etched being adjusted by controlling an RF bias of the plasma etching apparatus.

6. A dry etching method for performing a wiring process on a semiconductor substrate using a plasma etching apparatus; the method comprising:

a step of etching a material to be etched using a mask pattern composed of a photoresist and an inorganic film made of SiN, SiON, SiO and the like disposed on the material to be etched, wherein during processing of the material to be etched, the mask pattern and the processing dimension of the material to be etched are reduced substantially equally.

7. The dry etching method according to claim 6, wherein the reduction of the processing dimension is performed using a mixed gas composed of a halogen-based gas such as a chlorine-containing gas or a bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF₄, CHF₃, SF₆ and NF₃.

8. The dry etching method according to claim 6, wherein the reduction of the processing dimension is performed using a mixed gas composed of a halogen-based gas such as a chlorine-containing gas or a bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF_4 , CHF_3 , SF_6 and NF_3 , the ratio of the fluorine-containing gas being 40 to 90 percent of the mixed gas.

9. The dry etching method according to claim 6, wherein the reduction of the processing dimension is realized by controlling an RF bias of the plasma etching apparatus, according to which the reduction ratio of the material to be etched is adjusted.

10. The dry etching method according to claim 6, wherein the reduction of the processing dimension is performed using a mixed gas composed of a halogen-based gas such as a chlorine-containing gas or a bromine-containing gas and at least one fluorine-containing gas selected from a group of fluorine-containing gases composed of CF_4 , CHF_3 , SF_6 and NF_3 , the reduction ratio of the material to be etched being adjusted by controlling an RF bias of the plasma etching apparatus.

11. A dry etching method for performing a wiring process on a wiring layer disposed on a semiconductor substrate using a mask pattern formed of a photoresist and an inorganic film composed of SiN, SiON, SiO or the like in a plasma etching apparatus, the method comprising:

a first step of reducing using O_2 the mask pattern formed of the photoresist;

a second step of utilizing the reduced mask pattern formed of the photoresist so as to perform anisotropic etching of the mask pattern formed of the inorganic film composed of SiN, SiON, SiO or the like using a mixed gas containing CF_4 and CHF_3 ;

a third step of utilizing the mask pattern of the photoresist and the inorganic film composed of SiN, SiON, SiO or the like to etch the wiring layer and also reduce the mask pattern using a mixed gas containing Cl_2 and CF_4 ; and

a fourth step of utilizing the mask pattern of the inorganic film composed of SiN, SiON, SiO or the like subsequent to the third step to etch the wiring layer using a mixed gas containing HBr and O_2 .

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