

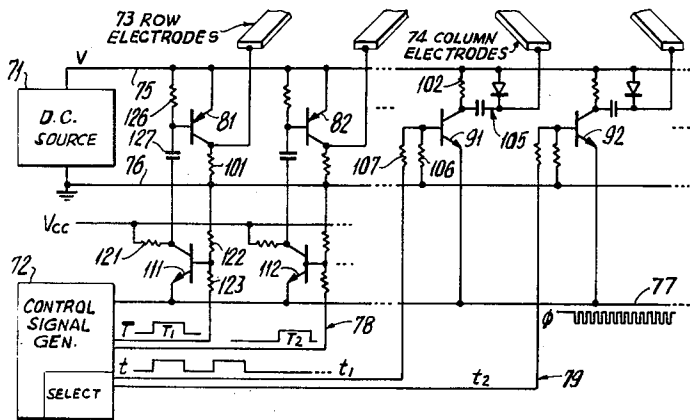
- [54] **DRIVING CIRCUIT FOR PLASMA DISPLAY PANEL COMPRISING MEANS FOR PLACING PEDESTAL ON ALTERNATING FIRING PULSES**
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- [22] Filed: **Jan. 30, 1973**
- [21] Appl. No.: **328,055**
- [30] **Foreign Application Priority Data**
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- [52] U.S. Cl. **315/169 TV, 315/167**
- [51] Int. Cl. **H05b 37/00**
- [58] Field of Search 315/169 R, 169 TV, 167

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- Primary Examiner*—Herman Karl Saalbach
Assistant Examiner—James B. Mullins
Attorney, Agent, or Firm—Sandoe, Hopgood & Calimafde

[57] **ABSTRACT**

A direct current pedestal is superposed on a group of alternating voltage pulses for producing a gas discharge in a selected cell of a plasma display panel. The circuit arrangement may be such that the pedestal is superposed on only those groups of the voltage pulses which would initiate a display.

2 Claims, 28 Drawing Figures



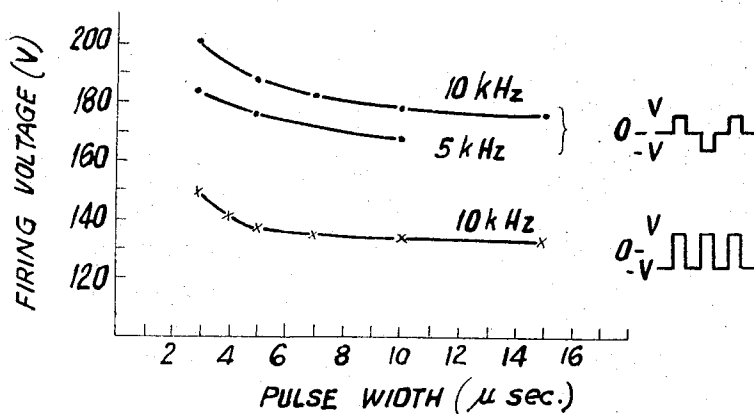
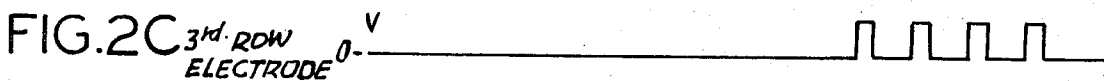
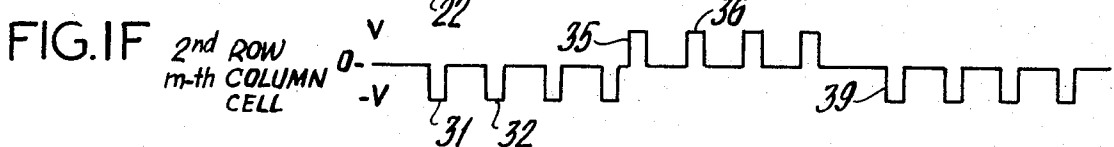
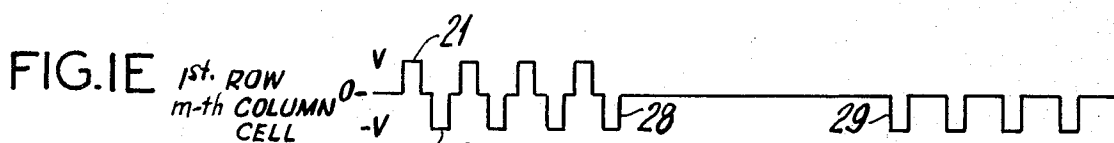
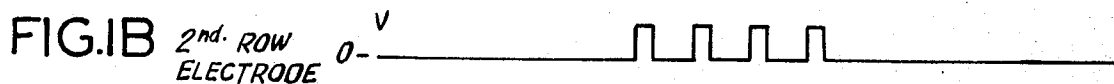
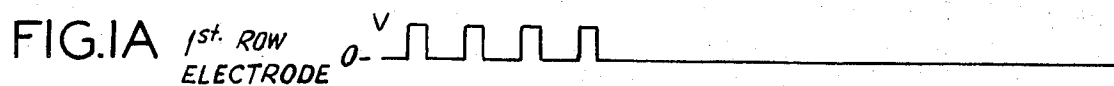


FIG. 3

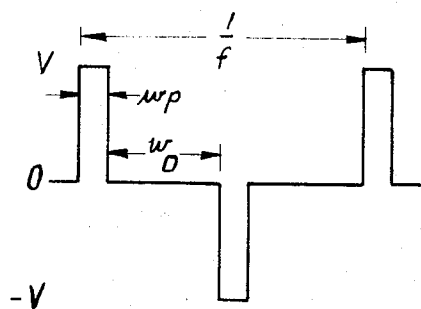


FIG. 4A

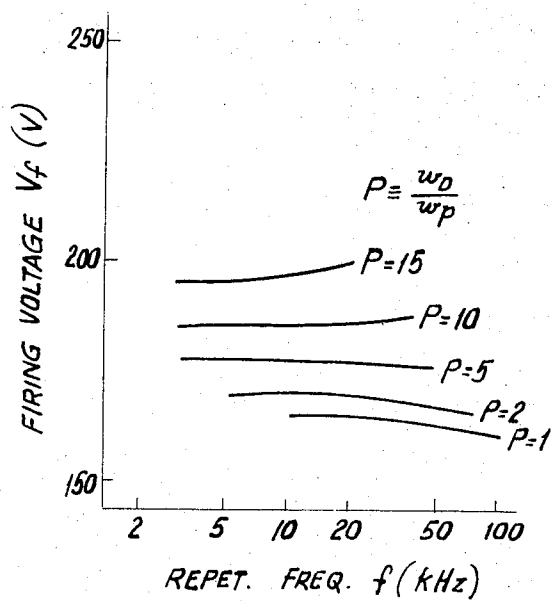


FIG. 4B

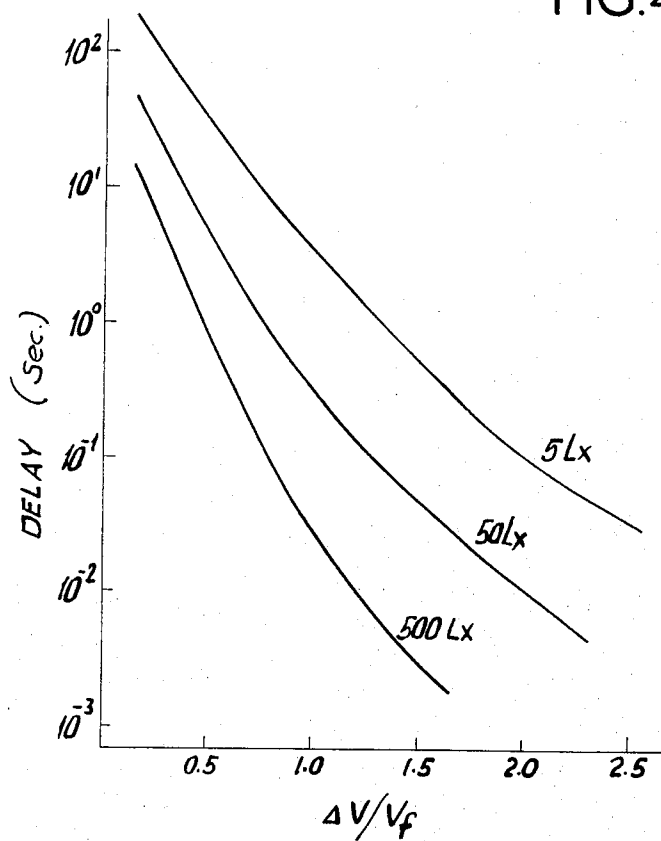


FIG. 5

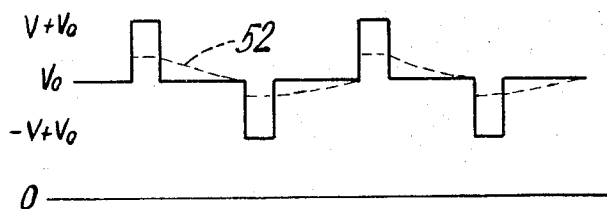


FIG. 6

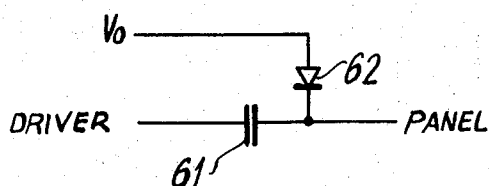
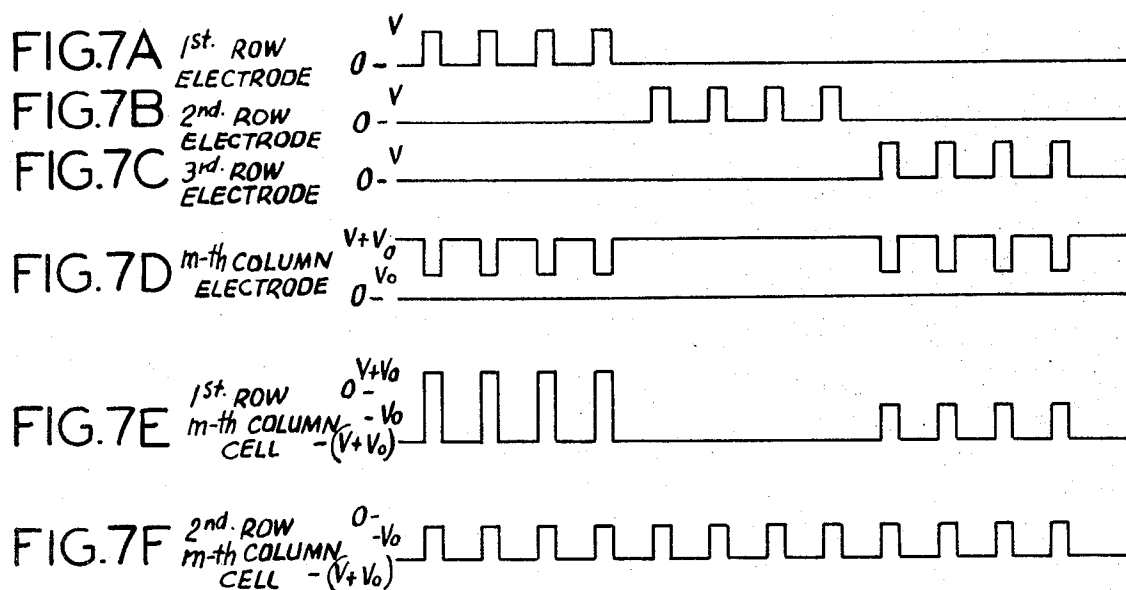


FIG. 8

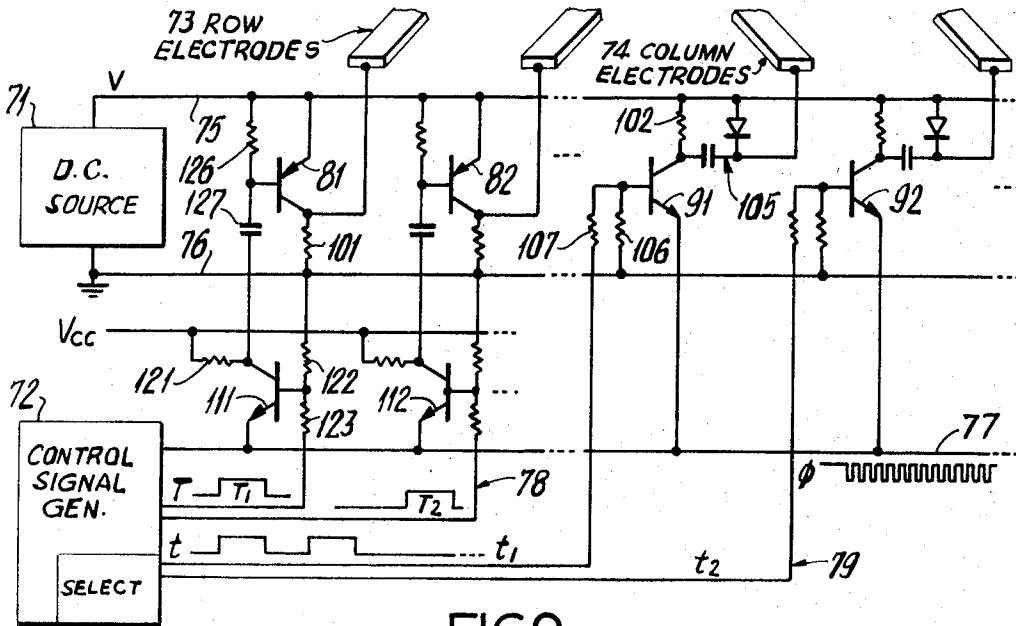


FIG. 9

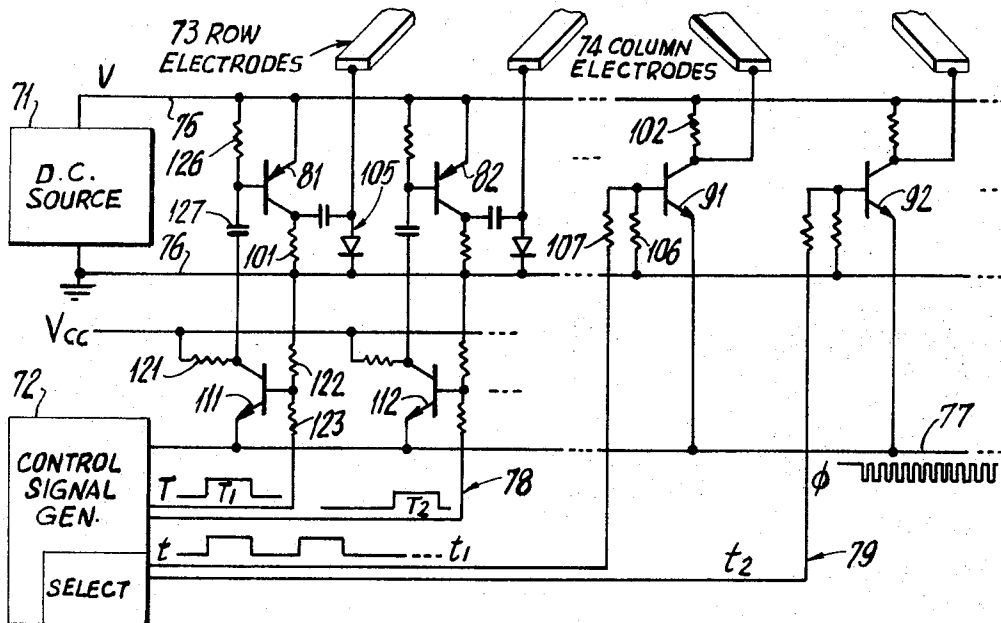


FIG. 10

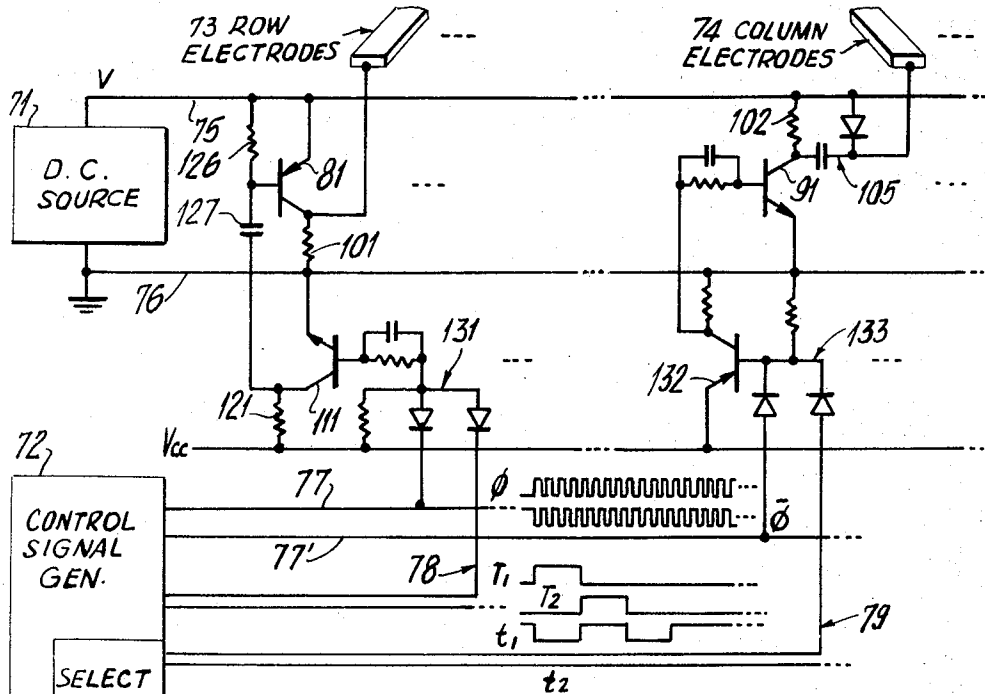


FIG. 11

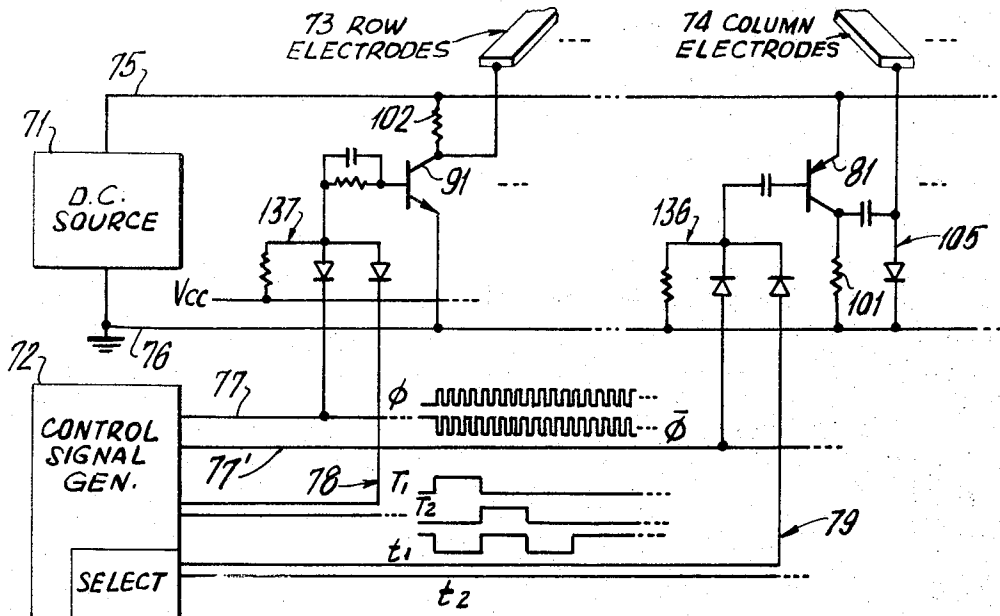


FIG. 12

DRIVING CIRCUIT FOR PLASMA DISPLAY PANEL COMPRISING MEANS FOR PLACING PEDESTAL ON ALTERNATING FIRING PULSES

BACKGROUND OF THE INVENTION

This invention relates to a driving circuit for driving an external electrode discharge display panel usually called a plasma display panel.

A plasma display panel generally comprises a stack of three thin flat glass or transparent dielectric plates. The central plate is provided with a plurality of perforations at predetermined locations. The periphery of the stack is hermetically sealed. The internal voids within the stack are evacuated and then filled with neon or similar inert gas or mixture of gases. Externally on both sides of the outer plates are disposed, the so-called matrix electrodes which consist of rows and columns of electrodes perpendicularly intersecting one another with the perforations interposed. The electrodes crossing at each of the selected perforations which correspond to the letter or symbol to be displayed are selectively supplied with a high frequency signal whereby a gas discharge is caused in the selected perforations to display the desired letter or symbol. In an improvement in the conventional plasma display panels of the construction mentioned above, two thick glass or transparent dielectric plates are used as the outer plates and provided with thin glass or other dielectric films on their inside surfaces, respectively. Furthermore, proposals have been made of a plasma display panel having no central plate and of a plasma display panel for numerals in which segmented electrodes are substituted for the matrix electrodes.

In any of the conventional panels, discharge occurs in a gas space (hereafter called a cell) identified by a pair of opposing external electrodes which are selectively supplied with a direct current voltage higher than the firing voltage of the cell (with the voltage drop across the dielectric plates being neglected). Once discharge occurs in a cell, charged particles generated by the discharge charge the dielectric plates to reduce the strength of the electric field within the cell until the discharge ceases when the sum of the supplied voltage and the reversed voltage resulting from the charges stored on the dielectric plates falls below the discharge sustaining voltage of the cell. If the polarity of the direct current voltage supplied between the opposing external electrodes is reversed to be of the same polarity as the voltage resulting from the charges, the voltages applied across the cell are superposed on each other to become sufficiently higher than the firing voltage. Thereupon, the discharge starts again until it eventually disappears. By repeating the processes, namely, by applying a voltage of alternating or successively reversed polarity between the opposing external electrodes, it is possible to sustain the intermittent discharge. If the frequency of repetition of the intermittent discharge per unit time is optimally determined (for example, 10 kilohertz), it is possible to provide a display of sufficient brightness.

In order to drive an external electrode discharge display panel in a time division fashion, there has been proposed a driving circuit of the first type, as referred to herein, such as disclosed in U.S. Pat. No. 3,614,769 and described below in greater detail, in which a group of the row electrodes and another group of the column electrodes are selectively supplied with pulse voltages,

the timing of the pulse voltages supplied to the respective groups of electrodes being adjusted in such a manner that one of the groups of electrodes is supplied with the voltage while other of the groups of electrodes is not supplied with the voltage. There has also been proposed a driving circuit of the second type, referred to herein, such as taught in the Japanese periodical named "Densi Zairyo" (Electronics Materials), 1971 July issue, page 89, and described in more detail below, in which the row electrodes and the column electrodes are selectively supplied with pulse voltages with the pulse voltages supplied to the respective groups being varied simultaneously.

The driving circuit of the first type has a disadvantage in that the disposition of the pulses tends to cause discharge in cells other than those selected and another disadvantage in that the presence of the time intervals during which all of the cells are supplied with no voltage leads to an increase in the firing voltage of the cells. The driving circuit of the second type does not have the above disadvantages.

It is, however, to be pointed out in connection with the driving circuits of the first and the second types that the initial discharge undergoes a considerable delay when the cells are supplied with voltage sufficiently higher than the firing voltage after being unoperated for several days. The delay amounts to ten seconds even with the panel exposed to an intensity of illumination of one hundred luxes.

In order to avoid the delay of the initial discharge, it has been proposed to provide electrons and/or ions constantly present within the cells. Attempts have been made to seal a radioactive gas in the cells and to apply a radioactive substance to the structure of the panel. These techniques are objectionable because it is not easy to deal with radioactive materials and it is difficult to dispose of worn out or damaged panels. In addition, such attempts have proved to be expensive because of the additional process of adding the radioactive material to the display panel.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a driving circuit for an external electrode discharge display panel having a delay of initial discharge that is negligible in practical applications.

It is another object of this invention to provide a plasma display panel of the type described, which is operable with low voltages.

It is still another object of this invention to provide a plasma display panel which includes no radioactive materials.

According to this invention there is provided a driving circuit for driving an external electrode discharge display panel having a coplanar array of similar gas discharge cells, and first and second pluralities of electrodes arranged externally to the cells so that each of cell is interposed between a pair of first and second electrodes. The driving circuit comprises pulse generating means for selectively supplying a group of pulses to a selected pair electrodes associated with a common cell to produce a gas discharge in the cell, said voltage being less than four times the firing voltage of each of said cells and greater than twice said firing voltage. The improvement comprises superposing means for superposing a direct current voltage on a group of said pulse voltages to be supplied across a selected pair of elec-

trodes, said direct current voltage not upsetting the varying polarity nature of the direct current voltage superposed pulse voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically shows wave forms (a) through (f) for use in a driving circuit of the first type, as referred to herein, for an external electrode discharge display panel;

FIG. 2 similarly illustrates wave forms (a) through (f) for use in driving circuit of the second type, as referred to herein;

FIG. 3 shows typical characteristics of the firing voltage versus the pulse width in the driving circuits of the first and the second types;

FIG. 4A shows the discharge producing wave form for use in the driving circuit of the first type, on an enlarged scale;

FIG. 4B shows typical characteristics of the firing voltage in the driving circuit of the first type versus the repetition frequency of the pulses for various duty ratios of the pulse voltage;

FIG. 5 illustrates the relations between the delay of the initial discharge and the voltage applied across the cell;

FIG. 6 is a graph of a typical wave form used in a driving circuit according to the instant invention;

FIG. 7 schematically illustrates wave forms (a) through (f) for use in a driving circuit according to this invention;

FIG. 8 shows a circuit essential to a driving circuit according to this invention; and

FIGS. 9 through 12 are circuit diagrams of several preferred embodiments of this invention.

DESCRIPTION OF PREFERRED EMBODIMENTS:

Before describing the preferred embodiments of the present invention the, operation of the conventional driving circuit for a plasma display panel will be analysed with reference to FIGS. 1 through 5 in order to facilitate an understanding of the principles on which the invention is based.

Referring specifically to FIG. 1, a driving circuit (not shown) of the first type, as referred to herein, such as disclosed in U.S. Pat. No. 3,614,769 referred to above, comprises means for supplying time division pulse voltages depicted in (a), (b), (c), and similar pulse voltages to the first, the second, the third, and the like row electrodes (not shown), respectively. Each of the pulse voltages consists of pulse groups of a predetermined duration, each group in turn consisting of pulses of a pulse height V sufficiently greater than the firing voltage V_f , a pulse width W_p , and a repetition frequency f . The pulse voltages for the successive row electrodes are shifted in order by a lag that is equal to the predetermined duration and refreshed with a period n times the predetermined duration, where n is the number of the row electrodes in a group, such as for a single letter. The driving circuit further comprises means for selectively applying second or address pulse voltages, such as depicted in (d), to at least one selected column electrodes, such as the m -th column electrode (not shown). When it is desired to produce the discharge in cells arranged along a particular column of electrodes, the second pulse voltage applied to the particular column electrode is provided with pulses of the height V in such a staggered relation to the pulses of the first pulse

voltages supplied to the row electrodes crossing the particular column electrode at the desired cells that the pulses of the second pulse voltage may appear within the predetermined durations of the first pulse voltages supplied to the last-mentioned row electrodes while the pulses of these first pulse voltages are absent. The driving circuit thus applies resulting pulse voltages depicted in (e) and (f) to the cells of the first row m -th column and of the second row m -th column, respectively. Referring more particularly to FIG. 1 (e), the discharge occurs in the cell of the first row m -th column in response to a first pulse 21 shown and then disappears as the inversed voltage grows as a result of the charged particles produced by the discharge. Responsive to a second pulse 22 applies across the cell in the same polarity as the voltage produced by the charges, the discharge gain occurs in the cell, until it eventually disappears. Similar processes follow up to an eighth pulse 28. Inasmuch as the inside of the cell is made of insulating materials, the inversed voltage resulting from the discharge caused by the eighth pulse 28 remains for a considerable duration such that the pulses of the polarity of the inversed voltage, such as a ninth pulse 29, are incapable of causing the discharge. From the foregoing, it would appear that the discharge occurs only in the cells selected by the wave forms of the pulse voltages applied to the column electrodes. The fact is, however, that the discharge occurs also, for example, in the cell of the second row m -th column due to the resulting voltage applied thereacross as shown in FIG. 1 (f). More particularly, a first pulse 31 introduces the discharge. A second pulse 32 and the following pulses of the polarity opposite to the voltage resulting from the charges do not produce the discharge. A fifth pulse 35 of the same polarity, however, is of the polarity opposite to the voltage resulting from the charges and again produces an instantaneous discharge. Although a sixth pulse 36 and the following pulses of the same polarity do not contribute to the discharge, a ninth pulse 39 again makes a transient discharge occur. The spurious discharges contribute to the brightness of the unwanted cells to result in a spurious display when the number of pulses in the predetermined duration is small. On the other hand, an increase in this number requires a high switching speed of the driving circuit and is objectionable both from economical and technical viewpoints.

Referring to FIG. 2, a driving circuit of the second type, as referred to herein, comprises means for supplying first pulse voltages depicted in (a), (b), (c), and similar pulse voltages to the first, the second, the third, and the like row electrodes (not shown), respectively. Each of the pulse voltages is of the same wave form as the first pulse voltages used in the driving circuit of the first type and is similarly refreshed. The driving circuit further comprises means for selectively applying second pulse voltages, such as depicted in (d), to at least one selected column electrode, such as the m -th column electrode (not shown). In case it is desired to produce the discharge in cells arranged along a specific one of the column electrodes, the second pulse voltage applied to the specific column electrode is provided with negative going pulses of the depth V in coincidence with the pulses of the first pulse voltages supplied to the row electrodes intersecting the specific column electrode at the desired cells. The driving circuit thus applies the resulting voltages depicted in (e) and (f) to the cells of the first row m -th column and of the

of these auxiliary transistors, such as 111, are supplied with the negative going high frequency pulses and the positive going pulses of the time division pulse train T1, the auxiliary transistor 111 turns on, amplifies the high frequency pulses, and applies the current amplified and polarity inverted pulses to the base electrode of the associated PNP switching transistor 81 through the capacitor 127 to intermittently turn the latter transistor 81 on during the cyclically positive going periods of the time division pulse train T1. Responsive to the intermittent turning on of the PNP switching transistor 81, the voltage of the associated row electrode 73 varies substantially between the ground potential and the positive voltage provided across the related resistor 101. The NPN switching transistors 91, 92, . . . serve as AND circuits responsive to the negative going high frequency pulses and the positive going pulses of the address pulse trains $r1$, $r2$, and so on. More particularly, the negative going high frequency pulses intermittently reduce the emitter potential of these NPN switching transistors substantially to the ground level. On the other hand, the positive going address pulses of the address pulse trains $r1$, $r2$, . . . raise the base potentials to apply forward voltages to the base-emitter junctions of these NPN switching transistors. During the selectively positive going periods of, for example, the address pulse train $r1$, the related NPN switching transistor 91 is intermittently turned on responsive to the negative going pulses to make that voltage of the associated column electrodes 74 fall towards the ground potential which is otherwise clamped substantially to the direct current voltage V. It is now understood that the voltage illustrated in FIG. 7 (e) is applied across the cell or cells interposed between the row and the column electrodes coupled to the switching transistors 81 and 91, respectively.

Referring further to FIG. 9, it will be readily understood that the output impedance of the driving circuit is very low for the significant portions of the paired pulse trains applied across the selected cell or cells because the associate switching transistors, such as 81 and 91, are turned on during these significant portions. It will also be understood that the time constant determined by the resistor 126 and the capacitor 127 will be sufficiently greater than the width of the high frequency pulses and that the resistance of the collector resistor 101 or 102 will be selected in such a manner that the time constant determined by the resistance and the stray capacity which exists between the associated electrodes 73 and 74 and the remaining electrodes 73 and 74 will be smaller than the interval between the high frequency pulses. On the other hand, the resistance of the collector resistor 101 or 102 should be appreciably large so as to reduce the power consumed in these resistors when the associated switching transistors are turned on. By way of example, it may be assumed that the capacity that is present between one of the electrodes 73 and 74 and the remaining electrodes is 30 pF and that the frequency and the pulse width of the high frequency pulses are 50 kHz and 5 microseconds, respectively. Under the circumstances, the resistance of each of the collector resistors may be 100 kilohms.

By way of example, use was made of an external electrode discharge display panel in which the firing voltage v_f is 130 V and the unidirectional firing voltage, namely, the firing voltage with application of the volt-

age only to the row or the column electrode or electrodes, is 220 V. The delay of the initial discharge was measured with the display panel placed in a dark room and with a driving circuit according to the first embodiment with a direct current voltage V of 160 V supplied by the direct current power source 71. The delays were less than 0.5 second. By way of reference, the delay was measured under the same circumstances with a like driving circuit but without the direct current component superposing circuits 105. The delays amounted to 80 seconds. In addition, the direct current voltage V was increased from the firing voltage to the unidirectional firing voltage with a driving circuit according to the first embodiment. No spurious was noticed.

Referring to FIG. 10, a second embodiment of the present invention is similar to the first embodiment except that the direct current component superposing circuits 105 of the principles illustrated with reference to FIG. 8 are now connected to the respective row electrodes 73 and to the row driver circuits to superpose a direct current component $-V$ to the row electrode voltage. The results of actual measurements of the initial discharge were the same as achieved with the corresponding circuits derived on the basis of the first embodiment.

It is to be noted here that the present invention is applicable to any one of the driving circuits of the second type but that the embodiments described above are based on the third embodiment of a plasma display panel driving circuit disclosed in Japanese Pat. application No. Syo 46-92088 (WN-537). These embodiments are advantageous for use with a control generator 72 having relatively high output impedance for the time division and the address pulse trains and are preferred in respect of its low output impedance for the cell firing pulses and the resulting high luminance of the display as compared with the conventional driving circuit of the second type.

Referring to FIG. 11, a third embodiment of the present invention is based on the first embodiment revealed in the above-referenced Japanese patent application and comprises similar components designated with like reference numerals as in the first and second embodiments of the present invention. Instead of a single continuous train of the negative going high frequency pulses, the control generator 72 now produces a pair of continuous trains ϕ and $\bar{\phi}$ of positive and negative going pulses on a third conductor pair 77 and 77', respectively. The emitter electrodes of the NPN auxiliary transistors, such as 111, are connected directly to the second conductor 76 rather than to the third conductor 77 or 77'. as these auxiliary transistors are supplied with the respective positive going time division pulse trains T1, T2, . . . through positive logic AND circuits, such as 131, respectively. Instead of making the NPN switching transistors, such as 91, serve also as AND circuits, the third embodiment comprises a plurality of PNP auxiliary transistors, such as 132, which are associated with the respective NPN switching transistors and supplied with the negative going high frequency pulse train $\bar{\phi}$ and the respective negative going address pulse trains, such as $r1$, through negative logic AND circuits, such as 133, respectively. In this connection, it will be understood that the positive going high frequency pulses and the time division pulses should rise from ground up to the collector voltage V_{cc} and that the negative going high frequency pulses and the ad-

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dress pulses should fall from the collector voltage to ground.

In operation, the positive logic AND circuit 131 depicted in FIG. 11 intermittently allows the positive going high frequency pulses to pass therethrough only while the positive going time division pulses of the train T1 appear. The associated NPN auxiliary transistor 111 current amplifies the gated high frequency pulses with the polarity reversed. The negative logic AND circuit 133 similarly intermittently allows the negative high frequency pulses to pass therethrough only when the negative going address pulses of the train t1 appear. The associated PNP auxiliary transistor 132 current amplifies the gated high frequency pulses, reversing the polarity thereof.

Referring now to FIG. 12, a fourth embodiment of the present invention is based on the second embodiment described in the abovesited Japanese patent application and comprises similar components designed with like reference numerals as in the third embodiment of the instant invention. The base electrodes of the PNP transistors, such as 81, are supplied with the negative going high frequency pulse train $\bar{\phi}$ and the negative going address pulse trains, such as t1, through negative logic AND circuits, such as 136, respectively. The base electrodes of the NPN transistors, such as 91, are supplied with the positive going high frequency pulse train ϕ and the positive going time division pulse trains T1, T2, . . . through positive logic AND circuits, such as 137, respectively. This embodiment is advantageous particularly where the output impedance of the control signal generator 72 is sufficiently small.

It is to be recalled here that the discharge once initiated in a cell of a plasma display panel produces charged particles. The discharge further produces photons. These charged particles and the like leak to the

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adjacent cells. Accordingly, the delay in the adjacent cells decreases if the voltage is applied across these cells during the life time of the charged particles. It is therefore sufficient that the direct current voltage be arranged to be superposed on the pulse voltage only at those cells at which the discharge may possibly start. In addition, it will now be understood that the plasma display panel may not necessarily have row and column electrodes but segment electrodes or other opposing electrodes.

What is claimed is:

1. For a discharge display apparatus including a coplanar array of similar gas discharge cells and first and second pluralities of electrodes external to said cells arranged so that each cell is interposed between an electrode of said first plurality and an electrode of said second plurality, a driving circuit comprising:

generating means for supplying a group of alternating polarity pulses to the electrodes associated with a selected cell, the voltage of said pulses being less than four times and greater than two times for firing voltage of said cell; and

means for superposing a direct current on said group of alternating polarity pulses whereby the initial discharge delay of the cell is reduced and spurious discharges are prevented.

2. The driving circuit of claim 1, wherein said superposing means comprises:

at least one capacitor interposed between said generating means and a pair of electrodes associated with a common cell; and

voltage clamping means for clamping the voltage of said pair of electrodes to the voltage level of the direct current from said superposing means.

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[54] **ELECTROSTATIC FLOCKING EQUIPMENT**

3,680,779 8/1972 Reilly..... 317/3 X

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[22] Filed: **Dec. 27, 1972**

[21] Appl. No.: **318,850**

Primary Examiner—J. D. Miller
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Attorney, Agent, or Firm—Tab T. Thein

[30] **Foreign Application Priority Data**

Dec. 29, 1971 Germany..... 2165387

[52] **U.S. Cl.**..... **317/3, 118/636**

[51] **Int. Cl.**..... **B05b 5/02**

[58] **Field of Search**..... 317/3; 118/621, 624, 625,
118/627, 636, 638

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[57] **ABSTRACT**

An electrostatic flocking equipment comprising a dosing system for flocks to be applied to a product, electrodes laterally disposed between the dosing system and the product, and means for applying an electrostatic charge to the flocks so as to accelerate them toward the product, the electrodes defining therebetween a substantially central flocking zone which is at least partly substantially free from the electrostatic charge, so as to eliminate chain and streak formation of the flocks, and thereby improve the quality of the flocked product.

9 Claims, 2 Drawing Figures

