



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

|                                                                            |    |                                                                                                                   |
|----------------------------------------------------------------------------|----|-------------------------------------------------------------------------------------------------------------------|
| (51) International Patent Classification <sup>5</sup> :<br><br>H01L 21/266 | A1 | (11) International Publication Number: WO 94/11900<br>(43) International Publication Date: 26 May 1994 (26.05.94) |
|----------------------------------------------------------------------------|----|-------------------------------------------------------------------------------------------------------------------|

(21) International Application Number: PCT/US92/09832

(22) International Filing Date: 9 November 1992 (09.11.92)

(71) Applicant (for all designated States except US): IXYS CORPORATION [US/US]; 2355 Zanker Road, San Jose, CA 95131 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): ZOMMER, Nathan [US/US]; 989 Covington, Los Altos, CA 94022 (US).

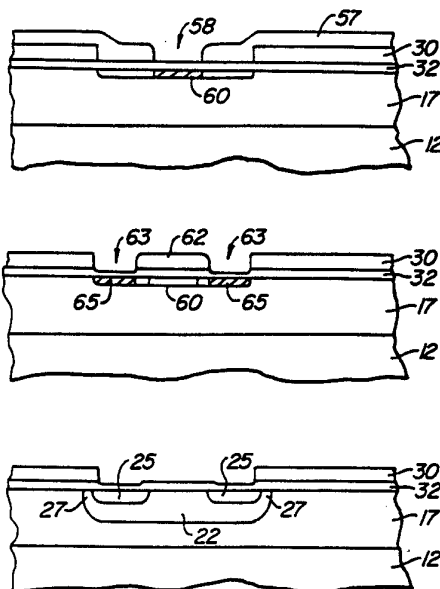
(74) Agent: SLONE, David, N.; Townsend and Townsend, One Market Plaza, 20th floor, Steuart Tower, San Francisco, CA 94105 (US).

(81) Designated States: JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, SE).

Published

With international search report.

(54) Title: SINGLE DIFFUSION PROCESS FOR FABRICATING SEMICONDUCTOR DEVICES



## (57) Abstract

A simplified process of making an insulated gate transistor entails forming the active regions in a single diffusion step. The method includes the steps of implanting and diffusing impurities of a first conductivity type (p for n-channel devices [55]), implanting and diffusing a heavy dose of impurities of the same conductivity type (p+ for n-channel devices [60]), and implanting and diffusing impurities of the other conductivity type (n+ for n-channel devices [65]), wherein the three types of impurities are diffused at the same time in the same step (22, 25, 27). In a preferred embodiment of an n-channel process, the p-type dopant is boron and the n-type is arsenic.

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

|    |                          |    |                                       |    |                          |
|----|--------------------------|----|---------------------------------------|----|--------------------------|
| AT | Austria                  | GB | United Kingdom                        | MR | Mauritania               |
| AU | Australia                | GE | Georgia                               | MW | Malawi                   |
| BB | Barbados                 | GN | Guinea                                | NE | Niger                    |
| BE | Belgium                  | GR | Greece                                | NL | Netherlands              |
| BF | Burkina Faso             | HU | Hungary                               | NO | Norway                   |
| BG | Bulgaria                 | IE | Ireland                               | NZ | New Zealand              |
| BJ | Benin                    | IT | Italy                                 | PL | Poland                   |
| BR | Brazil                   | JP | Japan                                 | PT | Portugal                 |
| BY | Belarus                  | KE | Kenya                                 | RO | Romania                  |
| CA | Canada                   | KG | Kyrgyzstan                            | RU | Russian Federation       |
| CF | Central African Republic | KP | Democratic People's Republic of Korea | SD | Sudan                    |
| CG | Congo                    | KR | Republic of Korea                     | SE | Sweden                   |
| CH | Switzerland              | KZ | Kazakhstan                            | SI | Slovenia                 |
| CI | Côte d'Ivoire            | LI | Liechtenstein                         | SK | Slovakia                 |
| CM | Cameroon                 | LK | Sri Lanka                             | SN | Senegal                  |
| CN | China                    | LU | Luxembourg                            | TD | Chad                     |
| CS | Czechoslovakia           | LV | Latvia                                | TG | Togo                     |
| CZ | Czech Republic           | MC | Monaco                                | TJ | Tajikistan               |
| DE | Germany                  | MD | Republic of Moldova                   | TT | Trinidad and Tobago      |
| DK | Denmark                  | MG | Madagascar                            | UA | Ukraine                  |
| ES | Spain                    | ML | Mali                                  | US | United States of America |
| FI | Finland                  | MN | Mongolia                              | UZ | Uzbekistan               |
| FR | France                   |    |                                       | VN | Viet Nam                 |
| GA | Gabon                    |    |                                       |    |                          |

SINGLE DIFFUSION PROCESS FOR FABRICATING  
SEMICONDUCTOR DEVICES

5

BACKGROUND OF THE INVENTION

The present invention relates generally to semiconductor processing, and more specifically to a method for making insulated gate transistors, including insulated gate  
10 field effect transistors (IGFETs) and insulated gate bipolar transistors (IGBTs).

The prior art will be described in terms of fabricating an n-channel enhancement mode power IGFET. IGFETs are often referred to as MOSFETs (metal-oxide-semiconductor  
15 field effect transistors), even though most modern IGFETs have polysilicon rather than metal gates. Further, the initial discussion will be limited to embodiments where the transistor comprises a large number of microscopically small cells, each defining a microscopic active device.

20 The device is fabricated by diffusing impurities into selected regions of an n- epitaxial (epi) layer formed on an n+ substrate. A typical cell comprises a p/p+ body (sometimes referred to as the p-well) formed in the epi layer and an n+ source region formed within the perimeter of the body. The  
25 body is p-type over most of its lateral extent but one or more central regions are doped p+. The portion of the body adjacent the surface and between the source region and the n- epi layer defines a channel region.

A polysilicon layer overlies the channel region of  
30 each cell and the regions between cells, and is separated from the epi surface by a thin layer of gate oxide. The polysilicon layer forms a common gate electrode for all the cells in the device. Portions of a top metal layer connect the source regions to a common source node while other portions of the top  
35 metal layer connect the polysilicon layer to a common gate node. A metal layer is formed on the bottom surface to form a common drain node.

Known technologies for fabricating insulated gate transistors entail multiple diffusions of impurities to define the active regions of the device. The process most commonly used in the industry is a three-diffusion process wherein the p+ portion of the p-well is diffused, followed by gate oxidation and other oxidation and deposition steps. The second diffusion step is then performed to create the larger p-well area, which is usually self-aligned to the polysilicon gate region. Then, the third diffusion step is performed to create the n+ source region. A two-diffusion manufacturing process is disclosed in U.S. Patent No. 4,860,072, issued August 22, 1989. In this process, the p-well is formed by two separate deposition steps but a single diffusion step.

#### SUMMARY OF THE INVENTION

The present invention provides a simplified process of making semiconductor devices, providing increased yield, reduced cycle time, and reduced energy and gas costs. The process utilizes existing VLSI processing techniques and can easily be incorporated into existing fabrication facilities.

In brief, the process of the invention entails forming all or at least three of the active regions of the device in a single diffusion step. Thus, in the context of making insulated gate transistors, the method includes the steps of implanting and diffusing impurities of a first conductivity type (p for n-channel devices), implanting and diffusing a heavy dose of impurities of the same conductivity type (p+ for n-channel devices), and implanting and diffusing impurities of the other conductivity type (n+ for n-channel devices), wherein the three types of impurities are diffused at the same time in the same step. Thus, all dopants are introduced sequentially with their corresponding masking steps in between, but there are no intervening diffusion steps or other high-temperature processing steps such as growing gate oxide or polysilicon. The single diffusion step forms the body and the source regions.

In a preferred embodiment of an n-channel process, the p-type dopant is boron and the n-type is arsenic. During the

diffusion step, the fast diffusing boron diffuses more deeply and spreads laterally more than the slow diffusing arsenic. Accordingly, the p-well and the n+ source regions are well defined with a controlled channel thickness. The p, p+, and n+ implantation doses, and the time and temperature of the diffusion allow the device to be optimized based on speed and voltage rating considerations.

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the attached drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a schematic cross-sectional view of a prior art IGFET structure;

Fig. 1B is a top view showing a possible cell layout of the IGFET of Fig. 1A;

Fig. 1C is a top view showing a possible stripe layout of the IGFET of Fig. 1A;

Figs. 2A-2E are schematic cross-sectional views illustrating the multiple implantations and single diffusion according to the present invention.

#### DESCRIPTION OF SPECIFIC EMBODIMENTS

##### Prior Art Device Structure and Fabrication Method

Fig. 1A is a simplified sectional view of portions of a prior art insulated gate field effect transistor (IGFET) chip 10. As shown in Fig. 1B and as will be discussed below, the active area of a typical chip may consist of hundreds or thousands of microscopically small cells 11, each defining an active device. For the IGFET shown, all the cells are the same and are connected in parallel. As shown in Fig. 1C, the chip may be laid out in microscopically narrow stripes 11' rather than cells.

An n+ substrate 12 has an n- epitaxial (epi) layer 17 formed on its upper surface, and the active regions are formed therein. A typical cell 11 of the IGFET comprises a p/p+ body 22 formed in epi layer 17 and an n+ region 25 formed within the

perimeter of body 22. Body 22 is p-type over most of its lateral extent with one or more central regions doped p+. The portion of body 22 adjacent the surface and between the source region and the n- epi layer defines a channel region 27.

5           A polysilicon layer 30 overlies the channel region and the regions between cells, and is separated from the epi surface by a thin layer 32 of gate oxide. The polysilicon extends over the surface of the device with an opening at each cell (for source/body contacts) so as to form a common gate  
10   electrode for all the cells in the device. Portions 35 of a top metal layer connect n+ region 25 to a common source/body node S. Other portions 36 of the top metal layer connect the polysilicon layer to a common gate node G. A metal layer 37 is  
15   formed on the bottom surface of the substrate to form a bottom drain electrode D common to all cells of the device.

Fig. 1B shows a simplified top view of a typical layout of an embodiment laid out in cells 11. The solid octagon denotes the opening in the gate polysilicon layer while the dashed lines show the channel region under the gate  
20   (bounded by the p-well boundary and the source region boundary). This particular type of cell has the n+ source region formed so that the body portion contacts the epi surface in two regions (denoted by solid rectangles). The contact opening for the source/body contact extends over both these  
25   regions and the intermediate n+ region. This type of cell is described in U.S. Patent 4,860,072, issued August 22, 1989.

Fig. 1C shows a simplified top view of an embodiment laid out in stripes 11'. In this embodiment, the p-well, channel, and source region extend longitudinally.

30           A representative prior art fabrication process for n-channel IGFETs may be briefly outlined as follows:

- (1) Provide an n+ substrate.
- (2) Grow n- epitaxial layer.
- (3) Grow localized field oxide to define peripheral  
35   non-active areas of the chip.
- (4) Deposit gate oxide.
- (5) Deposit polysilicon over gate oxide.

- (6) Create openings in the polysilicon and gate oxide to define the cells or stripes.
- (7) Implant p-type dopants aligned to polysilicon openings.
- 5 (8) Mask and implant p+ regions within the openings (non-critical alignment).
- (9) Diffuse to form p-well (body).
- (10) Mask at least portions of p+ diffusion and implant n+.
- 10 (11) Diffuse to form source regions and channel regions.
- (12) Deposit CVD oxide over wafer.
- (13) Etch poly contacts and source/body contacts.
- (14) Deposit metal layer.
- 15 (15) Etch metal layer to define gate electrode and source/body electrode.
- (16) Passivate.

The process can be used to make either IGFETs or IGBTs. IGBTs could be made by the above process, modified by providing a p+ substrate and then optionally doping the upper portion of the p+ substrate n+ prior to growing the n- epitaxial layer.

#### Fabrication Method According to the Invention

Figs. 2A-B show schematic cross-sectional views of a portion of transistor chip 10 at various stages of the fabrication method according to the present invention. Where a figure illustrates the result of a particular implantation, the implant is shown with cross-hatching. It is assumed that field oxide is already on the device and patterned accordingly to define the active regions of the chip.

Fig. 2A shows the chip after gate oxide layer 32 and polysilicon layer 30 have been deposited on epi layer 17, and an opening 50 has been made in polysilicon layer 30 as defined by a patterned layer of photoresist 52. As will be described below, all implants performed in connection with forming the body and source regions are performed without intervening high-temperature steps such as diffusions, gate oxide deposition, and polysilicon deposition.

Fig. 2B shows the chip after an implantation step has resulted in a region 55 of p-type impurities (preferably boron). This implantation is done with the polysilicon layer, either with or without photoresist 52, acting as the mask.

5 The energy of the boron implant should be high enough to ensure that the boron atoms go through the gate oxide into the underlying silicon surface. A typical dose is  $5 \times 10^{13}$  atoms/cm<sup>2</sup> at 140 KeV (or on the order of 50-100 KeV if the gate oxide was etched prior to implantation).

10 Fig. 2C shows the chip after photoresist 52 has been stripped, a photoresist layer 57 has been deposited, one or more openings 58 have been formed within the polysilicon opening for the p+ implant, and a heavy dose of p-type impurities has been implanted through opening(s) 58 to provide  
15 a resultant implanted area 60. This implant is at a higher dose (say  $2 \times 10^{15}$  atoms/cm<sup>2</sup> than the first implant but generally at comparable energy. However, depending on the implanter, it may be necessary to perform the implantation at a somewhat lower energy to achieve the high dose.

20 Fig. 2D shows the chip after photoresist 57 has been stripped, a patterned layer of photoresist 62 has been deposited to cover p+ region(s) 60, so as to leave an opening 63, and a heavy dose of n-type impurities (preferably arsenic) has been implanted through opening 63 to provide a resulting  
25 implanted area 65. The gate oxide is shown as having been etched to thin it prior to the implantation (it could also have been removed). Although two segments of opening 63 and region 65 appear in the figure, it should be understood that opening 63 and implanted region 65 extend along the entire periphery of  
30 the opening in the polysilicon, and thus are contiguous on the surface of the substrate.

The arsenic implant is shown as extending to the same depth as the boron implants, but it is possible, and sometimes desired, to make the implant shallower. A typical implant  
35 energy is 140 KeV, with lower values preferred for shallower implants. The arsenic inherently requires higher energy to penetrate the gate oxide, which is the reason for preferably

etching the oxide if it is not possible to achieve the energy necessary to penetrate it. A typical dose is  $5 \times 10^{15}$  atoms/cm<sup>2</sup>.

Fig. 2E shows the chip after photoresist 62 has been stripped and the wafer, with implants 55, 60, and 65 in place, has been subjected to a single diffusion step. The duration and temperature of the diffusion step are determined on the basis of the desired device parameters such as the voltage rating. This is carried out from 4 to 12 hours at temperatures generally in the range of 900-1200°C in an atmosphere such as nitrogen or nitrogen with traces of oxygen. The result of the diffusion step is to form p/p+ body 22, source region 25, and channel region 27. During the diffusion, the implanted boron atoms diffuse at a significantly higher rate than the arsenic atoms. Thus, they diffuse more deeply and more widely so as to define the channel. The width of the channel can thus be tailored for desired device characteristics.

The further processing steps, namely CVD oxide deposition, oxide etch for polysilicon and source/body contacts, metallization, metal etch, and passivation are standard and will not be described further.

### Conclusion

In summary, it can be seen that the present invention renders the fabrication of insulated gate transistors more efficient through the elimination of all but a single diffusion step. There are no special masking steps required beyond those required in the prior art processes, and the process parameters are generally within the scope of the pre-existing processes.

While the above is a complete description of a number of embodiments, various modifications, alternatives, and equivalents may be used. For example, while the specific description is in terms of fabricating insulated gate transistors, at least some bipolar transistors and thyristors could also be made using a single diffusion step following three or more implantation steps. Moreover, while the specific implementation for insulated gate transistors is an n-channel process, the technique would be applicable to p-channel processes as well, so long as the dopants are chosen to have

the correct relative diffusion rates. At present, known p-type dopants diffuse more rapidly than known n-type dopants, so the applicability to p-channel devices would appear limited.

Therefore, the above description should not be taken as  
5 limiting the scope of the invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. In a process of fabricating an insulated gate transistor having body and source regions, including the steps, performed after the deposition and patterning of a polysilicon layer, of (a) implanting and (b) diffusing impurities of one of two conductivity types, (c) implanting and (d) diffusing a heavy dose of impurities of the same conductivity type, and (e) implanting and (f) diffusing impurities of the other conductivity type, the improvement wherein:

said implanting steps (a), (c), and (e) are the only implanting steps performed in connection with forming the body and source regions

said implanting steps (a), (c), and (e) are performed with no intervening high-temperature processing steps; and

said diffusing steps (b), (d), and (f) are performed at the same time.

2. In an n-channel process of fabricating an insulated gate transistor having body and source regions, including the steps, performed after the deposition and patterning of a polysilicon layer, of implanting and diffusing p impurities, p+ impurities, and n+ impurities, the improvement wherein:

all implanting steps for forming the body and source regions, including said steps of implanting p impurities, implanting p+ impurities, and implanting n+ impurities, are performed after said deposition and patterning of the polysilicon layer and are performed with no intervening high-temperature processing steps; and

said steps of diffusing p impurities, diffusing p+ impurities, and diffusing n+ impurities are performed at the same time.

3. A method of fabricating an insulated gate transistor comprising the steps of:

providing a semiconductor doped to a first conductivity type;

forming a gate oxide layer on the semiconductor;  
forming a polysilicon layer on the gate oxide layer;  
forming an opening in the polysilicon layer;  
implanting impurities of a second conductivity type  
5 opposite the first conductivity type using the polysilicon as a mask;

implanting a heavy dose of impurities of the second conductivity type in a first portion of the region defined by the opening, the first portion being spaced inwardly from the  
10 periphery of the opening;

implanting a heavy dose of impurities of the first conductivity type in a second portion of the region defined by the opening, at least part of the second portion being disposed adjacent the periphery of the opening;

15 the second portion being generally non-overlapping with the first portion; and

thereafter, performing a single diffusion step to define a well region of the second conductivity type and a source region of the first conductivity type;

20 all implanting steps for forming the p-well and source region, including said three implanting steps being performed with no intervening high-temperature processing steps.

25 4. The method of claim 3 wherein said three implanting steps are performed in the order recited.

5. A method of fabricating an insulated gate transistor comprising the steps of:

30 (a) providing an n-type semiconductor;  
(b) forming a gate oxide layer on the semiconductor;  
(c) forming a polysilicon layer on the gate oxide layer;

(d) forming an opening in the polysilicon layer to  
35 define a p-well area;

(e) implanting p-type impurities using the polysilicon as a mask;

(f) implanting p+ impurities within the region defined by the opening to establish at least one p+ region paced inwardly from the periphery of the opening;

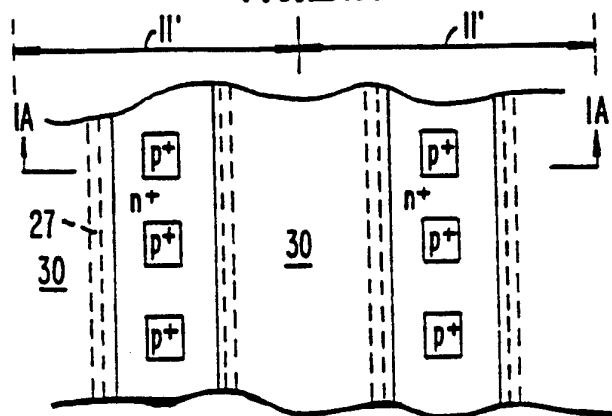
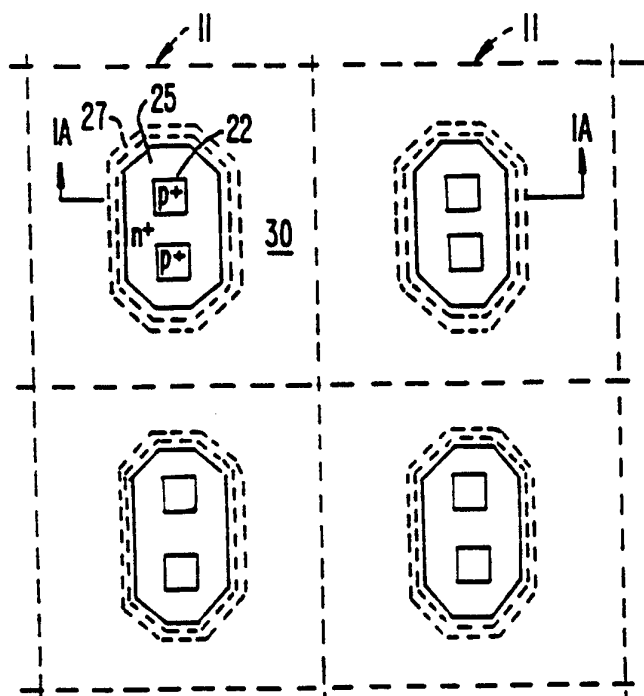
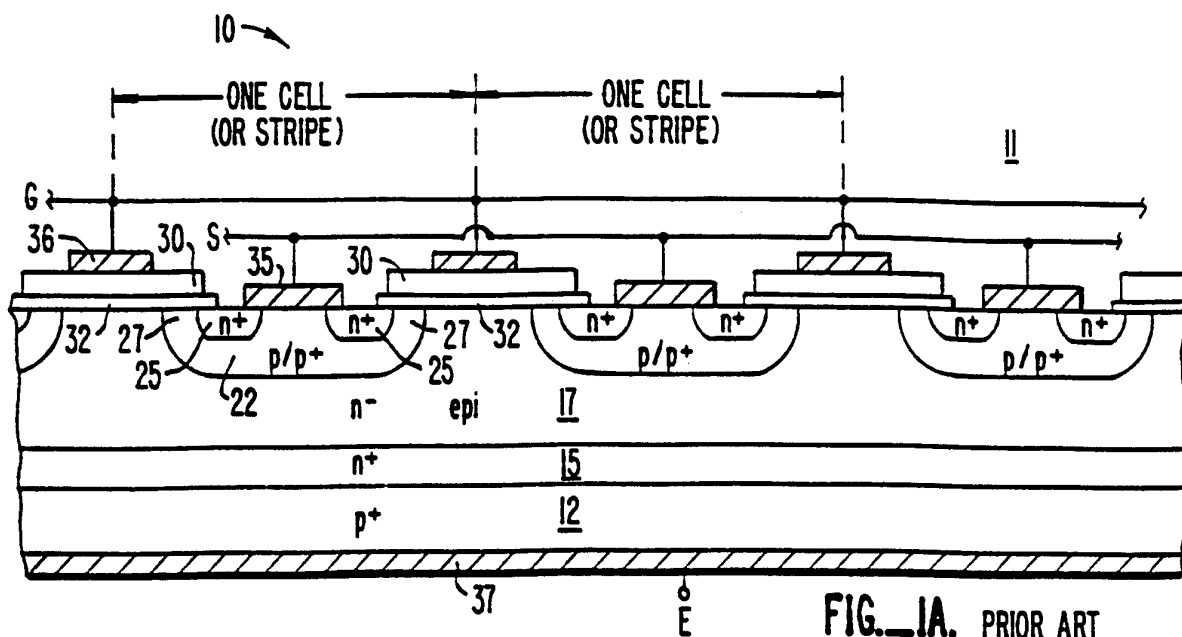
(g) implanting n+ impurities within the region  
5 defined by the opening to establish at least an n+ region, at least a part of which extends along the periphery of the opening, the n+ and p+ regions being generally non-overlapping; and

(h) thereafter, performing a single diffusion step to  
10 define a p-well and an n+ source region within the p-well;  
all implanting steps for forming the p-well and source region, including said steps (e), (f), and (g) being performed with no intervening high-temperature processing steps.

15 6. The method of claim 5 wherein said steps (e), (f), and (g) are performed in the order recited.

7. The method of claim 5 wherein said step of  
providing an n-type semiconductor comprises the steps of:  
20 providing an n+ substrate; and  
depositing an n- layer on the n+ substrate.

8. The method of claim 5 wherein each of said steps  
(d) through (h) is performed simultaneously over a plurality of  
25 discrete regions on the device.



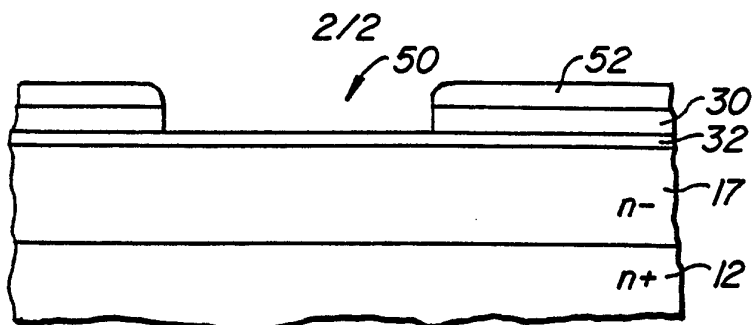


FIG. 2A.

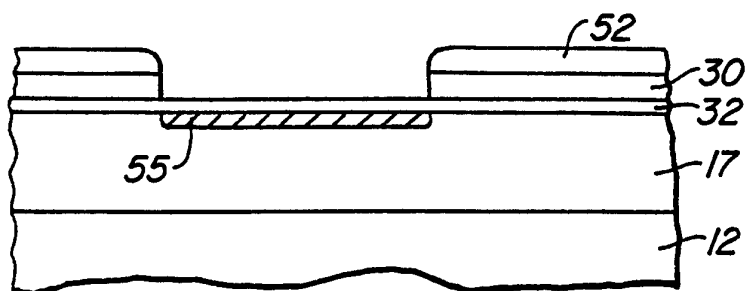


FIG. 2B.

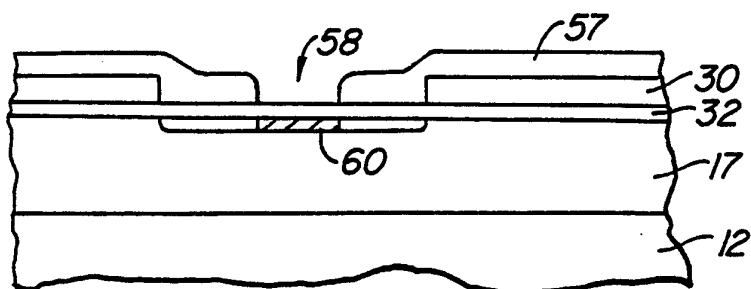


FIG. 2C.

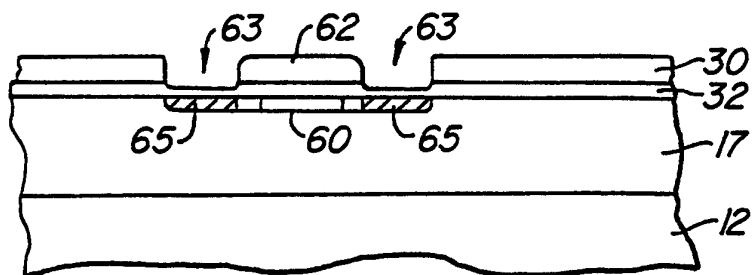


FIG. 2D.

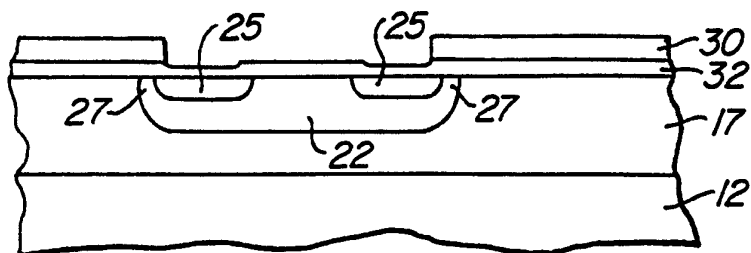


FIG. 2E.

## INTERNATIONAL SEARCH REPORT

PCT/US92/09832

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) :H01L 21/266

US CL :437/30,149,151; 148/DIG. 126

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/27,28,150,152,153,154; 148/DIG. 82; 257/341

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------|-----------------------|
| A         | JP, 2-296342 (HOSHI) 12 June 1990, See abstract and figs. 1d-1g.                   | 1-3,5                 |
| A         | US, A, 4,344,081 (PAO ET AL.) 10 August 1982, Text in columns 4-5, figs. 5-8.      | 1-8                   |
| A         | US, A, 4,697,333 (NAKAHARA) 06 October 1987, Text in column 3, figs. 2d-2f.        | 1-3,5,8               |
| A         | US, A, RE 32800 (HAN ET AL.) 13 December 1988, Text in column 4, figs. 5-7.        | 1-8                   |
| A         | US, A, 4,860,072 (ZOMMER) 22 August 1989, Text in columns 7,8, figs. 8,10-12.      | 1-8                   |

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

|                                                                                                                                                                         |                                                                                                                                                                                                                                                  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| * Special categories of cited documents:                                                                                                                                | *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention                                              |
| *A* document defining the general state of the art which is not considered to be part of particular relevance                                                           | *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone                                                                     |
| *E* earlier document published on or after the international filing date                                                                                                | *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
| *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | *Z* document member of the same patent family                                                                                                                                                                                                    |
| *O* document referring to an oral disclosure, use, exhibition or other means                                                                                            |                                                                                                                                                                                                                                                  |
| *P* document published prior to the international filing date but later than the priority date claimed                                                                  |                                                                                                                                                                                                                                                  |

Date of the actual completion of the international search

02 FEBRUARY 1993

Date of mailing of the international search report

09 MAR 1993

 Name and mailing address of the ISA/US  
 Commissioner of Patents and Trademarks  
 Box PCT  
 Washington, D.C. 20231

Facsimile No. NOT APPLICABLE

 Authorized officer *myman*  
 ANANDRA CHAUDHARI

Telephone No. (703) 308-1095

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US92/09832

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------|-----------------------|
| A         | US,A, 4,914,047 (SEKI) 03 April 1990, Text in column, 4, figs. 1d,2e-2g.           | 1-8                   |