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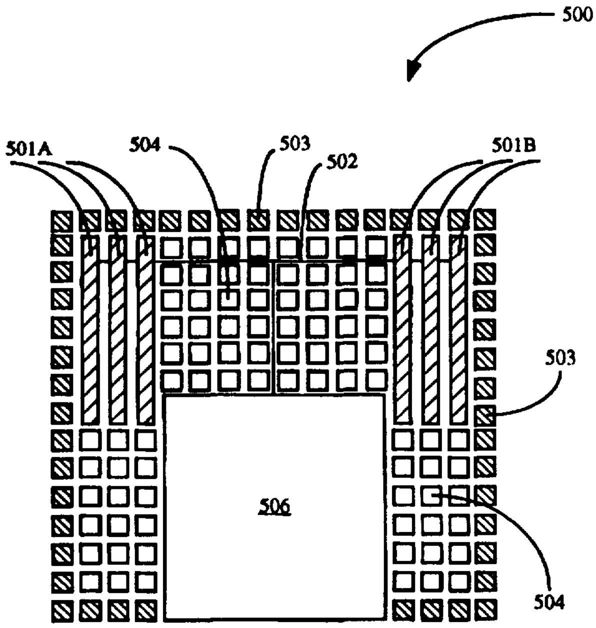
(57) Abstract

A chip (500) includes a programmable logic device and a microprocessor (506), wherein at least one of the associated registers (501A, 501B) of the microprocessor (506) is distributed in the programmable logic device. The distributed register (501A, 501B) is coupled to both the microprocessor (506) and the programmable logic device. In this manner, the microprocessor (506) has the ability to access the register and place a value into the programmable logic device all in one clock cycle. Additionally, the logic functions in the programmable logic device are also advantageously available to the microprocessor (506).



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MICROPROCESSOR WITH DISTRIBUTED REGISTERS ACCESSIBLE BY PROGRAMMABLE LOGIC DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to microprocessors, and in particular to a microprocessor having registers accessible by a programmable logic device.

Description of the Related Art

Microprocessors are well known in the art. Figure 1 illustrates a conventional configuration of a computer 100 having a microprocessor which includes an arithmetic logic unit (ALU) block 101 and a control unit 103. ALU block 101 manipulates data provided by input/output (I/O) device 102 and memory 104. I/O device 102 communicates with a user or a peripheral device (neither shown in Figure 1) via output bus 109A and input bus 109B. In one computer, I/O device 102 communicates with a keyboard or a field programmable gate array (FPGA)(described in further detail in reference to Figure 3). Memory 104 typically includes nonvolatile memory cells, such as electrically programmable read only memory (EPROM) cells for storing the computer program, and volatile memory cells, such as random access memory (RAM) cells for providing storage for data generated by ALU block 101. Control unit 103, relying on instructions provided in the computer program, controls the operation of ALU block 101, memory 104, and I/O device 102 via buses 111A/111B, 105A/105B, and 108A/108B, respectively.

Referring to Figure 2, ALU block 101 typically includes an ALU 112, a register file 114, multiplexer 121, and latches 113A, 113B, and 113C. An address from controller 103 (not shown) on bus 111A is provided to an input port 115A of register file 114, thereby selecting an output signal YA at a clock signal. Similarly another address from controller 103 on bus 111B is also provided to an input port 115B of register file 114, thereby selecting a second output signal YB at the same clock signal. In this manner, output signals YA and YB are provided simultaneously at the output ports of register file 114 on output lines 118A and 118B, respectively. Latches 113A and 113B are coupled between output lines 118A and 118B, respectively, and ALU 112. Thus, latches 113A and 113B, which continuously sample their input signals and change their output signals in response to their input signals independent of the clock signal provided to register file 114 in their enabled state, transfer output signals YA and YB to ALU 112. Multiplexer 121 is programmed to transfer either the output signal from ALU 112, the output signal from memory 104 via line 106A, or the output signal from I/O device 102 via line 107B to latch 113C. Latch 113C provides output signals to I/O device 102 and memory 104 on buses 107A and 106B, respectively. Note that latch 113C also typically provides a buffered feedback signal via buffer 120 on line 119 to a data input port DIN of register file 114.

In a conventional reduced instruction set computer (RISC) processor, an operation requires three machine operating cycles (hereinafter referred to as periods). These periods are Read, ALU Operating, and Write periods. For example, during the Read period, control unit 103 (Figure 1) retrieves an instruction from memory 104 and transfers the address portions of that instruction to register file 114 (Figure 2) via bus 111A or bus 111B to retrieve operands on output lines 118A/118B. During the ALU operating period, the operation designated by the instruction is performed in ALU 112. Finally, during the Write period, the result is stored in register file 114 via feedback line 119 and data input port DIN. Note that the data write address is included as part of the instruction and is typically saved until needed.

The Read, ALU Operating, and Write periods are overlapping. For example, a register may perform a Write operation in one-half of one period and perform a Read operation in the other half of that period. It logically follows that periods do not correspond to specific clock cycles. Addresses are provided on buses 111A or 111B from control unit 103 as necessary.

One typical instruction to register file 114 is to add the value in a first register to the value in a second register (neither register shown), and then put the result of this summation into the second register of register file 114. In this manner, ALU block 101 operates as an accumulator. Alternatively, the value in latch 113C is written to a I/O device 102, such as an FPGA, via output bus 107A. Thus, one instruction is required to move the data, whereas another instruction is required to retrieve the result, thereby introducing considerable delay in the microprocessor and I/O device interface.

Therefore, a need arises for a structure which minimizes instructions and associated delay in the interface between the microprocessor and the I/O device.

SUMMARY OF THE INVENTION

In accordance with the present invention, a programmable logic device and a microprocessor are formed on the same chip. In one embodiment, the programmable logic device is a field programmable gate array (FPGA) having configurable logic blocks (CLBs). At least one associated register of the microprocessor is distributed in the FPGA. The distributed register remains architecturally part of the microprocessor, but is accessible by at least one CLB in the FPGA. Additionally, because each distributed register is associated with a particular configurable logic block in the FPGA, a logic function in the configurable logic block is advantageously available via the distributed register to the microprocessor. Thus, the distributed register operates as a bridge between the logic in the FPGA and the microprocessor.

In one embodiment, a distributed register includes a plurality of D flip-flops. Each flip-flop samples its input signal and changes its output signal at the rising edge of a controlling clock signal provided by the microprocessor. The output terminals of the flip-flops are coupled to a first plurality of tristate buffers. A first decoder associated with the distributed register detects whether signals provided on a first address bus match an address which identifies the distributed register. Specifically, if the first decoder detects signals on the first address bus which match the address of the distributed register, then the first decoder enables the first plurality of tri-state output buffers, thereby placing the stored register values of the plurality of D flip-flops onto a first data bus. The first address bus and the first data bus form part of a bus structure which is coupled to the microprocessor and to the FPGA. In one embodiment, the bus structure is formed separately from the interconnect matrix of the FPGA.

In accordance with the present invention, the first data bus, in addition to providing output signals to the microprocessor, also serves as an input bus. Specifically, if predetermined signals are placed on the first address bus, the first decoder disables the first plurality of tri-state buffers and a second decoder activates the clock enable terminals of the flip-flops, thereby allowing the data on the first data bus to be written into these flip-flops.

In further accordance with the present invention, the output terminals of the flip-flops are also coupled to at least one configurable logic block in the FPGA. In this manner, one advantage of the present invention is that the output signals of the distributed registers are directly available at all times to any predetermined configurable logic block. In this embodiment, these output lines are formed as part of the interconnect matrix of the FPGA.

Therefore, the first data bus and the output lines of the flip-flops ensure that the distributed register is completely accessible to the configurable logic block. In this manner, the FPGA is effectively provided with a local connection to the microprocessor. This local connection in turn ensures a fast microprocessor/FPGA interface because an instruction from the microprocessor is simultaneously provided to the configurable logic block. Similarly, a logic function provided in the configurable logic block is provided to the microprocessor within one clock cycle (i.e. determined by the first and second decoders).

In another embodiment of the present invention, the output terminals of the flip-flops are coupled to a second plurality of tri-state buffers. If a third decoder detects signals on a second address bus which match the address of the distributed register, then the third decoder enables the second plurality of tri-state buffers, thereby placing the stored register values of the plurality of flip-flops onto a second data bus. The second address bus and the second data bus also form part of the above-referenced bus structure. In yet other embodiments of the present invention, the above-referenced bus structure forms part of the FPGA interconnect matrix.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a conventional configuration of a computer having a microprocessor.

Figure 2 shows a prior art ALU block having an associated register file.

Figure 3 illustrates a field programmable gate array (FPGA) having a plurality of configurable logic blocks.

Figure 4 shows an illustrative configurable logic block.

Figure 5 illustrates an FPGA chip in accordance with the present invention including a microprocessor and a plurality of distributed registers.

Figure 6 shows a register block in accordance with the present invention.

Figure 7 shows one embodiment of a flip-flop used in the distributed register of the present invention.

Figure 8 illustrates various locations in a configurable logic block for connection to a distributed register.

Figure 9 shows the interconnection of the ALU block with a distributed register of the present invention.

Figure 10 shows various locations in another configurable logic block for connection to a distributed register.

DETAILED DESCRIPTION OF THE DRAWINGS

In accordance with the present invention, a microprocessor and a field programmable gate array (FPGA) are formed on the same chip. Predetermined registers of the microprocessor are distributed in the FPGA, thereby significantly increasing the speed of operation of the microprocessor/FPGA interface in comparison to prior art interfaces.

FPGA's are well known in the art. Figure 3 illustrates a simplified FPGA 300 having configurable logic blocks 301-1 to 301-9. Each configurable logic block (CLB) 301 is capable of performing any one of a plurality logic functions depending on the input signals CLB 301 is provided (described in further detail in reference to Figure 4). A plurality of control signals (not shown) program an interconnect matrix 302, thereby determining the interconnection of CLBs 301-1 to 301-9 to each other and to I/O pads 303. Each I/O pad 303 provides an interface between an external package pin (not shown) and the internal logic of CLBs 301 via interconnect matrix 302. A detailed explanation of one interconnect matrix 302 and its operation is provided in U.S. Patent Re.34,363, reissued on August 31, 1993 which is herein incorporated by reference in its entirety.

An illustrative configurable logic block 301 is shown in Figure 4. In this embodiment, configurable logic block 301 includes a combinatorial function block 401 comprising a 32 by 1 look-up table to implement Boolean functions, two flip-flops 402, 403, and an internal control section (including multiplexers 404-412, and an OR gate 413). The five logic variable input signals, A, B, C, D, and E, and feedback signals QX, QY (from flip-flops 402, 403, respectively) determine which address in the look-up table is selected. The above-referenced internal control section determines whether the output signals of combinatorial function block 401, i.e. signals F and G, a data signal on line DATA IN, or output signals from flip-flops 402 and 403 are provided as output signals X and Y of configurable logic block 301. Specifically, multiplexers 411 and 412 select between providing the synchronous signals from registers 402 and 403 or the asynchronous signals from combinatorial function block 401. Multiplexers 404 and 410 determine whether the input signals provided to flip-flops 402 and 403, respectively, are derived from feedback lines, the DATA IN line, or the F or G output terminals of combinatorial function block 401 (determined by multiplexers 405 and 406). Multiplexers 404 and 410 are discussed in further detail in reference to Figure 7. A detailed explanation of configurable logic block 301 and its operation is provided on pages 2-109 to 2-117 of "The Programmable Logic Data Book" (which is herein incorporated by reference in its entirety), published in 1994 by Xilinx, Inc. having a location at 2100 Logic Drive, San Jose, California 95124.

Note that although the present invention is described in detail in reference to FPGA 300 and configurable logic block (CLB) 301, the present invention is implementable in other chip architectures and CLB configurations. For example, the present invention is equally applicable to the chip architectures and CLB configurations of the Xilinx XC4000™ family of devices (see Figure 10) and XC2000™ family of devices which are illustrated and described on pages 2-9 to 2-18 and pages 2-187 to 2-199, respectively, of "The Programmable Logic Data Book". Supra.

Figure 5 illustrates one embodiment of an FPGA chip 500 in accordance with the present invention. In this embodiment, FPGA chip 500 includes a microprocessor unit 506 (which, as described previously, comprises a control unit as well as an ALU block (neither shown for simplicity)), and a plurality of register blocks 501A and 501B which are distributed among CLBs 504. Thus, instead of physically locating all of register file 114 next to ALU 112 as taught in the prior art (Figure 2), the register file is divided into a plurality of register blocks which in turn are distributed throughout chip 500.

A bus structure 502, which connects register blocks 501A and 501B to microprocessor unit 506, includes an address bus and a data bus (described in detail in reference to Figure 6). In this embodiment of the present invention, both the address and data buses of bus structure 502 are formed separately from the FPGA interconnect matrix, whereas in another embodiment, both the address and data busses of bus structure 502 form part of the FPGA interconnect matrix. Chip 500 further includes a plurality of I/O blocks 503 positioned at the periphery of chip 500. I/O blocks 503 are described in detail in pages 2-107 to 2-108 of "The Programmable Logic Data Book". Supra.

Figure 6 illustrates one embodiment of a distributed register block 501 which includes a plurality of D flip-flops 601_1-601_N (wherein N is an integer). Each flip-flop 601 is a positive edge-triggered D flip-flop that samples its input signal at the D input terminal and changes its output signal on the Q output terminal at the rising edge of a controlling clock signal provided on the clock pulse (CP) terminal. This controlling clock signal is provided by microprocessor 506 (Figure 5) on line 610.

The WRITE operation associated with distributed register block 501 is triggered by a signal provided from microprocessor 506 via READ/WRITE (R/W) line 621 (Figure 6). For example in one embodiment of the present invention, a low signal provided on R/W line 621 indicates a WRITE operation. This low signal provided to decoder 605 prompts that decoder to disable tri-state buffers 602_1-602_N, thereby preventing any transfer of register values to data bus 618_N. If decoder 606, in addition to detecting the high signal provided by inverter 621A in the WRITE state, also detects signals on address bus 611_B which match the address of register block 501, then decoder 606 provides an enabling signal to the clock enable (CE) terminal of flip-flops 601_1-601_N.

Figure 7 shows one embodiment of an illustrative flip-flop 601, i.e. flip-flop 601_1, which includes a multiplexer

702 and a standard D flip-flop 701. If flip-flop 601_1 receives an enabling signal, multiplexer 702 transfers the signal provided on data line 618_{B1} to the D input terminal of D flip-flop 701. This signal is subsequently transferred to the Q output terminal of flip-flop 701 at the next clock signal provided on line 610.

In contrast, a high signal (indicating a READ operation) on R/W line 621 (Figure 6) is inverted by inverter 621A and provided to decoder 606. This low signal prompts decoder 606 to provide a disabling signal to the clock enable (CE) terminal of flip-flop 601. If flip-flop 601 receives a disabling signal from decoder 606 via line 705 (Figure 7), multiplexer 702 prevents a signal from being loaded from line 618_{B1} into the D input terminal of D flip-flop 701. Instead, in this disabled configuration, at each clock signal on line 610, multiplexer 702 transfers the output signal on the Q output terminal of D flip-flop 701 to its D input terminal via feedback loop 706. Thus, the signal on the Q output terminal of flip-flop 701 remains constant irrespective of the signal provided on line 608_{B1}.

Referring back to Figure 6, if decoder 605 detects signals on address bus 611_B which match the address of distributed register block 501 and detects the high signal on line 621 (indicating a READ state), then decoder 605 enables tri-state output buffers 602_1-602_N, thereby placing the stored register values on the Q output terminals of flip-flops 601_1-601_N onto data bus 618_B (assuming multiplexers 622_1-622_N, which are explained in detail in reference to Figure 8, are appropriately programmed). Thus, in the present invention, data bus 618_B, in addition to providing input signals to distributed register block 501 from microprocessor 506 (Figure 5), also serves as an output bus. Note that in one embodiment during an initial reset, flip-flops 601_1-609_N are reset by a signal provided on their reset terminals R via lines 709_1-709_N, respectively. Data bus 618_B forms part of bus structure 502 (Figure 5) which is coupled to microprocessor 506. Address buses 611_A and 611_B also form part of bus structure 502 of chip 500.

If decoder 604 detects signals on address bus 611_A which match the address of distributed register block 501, then decoder 604 enables tri-state output buffers 603_1-603_N, thereby placing the stored register values on the Q output terminals of flip-flops 601_1-601_N onto data bus 618_A (still ignoring multiplexers 622_1-622_N). Note that decoder 604 operates in a READ state irrespective of the signal on R/W line 621. Data bus 618_A forms part of bus structure 502 (Figure 5) which is coupled to microprocessor 506.

Figure 9 shows an illustrative interconnection of an ALU block 901 to distributed register block 501 (Figure 6). Specifically, buses 111A and 111B from controller 103 (Figure 1) transfer signals to buses 611_A and 611_B, respectively. Thus, buses 111_A and 111_B form part of bus structure 502 (Figure 5). Buses 611_A and 611_B in turn transfer signals to distributed register block 501 as well as ALU block 901. One of the lines of data bus 618_A, in Figure 9 line 618_{A1}, is coupled to output line 118A from register file 114. Similarly, one of the lines of data bus 618_B, in Figure 9 line 618_{B1}, is coupled to output line 118B from register file 114. Because of the bidirectional character of data bus 618_B (described in detail in reference to Figure 6), line 618_{B1} is also coupled to feedback line 119 of ALU block 901. In this embodiment, tri-state buffers 920A-920C selectively allow transfer of the signals to lines 118B, 618_{B1}, 118A, respectively. Control unit 103 (Figure 1) controls the operation of tri-state buffers 920A-920C.

Referring back to Figure 6, output lines 609_1 - 609_N of flip-flops 601_1-601_N, respectively, are coupled to at least one CLB 504 on FPGA chip 500 (Figure 5). In this embodiment, output lines 609_1 - 609_N form part of interconnect matrix 302 (Figure 3), wherein one output line 609 is provided to one CLB 504 (explained in detail in reference to Figure 8). Therefore, one advantage of the present invention is that an output signal of distributed register block 501 is available at all times to a predetermined CLB 504 (Figure 5) and thereafter to any CLB via the general interconnect. Thus, the lines of data bus

608_B and output lines 609 ensure that distributed register block 501 is locally accessible to CLBs 504. In this manner, the FPGA array is effectively provided with a fast connection to microprocessor 506. This fast connection in turn ensures a fast microprocessor/FPGA interface because a signal from microprocessor 506 is simultaneously provided to a CLB 504. Similarly, a logic function provided in a CLB 504 is provided to microprocessor 506 within one clock cycle (i.e. determined by decoders 604, 605, and 606).

In one embodiment of the present invention, the FPGA and the microprocessor are asynchronous, i.e. use different clocks. Therefore, a need arises for a "handshake" that indicates data which is provided to register block 501 by the microprocessor using the microprocessor clock has in fact been received by register block 501. Flip-flop 612 receives the identical clock enable signal and clock pulse signal as are received by flip-flops 601. However, unlike flip-flops 601, flip-flop 612 receives a constant logic one on its D input terminal and provides a signal FLAG to the FPGA logic and the microprocessor. Thus, a logic one provided on the Q output terminal of flip-flop 612 indicates that the data provided by the microprocessor has been received by register block 501. To complete the handshake and to prepare for the next data transfer, the FPGA logic provides a signal RESET to flip-flop 612 to reset the value of the signal stored on the Q output terminal to zero.

Figure 8 illustrates the locations in configurable logic block 301 which can provide connection to distributed register 501 (Figure 6). Specifically, shaded areas 800 indicate logic elements which can be coupled to either data bus 618_B or output lines 609_1-609_N. For example in one configuration, at least one of the Q output terminals of flip-flops 402 and 403 is coupled to data bus 618_B via a multiplexer 622 (Figure 6). In another configuration, at least one of the output terminals of multiplexers 404, 405, 406, 410, 411, or 412, or the F and G output terminals of combinatorial function block 401 is coupled to data bus 618_B via a multiplexer 622 (Figure 6). In yet another configuration, an output line 609 is coupled to an input terminal of either combinatorial function block 401, or to the input terminal of one of multiplexers 404, 405, 406, 410, 411, or 412 (wherein these multiplexers change in configuration from two-input to three-input multiplexers). Figure 10 illustrates a simplified block diagram of another configuration logic block (associated with the Xilinx XC4000™ family of devices), wherein shaded areas 1000 indicate logic elements which can be coupled to either data bus 618_B or output lines 609_1-609_N (Figure 6).

Note that in one embodiment, one bit of the register in the present invention is associated with the CLB (thereby implying that only one source in the CLB is selected for connection to the register), whereas in other embodiments two bits are associated with the CLB (thereby implying that two sources in the CLB are selected for connection to the register).

The present invention provides the following advantages:

1. The microprocessor is faster than prior art microprocessors because a microprocessor in accordance with the present invention executes, in a single period, specialized complex instruction implemented in FPGA logic. Therefore, programs contain fewer instructions and are executed in fewer periods.

2. Because all distributed registers are simultaneously available to the microprocessor and the FPGA, operations can be done in parallel.

3. The microprocessor has the ability to emulate logic in the FPGA. Thus, instead of having CLBs implementing logic, a software program can take certain input signals from the FPGA, combine them in the microprocessor, and then provide the results back to the FPGA. In this manner, the microprocessor may replace several function generators, thereby saving significant space on the FPGA chip.

4. The distributed registers provide for faster communication between the microprocessor and a peripheral device (through the FPGA logic). Note that in one

embodiment, the peripheral device is implemented in the FPGA.

The above-described embodiments of the present invention are illustrative only and not limiting. Other embodiments will be apparent to those skilled in the art in light of the Specification and its associated figures. The present invention is set forth in the appended claims.

CLAIMS

1. A chip comprising:

a programmable logic device; and

a microprocessor having an associated register, wherein said associated register is distributed in said programmable logic device.

2. The chip of Claim 1 wherein said associated register includes means for communicating with said microprocessor and said programmable logic device.

3. The chip of Claim 2 wherein said associated register includes a plurality of flip-flops, each flip-flop receiving a clock signal also provided to said microprocessor.

4. The chip of Claim 3 wherein said associated register includes means for directing the output signals of each flip-flop.

5. The chip of Claim 4 wherein said means for directing includes a first plurality of tri-state buffers coupled to the output terminals of said flip-flops.

6. The chip of Claim 5 further including a first data bus, wherein the output terminals of said first plurality of tri-state buffers are coupled to said first data bus.

7. The chip of Claim 6 further including a first address means, wherein if said first address means is activated by a first bit pattern, then said first plurality of tri-state buffers are activated to provide the stored output signals of said flip-flops onto said first data bus.

8. The chip of Claim 7 wherein said first address means includes a first address bus for providing said first bit pattern, and a first decoder coupled to said first

address bus for determining if said first bit pattern is detected.

9. The chip of Claim 8 wherein said first address means further includes a second decoder coupled to said first address bus and to an enable terminal of each flip-flop.

10. The chip of Claim 9 wherein said first data bus is further coupled to the data input terminals of said flip-flops.

11. The chip of Claim 10 wherein if a second bit pattern is provided on said first address bus, then said first decoder deactivates said first plurality of tri-state buffers and said second decoder activates said enable terminals of said flip-flops, thereby transferring signals on said first data bus to said data input terminals of said flip-flops.

12. The chip of Claim 11 wherein said first data bus is coupled to said microprocessor and said programmable logic device.

13. The chip of Claim 12 further including a plurality of output lines, wherein said output terminal of each flip-flop is coupled to a corresponding output line.

14. The chip of Claim 13 wherein said output lines are coupled to said programmable logic device.

15. The chip of Claim 14 further including a second plurality of tri-state buffers coupled to said output terminals of said flip-flops.

16. The chip of Claim 15 wherein said second plurality of tri-state buffers are coupled to a second data bus.

17. The chip of Claim 16 wherein said second data bus is coupled to said microprocessor.

18. The chip of Claim 17 further including a second address means, wherein if said second address means is activated by a third bit pattern, then said second tri-state buffers are activated to provide the stored output signals of said flip-flops onto said second data bus.

19. The chip of Claim 18 wherein said second address means includes a second address bus for providing said third bit pattern, and a third decoder coupled to said second address bus for determining if said third bit pattern is detected.

20. A method of reducing the delay of a microprocessor/ programmable logic device interface including the steps of:

forming a microprocessor and a programmable logic device on a chip;

distributing a plurality of registers associated with said microprocessor in said programmable logic device; and

connecting said plurality of registers to said microprocessor and said programmable logic device.

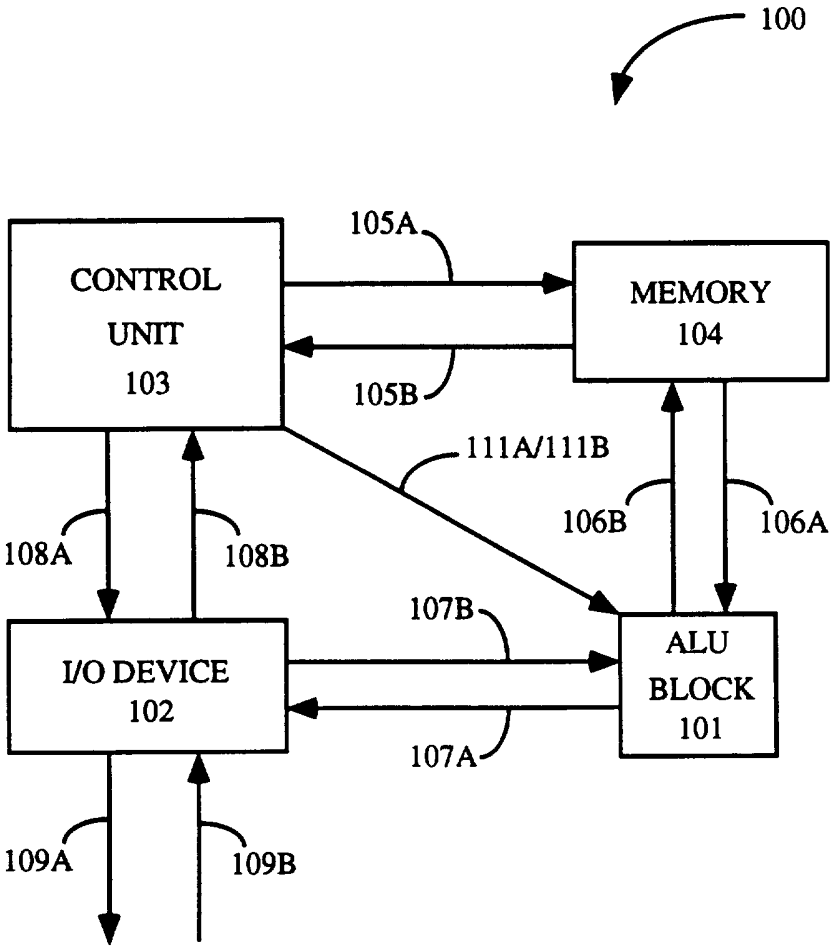


Figure 1
Prior Art

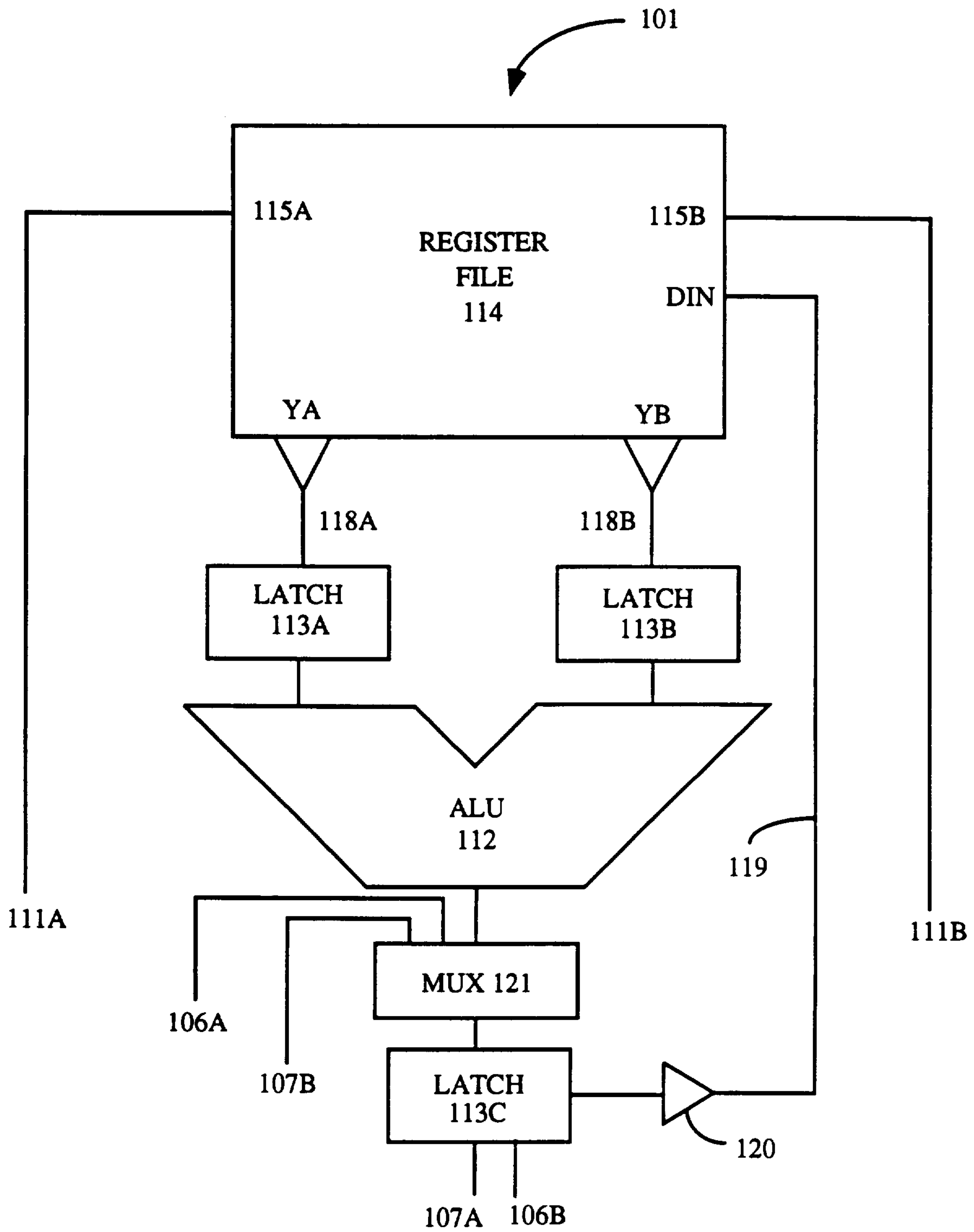


Figure 2

Prior Art

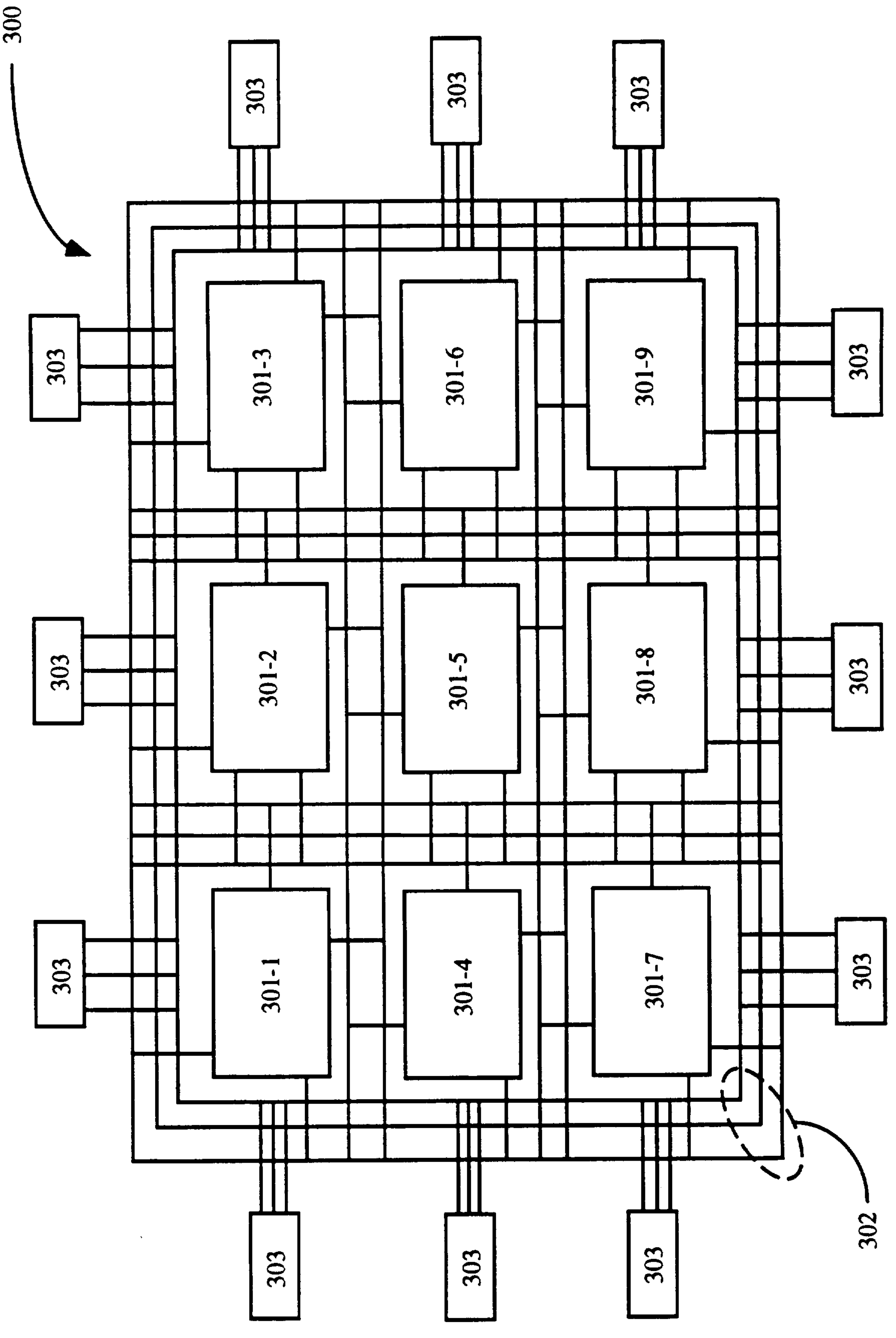
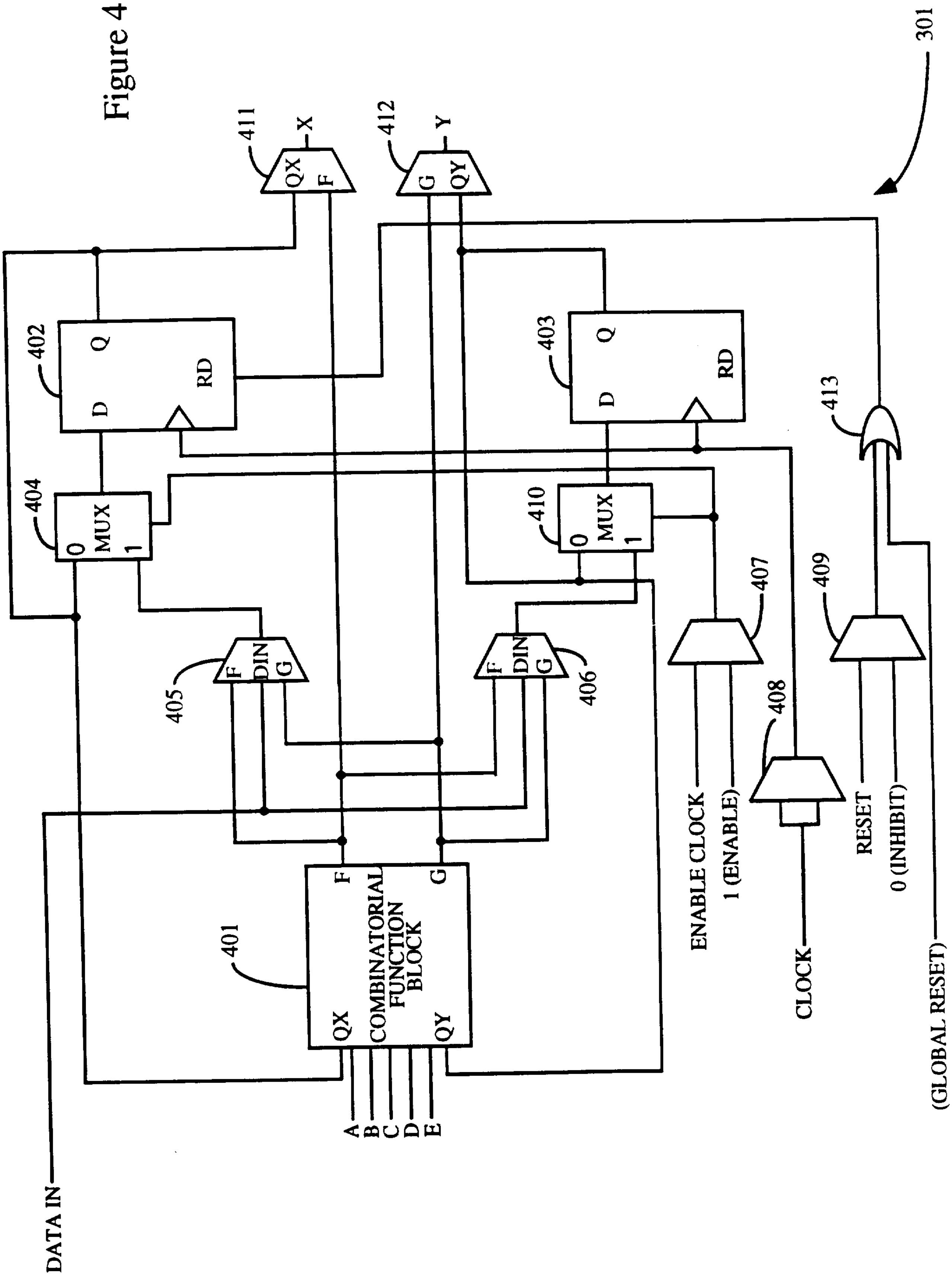


Figure 3

Figure 4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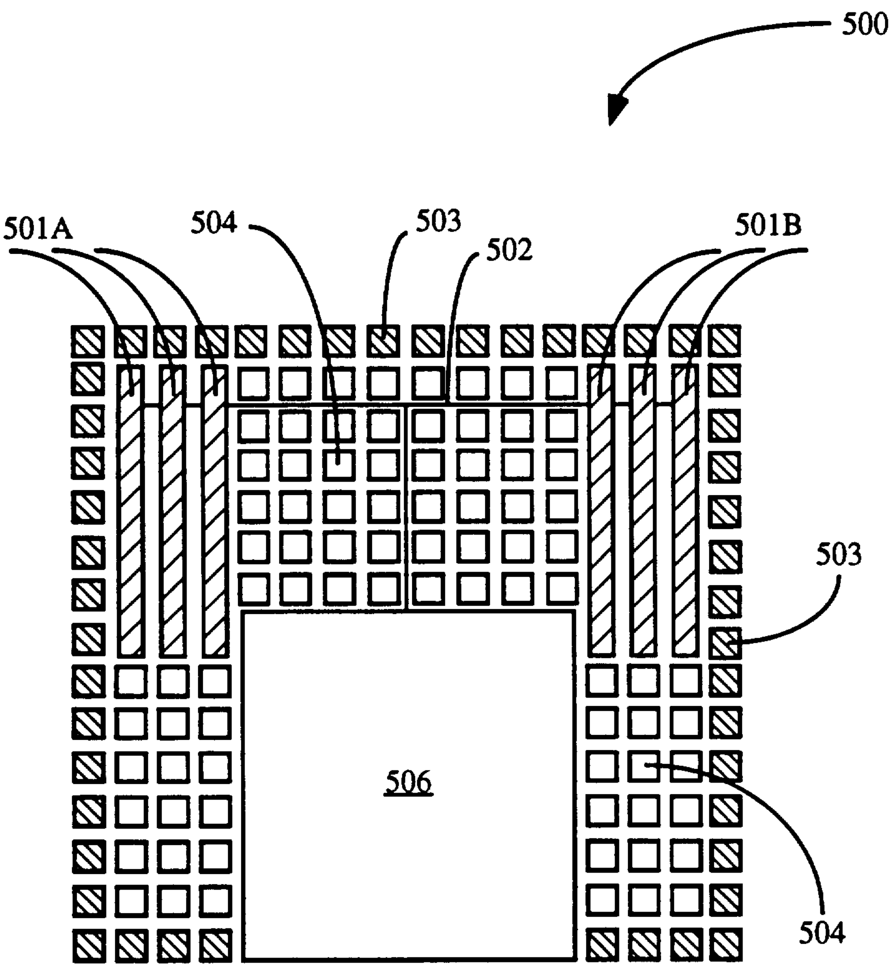
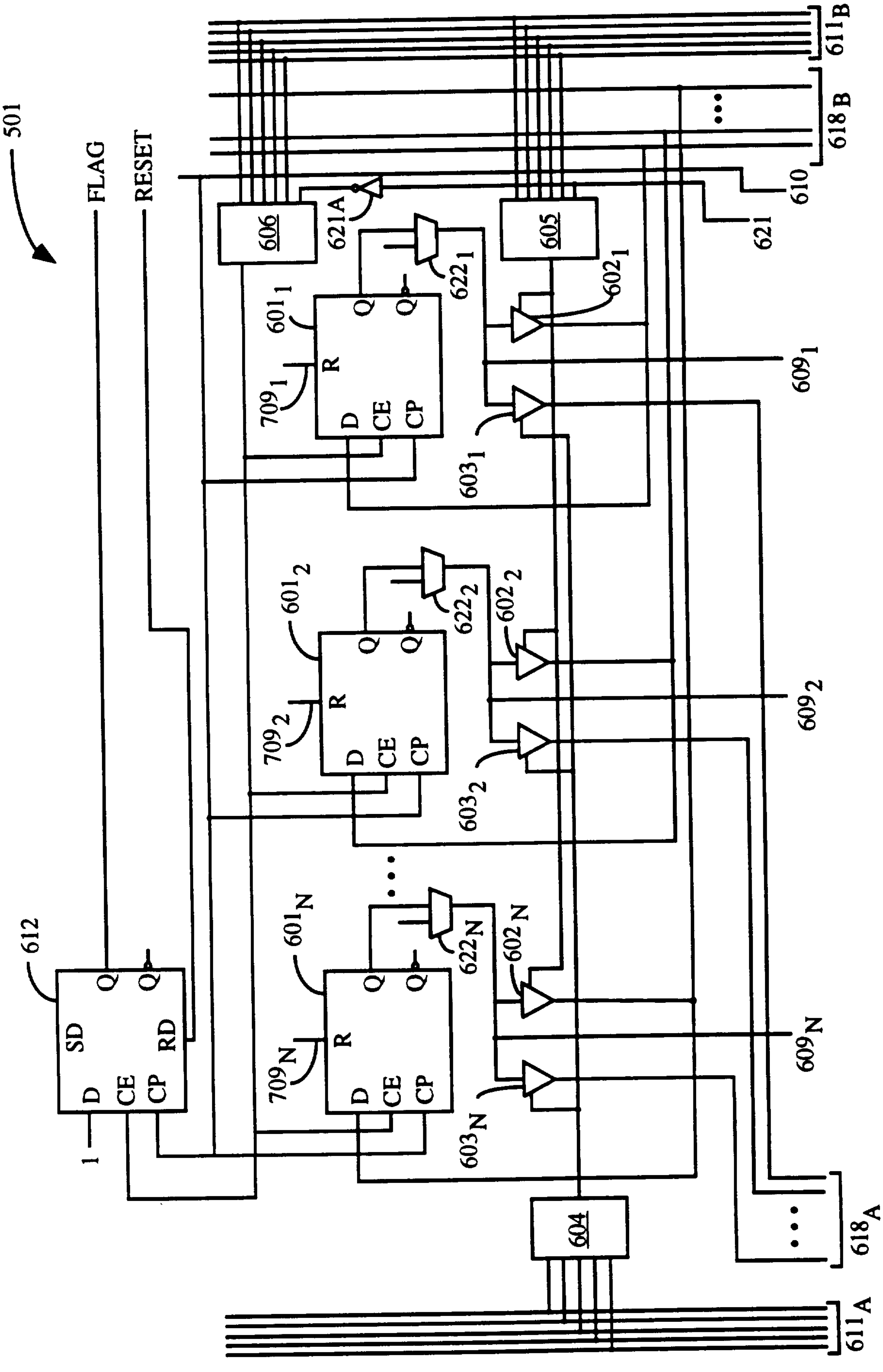


Figure 5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FLAG
RESET
611_B
618_B
610
621
621A
606
605
604
612
601_1
601_2
601_N
602_1
602_2
602_N
603_1
603_2
603_N
609_1
609_2
609_N
622_1
622_2
622_N
709_1
709_2
709_N
618_A
611_A
D
CE
CP
R
Q
SD
RD
1

Figure 6

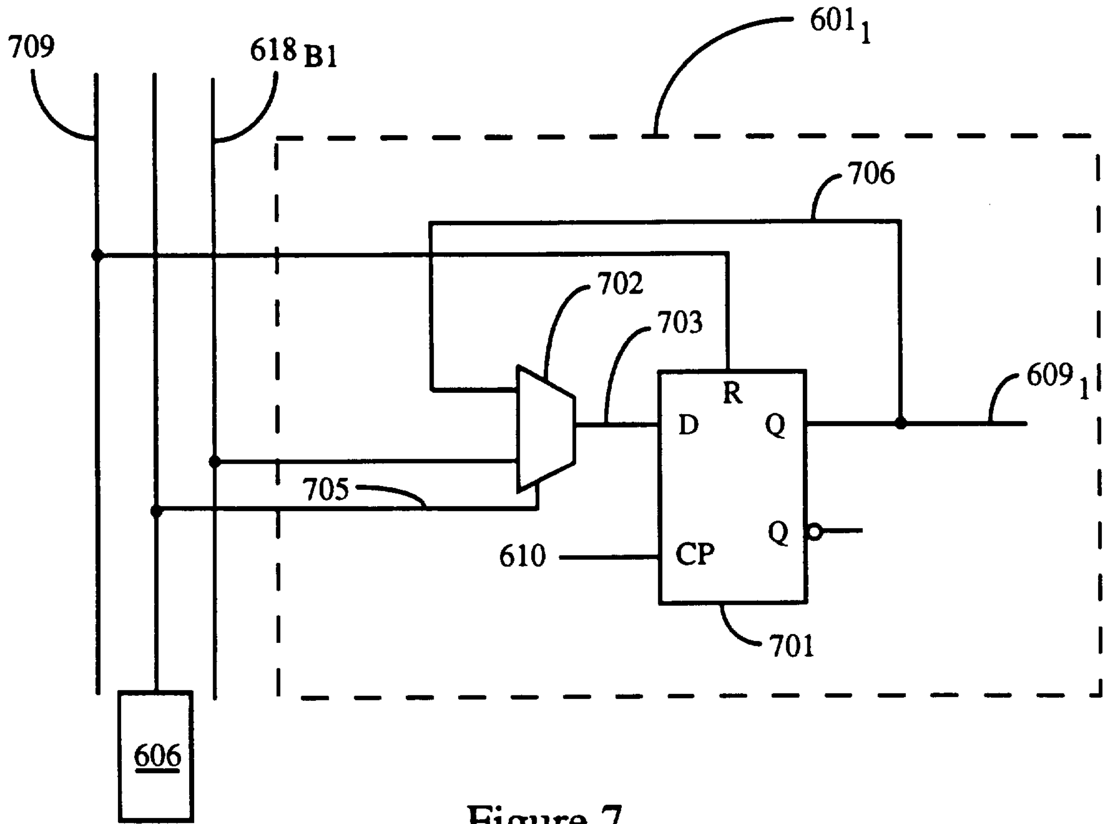

Figure 7

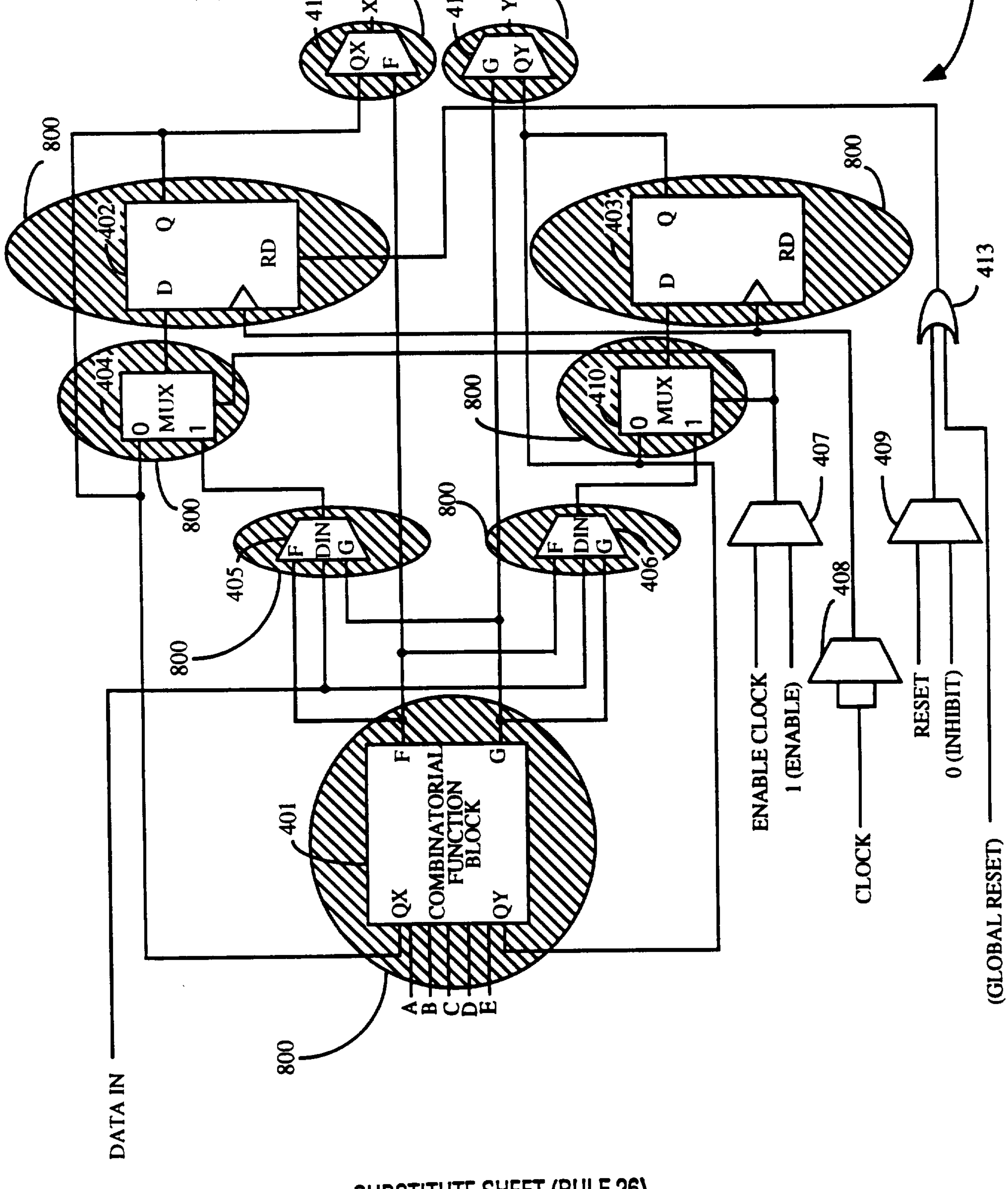
COMBINATORIAL
FUNCTION
BLOCK
QX
F
QY
G
A
B
C
D
E
401
402
403
D
Q
RD
404
410
MUX
0
1
405
406
F
DIN
G
407
408
409
411
412
413
QX
X
G
QY
Y
800
301
DATA IN
ENABLE CLOCK
1 (ENABLE)
CLOCK
RESET
0 (INHIBIT)
(GLOBAL RESET)

Figure 8

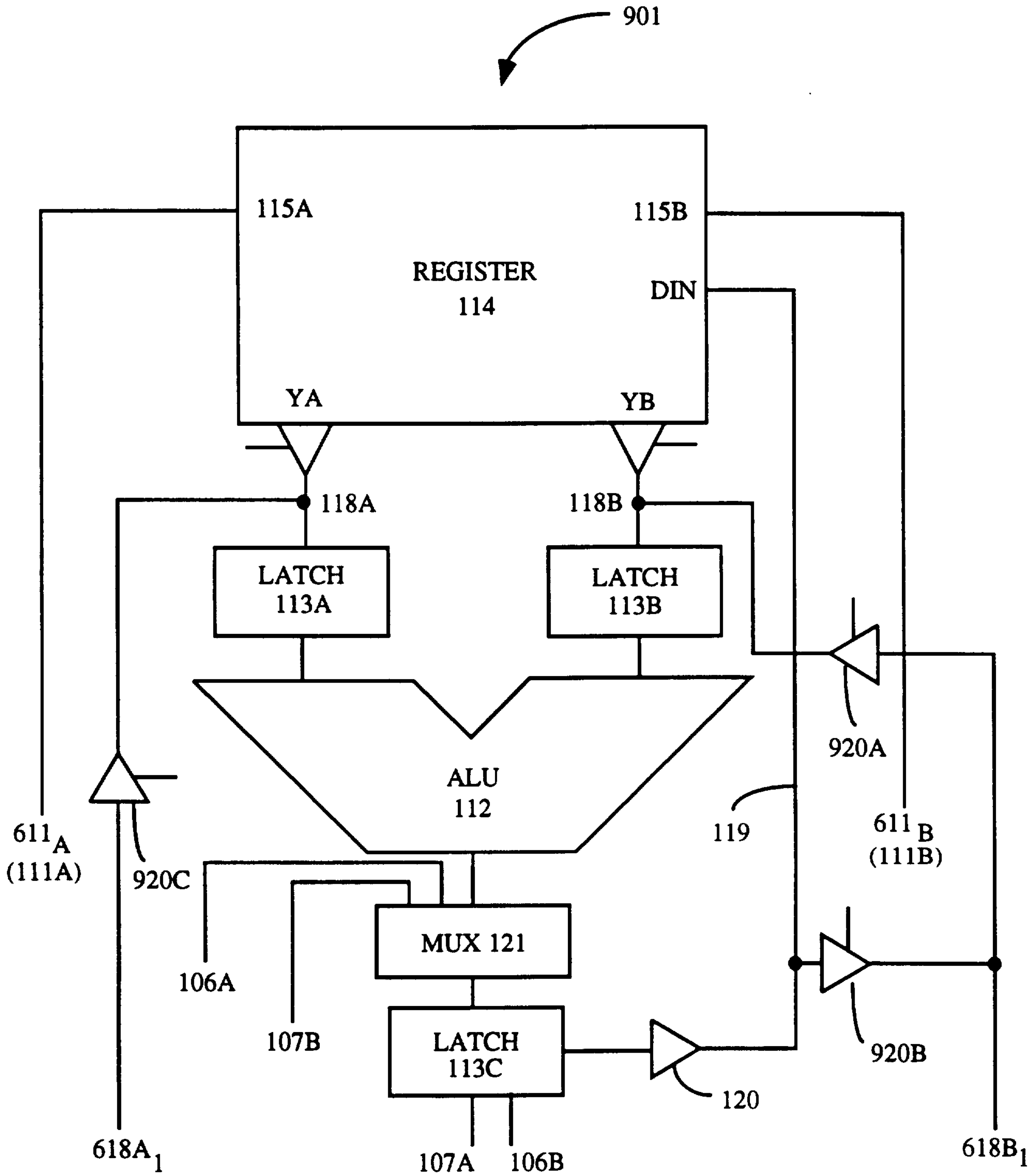
901
115A
115B
REGISTER
114
DIN
YA
YB
118A
118B
LATCH
113A
LATCH
113B
920A
ALU
112
119
611A
(111A)
920C
611B
(111B)
MUX 121
106A
107B
LATCH
113C
920B
120
618A1
107A
106B
618B1

Figure 9

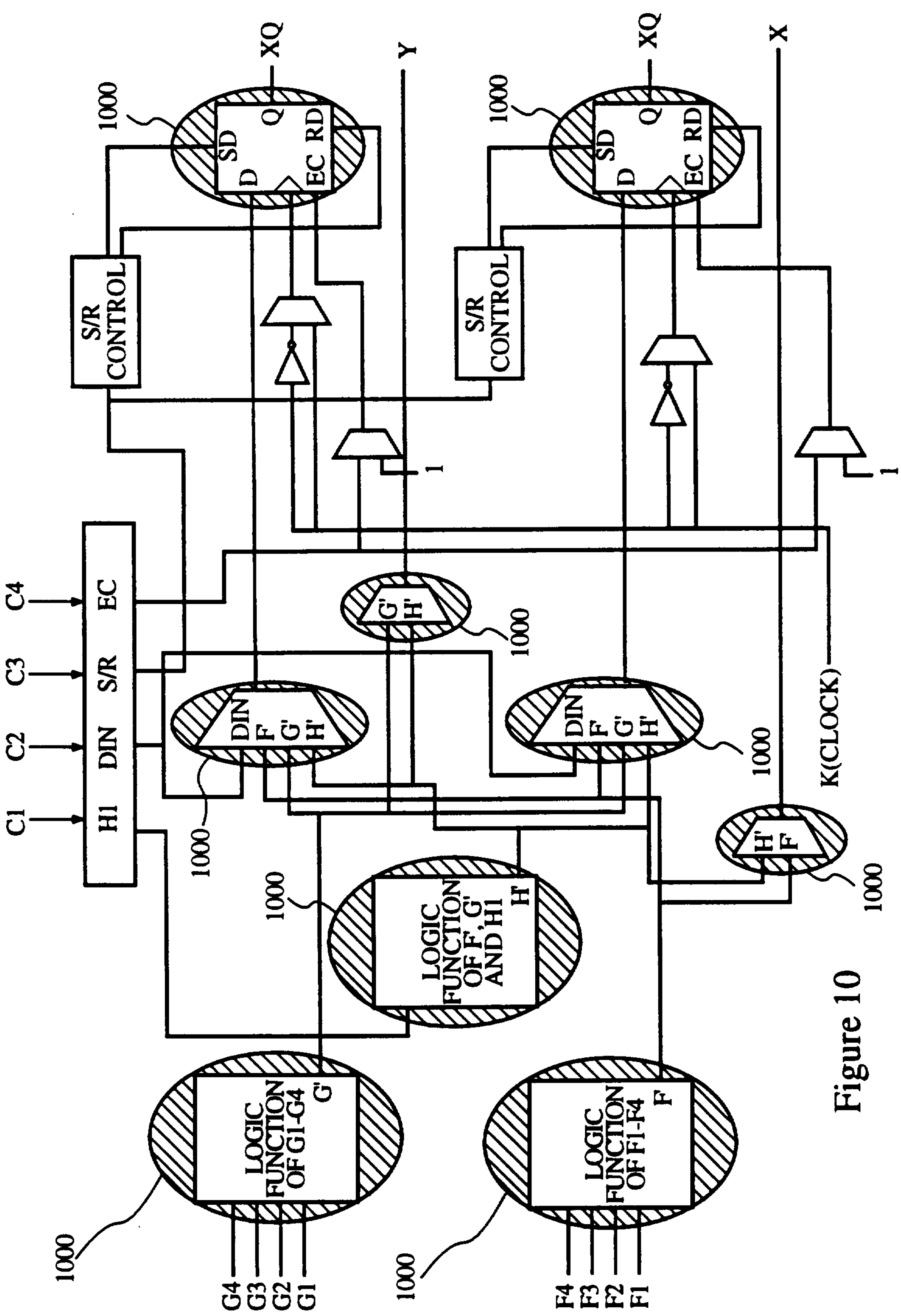
C1
C2
C3
C4
H1
DIN
S/R
EC
S/R CONTROL
S/R CONTROL
SD
D
Q
EC
RD
XQ
Y
X
1
DIN
F'
G'
H'
K(CLOCK)
LOGIC FUNCTION OF F', G' AND H1
LOGIC FUNCTION OF G1-G4
LOGIC FUNCTION OF F1-F4
G4
G3
G2
G1
F4
F3
F2
F1
1000

Figure 10

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/05847

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F15/78 H03K19/177

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 315 275 (LSI LOGIC CORP) 10 May 1989 see column 2, line 50 - column 3, line 17 see column 5, line 8 - line 31; figures ---	1-6,20
A	US,A,5 142 625 (NAKAI MASAAKI) 25 August 1992 see the whole document ---	1-20
A	PROCEEDINGS OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE, SAN DIEGO, MAY 9 - 12, 1993, no. CONF. 15, 9 May 1993, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 3.02.01-3.02.04, XP000409635 DAVIDSON J: "FPGA IMPLEMENTATION OF A RECONFIGURABLE MICROPROCESSOR" see the whole document -----	1,20

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
2 August 1996	26.08.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Blaas, D-L

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/05847

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0315275	10-05-89	US-A-	4878174	31-10-89
		DE-D-	3853613	24-05-95
		DE-T-	3853613	24-08-95
		JP-A-	2035523	06-02-90
		US-A-	5155819	13-10-92
US-A-5142625	25-08-92	JP-A-	61285545	16-12-86
		JP-A-	61285567	16-12-86
		JP-A-	61285546	16-12-86
		JP-A-	61285547	16-12-86
		JP-A-	61285568	16-12-86