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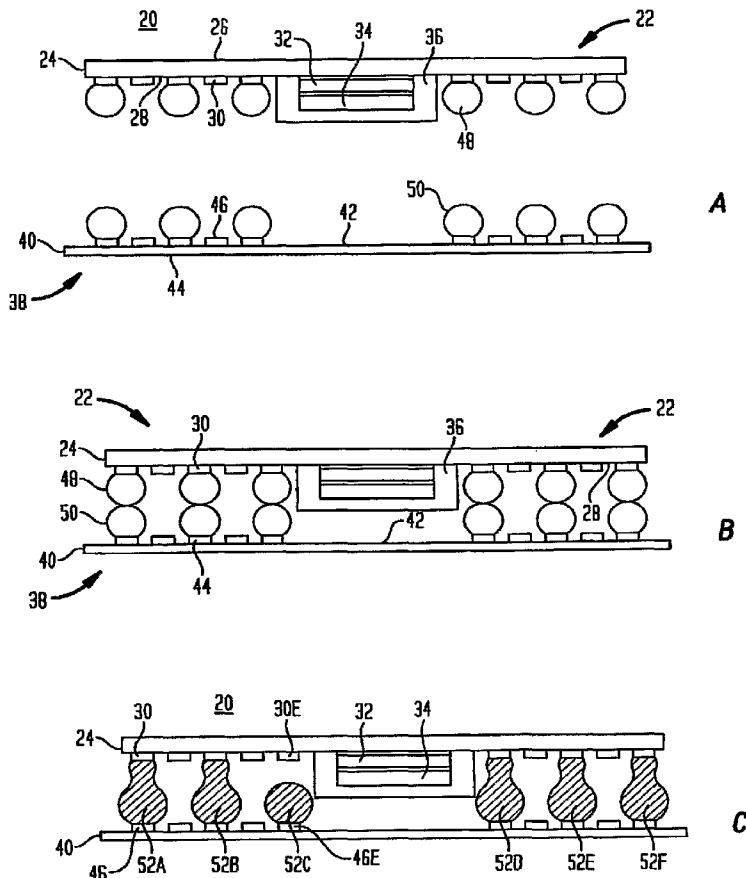
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[Continued on next page]

(54) Title: MICROELECTRONIC ASSEMBLIES HAVING VERY FINE PITCH STACKING



(57) Abstract: A method of making a stacked microelectronic assembly includes providing a first microelectronic package 122A having a first substrate 124A and conductive posts 130A extending from a surface 128A of the first substrate 124A, and providing a second microelectronic package 122B having a second substrate 124B and conductive, fusible masses 148B extending from a surface 126B of the second substrate 124B. A microelectronic element 154A is secured over one of the surfaces of the first and second substrates 124A, 124B, the microelectronic element 154A defining a vertical height H<sub>1</sub> that extends from the one of the surfaces of the first and second substrate to which the microelectronic element is secured. The tips 131A of the conductive posts 130A of the first substrate are abutted against the apices of the fusible masses 148B of the second substrate, whereby the vertical height of each conductive post/fusible mass combination is equal to or greater than the vertical height of the microelectronic element 154A secured to the one of the surfaces of said first and second substrates.

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FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,  
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**INTERNATIONAL SEARCH REPORT**

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**B. FIELDS SEARCHED**

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	the whole document	7, 10, 11, 19, 20, 34, 37, 38
Y	US 6 476 503 B1 (IMAMURA KAZUYUKI [JP] ET AL) 5 November 2002 (2002-11-05)  column 22, lines 22-67; figures 49, 50 column 20, lines 40-47; figures 54A, 54B  ----- -/--	7, 10, 11, 19, 20, 34, 37, 38

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Information on patent family members

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