

[54] **CURRENCY TESTING SYSTEM**

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[51] Int. Cl. **B07c 3/12**

[58] Field of Search **209/72, 75, 82; 250/219 219LG**

[56] **References Cited**

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Primary Examiner—Richard A. Schacher

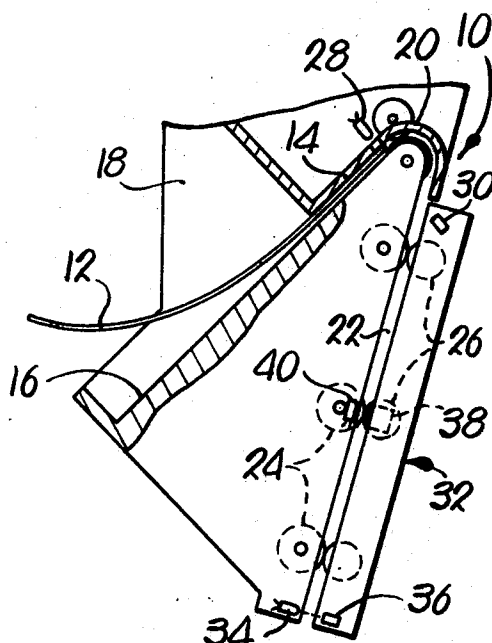
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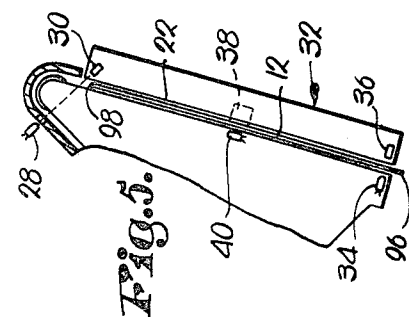
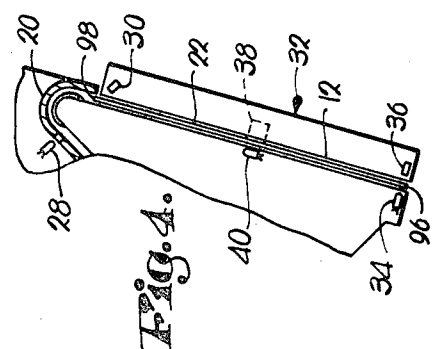
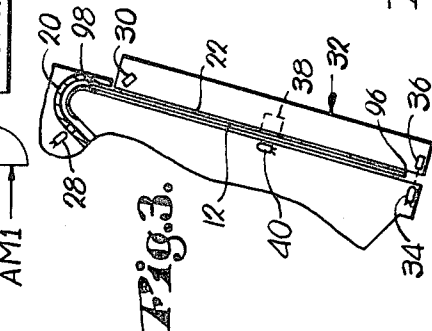
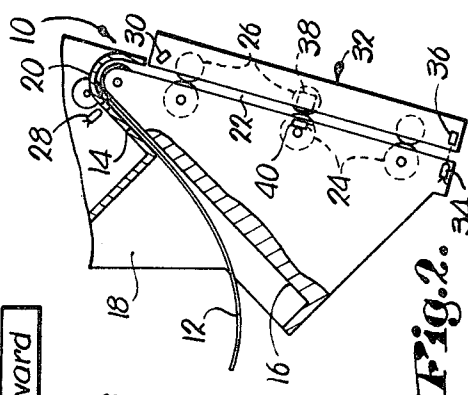
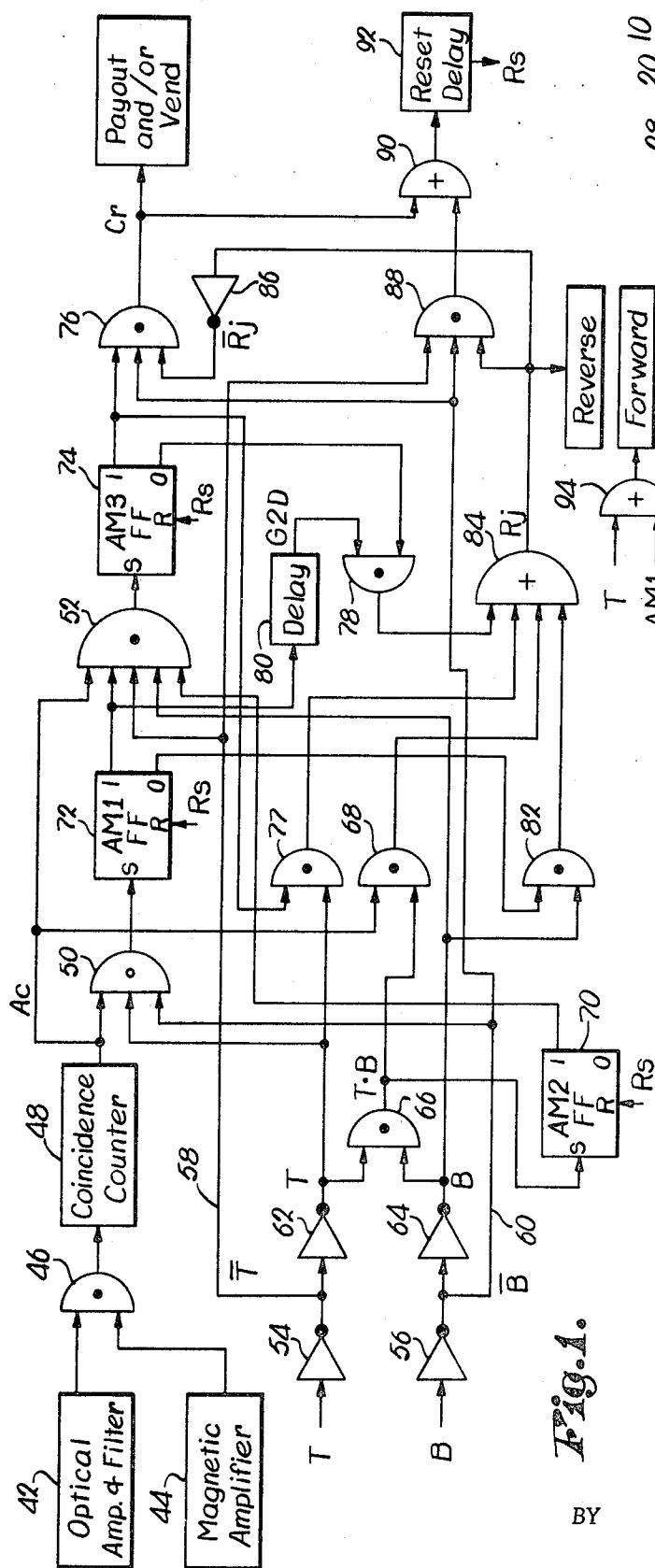
[57] **ABSTRACT**

In a currency acceptor, a transport having a reversible

drive conveys a bill to be tested along a path of travel past a first photoelectric detector, a transducer head at a test station for sensing the physical properties of the bill, and then a second photoelectric detector. If the grid areas on opposite sides of the portrait on the bill have physical properties indicative of validity, testing circuitry responsive to the head produces an accept signal as each grid area passes the head. To be deemed valid, the first grid area must cause the production of an accept signal, the leading and trailing edges of the bill must be concurrently detected by the two photoelectric detectors as the portrait passes the head (determines that the bill is not too short), the second grid area must cause the production of a second accept signal by the time the bill reaches a predetermined position along the path, and thereafter the first photoelectric detector must not detect the bill or another, following bill until such time that the bill completely passes the second photoelectric detector and is accepted. If an invalid condition is encountered, the transport drive is reversed and the bill or counterfeit material is returned to the depositor and thereby rejected.

6 Claims, 8 Drawing Figures





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Standby

T	Mtr.	Opt.	Mag.	Ac	AM1	B	AM2	AM3	Cr	Rs
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	0
1	1	0	0	0	1	1	1	0	0	0
0	1	0	0	0	1	1	1	0	0	0
0	1	1	1	0	1	1	1	0	0	0
0	1	1	1	1	1	1	1	0	0	0
0	1	1	1	1	1	1	1	1	0	0
0	1	0	0	0	1	1	1	1	0	0
0	1	0	0	0	1	0	1	1	1	0
0	1	0	0	0	1	0	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0

Fig.8.

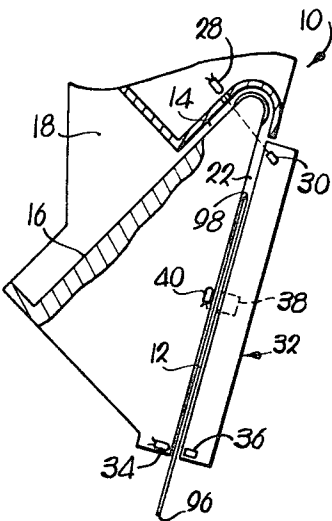


Fig.6.

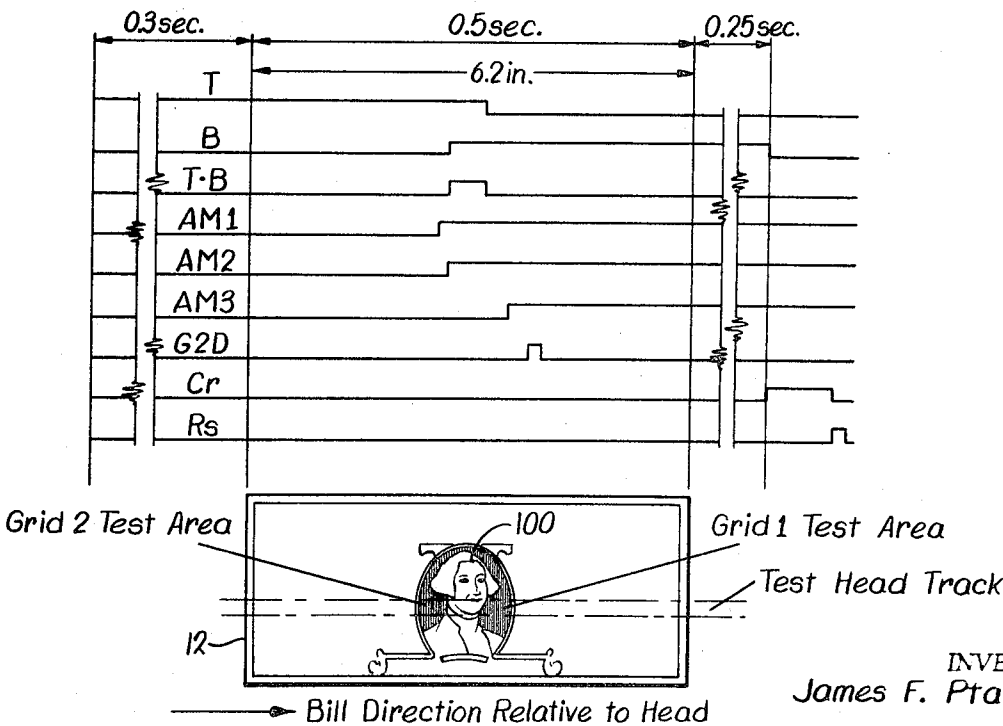


Fig.7.

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CURRENCY TESTING SYSTEM

CROSS-REFERENCES

See my concurrently filed copending application, Ser. No. 79,456, now U.S. Pat. No. 3,656,835 issued Apr. 18, 1972 entitled "Receiving and Transporting Apparatus for Currency," and the copending application of Boley A. Andrews and James F. Ptacek, Ser. No. 886,530, filed Dec. 19, 1969, and entitled "Combined Optical and Magnetic Transducer", now U.S. Pat. No. 3,612,835 issued Oct. 12, 1971.

This application relates to improvements in systems for testing a bill deposited in a currency acceptor or validator, in order to determine whether the bill is valid or invalid and to effect acceptance if valid or rejection if invalid.

It is an important object of the present invention to provide, in a currency acceptor for receiving individual bills inserted therein, an improved system for running a series of tests on an inserted bill to determine the validity thereof.

Another important object of this invention is to provide a system as aforesaid capable of running sequential tests regarding the physical properties of the bill, the length thereof and the locations of various features of the bill relative to its length.

Still another important object of the invention is to provide a system as aforesaid in which the various tests are run as the bill is conveyed by a transport along a predetermined path of travel, and wherein essentially instantaneous rejection of the bill by reversal of the transport drive is effected if an invalid condition is encountered.

Other objectives and features of the present invention will become apparent as the detailed description proceeds.

In the drawings:

FIG. 1 is a block and logic diagram of the currency testing system;

FIG. 2 is a diagrammatic, sectional view of a currency acceptor employing a bill transport of the type shown and described in my above-identified copending application Ser. No. 79,456, now U.S. Pat. No. 3,656,615 issued Apr. 18, 1972 showing the locations of the photoelectric detectors and the transducer head;

FIGS. 3-6 are a series of views similar to FIG. 2 showing the inserted bill at progressive stages of advancement through the acceptor;

FIG. 7 shows the test areas of a one dollar bill of United States currency, and includes a graph illustrating the timing of certain signals produced by the system; and

FIG. 8 is a table explaining the logic of the system.

DESCRIPTION — FIGS. 1 AND 2

Referring initially to FIG. 2, a currency acceptor is shown having a bill transport 10 which receives a bill 12 guided into a slot 14 by a ramp 16 that, together with other parts of the acceptor housing, presents an insert opening 18. The bill 12 is initially placed in the opening 18 upon the ramp 16 and its leading edge is manually fed into the slot 14, causing activation of the transport 10 in a manner to be subsequently described.

The transport 10 advances the bill 12 around a sharp bend 20 and then along a path of travel defined by an elongated, longitudinally straight, narrow channel 22.

The bill 12 is conveyed by friction rollers such as illustrated at 24 and, in the channel 22, such rollers are opposed by idler rollers 26. The transport 10 employs a constant speed, reversible drive, all of the rollers 24 being of the same diameter and driven at the same speed. Accordingly, the bill 12 is maintained in a flat condition sandwiched between the opposed rollers 24 and 26, as it is advanced along the rectilinear path defined by the narrow channel 22.

A small lamp 28 (hereinafter referred to as the "top light") is arranged to direct a beam of light toward a phototransistor 30 located in an electronics module 32. The light beam is interrupted by the bill 12 when the leading edge of the bill is fully inserted in the slot 14 as illustrated in FIG. 2. The beam from top light 28 will continue to be blocked by the bill 12 until the trailing edge thereof passes the upper end of the channel 22, as will be discussed hereinafter. A second electric lamp 34 (hereinafter referred to as the "bottom light") is located at the bottom of the channel 22 and directs a beam of light across the channel 22 toward a phototransistor 36. If further details are desired respecting the structure and operation of the transport 10, the physical arrangement of the bill detection devices or the test station to be subsequently described, reference may be made to my above-identified copending application Ser. No. 79,456.

A combined optical and magnetic transducer 38 presents the test station and is mounted in the electronics module 32 midway between the phototransistors 30 and 36 and is opposed by an electric lamp 40 on the other side of the channel 22. A combined transducer head of this type is shown and described in the above-identified copending application of Andrews and Ptacek, Ser. No. 886,530, and may be referred to for a disclosure of the exact construction of the head. It should be understood, however, that other types of transducers may be employed in the present invention depending upon the nature of the circuitry responsive to the transducer utilized to determine whether or not the physical properties of the bill sensed by the transducer are characteristic of a genuine bill.

In FIG. 1 an optical amplifier and bandpass filter 42 is illustrated and is responsive to the optical sensing of the transducer head 38, in this instance the transmittance of the bill 12. An amplifier 44 is responsive to the electrical output of the transducer head 38, which will be a function of the magnetic properties of the printing on the bill 12. The outputs of the optical and magnetic channels are fed into an AND gate 46 that, in turn, has its output connected to the input of a coincidence counter 48. As will be discussed more fully hereinafter, physical properties of the bill indicative of validity cause the counter 48 to deliver an accept signal Ac to both a three-input AND gate 50 and a five-input AND gate 52.

The input of a logic inverter 54 is designated T, and the input of a logic inverter 56 is designated B. T represents interruption of the light beam from the top light 28, which causes the bill 12 to be detected by the phototransistor 30 since the light normally impinging thereon is blocked. Likewise, B represents interruption of the light path of the bottom light 34, which causes the phototransistor 36 to detect the bill since the light

normally impinging thereon is now blocked by the presence of the bill. By inversion, $\bar{T}$ appears on line 58 from the output of the inverter 54, and $\bar{B}$ appears on line 60 from the output of the inverter 56.

An inverter 62 is in series with the inverter 54 and thus its output is designated T. Likewise, an inverter 64 in series with the inverter 56 delivers an output designated B. A two-input AND gate 66 delivers an output T-B which is fed to one input of a reject AND gate 68 and to the set input (S) of a set-reset flip-flop 70.

The output of the AND gate 50 is connected to the set input (S) of a set-reset flip-flop 72 having outputs designated "1" and "0". This same nomenclature is used to identify the outputs of the flip-flop 70, and it may be seen that the "1" outputs of both of the flip-flops 70 and 72 are connected to inputs of the AND gate 52. The two remaining inputs of AND gate 52 are connected to line 58 and the output of inverter 64.

The output of AND gate 52 is fed to the set input (S) of a set-reset flip-flop 74 having its "1" output connected to one input of a three-input AND gate 76, and to one input of a two-input reject AND gate 77. The "0" output of flip-flop 74 is connected to one input of a two-input reject AND gate 78, the other input thereof being connected to the "1" output of flip-flop 72 via a delay circuit 80. A fourth reject AND gate 82 has two inputs connected to the "0" output of flip-flop 72 and the output of inverter 64 respectively. The outputs of the four reject AND gates, 68, 77, 78 and 82 are connected to respective inputs of a four-input OR gate 84. When one of its inputs is excited at the 1 logic level, the OR gate 84 delivers a reject command Rj at its output which effects a reversal of the transport drive, as diagrammatically indicated by the block labelled "Reverse." An inverter 86 is connected between the output of OR gate 84 and one of the inputs of AND gate 76, the output of inverter 86 being designated by the logic notation $\bar{R}_j$.

The remaining input of AND gate 76 is connected to line 60, such gate being operable to deliver a credit signal Cr at its output which is fed to the credit establishing circuitry of a vending machine, or initiates change payout, etc. This broad function is represented by the block labelled "Payout and/or Vend." Manifestly, the particular use to be made of the credit signal Cr is dependent upon the particular apparatus with which the testing system of the present invention is utilized.

A reset AND gate 88 is responsive to Rj and has its output connected to one input of a two-input reset OR gate 90, the other input thereof being responsive to Cr. The output of OR gate 90 is fed to a delay circuit 92 that, in turn, delivers a reset pulse Rs to the reset inputs (R) of the flip-flops 70, 72 and 74.

The reversible drive of the bill transport 10 is functionally illustrated by the blocks carrying the legends "Forward" and "Reverse." The reverse mode in response to Rj is discussed above. Normal operation in the forward direction is initiated by T, and such operation is sustained by the occurrence of the 1 logic level at the "1" output of flip-flop 72, represented by the notation AM1. Both T and AM1 are applied to respective inputs of an OR gate 94 whose output executes the forward drive function.

LOGIC EXPLANATION AND CORRELATION WITH FIGS. 3-6

It should be understood that the various gates and flip-flops are responsive only to input signals at the 1 logic level. The flip-flop 72 is the first accept memory in the logic system and, when set, the 1 logic level appears at its "1" output and is referred to herein as AM1. The flip-flop 70 is the second accept memory of the system; accordingly, a 1 logic level at its "1" output will be referred to as AM2. The flip-flop 74 is the third accept memory of the system, thus setting thereof produces a 1 logic level at its "1" output that will be referred to herein as AM3.

The table illustrated in FIG. 8 shows the operation of the system in logic steps from the standby condition to reset (return to standby). The presence of a "0" in a particular column of the table indicates that the particular function or signal represented in the column is not being produced; conversely, the appearance of a "1" indicates the presence of such function. The second column identified "Mtr" refers to the motor or drive of the bill transport 10. The third and fourth are identified "Opt." and "Mag." respectively, referring to the optical and magnetic channels of the discriminator circuitry. The other column headings have been previously identified.

FIG. 3 illustrates the position of the bill 12 in the acceptor at the time AM1 is produced (flip-flop 72 set), assuming that the bill has passed the first validity test. Note that the leading edge 96 of the bill is approaching but has not as yet interrupted the light impinging on the bottom phototransistor 36. The trailing edge 98 still blocks the light emanating from the top light 28.

FIG. 4 shows the position of the bill 12 at the time of occurrence of T-B and the setting of flip-flop 70, producing AM2. The rays from both the bottom light 34 and the top light 28 are blocked by the leading and trailing edges 96 and 98 respectively.

FIG. 5 shows the bill 12 at the time that the flip-flop 74 is set, producing AM3, assuming that the appropriate test has been passed. Note that the trailing edge 98 of the bill 12 now does not block light from the top light 28.

FIG. 6 shows the bill 12 still later in its path of travel at a time when a second grid delay pulse G2D is delivered by the delay circuit 80. This will be discussed more fully hereinafter.

OPERATION

The bill 12 is inserted into opening 18 and advanced by hand into slot 14 in a prescribed orientation until the light path from the top light 28 is interrupted. This occurrence is T and starts the transport drive in the forward direction. Referring to FIG. 7, the graph illustrates that, in an exemplary drive arrangement, 0.3 sec. elapses from the time that the drive is activated until the leading edge of the bill 12 is between the transducer head 38 and the opposing lamp 40. A time period of 0.5 sec. is then required for the bill to pass completely by the head, i.e., at the expiration of the next 0.5 sec., the trailing edge of the bill will be leaving the head 38. Being a constant speed drive, time may be equated to distance. Accordingly, a one dollar bill of United States currency is illustrated having a length of approximately 6.2 inches, which is equivalent to the 0.5 sec. period.

At the end of the remaining 0.25 sec. the bill leaves the acceptor, assuming that it has been deemed valid.

As the bill 12 advances from the position shown in FIG. 2 to the position shown in FIG. 3, the optical and magnetic channels are activated as indicated by the table of FIG. 8. This occurs as the first test area or zone of the bill passes the head 38, such zone being identified in FIG. 7 as the "Grid 1 Test Area." The grid is on both sides of the portrait 100 and constitutes a portrait background which may be advantageously sensed for optical and magnetic properties indicative of genuine printing. If grid 1 is deemed valid, the outputs of the optical amplifier and filter combination 42 and the magnetic amplifier 44 will be of similar wave form and in phase, and of sufficient amplitude to operate the AND gate 46. The output of gate 46 is fed to the coincidence counter 48 which is of the integrating type and requires a minimum of outputs from gate 46 (a specified pulse train) before it will produce the accept signal Ac. Assuming grid 1 to be valid, Ac is fed into AND gate 50 together with the T and B functions. The output from AND gate 50 sets the accept flip-flop memory 72 thereby executing the AM1 function. AM1 via OR gate 94 maintains the transport drive in the forward direction.

T-B occurs when the bill 12 is essentially centered with respect to the head 38 (FIG. 4). This function sets accept memory 70 to produce the AM2 signal. It should be noted that the function T-B constitutes a minimum length test because, in order to set accept memory 70, the bill 12 must not be less than the proper length, the top and bottom light paths in the channel 22 being approximately 6.2 inches apart.

AM2 is fed to the AND gate 52, and it should be noted that AM1 was previously fed to the delay circuit 80. The next event is another accept signal Ac from the coincidence counter 48 as the Grid 2 Test Area passes the head 38. The AND gate 52 requires five concurrent inputs: T, B, Ac, AM1, and AM2. Again assuming that the test area is deemed valid (Ac produced), the output from AND gate 52 sets the accept memory 74 thereby generating the AM3 signal. If the five simultaneous inputs just referred to occur before the delay circuit 80 times out, the reject AND gate 78 is blocked since the 1 logic level from accept memory 74 is removed and G2D is ineffective to trigger the gate.

The bill 12 continues in the forward direction until the bottom light path is cleared, thereby executing the B function and initiating the credit signal Cr at the output of AND gate 76. This also initiates the reset delay via reset OR gate 90 to effect resetting of all of the flip-flop memories and return of the system to standby.

The foregoing operational description has assumed that an invalid condition is not encountered. However, failure to pass any one of the validity tests will cause the bill or counterfeit material to be rejected by one of several logic sequences. When an invalid condition is encountered, the reject OR gate 84 is triggered to produce Rj and effect reversal of the transport drive, thereby returning the bill or counterfeit material to the depositor. Each of the possible invalid conditions will not be described.

If the bottom light path is interrupted and accept memory 72 is not set, the function B-AM1 triggers AND gate 82 to, in turn, trigger the reject OR gate 84.

This condition occurs when grid 1 does not have physical properties indicative of validity, thus Ac was not produced.

If Ac occurs when both the upper and lower light paths are interrupted (T-B), AND gate 68 is triggered to, in turn, activate the reject OR gate 84. This occurs when an accept signal Ac is produced from what should be the center of the portrait, indicating that the locations of the portrait and background grids relative to the length of the bill are in accordance with the arrangement of a genuine bill.

If the top light path is again interrupted after the accept memory 74 is set, AND gate 77 is triggered to, in turn, trigger the reject OR gate 84. This condition would occur, for example, if the bill was closely followed by a second bill inadvertently inserted by the depositor.

If G2D occurs and accept memory 74 has not been set, the function G2D-AM3 activates AND gate 78 to, in turn, trigger the reject OR gate 84. This requires that the output signal from the five-input AND GATE 52 occur by the time the bill reaches a predetermined position in the channel 22. For instance, sensing of grid 2 must not be delayed until after the occurrence of G2D. This function initiates rejection of the bill in the event that accept memory 70 was not previously set, which would occur if the bill failed to pass the length test executed by the T-B function.

Having thus described the invention, what is claimed as new and desired to be secured by Letters Patent is:

1. In a currency testing system:

a transport for receiving a bill inserted therein and for conveying the inserted bill along a predetermined path of travel for testing thereof;

a device disposed to detect the presence of said bill upon said insertion thereof into the transport, said device being operably associated with said transport for rendering the latter operational when the bill is detected by the device, whereby to effect advancement of the bill along said path;

a test station in said path having means for sensing physical properties of the advancing bill as it passes the test station;

testing means coupled with said sensing means and responsive thereto for producing an accept signal if the portion of the bill being sensed has physical properties indicative of validity,

said testing means effecting a first test of said bill and delivering said accept signal if a predetermined test zone on the bill has said physical properties indicative of validity;

a memory coupled with said testing means and responsive to said accept signal from said first test; means responsive to further movement of the bill along said path for effecting a second validity test while the validity indication from the first test is held in said memory, said second test effecting means including a second bill detection device spaced along said path from the first mentioned device and disposed to detect the leading edge of a bill of proper length at the time that said first device is detecting the trailing edge thereof, and means responsive to simultaneous detection of the inserted bill by said first and second devices for delivering a minimum length test signal indicating that the bill is of at least the proper length;

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a second memory responsive to said minimum length test signal; and
 output means coupled with said testing means responsive to physical properties, said devices, and said memories for delivering an output signal if an accept signal is again produced at a second, subsequent test zone and said first device is not detecting the bill, said second device is detecting the bill, and said memories are holding validity indications from their respective tests.
 2. In the system as claimed in claim 1, said transport having a reversible drive; and means coupled with said drive for reversing the latter to reject the inserted bill if no accept signal occurs by the time the bill reaches a predetermined position in said path.
 3. In the system as claimed in claim 1, said transport having a reversible drive; and means coupled with said drive for reversing the latter to reject the inserted bill in response to the concurrent presence of an accept signal and said

minimum length test signal.
 4. In the system as claimed in claim 1, said transport having a reversible drive; and means coupled with said output means and said drive for reversing the latter to reject the inserted bill unless said output signal occurs by the time the bill reaches a predetermined position in said path.
 5. In the system as claimed in claim 1, said transport having a reversible drive; and means coupled with said output means, said first device, and said drive for reversing the latter to reject the inserted bill if the first device detects the presence of the bill or another inserted bill after delivery of said output signal.
 6. In the system as claimed in claim 1, there being means coupled with said output means and said second device for delivering a credit signal indicating that the bill is deemed valid, in response to said output signal and when said second device no longer detects the bill.

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