



(51) International Patent Classification:

H01L 21/768 (2006.01) C23C 16/04 (2006.01)
C23C 14/04 (2006.01)

(21) International Application Number:

PCT/US2019/066919

(22) International Filing Date:

17 December 2019 (17.12.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/235,765 28 December 2018 (28.12.2018) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US 16/235,765 (CON)
Filed on 28 December 2018 (28.12.2018)

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,

HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: METHODS OF FORMING TUNGSTEN STRUCTURES

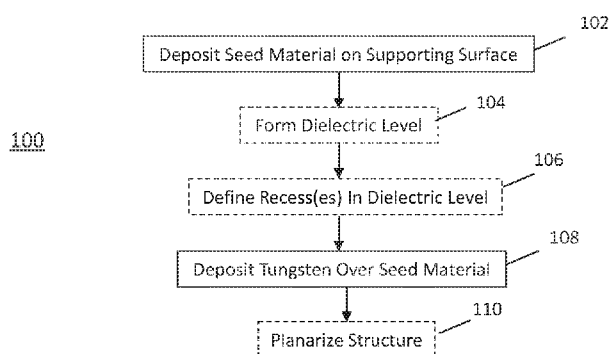


FIG. 1

(57) Abstract: Described are methods for forming a multilayer conductive structure for semiconductor devices. A seed layer is formed comprising a metal and an additional constituent that in combination with the metal inhibits nucleation of a fill layer of the metal formed over the seed layer. Tungsten may be doped or alloyed with silicon to form the seed layer, with a tungsten fill being formed over the seed layer.

METHOD OF FORMING TUNGSTEN STRUCTURES

Priority Application

[0001] This application claims the benefit of priority to U.S. Application Serial Number 16/235,765, filed December 28, 2018, which is incorporated herein by reference.

Technical Field

[0002] Embodiments described herein relate generally to manufacturing of tungsten structures of microelectronic devices, such as tungsten structures on a semiconductor die; and more particularly relate both to methods of forming such tungsten structures during manufacture of such microelectronic devices, for example during processing of semiconductor wafers, and the resulting devices.

Background

[0003] Microelectronic devices permeate every aspect of daily life. A continuous demand exists for miniaturization and reduction of power requirements, but also for increased processing power and speed. With these competing demands, the complexity and density of the underlying circuitry grows, along with the complexity of manufacturing processes to form such circuitry. As the density of structures forming such circuitry increases, with the result of the dimensions of individual conductive structures shrinking, manufacturing conductive structures with acceptable electrical properties becomes increasingly challenging.

[0004] Examples of such microelectronic devices include semiconductor structures (such as semiconductor devices formed on a semiconductor substrate (termed “semiconductor die”)), as well as circuit components and interconnections that may be formed over interposers and/or other non-semiconductor substrates. Semiconductor structures include semiconductor,

dielectric, and conductive elements, all patterned to form circuit components and desired interconnections between the circuit components. The conductive structures are often formed from one or more metals or metal-containing materials. However, the resistance of conventionally formed conductive structures generally increases as the critical dimensions of the conductive structures are reduced, potentially complicating the manufacture of semiconductor structures with necessary electrical properties. As a result, conventionally formed conductive structures may require larger than desired line widths to maintain suitable electrical properties (such as an acceptably low resistance), for operation of the device; or may require use of exotic materials and/or processing methods to form suitable structures.

Brief Description of the Drawings

[0005] FIG. 1 is a block diagram illustrating an example process for manufacturing a substrate (such as, for example, a semiconductor die substrate) having tungsten conductive structures in accordance with the present description.

[0006] FIGS. 2A-2E illustrate simplified cross-sectional representations of a representative portion of an example semiconductor die incorporating tungsten conductive structures during sequential stages of an example processing flow.

Description of Embodiments

[0007] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

[0008] As the critical dimension of conductive structures using conventional materials in semiconductor devices decreases, e.g. reaching 20

nm and below, however, the resistance of the conventionally-formed conductive materials typically increases. In some applications, in which longer conductor lengths are desired, at reduced critical dimensions, the increased resistance may preclude the use of otherwise preferred conductive materials. The increasing resistance thus impacts device design and may cause more exotic materials or processing methods to be used, or new complex device designs to be designed and implemented, to diminish the effects from the reduced dimensions.

[0009] The present disclosure addresses various embodiments for forming conductive structures of tungsten in a manner to offer improved conductivity relative to conventionally formed tungsten structures. In the described example processes, tungsten is deposited through use of a seed material. The seed material includes both tungsten and another material in a composition to facilitate formation of a fill material of desired properties over the seed material. The inventors have identified that a relatively low resistance tungsten structure may be formed if at least a majority portion (50% or more) of the tungsten is in the alpha state (as discussed later herein), and if a majority of the tungsten exhibits large grain size. For example, a desired physical property of the tungsten fill material may be that a majority of the tungsten fill material exhibits a grain size (as determined by a longest dimension the grains), of about 20 nm or greater; and for many examples, a grain size in the range of about 30-50 nm will be desirable. The term “about” herein is meant to include a variance of $\pm 10\%$ to provide for variances of manufacturing processes, measuring techniques, etc.

[0010] As a result, the additional material in the seed material will be selected to inhibit nucleation of subsequently formed tungsten fill material when formed on the seed layer, thereby promoting formation of such relatively large grained tungsten as described above. The nucleation-inhibiting properties need not exist as to such material alone, but need be present in the seed layer when the tungsten fill is formed over the seed layer. In some examples, this additional nucleation-inhibiting material may be present as a dopant of the

metal; while in other examples, the nucleation-inhibiting material may be alloyed with the tungsten. In some embodiments, the composition of the seed material, and the inhibition of nucleation of the tungsten fill material (the fill material forming the bulk of the conductive structure), will also result in a majority of the tungsten fill material being formed of larger grains (e.g., in some examples, within the range of 30-50 nm). For some examples, the tungsten fill material having grains having a longest dimension in excess of 20 nm may form at least about 70% of the tungsten fill material. In other examples, tungsten fill material having grains with a longest dimension in excess of 20 nm may offer beneficial electrical properties if present in only about fifth % of the tungsten fill material.

[0011] For purposes of the present description, the term “seed layer” is used to describe the forming of a structure having both a metal and a nucleation-inhibiting material. The term “seed layer” does not imply any form in which either material is formed (i.e., the materials may be deposited in a form other than what persons skilled in the art might consider a “layer,” and the two constituent materials may be deposited simultaneously, or sequentially; and use of the term “layer” does not imply any degree of uniformity, or of contiguous coverage of an underlying support structure on which is formed). For example, the seed layer may, or may not be deposited as a film (for example having a dimension of 10 nm or less); and may not necessarily cover the entirety of a support surface over which the tungsten fill will be formed.

[0012] In the described examples, the seed layer includes tungsten, with silicon present to inhibit nucleation of a subsequent tungsten fill; and may be formed on a supporting surface of the substrate over which the conductive tungsten structure will be formed. In some examples such seed layer may include silicon present in a range of 4% to 28% by atomic weight.

[0013] As discussed in more detail below, the supporting surface can be of various materials and configurations. One example configuration that may be used is one in which the supporting surface is a surface defining, at least in

part, a recess in a structure. For example, the supporting surface may be defined, at least in part, by a dielectric layer. In some examples, the recess may be a trench through which an elongated conductive line is to be formed.

[0014] One example application in which elongated conductive traces are used is in memory arrays. In memory arrays, conductive lines such as word lines and bit lines typically extend across substantial portions (or all) of the memory array. While tungsten has often been a preferred material for at least some of these lines, use of conventionally deposited tungsten can yield less than optimal electrical characteristics in structures of reduced dimensions; for example, in structures in which the critical dimension of the tungsten structures is 100 nm or less.

[0015] Microelectronic devices can include multiple structures potentially benefiting from relatively low resistance tungsten conductive lines, including structures on a semiconductor die itself, as well as on package substrates, interposers, redistribution layers, etc. For purposes of the present disclosure, the term “substrate” will be used to identify any structure for inclusion in a microelectronic device on which the described tungsten structures will be formed (which may be, for example, a semiconductor wafer, an individual semiconductor die, interposers, etc. (as discussed above); while the term “semiconductor device substrate” is used to specifically identify the structures present at any of the multiple stages of forming a semiconductor die on a semiconductor wafer or on an analogous semiconductor structure. Any or all such structures may benefit from the formation of relatively low resistance tungsten structures therein.

[0016] FIG. 1 depicts a flow chart of an example process for producing a conductive tungsten structure over a substrate. For purposes of the examples herein, the substrate is described in the context of a semiconductor device substrate (for example, a substrate of a semiconductor die). As a result, the substrate semiconductor material (termed herein, a “wafer”) may be, for example, Si, Ge, or a compound semiconductor such as SiC, SiGe, a III-V semiconductor (e.g., GaAs or InP or ternary/quaternary semiconductors), or

other semiconductor materials known to persons skilled in the art). One illustrative embodiment of the various examples above is forming a tungsten structure on a supporting surface of a semiconductor die substrate.

[0017] As indicated at 102, process 100 includes forming a seed layer on a supporting surface. In many examples, the seed layer will include tungsten, and in embodiments discussed herein will further include silicon. Forming the seed layer on the supporting surface may optionally include forming of the supporting surface of a desired configuration and material. For example, process 100 may include optional operations, 104 and 106, (indicated by dashed lines within the flowchart). which may be used in forming the supporting surface in preparation for the seed layer. As indicated at 104, a dielectric level may be formed over, for example, a semiconductor substrate. The term “level” is used herein to identify the presence of a structure which may be a single material, or multiple materials. For example, the dielectric level may be formed of a single dielectric material or of multiple dielectric materials. As indicated at 104, a recess may be formed in the dielectric level. In some embodiments, the recess (for example, a trench or via) will define a path in which the tungsten will be formed. Such recesses may, in some embodiments, be etched from an upper surface of the dielectric level into the dielectric level. The recesses may be formed, in some example implementations, of about 50-200 nm in depth and may be of about 10 nm to 40 nm in width. Other implementations may include recesses, shallower or deeper, and/or narrower or wider. Accordingly, the identified dimensions are examples only.

[0018] As will be discussed further in reference to Figures 2A-2E, in some examples the dielectric level may include first and second vertically disposed (or upper and lower/underlying) dielectric materials. In some such examples, the upper dielectric material (204, 202 in Figures 2A-F) may be, for example, silicon oxide (SiO₂), and the underlying dielectric material (202 in Figures 2A-F) may be different, for example, silicon nitride (SiN). In some examples, the upper dielectric material may have a vertical dimension of about 50-200 nm. In the depicted example, recesses (206 in Figures 2B-F) are formed

through the upper dielectric level, such that upper dielectric defines the sidewalls of the recesses, and lower dielectric defines the bottom surface of the recesses. the recesses may be formed through a photolithographic process as known to persons skilled in the art, which may include depositing a photoresist over the upper dielectric level 204, patterning the photoresist using a mask, removing either the unexposed or exposed portions of the photoresist, etching the exposed portion of the upper dielectric level 204 via wet or dry chemical etching, for example, and removing the remaining photoresist after formation of the recesses by ashing, for example.

[0019] Thus, in embodiments in which the recesses extend within a dielectric material, the dielectric material may include one or more grown or deposited insulative materials. In addition to SiN or SiO₂, mentioned above, the recesses may be formed in other types of nitrides and/or oxides. In the latter case, for example, the recesses may extend into a high-K dielectric, for example a high-K oxide (for example, zirconium or hafnium oxide) rather than, or in addition to, SiO₂.

[0020] In forming the seed layer, as indicated at 102, the seed layer may be formed on one or more dielectric levels (or other material levels) formed above the substrate, and in many examples will be may be formed at least in part in recesses extending through one or more dielectric levels. In other embodiments, the seed layer may be formed in a structure (such as a trench) formed within the semiconductor substrate material itself (and in most such embodiments, lined with a dielectric film to isolate the seed layer and other conductive structures to be formed from the semiconductor substrate material).

[0021] In some examples, the seed layer can be in the form of a thin layer (in some examples, having a thickness of approximately 5-10 nm). As noted previously, the seed layer may be contiguous or non-contiguous over at least some portion of a supporting surface. In some examples, the supporting surface may be a patterned material, for example, either a patterned region of

the substrate, or of another material formed over the substrate (such as to form recesses, as discussed above).

[0022] In some examples, the recesses may be formed in one material, and then lined with another material (for example, through a conformal coating), prior to deposition of the seed layer. For example, a recess may be formed in a first dielectric material, for example a nitride (SiN) or an oxide (SiO), and then lined on one or all surfaces with another dielectric material before forming of the seed layer.

[0023] The seed layer may be deposited via any of the techniques above, for example, plasma vapor deposition (PVD). PVD may desirably be used to form the seed layer in many implementations due to the lower temperature and enhanced controllability of composition and film thickness compared to CVD, which usually operates a high temperature of between about 300 °C and 900 °C, and which would thus increase the complexity of the deposition process for the seed layer. The lower processing temperatures associated with PVD can be beneficial to establishing some percentage of beta phase tungsten in the seed layer, which is believed to be beneficial in inhibiting nucleation of the subsequent tungsten fill material.

[0024] Tungsten, whether in a seed layer or the later-formed tungsten fill, may be at least in part in either alpha or beta phase. Alpha phase tungsten is a cubic crystalline structure that has a space group of Im-3m (body centered Bravais lattice with 3m symmetry elements) and 2 atoms/unit per cell. Beta phase tungsten is a cubic crystalline structure that has a space group of Pm-3n (primitive with 3n symmetry elements) having 8 atoms/unit per cell. Alpha phase tungsten is desirable to use in structures such as those above due to the lower resistance compared to beta phase tungsten. Additionally, relatively larger crystals of alpha phase tungsten exhibit further reduced resistivity.

[0025] The ratio of alpha phase tungsten to beta phase tungsten in the tungsten fill is dependent on the deposition conditions and the underlying layer on which the tungsten is deposited (in the present examples the seed layer). The same considerations also impact avoiding higher resistance amorphous

phase tungsten in the tungsten fill. The inventors have identified that beta phase tungsten in the seed layer inhibits nucleation of a tungsten fill material formed on the seed layer, and in doing so promotes formation of relatively larger crystals of alpha phase tungsten than would be formed in the absence of the beta phase tungsten. Beta phase tungsten is relatively unstable, and creation of a seed layer with operationally significant amounts of beta phase tungsten is assisted by forming the seed layer by a method not requiring high temperatures and/or pressures (such as PVD).

[0026] To establish beta phase tungsten in the seed layer, and to increase the grain size of the later-deposited conductive material on the seed layer, the seed layer may include a doped or alloyed material. For purposes of the description herein, the seed layer will include both tungsten and silicon (Si), in which the silicon may be present either as a dopant or an alloy. Doping, as used herein, is the intentional introduction of impurities into the base material to modulate the properties of the base material. Doping may occur at the time of deposition, or after the tungsten has been deposited.

[0027] In such examples using a seed layer including tungsten and silicon, the tungsten may be a mixture of alpha and beta phase tungsten, ranging from about 10-60% beta phase tungsten by atomic weight, which in many cases will vary in response to the silicon percentage in the seed layer. In some examples, the creation of beta phase tungsten through use of a silicon-doped tungsten seed layer will beneficially include about 4% to about 28% Si by atomic weight. In some implementations, a Si percentage greater than about 28% may cause the seed layer to be at least partially in an amorphous phase, rather than a crystalline phase; and/or may result in the tungsten fill material deposited thereon to be predominantly higher resistance beta phase tungsten and lacking the desired larger grain sizes.

[0028] As noted above, the use of a containing tungsten seed layer also enables the use of room temperature PVD to form the seed layer rather than higher temperature processes such as CVD. The use of PVD also permits the formation of the seed layer directly on an underlying dielectric level, if desired,

without the use of intermediate layers therebetween. In some embodiments, the seed layer may be formed in a trench formed within an oxide layer, wherein an underlying dielectric level forms the bottom of the recess, and may be, for example, a nitride level. In other embodiments, CVD and ALD processing may be used, if desired, to deposit the seed layer.

[0029] Certain dopants/impurities or alloying elements may help to stabilize the beta phase of the material. The structure of the containing tungsten seed layer is less dependent on temperature than a tungsten seed layer. Experiments performed on containing tungsten indicate that at the above doping levels, the tungsten was able to withstand thermal processing of up to about 400 °C (a typical temperature for CVD processes) for up to 30 minutes without substantial alteration of its characteristics (such as would affect the fill material).

[0030] To obtain the desired composition for the PVD process, one or more targets may be used to co-deposit the tungsten and silicon. For example, a pure tungsten target may be used in combination with a pure Si target to deposit the seed layer. In such examples, the deposition from both the pure silicon target and the other target may be controlled to arrive at the desired composition. In other embodiments, a single target, such as composite WSi_x, may be used to result in the desired composition of the seed layer. The composite target may be formed from powdered raw materials and the W/Si ratio may be adjusted by varying the W, Si, and/or WSi₂ powder content.

[0031] In other examples, the seed layer may be formed by PVD of tungsten alone, and subsequently doped with silicon, such as by silicon implantation techniques known to persons skilled in the art. In yet other examples, as noted above, the tungsten and silicon may each be deposited by atomic layer deposition (ALD) to form layers of tungsten and silicon distributed in a desired ratio.

[0032] After deposition of the seed layer at 102, the process may continue by deposition of the tungsten fill layer over the seed layer at operation 108. For example, when recesses are formed, the seed layer is

formed, at least partially in the recesses and the recesses may be filled by the tungsten fill material.

[0033] As identified above, the tungsten fill material may be predominantly (50% or greater, by atomic weight) alpha phase tungsten with grains having a grain size of least about 20 nm, and for many applications within the range of about 30-50 nm) in the recess, and otherwise being constrained by the width of the recesses. For the avoidance of doubt, the grain size referred to herein is the longest dimension (i.e. length) of grains within the tungsten fill material, at least within a selected region. In contrast, the grain size of tungsten fill material deposited over conventional titanium nitride (TiN) seed layer or without the silicon-containing tungsten seed layer is about 6-15 nm.

[0034] The relatively lower resistance of the alpha phase tungsten is enhanced with a larger grain size, as discussed above, as compared with tungsten fill material as would be formed in the absence of the doped or alloyed seed layer. While the silicon-containing tungsten seed layer itself has relatively increased resistance due to its mixed alpha and beta phase composition, this additional resistance is more than compensated for by the lower resistance of the larger grain size, alpha phase tungsten fill, which forms the majority of the conductive structure. The resistance of such tungsten fill material in the recesses is thus relatively low (about 2-4 Ω/sq for about a 20 nm wide deposition that is 65-100 nm in depth) compared with alpha phase tungsten fill typically deposited without the seed layer (>5 Ω/sq for a similar structure) under similar conditions.

[0035] In an example in which the recesses are formed, the deposition of the tungsten over the seed material includes depositing the tungsten within at least some portion of the recesses defined at optional operation 104. In many examples, the recesses may be completely filled with the tungsten fill after deposition of the silicon-containing tungsten seed layer. In some embodiments, the entire surface of the support structure defining the recess may be covered by the silicon-containing tungsten seed layer.

[0036] The silicon-containing tungsten seed layer may be deposited, as above, using a PVD process, while the tungsten fill layer may be deposited by a CVD process. As above, the silicon-containing tungsten seed layer may help to stabilize the tungsten fill during formation to essentially eliminate the formation of beta phase tungsten, which is more favorable to form at higher temperatures in the absence of the silicon-containing tungsten seed layer. CVD deposition may be used for depositing the tungsten fill material rather than PVD for cost and speed reasons, as well as for controllability due to the less stringent process requirements to form the thicker CVD-deposited tungsten fill material than the seed layer. The CVD process used to deposit the tungsten fill material in the recesses (and on the support surfaces in which the recesses are formed) may be run at a temperature of 200-500 °C or more specifically between about 375 °C and 425 °C. The CVD process may use a high-power long-throw plasma of about 4-40 kW for about 10-100 s. The chamber pressure for bulk CVD deposition of tungsten to increase the tungsten grain size may be in a range of about between 0.1 Torr and 300 Torr, or in many examples, between about 30 Torr and 50 Torr.

[0037] The CVD process may comprise a variety of processes such as bulk deposition, diborane (B_2H_6) based nucleation and/or silane (SiH_4) based nucleation for example. The CVD process may include bulk deposition or pulsed nucleation. A diborane (B_2H_6) nucleation cycle for the CVD deposition process includes a diborane (B_2H_6) soak, tungsten fluoride (WF_6) dose followed by [B_2H_6/WF_6] pulses. Such a nucleation cycle may be repeated in a range of 1 to 20 times or between 1 and 4 times. Conditions for a silane (SiH_4) based nucleation cycle for the CVD tungsten process includes a silane (SiH_4) soak, tungsten fluoride (WF_6) dose followed by [SiH_4/WF_6] pulses. This nucleation cycle may be repeated in a range of 1 to 20 times or more particularly between 3 and 5 times. In some embodiments, a diborane or silane nucleation temperature range may be between about 250 °C and 350 °C, with the chamber temperature and pressure ranges mirroring the above.

[0038] After deposition of the tungsten over the seed layer, as discussed relative to 108, optional further processing may occur. For example, as shown at optional operation 110 (again indicated by dashed lines), the resulting structure may be planarized. One manner of planarization may include a chemical-mechanical polishing (CMP) process. Such planarization can be utilized to remove extra tungsten stack materials (such as where such materials extend over a surface of a dielectric, rather than only in recesses within the dielectric); and can also be used to establish a planar surface upon which additional material levels and other structures may be formed.

[0039] As an alternative optional operation, once the tungsten fill has been formed, a portion of the supporting surface may be removed. For example, oxide defining the sides of recesses in which the tungsten fill is formed may be etched to define gaps extending between the formed tungsten lines, as a dielectric region between the formed tungsten conductors. Such gaps may be air gaps, or may have another gas therein.

[0040] In some embodiments, contact may be made to the tungsten fill through vias formed in material levels extending over the tungsten. For example, if one or more other dielectric materials (and perhaps additional metal layers) are fabricated over the structure containing the tungsten conductors, contacts to the tungsten may be formed subsequently through the layers via a photolithographic process similar to that discussed above.

[0041] FIGS. 2A-2E depict simplified, cross-sectional representations of representative portions of a semiconductor die during representative stages of forming a tungsten structure of the semiconductor device. FIGS. 2A-2E depict such stages as may be used in accordance with an example process such as that discussed relative to process operations 102-110 of process 100, wherein tungsten structures are formed within recesses in a dielectric. Such tungsten structures may be formed to serve as conductive structures of a memory device, for example, a memory device wordline, bitline, source line, and/or other interconnect features for the memory device; or, alternatively, for conductive structures of logic or high frequency devices. In FIG. 2A, the

structure 200 may comprise a dielectric level 202. The dielectric level 202 may be formed on a substrate 214 or on other layers above the substrate 214, as indicated above. Structure 200 is represented in the example of a section of a semiconductor die of a memory device, in which the recesses 206, formed in FIG. 2B, may be considered a cross-sectional representation of a trench that will contain a conductive line extending across a substantial portion of a memory array in a memory device. As depicted, not all recesses will have the same dimensions, depending upon length and function of the conductive structures that will be formed therein (and the depictions are not to scale).

[0042] The dielectric level may be formed from a nitride, such as SiN. Another dielectric level 204 may be formed on the underlying dielectric level 202. The top dielectric level 204 may be, for example, an oxide. The oxide layer 204 may be formed from oxide materials such as, aluminum oxide or silicon oxide.

[0043] In FIG. 2B, recesses 206 are etched in the oxide dielectric level 204, terminating at the nitride dielectric level 202. The recesses 206 may be formed by a photolithographic process. In some embodiments, a photoresist may be disposed on the oxide dielectric level 204. A mask may be placed over the photoresist and the photoresist may be patterned by exposing a portion of the photoresist to UV radiation. Either the exposed or unexposed portion of the photoresist may be removed, depending on whether the photoresist is positive or negative. Once the desired portion of the photoresist is removed, the underlying oxide dielectric level 204 may be removed by wet chemical or dry plasma/laser etching. The etching to form the recesses 206 may terminate at the surface of the nitride dielectric level 202. After etching the recesses 206, the remaining photoresist may be removed by ashing.

[0044] FIG. 2B shows the structure after removing the remaining photoresist. In some bitline applications, the recesses 206 may be about 20 nm wide and 50-100 nm in depth (e.g., the thickness of the oxide layer 204), such as about 80 nm in depth.

[0045] In FIG. 2C, a seed layer 208 may be deposited on the structure after formation of the recesses 206. In some embodiments, the seed layer 208 may be in contact with the periphery of the oxide dielectric level 204 and nitride dielectric level 202 in the recesses 206. In some embodiments, the seed layer 208 may have a thickness less than about 10 nm. As noted previously, the seed layer 208 composition may be selected to increase the grain size in a tungsten fill material deposited on the seed layer to inhibit nucleation of the fill in the recesses 206, as discussed above in reference to Figure 1.

[0046] In FIG. 2D, a tungsten fill material 210 may be deposited on the seed layer in the recesses 206. The tungsten fill material 210 may be deposited over the seed layer 208 using CVD. The seed layer 208 may enable a CVD tungsten layer 210 to be formed in which the grain size is increased compared with the grain size if no seed layer 208 had been deposited. The increased grain size may result in a reduction in resistivity, enabling smaller dimensions of conductive structures (e.g., smaller width and/or depth).

[0047] In some embodiments, the seed layer 208 may be the only structure disposed between the oxide dielectric level 208 and the tungsten fill material 210. In other embodiments, one or more intervening layers may be formed between the silicon containing tungsten film and the oxide dielectric level 204. Such intervening layers may comprise a variety of materials such as tungsten nitride or tantalum nitride, or additional other dielectric materials.

[0048] Note that although tungsten is discussed herein, in some embodiments, other metals or alloys may be used instead or in addition to tungsten, and other materials may be used to inhibit nucleation in the fill material. For example, Ge, Sb, C, N, O or S may be used to inhibit nucleation and thereby promote relatively increased grain size in the fill material. The atomic percentage of these materials in tungsten or other metals may vary depending on the metal and/or dopant.

[0049] After the tungsten fill material 210 has been deposited, the structure may be planarized, as shown in FIG. 2E. In some embodiments, both the seed layer 208 and the tungsten fill material 210 may be removed from

locations outside the recesses 206. CMP or another planarization technique may be used to remove the layers. In some embodiments, the resulting conductive structures (recesses filled with the seed layer 208 and the tungsten fill material 210) may be electrically isolated by the oxide dielectric level 204. The resulting structure 200 may be used in assembly of a variety of devices, such as a memory device word line, a bit line, NAND gates and/or other interconnect features for memory logic, or other types of devices. As above, the recesses may extend along a length of the memory device to form the word lines and/or bit lines. In some embodiments, a thin low-k dielectric that results in a low capacitance may be formed between the film and the underlying oxide.

[0050] Although the seed layer has been described as deposited in one or more recesses through a dielectric level, the recess may extend through one or more layers that may include insulating and/or metal layers. Alternatively, the seed layer may be deposited on a dielectric level without recesses and the bulk CVD tungsten deposited on the seed layer to create the large grain bulk tungsten layer.

[0051] To further clarify the described subject matter, the following individual Examples are included.

[0052] Example 1 is a method of forming a multilayer structure, the method comprising: forming a recess in a dielectric level; forming a seed layer comprising tungsten and silicon in the recess; and forming a tungsten fill over the seed layer, wherein a majority of the tungsten of the tungsten fill has grains having a longest dimension of at least 20 nm.

[0053] In Example 2, the subject matter of Example 1 optionally includes 4-28% by atomic weight of the seed layer.

[0054] In Example 3, the subject matter of any one or more of Examples 1–2 wherein tungsten of the seed layer comprises both alpha and beta phase tungsten.

[0055] In Example 4, the subject matter of Example 3 optionally includes 10-60% beta phase tungsten by atomic weight.

[0056] In Example 5, the subject matter of any one or more of Examples 1–4 wherein the seed layer contacts both the dielectric level and the tungsten fill in the recess.

[0057] In Example 6, the subject matter of any one or more of Examples 1–5 wherein forming the seed layer comprises doping the tungsten with silicon to form a silicon-doped tungsten seed layer.

[0058] In Example 7, the subject matter of any one or more of Examples 1–6 wherein forming the seed layer comprises depositing silicon and tungsten simultaneously.

[0059] In Example 8, the subject matter of any one or more of Examples 1–7 wherein the majority of the tungsten in the tungsten fill is alpha phase tungsten and has a grain size having a longest dimension between 30 and 50 nm.

[0060] In Example 9, the subject matter of any one or more of Examples 1–8 optionally include performing high temperature processing after deposition of the silicon-doped tungsten seed layer.

[0061] In Example 10, the subject matter of any one or more of Examples 8–9 wherein forming the seed layer comprises depositing tungsten by physical vapor deposition (PVD).

[0062] In Example 11, the subject matter of any one or more of Examples 9–10 wherein the tungsten fill is deposited by chemical vapor deposition (CVD).

[0063] Example 12 is a multilayer structure, the multilayer structure comprising: a first dielectric level; a second dielectric level disposed on the first dielectric level, the second dielectric level comprising recesses formed therein, at least some of the recesses extending to the first dielectric level; a seed layer comprising tungsten and silicon disposed in the recesses and contacting both the first dielectric and the second dielectric level in the recesses; and a tungsten fill disposed on the seed layer and filling the recesses in which the seed layer is present, the majority of the tungsten in the tungsten fill having grains with a maximum dimension of at least about 30-50 nm.

[0064] In Example 13, the subject matter of Example 12 wherein an amount of the silicon in the seed layer is between about 4-28% by atomic weight.

[0065] In Example 14, the subject matter of Example 13 optionally includes 10-60% beta phase tungsten by atomic weight.

[0066] In Example 15, the subject matter of any one or more of Examples 13–14 includes at least 40% alpha phase tungsten and has a grain size with a maximum dimension between 30 and 50 nm.

[0067] In Example 16, the subject matter of any one or more of Examples 13–15 wherein a resistivity of the seed layer is higher than that of the alpha phase tungsten and a resistivity of a combination of the seed layer and the tungsten fill is less than that of alpha phase tungsten without the silicon-doped tungsten seed layer deposited under similar processing conditions.

[0068] In Example 17, the subject matter of any one or more of Examples 13–16 wherein a resistivity of the tungsten fill material is 2-4 Ω/sq for a recess of about 10-20 nm wide and between 50-100 nm in depth.

[0069] In Example 18, the subject matter of any one or more of Examples 13–17 wherein the first dielectric level is a nitride, the second dielectric level is an oxide, and the recesses terminate at the nitride.

[0070] Example 19 is a memory device, comprising: an oxide level comprising recesses; a silicon-containing tungsten seed layer disposed in the recesses; and a tungsten fill material disposed in the recesses on the silicon-containing tungsten seed layer, an upper surface of the tungsten fill material in the recesses planar with an upper surface of the oxide level outside the recesses, the silicon-containing tungsten seed layer disposed between the tungsten fill material and the oxide level, the majority of the tungsten fill material having a grain size of about 30-50 nm.

[0071] In Example 20, the subject matter of Example 19 wherein the recesses extend along a length of the memory device to form word lines or bit lines of the memory.

[0072] In Example 21, the subject matter of any one or more of Examples 19–20 wherein an amount of the silicon in the silicon-containing tungsten seed layer is between about 4-28% by atomic weight.

[0073] In Example 22, the subject matter of any one or more of Examples 19–21 wherein the silicon-doped tungsten film is formed from a mixture of alpha and beta phase tungsten, the silicon-doped tungsten film containing about 10-60% beta phase tungsten by atomic weight, a majority of the tungsten fill material is alpha phase tungsten, and a resistivity of the tungsten fill material is 2-4 Ω/sq for a recess of about 20 nm wide and between 50-100 nm in depth.

[0074] Example 23 is a method of forming a semiconductor device, comprising: forming a seed layer comprising tungsten and silicon over a support surface of the semiconductor device; and forming a tungsten structure over the doped tungsten-comprising seed layer, the tungsten structure forming a conductive line in which at least 50% of the tungsten is in alpha phase; and wherein at least 50% of the tungsten has a grain size with a maximum dimension of at least about 20 nm.

[0075] In Example 24, the subject matter of Example 23 wherein forming the seed layer comprises doping tungsten with silicon.

[0076] In Example 25, the subject matter of any one or more of Examples 23–24 wherein forming the seed layer comprises depositing an alloy comprising tungsten and silicon.

[0077] In Example 26, the subject matter of Example 25 optionally includes wherein forming the seed layer comprises co-depositing silicon and tungsten by plasma vapor deposition.

[0078] In Example 27, any one or more of the structures of Examples 12-22 may be constructed through use of a method as set forth in any of Examples 1-11 or 23-26.

[0079] In Example 28 any one or more of the structures of Examples 12-22 may be incorporated into memory structures.

[0080] In Example 29 the memory structures of example 28 may be memory devices.

[0081] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as “examples.” Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[0082] In this description, prepositions such as “on,” “over,” and “under” are defined with respect to the conventional plane or surface being on the top or exposed surface of the substrate, regardless of the orientation of the substrate; and while “on” is intended to identify a direct contact of one structure with another structure which it lies “on” (in the absence of an express indication to the contrary); the terms “over” and “under” are expressly intended to identify a relative placement of structures (or layers, features, etc.), which expressly includes--but is not limited to--direct contact between the identified structures unless specifically identified as such. Similarly, the terms “over” and “under” are not limited to horizontal orientations, as a structure may be “over” a referenced structure if it is, at some point in time, an outermost portion of the construction under discussion, even if such structure extends vertically relative to the referenced structure, rather than in a horizontal orientation.

[0083] The terms “wafer” and “substrate” are used herein to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. The

following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the various embodiments is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0084] In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of “at least one” or “one or more.” In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In this document, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

[0085] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description. In the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

Claims

We claim:

1. A method of forming a multilayer structure, the method comprising:
forming a recess in a dielectric level;
forming a seed layer comprising tungsten and silicon in the recess; and
forming a tungsten fill over the seed layer, wherein a majority of the tungsten of the tungsten fill has a grain size having a longest dimension of at least 20 nm.
2. The method of claim 1, wherein an amount of the silicon in the seed layer is between about 4-28% by atomic weight of the seed layer.
3. The method of claim 1, wherein tungsten of the seed layer comprises both alpha and beta phase tungsten.
4. The method of claim 3, wherein the seed layer is about 10-60% beta phase tungsten by atomic weight.
5. The method of claim 1, wherein the seed layer contacts both the dielectric level and the tungsten fill in the recess.
6. The method of claim 1, wherein forming the seed layer comprises doping the tungsten with silicon to form a silicon-doped tungsten seed layer.
7. The method of claim 1, wherein forming the seed layer comprises depositing silicon and tungsten simultaneously.
8. The method of claim 1, wherein the majority of the tungsten in the tungsten fill is alpha phase tungsten and has a grain size between 30 and 50 nm.

9. The method of claim 1, further comprising performing processing to deposit the tungsten fill at temperatures of 300 °C or greater, after deposition of the silicon-containing tungsten seed layer.
10. The method of claim 8, wherein forming the seed layer comprises depositing tungsten by physical vapor deposition (PVD).
11. The method of claim 9, wherein the tungsten fill is deposited by chemical vapor deposition (CVD).
12. The method of claim 1, wherein forming the tungsten fill over the seed layer comprises forming a tungsten structure over the tungsten-comprising seed layer, the tungsten structure forming a conductive line in which at least 50 percent of the tungsten is in alpha phase, and wherein at least 50 percent of the tungsten has a grain size with a maximum dimension of at least about 20 nanometers.
13. The method of claim 12, wherein forming the seed layer comprises doping tungsten with silicon.
14. The method of claim 13, wherein forming the seed layer comprises depositing an alloy comprising tungsten and silicon.
15. The method of claim 12, wherein forming the seed layer comprises co-depositing silicon and tungsten by plasma vapor deposition.
16. A semiconductor device, comprising:
 - a dielectric level comprising recesses;
 - a silicon-containing tungsten seed layer disposed in the recesses; and
 - a tungsten fill material disposed in the recesses on the silicon-containing tungsten seed layer, an upper surface of the tungsten fill material in the recesses planar with an upper surface of the oxide level outside the recesses, the silicon-containing tungsten seed layer disposed between the tungsten fill material and the

oxide level, the majority of the tungsten fill material having a grain size of about 30-50 nm.

17. The semiconductor device of claim 16, wherein the recesses extend along a length of the memory device to form word lines or bit lines of the memory device, the recesses being between about 50-200 nm in depth and about 20 nm in width.
18. The semiconductor device of claim 16, wherein an amount of the silicon in the silicon-containing tungsten seed layer is between about 4-28% by atomic weight.
19. The semiconductor device of claim 16, wherein:
the silicon-containing tungsten film includes a mixture of alpha and beta phase tungsten, the silicon-doped tungsten film containing about 10-60% beta phase tungsten by atomic weight,
a majority of the tungsten fill material is alpha phase tungsten, and
a resistivity of the tungsten fill material is 2-4 Ω/sq for a recess of about 20 nm wide and between 50-100 nm in depth.
20. The semiconductor device of claim 16, wherein the dielectric level comprising recesses, comprises:
a first dielectric material;
a second dielectric material disposed on the first dielectric level, the second dielectric level having recesses formed therein, at least some of the recesses extending to the first dielectric level.
21. The semiconductor device of claim 20, wherein the seed layer comprising tungsten and silicon disposed in the recesses contacts both the first dielectric material and the second dielectric material.

22. The semiconductor device of claim 16, wherein the semiconductor device includes a memory structure, and wherein the tungsten fill material forms a conductive line of the memory structure.
23. The semiconductor device of claim 16, wherein the tungsten fill comprises at least about 40% alpha phase tungsten.
24. The semiconductor device of claim 16, wherein a resistivity of the tungsten fill material is 2-4 Ω/sq for a recess of about 10-20 nm in width and between 50-100 nm in depth.
25. The multilayer structure of claim 20, wherein the first dielectric material is a nitride and the second dielectric level is an oxide, and wherein the recesses terminate at the nitride.

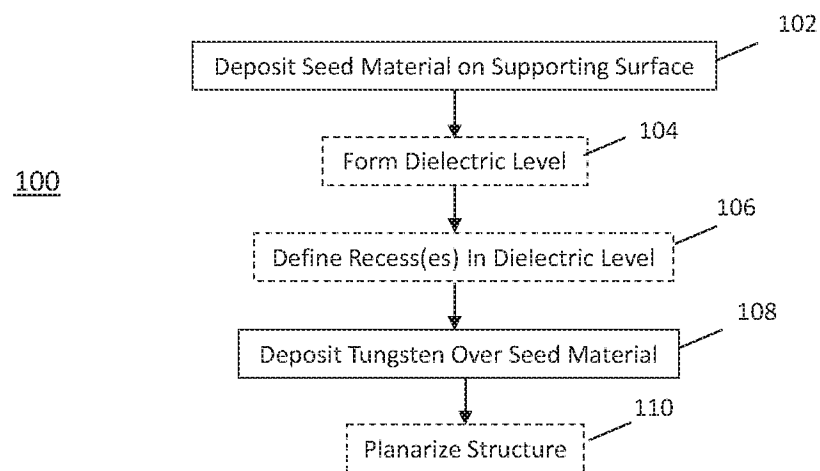


FIG. 1

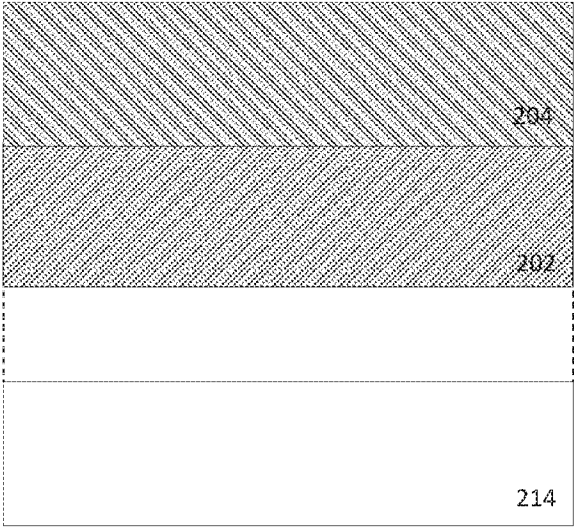


FIG. 2A

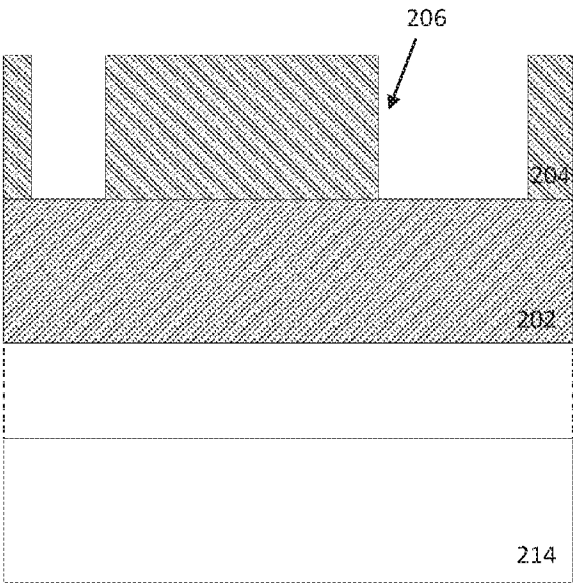


FIG. 2B

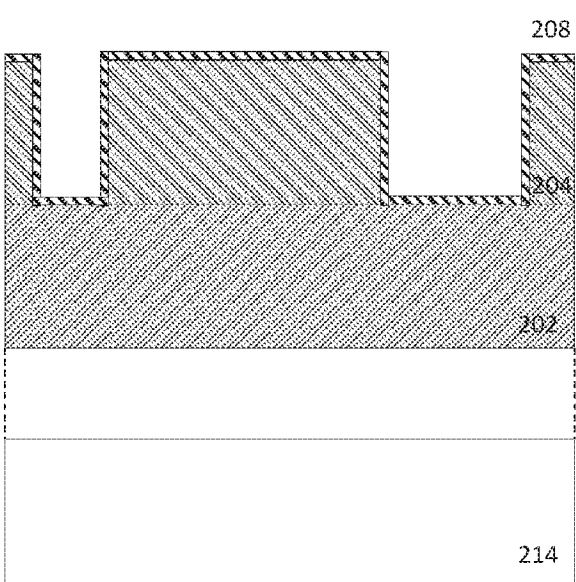


FIG. 2C

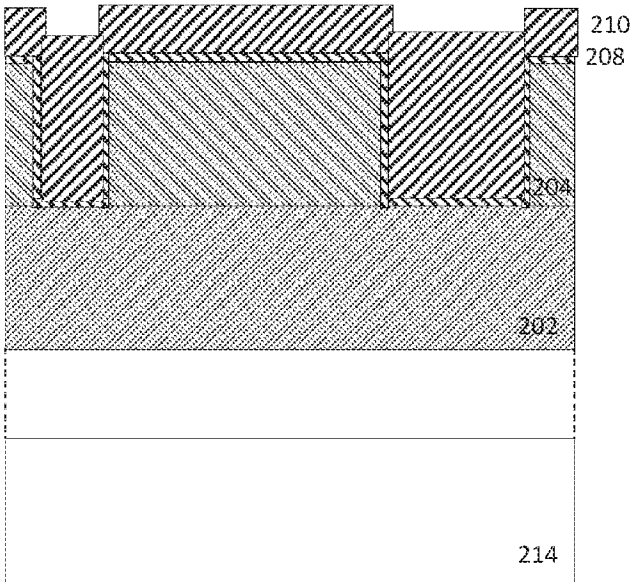


FIG. 2D

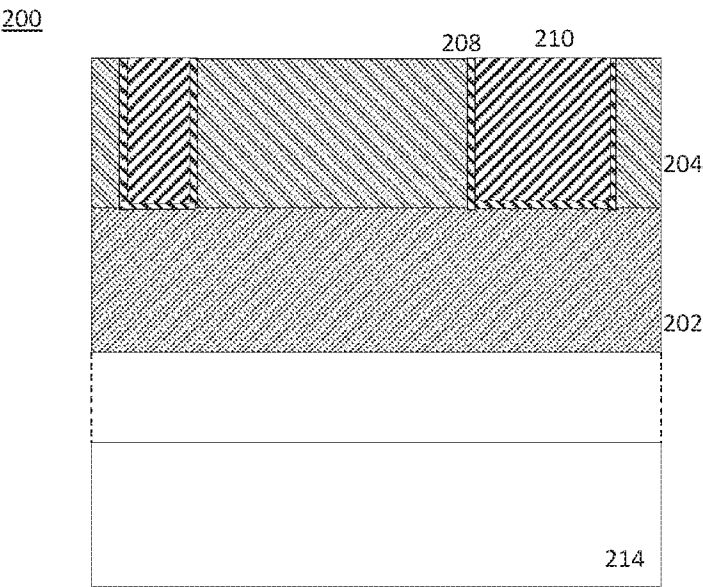


FIG. 2E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/066919**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/768(2006.01)i, C23C 14/04(2006.01)i, C23C 16/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; C23C 14/00; H01L 021/4763; H01L 21/28; H01L 21/285; H01L 2144; H01L 214763; H01L 27/115; C23C 14/04; C23C 16/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: tungsten fill, grain size, doping seed layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002-0048938 A1 (HOTAHA ISHIZUKA et al.) 25 April 2002 paragraphs [0049]-[0057] and figures 2A-2D	1-8, 12-25
Y		9-11
Y	EP 1094504 A2 (APPLIED MATERIALS, INC.) 25 April 2001 paragraphs [0011]-[0015]	9-11
A	US 6579788 B1 (CLIVE MARTIN JONES et al.) 17 June 2003 claim 1 and figures 4A-4D	1-25
A	KR 10-0705936 B1 (HYNIX SEMICONDUCTOR INC.) 13 April 2007 claims 1-9 and figures 1a-1d	1-25
A	WO 2016-085572 A1 (SANDISK TECHNOLOGIES, INC.) 02 June 2016 paragraphs [0090]-[0091]	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 April 2020 (22.04.2020)

Date of mailing of the international search report

22 April 2020 (22.04.2020)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/066919

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