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(54) **Title**: START-UP SUPPLY

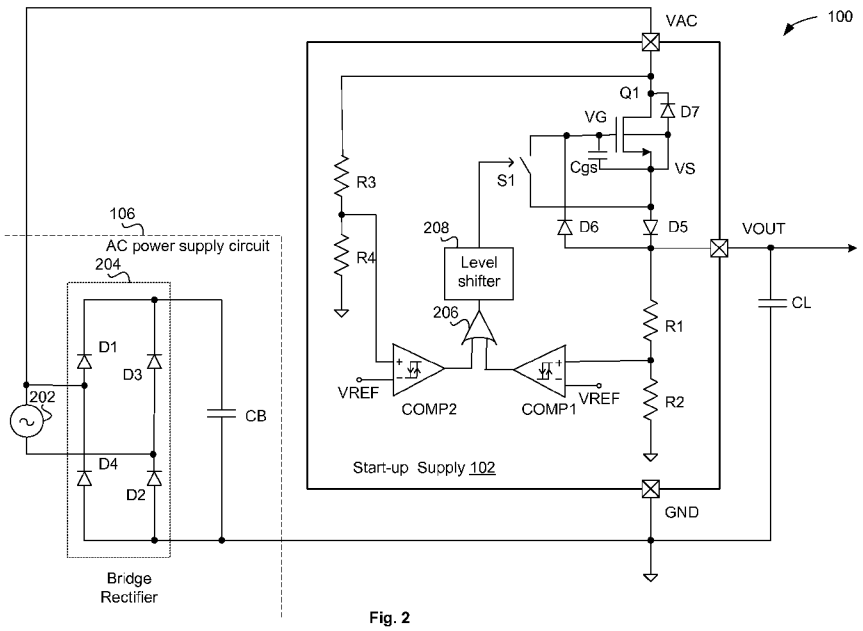

Fig. 2

(57) **Abstract**: In one embodiment, an apparatus includes a transistor having a gate, a drain, and a source. The drain is coupled to receive an AC power supply signal. A component is coupled between an output node and the gate of the transistor. The component couples an output voltage from the output node to charge a gate-source capacitor during a first portion of the AC power supply signal. The transistor is configured to turn on during a second portion of the AC power supply signal to send a charge to the output node where the charge is used to power a circuit of a power supply.

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Start-Up Supply

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure claims priority to U.S. Provisional App. No. 61/289,897 for "High-Input Voltage SMPS Start-Up Supply" filed December 23, 2009, which is incorporated herein by reference in its entirety for all purposes.

BACKGROUND

[0002] Particular embodiments generally relate to power supplies.

[0003] Unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

[0004] A switched mode power supply (SMPS) regulates an input voltage to provide an output voltage. A power factor correction (PFC) controller is used in the conversion and regulation. The PFC controller typically requires a minimumsupply voltage to operate. During operation, the output voltage of the SMPS is used to supply the required operating voltage for the PFC controller. However, at certain times, such as during the SMPS power-up or when a device is in a standby mode (e.g., the output voltage of the SMPS is down), an input voltage is needed for a PFC controller.

[0005] A start-up supply may be used to supply the operating voltage for the PFC controller during the start-up and when the device is in the standby mode. The operating voltage is supplied until the SMPS powers up. After the SMPS powers up, the start-up supply is then deactivated until needed again.

SUMMARY

[0006] In one embodiment, an apparatus includes a transistor having a gate, a drain, and a source. The drain is coupled to receive an alternating current (AC) power supply signal. A component is coupled between an output node and the gate of the transistor. The component couples an output voltage from the output node to charge a gate-source capacitor during a first portion of the AC power supply signal. The transistor is configured to turn on during a

second portion of the AC supply signal to send a charge to the output node where the charge is used to power a circuit of a power supply.

[0007] In one embodiment, the component includes a first component and the apparatus further includes a second component coupled to the source of the transistor and the output node. The second component causes the source of the transistor to follow the AC power supply signal until the transistor turns on.

[0008] In one embodiment, a switch is configured to be controlled to discharge the gate-source capacitor.

[0009] In one embodiment, a system includes a capacitor configured to be charged when the transistor is turned on.

[0010] In one embodiment, a method includes: coupling an AC power supply signal to a transistor; coupling an output voltage from an output node to a gate of the transistor to charge a gate-source capacitor; and turning the transistor on to send a charge to the output node, the charge being used to power a circuit of a power supply.

[0011] The following detailed description and accompanying drawings provide a more detailed understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 depicts an example of a switched mode power supply (SMPS) according to one embodiment.

[0013] Fig. 2 depicts a more detailed example of the start-up supply according to one embodiment.

[0014] Fig 3 depicts waveforms of the start-up supply according to one embodiment.

[0015] Fig. 4 depicts an example of a start-up supply to provide a path for charging gate-source capacitor Cgs from the AC power supply according to one embodiment.

[0016] Fig. 5 depicts a simplified flow chart of a method for operating start-up supply according to one embodiment.

[0017] Fig. 6 depicts a simplified flowchart of a method for providing start-up assistance according to one embodiment.

DETAILED DESCRIPTION

[0018] Described herein are techniques for a start-up supply. In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to provide a thorough understanding of embodiments of the present invention. Particular embodiments as defined by the claims may include some or all of the features in these examples alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

[0019] Fig. 1 depicts an example of a switched mode power supply (SMPS) 100 according to one embodiment. A start-up supply 102, a power factor correction controller 104, and an alternating current (AC) power supply circuit 106 are provided. Although a switched mode power supply is discussed, particular embodiments may be used with other power supply configurations that require start-up supply 102.

[0020] AC power supply circuit 106 provides an AC signal to a node VAC of start-up supply 102. As will be described in more detail below, a half-rectified signal may be provided to node VAC.

[0021] Start-up supply 102 is configured to receive the AC power supply signal and provide an output signal at a node VOUT to charge a capacitor CL. Capacitor CL is charged to supply a sufficient voltage to PFC controller 104 during times when SMPS 100 is not supplying a sufficient auxiliary voltage. The auxiliary voltage may be from the output voltage of SMPS 100, which is different than the output voltage Vout of start-up supply 102. The auxiliary voltage of SMPS 100 may be the voltage that is being supplied to a computing device being powered by SMPS 100. The output voltage from start-up supply 102 and the auxiliary voltage may be a direct current (DC) voltage.

[0022] Start-up supply 102 may supply the necessary charge to capacitor CL, which provides the charge to PFC controller 104. The charge may be supplied during power-up of the computing device and also when the computing device is in a standby mode. When the computing device is starting up or in standby mode, the auxiliary voltage is down.

[0023] When SMPS 100 has started up and is providing a sufficient auxiliary voltage, the auxiliary voltage can be used to provide power to PFC controller 104. At this point, start-up supply 102 may not be needed. Thus, start-up supply 102 may be turned off (e.g., a transistor

(not shown) in start-up supply 102 is turned off) such that start-up supply 102 is not supplying charge to capacitor CL. This state continues until start-up supply 102 is needed again, such as when the computing device is powered down and restarted, or when the computing device is in the standby mode and is restarted.

[0024] Start-up supply 102 may be included on an integrated circuit (IC) chip that includes three pins, a pin for node VAC, a pin for node VOUT, and a pin for ground (GND). By using only three pins, pin count is limited for the chip. Also, as will be described in more detail below, a voltage from node VOUT is used to provide a necessary voltage to charge a gate-source capacitor of a transistor (not shown) in start-up supply 102.

[0025] Fig. 2 depicts a more detailed example of the start-up supply 102 according to one embodiment. AC power supply circuit 106 includes an AC power source 202 and a bridge rectifier 204. AC power source 202 may provide an AC signal, such as a 220 volt root mean square (RMS) signal. Bridge rectifier 204 includes diodes D1, D2, D3, and D4. Bridge rectifier 204 may be a half wave rectifier, which takes the AC supply signal and blocks the negative half of the AC supply signal. In this case, the positive half of the AC supply signal is provided to node VAC of start-up supply 102.

[0026] A transistor Q1 receives the rectified AC power supply signal from node VAC and provides an output voltage at node VOUT. Transistor Q1 has its drain coupled to node VAC. Also, the body of transistor Q1 is coupled to a source of transistor Q1 and a diode D7 is coupled through the body to the drain of transistor Q1. A gate-source capacitor Cgs is shown to represent the capacitance between the gate and source of transistor Q1.

[0027] A diode D5 couples the source to the output node VOUT. Also, the output node VOUT is coupled to the gate of transistor Q1 through a diode D6. Particular embodiments use the output voltage VOUT to charge gate-source capacitor Cgs to a necessary drive voltage during at least a portion of the AC power supply signal. For example, as will be discussed in more detail below, the gate-source capacitor Cgs is charged while the AC power supply signal is negative. This allows transistor Q1 to turn on during a phase when conduction is permitted, but before the AC voltage becomes sufficient enough to start charging capacitor CL. The turn on time is determined by a conduction angle, which is the portion of a cycle of the AC power supply signal during which the transistor Q1 conducts.

[0028] The operation of start-up supply 102 will be described with respect to Fig. 2 and Fig. 3. Fig 3 depicts waveforms of SMPS 100 according to one embodiment. A graph 302

shows the AC power supply signal, a graph 304 shows the rectified AC power supply signal, a graph 306 shows the voltage at the source of transistor Q1, and a graph 308 shows the voltage at the gate of transistor Q1.

[0029] During the negative half cycle of the AC supply signal, the drain of transistor Q1 is held at a potential below ground (e.g., by a diode drop via diode D7) for a part or the entire period based on the load on capacitor CB on bridge rectifier 204.

[0030] When the voltage at node VAC is zero, gate-source capacitor Cgs is charged to the output voltage through diode D6. For example, the output voltage turns diode D6 on and capacitor Cgs is charged. A charging point is shown at 310 where the AC supply signal is negative.

[0031] When the positive cycle of AC supply signal starts, the VAC voltage at node VAC increases above zero. The source of Q1 (node VS) also follows the VAC voltage at node VAC due to having diode D5 in place. For example, diode D5 may be reverse biased until the source of transistor Q1 is sufficient to forward bias diode D5. The source of transistor Q1 follows the VAC voltage until the voltage VS becomes equal to a voltage VOUT (the diode drop across diode D5 is ignored for discussion purposes) when transistor Q1 starts conducting to charge capacitor CL. The voltage across gate-source capacitor Cgs does not change when the source of transistor Q1 moves above zero because there is no path from the gate of transistor Q1 to discharge gate-source capacitor Cgs. Accordingly, the voltage at the gate of transistor Q1 continues to provide sufficient drive to have transistor Q1 conducting.

[0032] Transistor Q1 conducts for a certain phase (according to the conduction angle) of the AC power supply signal. When the conduction angle ends, transistor Q1 is turned off to stop charging capacitor CL. The conduction angle is used to increase efficiency. For example, the efficiency is greater when the VAC voltage is smaller. Accordingly, as shown in Fig. 3, capacitor Cgs is discharged and transistor Q1 is turned off when the conduction angle is reached. At this point, capacitor CL is not being charged by start-up supply 102. Switch S1 may be closed to provide a path to discharge gate-source capacitor Cgs. The discharge of gate-source capacitor Cgs will be described in more detail below. By having transistor Q1 be OFF for the remaining portion of the AC power supply signal cycle after charging the output voltage VOUT adequately, higher power efficiency is achieved for the charging process.

[0033] The above process continues when the AC power supply signal goes negative and gate-source capacitor Cgs is charged. Then, transistor Q1 is turned on to charge capacitor CL when voltage VS becomes equal to a voltage VOUT.

[0034] As discussed above, the charge across capacitor CL is used to supply a voltage to PFC controller 104. The above process continues until SMPS 100 is powered up and a sufficient auxiliary voltage being output by SMPS 100 can be supplied to PFC controller 104. The auxiliary voltage may then be used to charge capacitor CL. At this point, transistor Q1 is turned off until it is needed again to provide a start-up charge. Another important part is that the

[0035] Referring back to Fig. 2, output regulation and conduction angle regulation will be described in more detail. Output voltage regulation may be provided by a resistor R1, a resistor R2, and a comparator COMP1. Also, conduction angle regulation may be provided by a resistor R3, a resistor R4, and a comparator COMP2.

[0036] Output regulation is used to determine when to control switch S1 to turn off transistor Q1. At this point, SMPS 100 may be able to provide the auxiliary voltage to power PFC controller 104. In one embodiment, when a voltage input into the positive terminal of comparator COMP1 reaches a certain level as compared to a voltage reference VREF, switch S1 is controlled to be closed. In this case, gate-source capacitor Cgs cannot be charged to allow transistor Q1 to conduct. For example, when starting up, voltage VOUT may be below a voltage that causes the input into comparator COMP1 to be below the voltage reference VREF (via resistor divider of resistors R1 and R2). When SMPS 100 can supply the auxiliary voltage, voltage VOUT goes above a level where the input into comparator COMP1 goes above the voltage reference VREF. Comparator COMP1 then outputs a logic high signal. Logic gate (e.g., Or gate) 206 outputs a logic high signal to a level shifter 208. Level shifter 208 may be used to shift the voltage level to a level that may turn on a transistor (not shown) acting as the switch to close switch S1.

[0037] In conduction angle regulation, when a voltage input into the positive terminal of comparator COMP2 reaches a certain level compared with voltage reference VREF, switch S1 is controlled to discharge capacitor Cgs. For example, when the VAC voltage reaches a certain level, switch S1 is closed to discharge gate-source capacitor Cgs according to the conduction angle. The VAC voltage is divided by a resistor divider network of resistor R3 and resistor R4. When the input signal from the resistor divider network into comparator

COMP2 goes above reference voltage VREF, comparator COMP2 outputs a logic high signal. Logic gate 206 outputs a logic high signal to level shifter 208. In one example, the output from comparator COMP2 may be a logic low level at this point (e.g., because the voltage VOUT is lower then reference voltage VREF because voltage VOUT has not reached the desired level during start up). Level shifter 208 shifts the voltage level to a level that may turn on the transistor (not shown) to close switch S1.

[0038] When the VAC voltage goes below a certain level, the signal input into comparator COMP1 goes below reference voltage VREF. Comparator COMP2 then outputs a logic low level, which turns off the transistor (not shown) and opens switch S1. The above process continues as switch S1 is closed and opened according to the conduction angle.

[0039] At certain times, such as before power-up of SMPS 100, capacitor CL is relaxed or does not include a charge across it. Thus, the output voltage VOUT cannot be used to charge gate-source capacitor Cgs. Accordingly, start-up assistance is used to charge gate-source capacitor Cgs. Fig. 4 depicts an example of start-up supply 102 to provide a path for charging gate-source capacitor Cgs according to one embodiment. The VAC voltage is used to charge gate-source capacitor Cgs. Resistor R3 of Fig. 2 may be modified into resistors R3a, R3b, and R3c. This provides a path for charging gate-source capacitor Cgs from node VAC. For example, a path is provided through a resistor R3c and a diode D8 to charge gate-source capacitor Cgs.

[0040] Once capacitor CL is charged fully for the first time, this path is not needed. Rather, as was described above, output voltage VOUT is used to charge gate-source capacitor Cgs. Thus, a switch S2 is used to de-couple the path to charge gate-source capacitor Cgs. For example, when a voltage VOUT reaches a certain level, the output of comparator COMP1 goes high and a latch 402 is used to control switch S2. For example, switch S2 is closed to couple resistor R3c to ground. At this point, resistors R3a, R3b, R3c, and R4 together determine the conduction angle. Also, diode D8 prevents charge from flowing from the output voltage through resistor R3c.

[0041] Fig. 5 depicts a simplified flow chart 500 of a method for operating start-up supply 102 according to one embodiment. At 502, the output voltage from node VOUT is coupled to the gate of transistor Q1 to charge gate-source capacitor Cgs. At 504, transistor Q1 is turned on to charge capacitor CL. At 506, when the end of the conduction angle is reached, gate-source capacitor Cgs is discharged.

[0042] Fig. 6 depicts a simplified flowchart 600 of a method for providing start-up assistance according to one embodiment. At 602, the VAC voltage is coupled to the gate of transistor Q1. At 604, gate-source capacitor Cgs is charged by the VAC voltage. At 606, switch S2 is closed when capacitor CL is charged fully for the first time.

[0043] Accordingly, particular embodiments provide a start-up supply that avoids a higher power dissipation because a second rectified signal that is off-chip is not used to charge gate-source capacitor Cgs. Rather, the output voltage VOUT is used to charge gate-source capacitor Cgs. This avoids the use of an extra resistor that is coupled between the gate of transistor Q1 and a pin that would be needed to couple the second rectified signal to charge gate-source capacitor Cgs. Also, this lowers the power dissipation and the pin count of the IC chip. Further, diode D5 is placed on-chip which reduces the bill of materials (BOM) that is needed to produce SMPS 100.

[0044] As used in the description herein and throughout the claims that follow, "a", "an", and "the" includes plural references unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0045] The above description illustrates various embodiments of the present invention along with examples of how aspects of the present invention may be implemented. The above examples and embodiments should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the present invention as defined by the following claims. Based on the above disclosure and the following claims, other arrangements, embodiments, implementations and equivalents may be employed without departing from the scope of the invention as defined by the claims.

WHAT IS CLAIMED IS:

1. An apparatus comprising:

a transistor having a gate, a drain, and a source, wherein the drain is coupled to receive an alternating current (AC) power supply signal; and

a component coupled between an output node and the gate of the transistor, wherein the component couples an output voltage from the output node to charge a gate-source capacitor during a first portion of the AC power supply signal,

wherein the transistor is configured to turn on during a second portion of the AC power supply signal to send a charge to the output node, the charge used to power a circuit of a power supply.

2. The apparatus of claim 1, wherein the component comprises a first component, the apparatus further comprising a second component coupled to the source of the transistor and the output node, wherein the second component causes the source of the transistor to follow the AC power supply signal until the transistor turns on.

3. The apparatus of claim 2, wherein the first component comprises a first diode and the second component comprises a second diode.

4. The apparatus of claim 1, wherein the transistor is configured to turn off for a third portion of the AC power supply signal.

5. The apparatus of claim 4, wherein:

the second portion comprises a first time period when the gate-source capacitor is charged; and

the third portion comprises a second time period when the gate-source capacitor is discharged.

6. The apparatus of claim 1, further comprising a switch configured to be controlled to discharge the gate-source capacitor.

7. The apparatus of claim 6, further comprising a conduction angle circuit configured to control the switch to discharge the gate-source capacitor when the AC power supply signal reaches a threshold.

8. The apparatus of claim 6, further comprising an output regulation circuit configured to control the switch to keep the gate-source capacitor discharged when the output voltage reaches a threshold.

9. The apparatus of claim 1, wherein the circuit comprises a first circuit, the apparatus further comprising a second circuit configured to charge the gate-source capacitor, the second circuit coupling the AC power supply signal to the gate of the transistor.

10. The apparatus of claim 9, wherein the second circuit couples the AC power supply signal to the gate of the transistor when an external capacitor coupled to the output node does not have a charge across the external capacitor until the output voltage reaches a threshold.

11. The apparatus of claim 9, wherein the second circuit comprises:
a resistor coupled to the AC power supply signal; and
a second switch; and
a second switch control circuit configured to control the second switch to couple the resistor to ground.

12. The apparatus of claim 1, wherein the apparatus comprises three pins, wherein the three pins comprise:
a first pin coupled to the AC power supply signal;
a second pin coupled to the output node; and
a third pin coupled to ground.

13. A system comprising the apparatus of claim 1, the system comprising:
a capacitor configured to be charged when the transistor is turned on.

14. The system of claim 13, wherein:
the circuit comprises a power factor correction circuit configured to use an auxiliary output voltage from the power supply to provide a charge to the capacitor, and
the transistor is configured to not provide the charge to the output node when the auxiliary output voltage is at a level to provide the charge to the capacitor.

15. A method comprising:
coupling an AC power supply signal to a transistor;

coupling an output voltage from an output node to a gate of the transistor to charge a gate-source capacitor; and

turning the transistor on to send a charge to the output node, the charge used to power a circuit of a power supply.

16. The method of claim 15, further comprising discharging the gate-source capacitor when the AC power supply signal reaches a threshold.

17. The method of claim 15, turning off the transistor when the output voltage reaches a threshold.

18. The method of claim 15, further comprising coupling the AC power supply signal to the gate of the transistor to charge the gate-source capacitor.

19. The method of claim 18, wherein the AC power supply signal is coupled to the gate of the transistor when an external capacitor coupled to the output node does not have a charge across the external capacitor until the output voltage reaches a threshold.

20. The method of claim 15, wherein:

the circuit comprises a power factor correction circuit, and

the charge is provided to the output node to charge a capacitor, the capacitor configured to provide a charge to the power factor correction circuit.

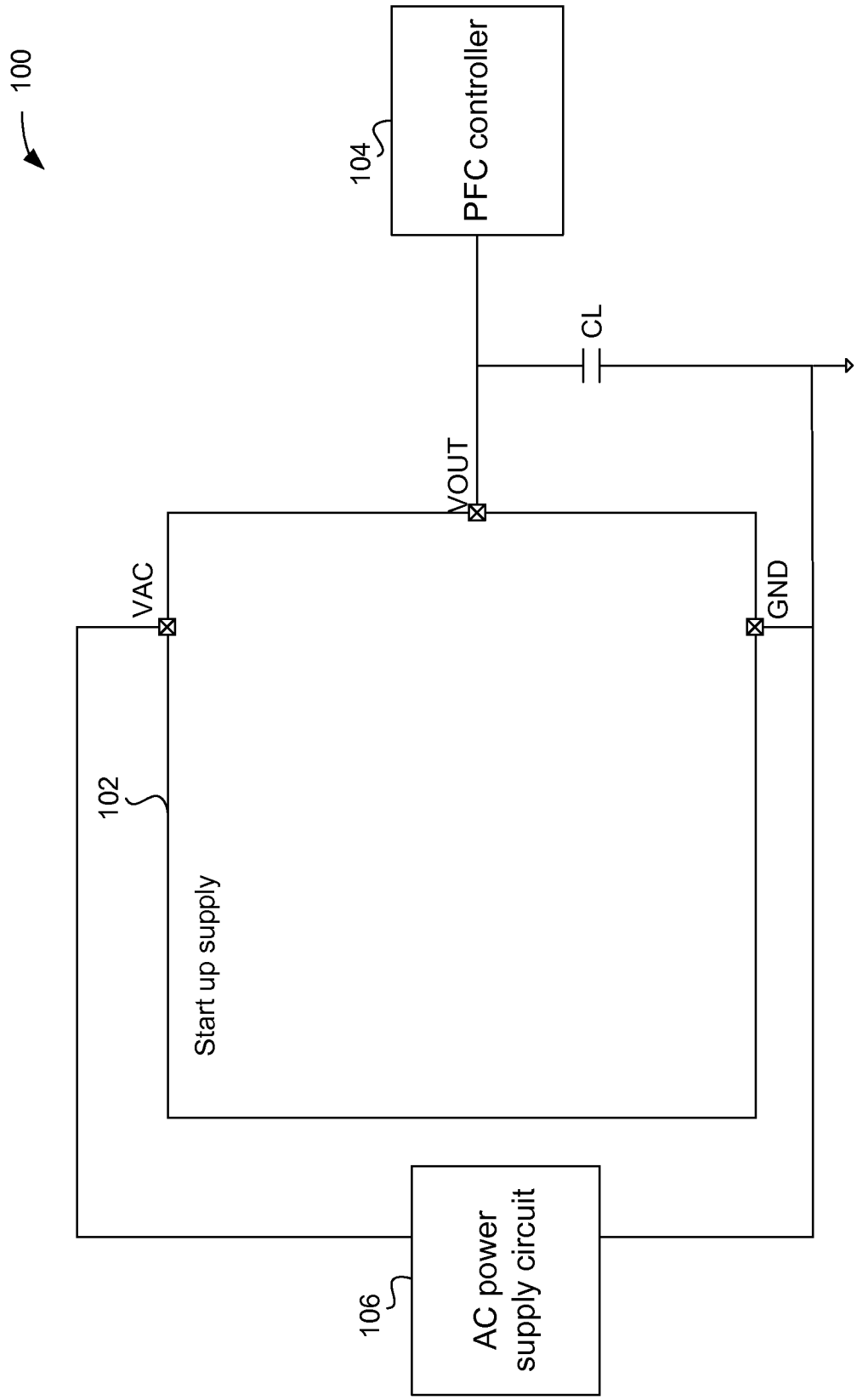
100
PFC controller
104
CL
VOUT
VAC
GND
102
Start up supply
AC power supply circuit
106

Fig. 1

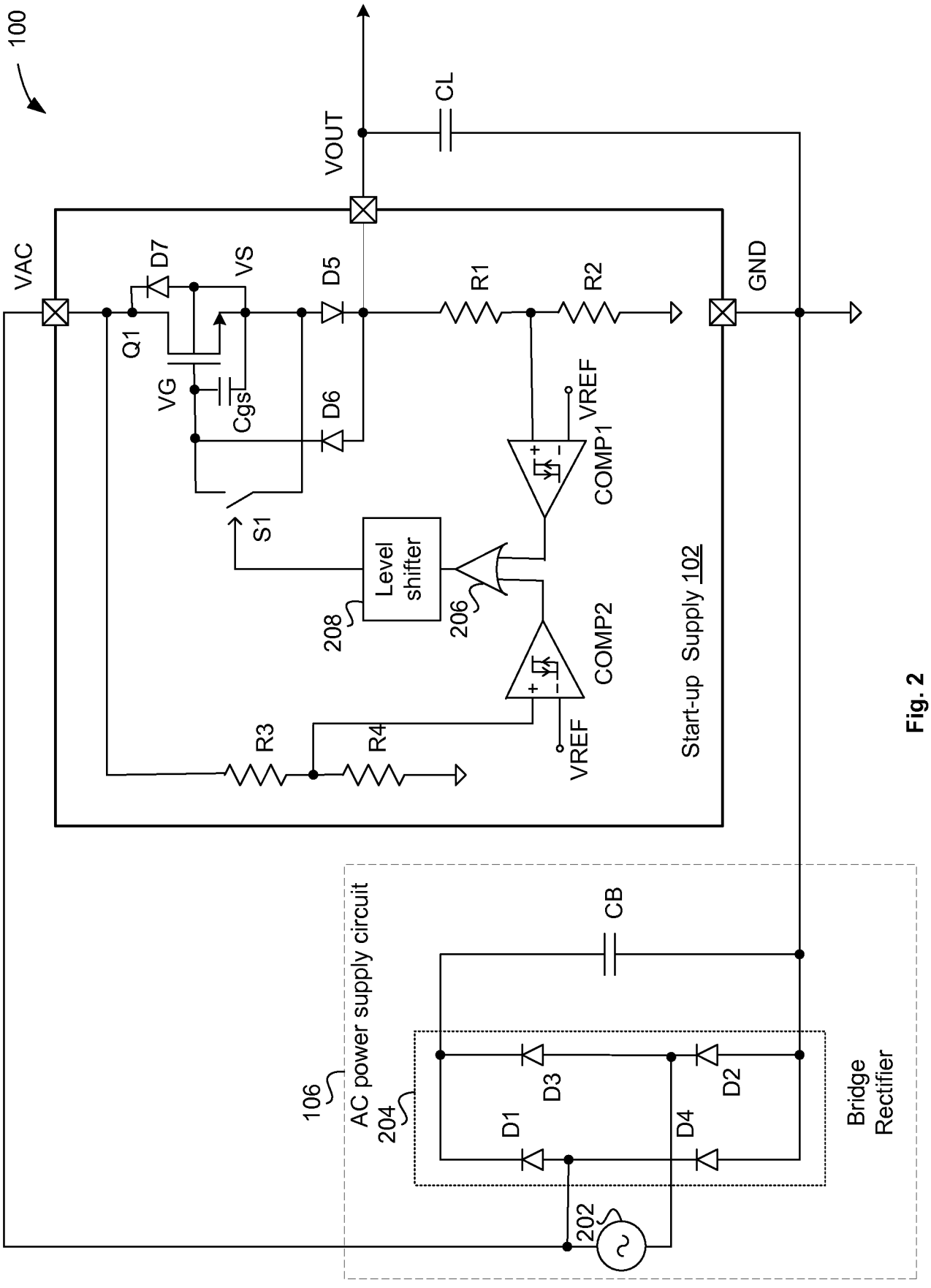
100
VOUT
CL
VAC
D7
VS
D5
R1
R2
GND
Q1
VG
Cgs
D6
VREF
COMP1
S1
Level shifter
208
206
COMP2
Start-up Supply 102
R3
R4
VREF
CB
106
AC power supply circuit
204
D1
D3
D2
D4
Bridge Rectifier
202

Fig. 2

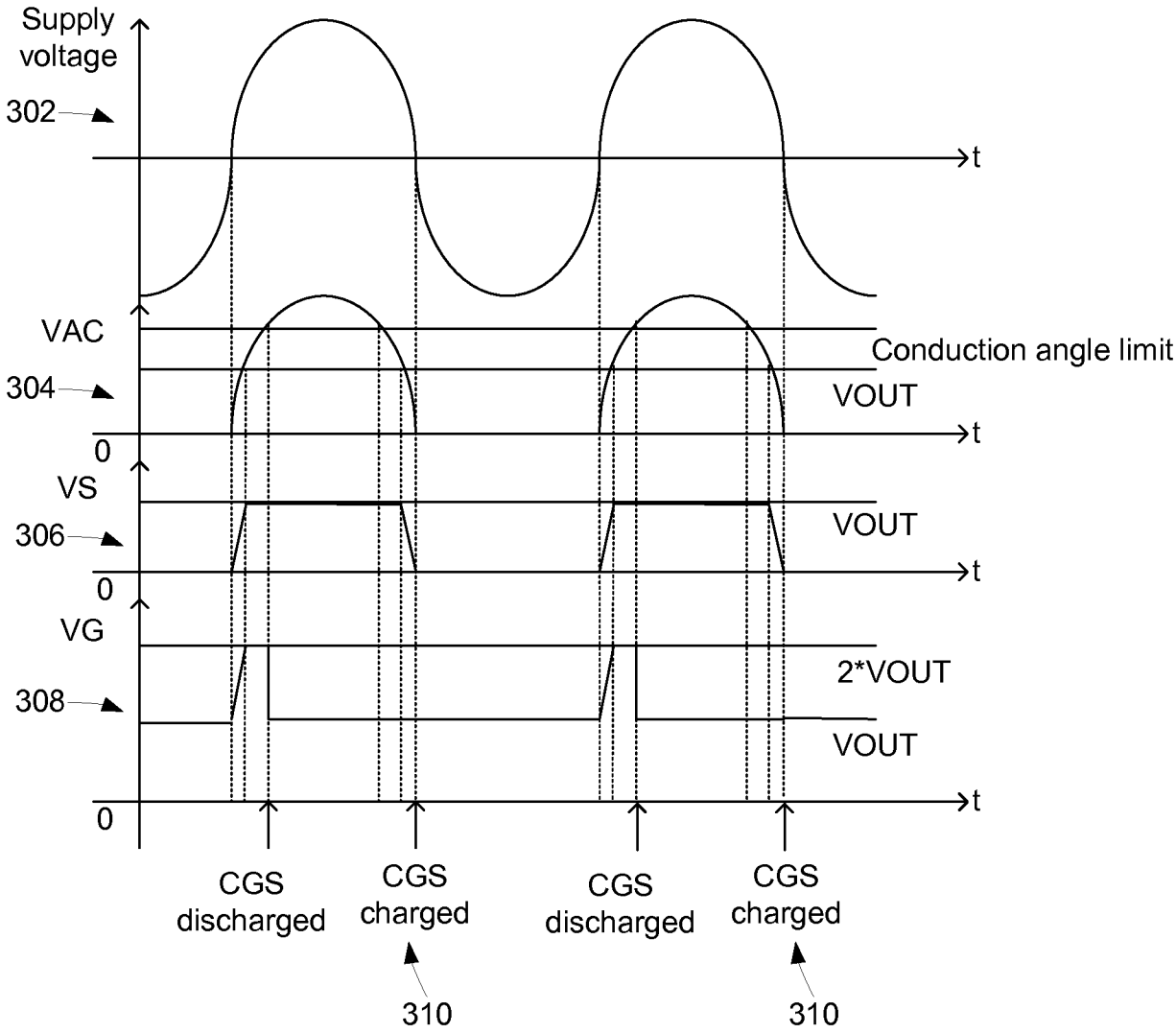
Supply voltage
302
t
VAC
304
Conduction angle limit
VOUT
0
t
VS
306
VOUT
0
t
VG
308
2*VOUT
VOUT
0
t
CGS discharged
CGS charged
CGS discharged
CGS charged
310
310

Fig. 3

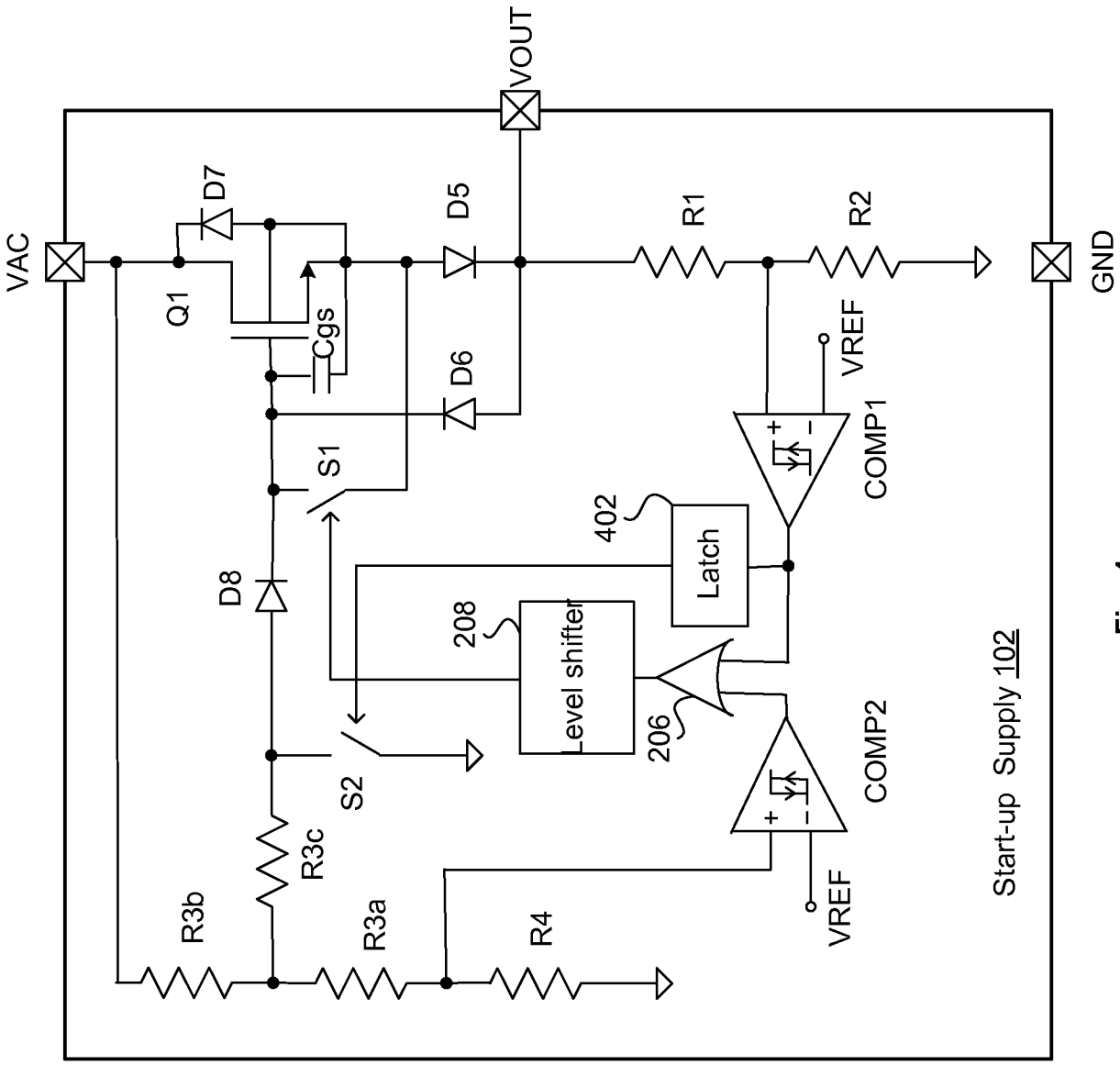
VOUT
VAC
GND
D7
D5
R1
R2
Q1
Cgs
D6
VREF
COMP1
S1
402
Latch
D8
208
Level shifter
206
COMP2
S2
R3c
R3b
R3a
R4
VREF
Start-up Supply 102

Fig. 4

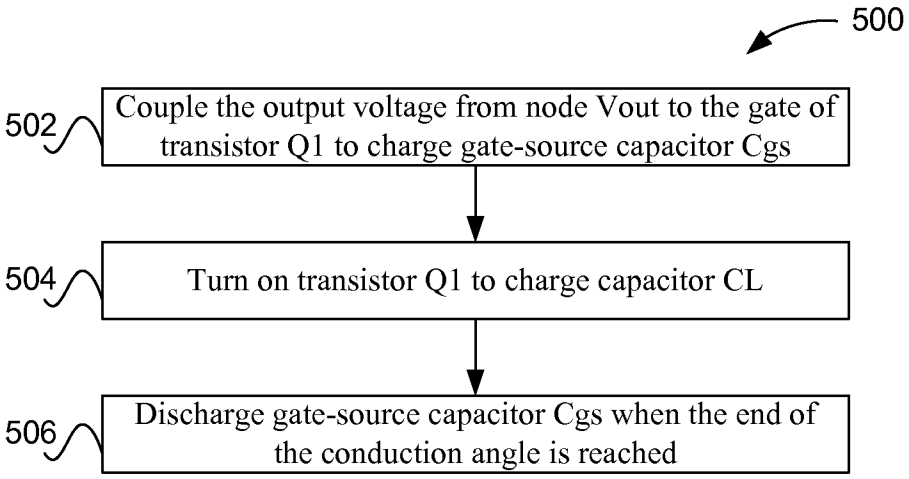
500
502
Couple the output voltage from node Vout to the gate of transistor Q1 to charge gate-source capacitor Cgs
504
Turn on transistor Q1 to charge capacitor CL
506
Discharge gate-source capacitor Cgs when the end of the conduction angle is reached

Fig. 5

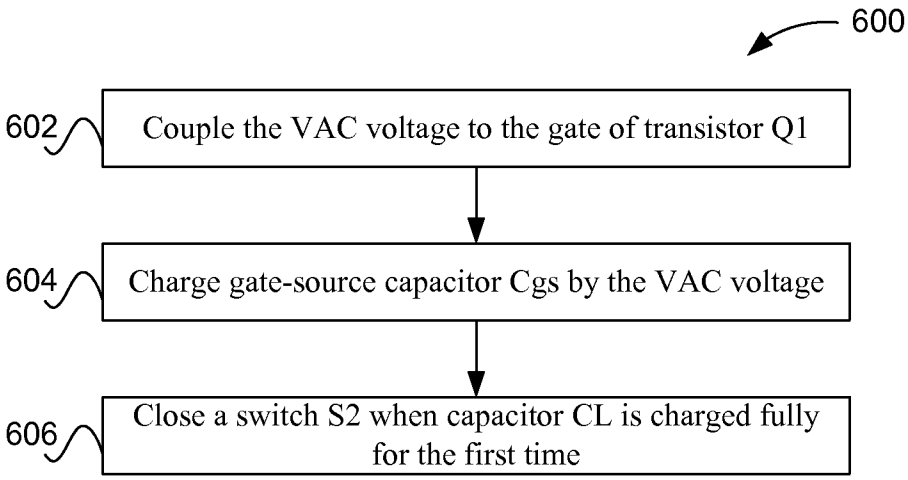
600
602
Couple the VAC voltage to the gate of transistor Q1
604
Charge gate-source capacitor Cgs by the VAC voltage
606
Close a switch S2 when capacitor CL is charged fully for the first time

Fig. 6