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Method of determining clock timing error in multicarrier system

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Abstract

In a multi-carrier transmission system, a clock timing error (τ_e) is calculated at the receivers side and used for synchronisation between a transmitting modem and a receiving modem (RX1). The clock timing error (τ_e) is calculated from phase errors (ϕ_0, ϕ_1, ... , ϕ_i, ..., ϕ_{N-1}) detected for a plurality of pilot carriers during a tracking mode in such a way that the share (A_i) of a phase error (ϕ_i) detected for a particular pilot carrier in the clock timing error (τ_e) depends on the transmission quality (SNR_i) of that pilot carrier over the transmission medium in between the two modems. In this way, the robustness of the synchronisation for narrowband noise near a pilot carrier is improved significantly.

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Invention Title:

"METHOD OF DETERMINING CLOCK TIMING ERROR IN MULTI-CARRIER SYSTEM"

The following statement is a full description of this invention, including the best method of performing it known to us:-

METHOD OF DETERMINING CLOCK TIMING ERROR IN MULTI-CARRIER SYSTEM

Field of the invention

This invention relates to a method to determine during a tracking mode a clock timing error in a multi-carrier transmission system.

Background of the invention

Such a method and related equipment to perform this method are already known in the art, e.g. from the European Patent Application EP 0 453 203, entitled 'Method and apparatus for correcting for clock and carrier frequency offset, and phase jitter in multicarrier modems' from applicant Telebit Corporation. Therein, phases of a few pilot carriers are detected and used to calculate a clock timing error named a phase correcting signal (see page 3, lines 11-35 of the cited European Patent Application). As is indicated on page 6, lines 24-26 of EP 0 453 203, the phase correcting signal is used in a phase-locked loop (PLL) to realise synchronisation between a transmitting multi-carrier modem and a receiving multicarrier modem.

In case of a narrowband interferer in the vicinity of one of the pilot carriers whose phases are detected to calculate the clock timing error, use of phase information extracted from this pilot carrier renders the so called clock timing error or phase correcting signal less accurate as a measure for the timing difference between transmitting and receiving modem. As a consequence, synchronisation between the transmitting and receiving modem may be lost in the known system when one of the pilot carriers is affected by noise.

Summary of the invention

An object of the present invention is to provide a method, arrangement and synchronisation units similar to those known, but whose robustness for narrowband noise near the pilot carriers is optimised.

According to a first embodiment of the invention there is provided a method to determine during a tracking mode in a multi-carrier system a clock timing error used for synchronisation purposes, the method including the steps of detecting a phase error for each of a plurality of pilot carriers and calculating the clock timing error from the phase errors, wherein the clock timing error is calculated as a weighted sum of the phase errors whereby, for each phase error, a weight coefficient depends on a signal-to-noise ratio value

measured for transmission of a corresponding pilot carrier for which the phase error is measured.

According to a second embodoment of the invention there is provided an arrangement to determine during a tracking mode in a multi-carrier system a clock timing error used for synchronisation purposes, the arrangement including:

- phase error detection means whereto a multi-carrier signal is applied, the phase error detection means being adapted to detect phase errors for each of a plurality of pilot carriers; and
- calculation means, coupled to the phase error detection means, and adapted to calculate the clock timing error from the phase errors,

wherein the arrangement including:

- weight coefficient determination means, having an output coupled to the calculation means and being adapted to receive via an input thereof signal-to-noise ratio values related to the plurality of pilot tones and to determine weight coefficients of the phase errors in the clock timing error from the signal-to-noise ratio values; wherein
- the calculation means is adapted to receive via an input thereof the weight coefficients and to calculate the clock timing error from the weight coefficients and the phase errors as a weighted sum of the phase errors.

Preferably, the clock timing error becomes a linear combination of the phase errors detected for the different pilot carriers so that calculation of the clock timing error involves low mathematical complexity. Via the weights of the different terms in the linear combination, the phase errors get different shares in the clock timing error. These weights, according to the present invention, are dependent on the transmission quality represented by the signal-to-noise ratio values of the respective pilot carriers.

Indeed, giving the phase error detected for a first pilot carrier which is transferred with a low transmission quality a relatively low share in the clock timing error used for synchronisation, and giving the phase error detected for a second pilot carrier which is transferred with a high transmission quality a relatively high share in the clock timing error used for synchronisation, has a filtering effect on the narrowband noise which affects the transmission quality of the first pilot carrier for this clock timing error. As a consequence, the variance of the clock timing error is reduced according to the present invention

resulting in a better tracking of the timing-locked loop whereto the clock timing error is applied as input. This implies that the synchronisation process is made less sensitive for narrowband noise.

Signal-to-noise ratio values of the different pilot carriers are excellent measures for the transmission quality of the medium between the multi-carrier modems. In an Asymmetric Digital Subscriber Line (ADSL) system operating according to the ANSI Standard T1.413-1995 entitled 'Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface', a signal-to-noise ratio value is measured for each carrier during initialisation and used for bit allocation. This is indicated in paragraphs 12.6.6, 12.7.8 and 6.5 of the cited ANSI Standard. Alternative implementations of the present invention however may use other transmission quality parameters, for instance the noise level, to determine the shares of the phase errors of different pilot carriers in the clock timing error used for synchronisation.

It is noticed that PCT Application WO 96/02991 describes a technique for compensating errors in frame alignment between a DMT transmitter and DMT receiver. The frame alignment error is determined by transmitting a predetermined frame from the DMT transmitter to the DMT receiver and performing correlations at the receiver. In the correlation result, which server as a measure for the frame alignment error, the different tones have different shares in proportion to the SNR measured at these tones. Clock timing errors in WO 96/02991 however are still compensated for in the traditional way, ie, via a single pilot carrier and a phase locked loop. It is to be noticed that the term 'comprising', used in the claims, should not be interpreted as being limitative to the means listed thereafter. Thus, the scope of the expression 'a device comprising means A and B' should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

Similarly, it is to be noticed that the term "coupled", also used in the claims, should not be interpreted as being limitative to direct connections only. Thus, the scope of the expression 'a device A coupled to a device B' should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means.

According to a third embodiment of the invention the signal-to-noise ratio value is determined during an acquisition mode preceding the tracking mode.

It can be expected that the transmission quality of the medium in between two multi-carrier modems at a certain frequency does not change abruptly, unless impulse noise disturbs the medium. If the transmission quality of the medium at that certain frequency is measured once during an acquisition mode or initialisation procedure, the measured quality can be used for a long period. In Discrete Multi Tone (DMT) systems such as an Asynchronous Digital Subscriber Line (ADSL) system, the transmission quality of the medium has to be measured as a function of frequency during initialisation of the system to be able to execute the bit allocation procedure: the process wherein each carrier is assigned a number of bits depending on the transmission quality of this carrier. In such systems, the information required to perform the method according to the present Invention is available once the system is in operation so that no additional measurements are required to determine the shares of phase errors of different pilot carriers in the clock timing error used for synchronisation. Only the phase errors of the different pilot carriers have to be detected during the tracking mode or normal operation process.

According to a another embodiment of the invention the weight coefficient is linearly proportional to the signal-to-noise ratio value.

As will be proven later on in this document, a maximum likelihood based approach of the problem of calculating the clock timing error out of phase errors detected for a plurality of pilot carriers results in a linear relationship between the weights and the transmission quality of the pilot carriers.

According to a further embodiment of the invention a proportionality factor between the weight coefficient and the signal-to-noise value is linearly dependent on a frequency of the corresponding pilot carrier.

Another result of the maximum likelihood approach set out later on in this document is that, for a particular pilot carrier, the coefficient which has to be multiplied with the transmission quality value to obtain the weight related to that pilot carrier is proportional to the frequency of that pilot carrier or the pilot carrier index in case the frequency is determined thereby.

According to a another embodiment of the invention there is provided the weighted sum is normalised by a linear combination of signal-to-noise ratio values measured for the plurality of pilot carriers.

Preferably, the weights are normalised.

According to a further embodiment of the invention there is provided a coefficient in the linear combination depends on a square frequency of a pilot carrier.

Preferably, the complete gain of the arrangement that determines the clock timing error is made equal to one. This feature is particularly advantageous in a system where the number of pilot carriers used for synchronisation is adaptive. Independence of the level of the clock timing error from the number of pilot carriers used to determine this clock timing error, obtained by a normalisation as defined in claim 7, is advantageous from the point of view of hardware implementation.

Brief description of the drawings

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

Figure 1 shows a block scheme of a receiving multi-carrier modem RX equipped with an embodiment of the clock timing error determination arrangement ARR according to the present invention;

Figure 2 shows a block scheme of a receiving multi-carrier modem RX2 equipped with a second synchronisation unit SYNCHRO2 including an embodiment of the clock timing error determination arrangement ARR according to the present invention; and

Figure 3 shows a block scheme of a receiving multi-carrier modem RX3 equipped with a third synchronisation unit SYNCHRO3 including an embodiment of the clock timing error determination arrangement ARR according to the present invention.

Detailed description of the embodiments

The multi-carrier receiver RX1 drawn in Figure 1 is provided with a skip and duplicate device S/D, a serial-to-parallel converter S/P, a fast fourier transformer FFT, a rotation device ROTOR, a clock timing error determination arrangement ARR, a feedback loop FBL, a channel gain device CHANNEL and a channel analysing device SNR. The rotation device ROTOR is equipped with N multipliers MU_0, MU_1, ..., MU_{N-1}, and the clock timing error determination arrangement ARR includes a phase detection unit PHASE, a weight determination unit WEIGHT, and a calculation unit CALC. The latter calculation unit CALC comprises N multipliers M_0, M_1 ... , M_i .., M_{N-1}, an adder S and a divider DIV. The feedback loop FBL includes a filter FIL. The skip and duplicate device

S/D, the rotation device ROTOR, the clock timing error determination arrangement ARR and the feedback loop FBL constitute a synchronisation system SYNCHRO1.

The incoming communication line is coupled via hybrid means, filtering and amplifying circuitry and an analogue to digital converter, not shown in Figure 1, to an input of the skip and duplicate device S/D. An output of the skip and duplicate device S/D is connected to an input of the serial-to-parallel converter S/P and the outputs of this serial-to-parallel converter S/P are coupled to respective inputs of the fast fourier transformer FFT. Each output terminal of the fast fourier transformer FFT is coupled to both an input of the channel analysing device SNR and an input of the rotation device ROTOR. More detailed, a first output of the fast fourier transformer FFT is coupled to the first multiplier MU_0 in the rotation device ROTOR, a second output of the fast fourier transformer FFT is coupled to the second multiplier MU_1 in the rotation device ROTOR, ..., and the N'th output of the fast fourier transformer FFT is coupled to the N'th multiplier MU_{N-1} in the rotation device ROTOR. The N multipliers MU_0, MU_1, ..., MU_{N-1} further are coupled to respective inputs of the phase detection unit PHASE, and N outputs of this phase detection unit PHASE are coupled to the N multipliers M_0, M_1, ... M_i,..., M_{N-1} in the calculation unit CALC respectively. The N multipliers M_0, M_1, ... M_i,..., M_{N-1} have outputs connected to input terminals of the adder S, and this adder S is further connected to the divider DIV. An output of the divider DIV is feedback coupled to a control input of the skip and duplicate device S/D and to control terminals of the multipliers MU_0, MU_1, ..., MU_{N-1} In the rotation device ROTOR via the filter FIL in the feedback loop FBL. Outputs of the channel gain device CHANNEL are also coupled to these control terminals of the multipliers MU_0, MU_1, ..., MU_{N-1} via other multipliers MU'_0, MU'_1, ..., MU'_{N-1} Inserted in the feed back loop from the divider DIV to the rotation device ROTOR. The channel analysing device SNR is via an output thereof coupled to an input of the weight determination unit WEIGHT which has N+ 1 outputs, labelled A_0, A_1, ..., A_i, ..., A_{N-1}, and B in Figure 1. These outputs are coupled to second inputs of the multipliers M_0, M_1, ... M_i,..., M_{N-1} and of the divider DIV in the calculation unit CALC respectively.

The receiver RX1 is supposed to be of the ADSL (Asymmetric Digital Subscriber Line) type and consequently receives at its input a multi-carrier signal following the recommendations of the already cited ADSL Standard. This implies for instance that the multi-carrier signal received by the modem RX1 is composed of a sequence of DMT (Discrete Multi Tone) symbols. Such a DMT symbol has a predetermined length in time

and consists of the superposition of 256 modulated carriers with equidistant frequencies. In the symbol timing synchronisation process, the receiving modem RX1 basically detects the boundaries of the received DMT symbols in order to select the correct block of consecutive samples to be fed to the fast fourier transformer FFT. In other words, symbol timing recovery is defined as the process to determine for each incoming DMT symbol which is the first sample of the sequence of consecutive samples to be sent to the fast fourier transformer FFT. Several algorithms for symbol synchronisation are described in literature. Estimation of the symbol boundaries for instance may be executed with an accuracy equal to one sample period during an acquisition phase.

The present invention however is related to the process of sample timing synchronisation, wherein the receiving modem RX1 monitors the increase in difference in phase between the transmitter clock and the receiver clock and compensates for this difference via a feedback algorithm. The difference between the transmitter timing basis and receiver timing basis is compensated for during the normal transmission mode instead of during the acquisition phase because the clock differences can change all the time. The invention concerns the method to estimate the difference in clock timing between the transmitter and receiver clock. The more accurate this clock timing difference is determined, the better the sample timing synchronisation process will compensate for it. In the following paragraph, the role of the functional blocks drawn in Figure 1 is discussed briefly. In an additional paragraph, a lower bound is derived for the variance on the estimation error of the clock timing error determined according to the present invention in function of the number of pilot carriers involved in the clock timing error determination method. A further paragraph describes a most likelihood based approach of the problem of determining the clock timing error and results in deriving a preferred embodiment of the present invention. Alternative synchronisation units for the one drawn in Figure 1 wherein the same clock timing error determination arrangement ARR is used but which include other circuitry to realise the sample timing synchronisation are described in yet another paragraph which deals with Figure 2 and Figure 3. Some remarks and notes concerning the applicability of the present invention are listed in the paragraphs concluding the description of the present application.

After digitisation and having passed the skip and duplicate device S/D, the digitised multi-carrier signal is serial-to-parallel converted. The serial-to-parallel converter S/P thereto applies subsequent samples of one and the same DMT (Discrete Multi Tone)

symbol to subsequent ones of its outputs. The fast fourier transformer FFT in addition converts these samples of one DMT symbol from time domain to frequency domain by executing the well-known Discrete Fourier Transformation. As a result thereof, each signal at an output terminal of the fourier transformer FFT represents a modulated carrier and can be seen as a vector point in a two-dimensional vector plane wherein the modulation constellation represents a set of points. The amplitude and phase that can be associated to this vector point in the two-dimensional vector plane correspond to the amplitude and phase of the modulated carrier at the output of the fast fourier transformer FFT. The rotation device ROTOR, coupled to the fast fourier transformer FFT, has the task to compensate for differences between the clocks in the transmitting modem, not drawn in the figure, and receiving modem RX1. The clock signal In the receiving modem RX1 is generated by a free running crystal, not shown in Figure 1, and supplied to the clock input of the analogue to digital converter mentioned above. The clock differences introduce phase errors which are proportional to the frequencies of the carriers. The rotation device ROTOR consequently applies a phase shift or so called rotation to each one of the carriers In proportion to the frequency of the respective carrier so that the clock speed difference is compensated for. The channel gain device CHANNEL thereto realises that the signals fed back to the multipliers MU_0, MU_1, ..., MU_{N-1} are proportional to the frequencies of the respective carriers. To be able to precisely compensate for the clock difference, the rotation device ROTOR needs accurate information with respect to the clock timing error τ_e. It is the task of the clock timing error determination arrangement ARR and the feedback loop FBL to determine this clock timing error τ_e precisely and to feed it back to the rotation device ROTOR. As soon as the clock timing error re to be compensated for by the rotation device ROTOR becomes larger than one sample period, a sample has to be skipped or duplicated in the incoming digitised signal. This is the task of the skip and duplicate device S/D which therefor also receives the information generated by the clock timing error determination arrangement ARR and feedback loop FBL. The operation of the skip and duplicate device S/D and that of the rotation device ROTOR accords to well-known techniques described for instance in *the contribution to the ADSL Standard TIE 7.4193-025, paragraphs 2.2,* 2.2.7, 2.2.8 , *3.2, 3.2.7 and 3.2.8. This contribution is entitled 'VLSI DMT Implementation for ADSL' and originates from Amati Communications* Corporation. The accurateness of the clock timing error τ_e determined by the clock timing error determination arrangement ARR is of significant importance, since

it determines the accurateness of the operations performed by the rotation device ROTOR and the skip and duplicate device S/D and thus also the accurateness of the whole synchronisation process between transmitting modem and receiving modem RX1. As will be shown in the following paragraph, a larger robustness for narrowband noise is obtained when multiple pilot carriers are used. Therefor, the phase detection unit PHASE produces phase errors ϕ_0, ϕ_1, ..., ϕ_i, ..., ϕ_{N-1} for N carriers from observations of the fast fourier transformers outputs. Although the phase detection unit PHASE measures the phase of the signals at the output of the fast fourier transformer FFT, it has to be noted that an alternative implementation of the phase detection unit PHASE may determine the difference between a received vector and an expected vector (determined by the closest constellation point in the constellation diagram) and can approximate the phase errors therefrom. Each phase error is multiplied with a corresponding weight coefficient A_0, A_1, ..., A_i, ..., A_{N-1} . These weights A_0, A_1, ..., A_i, ..., A_{N-1} are determined by the weight determination unit WEIGHT on the basis of signal-to-noise ratio values SNR_i measured for the different pilot carriers. During the acquisition mode, a predetermined sequence of bits is modulated on the carriers. The channel analyser SNR analyses these modulated carriers after transmission thereof over the communication line and measures the signal-to-noise ratio for each carrier. During tracking mode, the channel analyser SNR applies the signal-to-noise ratio values SNR_j to the weight determination unit WEIGHT which determines the weight coefficients A_0, A_1, ..., A_i, ..., A_{N-1} and applies them to the multipliers M_0, M_1, ... M_i,..., M_{N-1} respectively. The weighted phase errors are summed together by the adder S and normalised with a normalisation factor B by the divider DIV. The normalisation factor B is also determined by the weight determination unit WEIGHT from the signal-to-noise ratio values SNR_i. The clock timing error τ_e obtained in this way at the output of the calculation unit CALC is fed back via the filter FIL and digital voltage controlled oscillator to the rotation device ROTOR and skip and duplicate device S/D. The feedback loop FBL may perform the function of a traditional phase locked loop (PLL). The rotation device ROTOR phase shifts each carrier of the multi-carrier signal proportional to the calculated clock timing error τ_e and to the frequency of the respective carrier. The signal supplied to the second terminals of the multipliers MU_0, MU_1, ..., MU_{N-1} is made proportional to the frequency of the respective carriers by the channel gain device CHANNEL and the multipliers MU'_0, MU'_1, ..., MU'_{N-1}. When the clock timing error τ_e, becomes larger than

one sample period, the skip and duplicate device S/D is activated to either skip or duplicate a sample in the incoming multi-carrier signal.

Consider the received continuous time multi-carrier signal r(t) at the input of the receiver RX1:

$$r(t) = \sum_{m=-\infty}^{+\infty} \sum_{k=0}^{2N-1} \sum_{n=-\upsilon}^{2N-1} a_m^k . g\left(t - \frac{n.T}{2} - m(2.N + \upsilon)\frac{T}{2}\right) . e^{i.\frac{2\pi}{2N}.k.n} + n(t) \qquad (1)$$

Herein, the following notation is used:

N	:	Number of carriers in the DMT signal, i.e. 256 in an ADSL system;
a_m^k	:	symbol modulating the k'th carrier in the m'th DMT symbol period;
g(t)	:	composite channel impulse response, i.e. the channel impulse response that is eventually equalised to reduce intersymbol interference;
t	:	time;
$\frac{2}{T}$	:	sampling rate;
n(t)	:	additive noise component;
n	:	sample index;
k	:	carrier index;
m	:	DMT symbol index;
	:	number of guardband samples, i.e. the number of redundant samples in a cyclic prefix added to each DMT symbol to compensate for intersymbol interference;
i		square root of -1;
π	:	pi=3.1415;
∞	:	symbol representing infinity;
τ_e	:	clock timing error at the output of the arrangement ARR;
τ	:	estimated time difference at the output of the feedback loop FBL; and
$\tilde{\tau}$	:	time difference or difference in sample timing between the

transmitting modem and receiving modem,

After the acquisition mode and assuming no timing error, the output of the fast fourier transformer FFT can be expressed as:

$$F_m^k = a_m^k . G^k + N^k \qquad (2)$$

Herein, G^k represents the fourier transform of g(t) evaluated at the k'th carrier frequency which is equal to $\frac{k}{N.T}$ and N^k represents the contribution of the additive noise at the k'th carrier frequency.

In case of a clock timing difference equal to τ, the output of the fast fourier transformer FFT can be expressed as:

$$F_m^k = a_m^k . G^k . e^{-i.\frac{2\pi.2\tau}{2N.T}.k} + \tilde{N}^k \qquad (3)$$

This expression (3) is correct as long as the clock timing difference τ is smaller than the difference between the channel impulse response duration and the guard time duration. The Cramer-Rao bound is a fundamental lower bound on the estimation of unbiased parameters. Estimation of the clock timing differences τ, denoted by $\tilde{\tau}$ can be derived from observations of the fast fourier transform outputs. In the assumption that the additive noise contributions at the output of the fast fourier transformer FFT are uncorrelated, the lower bound on the timing error variance can be expressed as:

$$E\left\{\left(\tau-\tilde{\tau}\right)^2\right\}=\left(\frac{T}{2}\right)^2.\left(\frac{2N}{2\pi}\right)^2.\frac{1}{M}.\left(\sum_k SNR_k . k^2\right)^{-1} \qquad (4)$$

Herein, $E\left\{\left(\tau-\tilde{\tau}\right)^2\right\}$ represents the Cramer-Rao lower bound on the variance of the clock timing error $\tau-\tilde{\tau}=\tau_e$, M is the observation window expressed as an integer number of DMT symbols, and SNR_k is the signal-to-noise ratio value associated with the k'th carrier. By definition, this signal-to-noise ratio value SNR_k is equal to:

$$SNR_k = \frac{E\left\{\left|a_m^k\right|^2\right\}.\left|G^k\right|^2}{E\left\{\left|N_m\right|^2\right\}} \qquad (5)$$

In (5), $E\left\{\left|a_m^k\right|^2\right\}$ represents the mean power of the m'th symbol, $\left|G^k\right|^2$ represents the gain of the channel, and $E\left\{\left|N_m\right|^2\right\}$ represents the mean noise power on carrier k. For transmission over a FEXT (Far End Crosstalk) dominated channel, the signal-to-noise ratio SNRk can be expressed as:

$$SNR_k = \frac{1}{K_f.d}.\left(\frac{NT}{k}\right)^2 \qquad (6)$$

This is indicated in paragraph 6.2.1 of the 'VDSL System Requirements' with reference T1E1.4/96-153R3, published on December 31, 1996. In expression (6), d equals the length of the transmission cable and K_f represents the FEXT coupling constant. Substituting (6) in (4) gives for the Cramer-Rao lower bound the following expression:

$$E\left\{\left(\tau-\tilde{\tau}\right)^2\right\} = \frac{1}{K}.\frac{K_f.d}{4.M.\pi^2} \qquad (7)$$

Herein, K represents the number of outputs of the fast fourier transformer FFT used to produce the clock timing error τ_e.

From (7) it can be concluded that it is advantageous to base the calculation of the clock timing error τ_e on multiple carriers. In a FEXT dominated environment the variance on the clock timing error τ_e is proportional to the inverse of the number of carriers used. When selecting only a limited number of pilot carriers to produce the clock timing error τ_e one should take the carriers with the largest product of the signal-to-noise ratio and squared carrier index in order to obtain the lowest clock timing error variance. In the receiver RX1 of Figure 1, all carriers are used by the clock timing determination arrangement ARR to produce the estimate of the clock timing error τ_e,

In a most-likelihood based approach, new timing error estimates are based on snapshots of the log likelihood function $L_m\left(\tilde{\tau}_m\right)$ whereby:

$$L_m\left(\tilde{\tau}_m\right) = -\frac{K}{2}.\ln(2\pi) - \frac{1}{2}.\sum_k \ln\left(E\left\{ \left| N^k \right|^2 \right\} \right) - \sum_k \frac{\left| F_m^k - a_m^k . G^k . e^{-i.\frac{2\pi . 2\tilde{\tau}_m}{2N.T}.k} \right|^2}{2.E\left\{ \left| N^k \right|^2 \right\}} \qquad (8)$$

During tracking mode, the clock timing error determination arrangement ARR produces reliable estimates of the transmitted data sequence while channel gains are known to the receiver (they have been measured during modem initialisation). Hence, at the m'th DMT symbol period, a Data Aided Most Likelihood (DAML) clock timing error determination arrangement ARR produces the value τ_e:

$$\tau_m \quad -2.\Im\left\{ \frac{\pi}{n}.\frac{2\tilde{\tau}_m}{T}.\sum k.\frac{F_m^k.\left(a_m^k . G^k\right)^* . e^{i.\frac{2\pi . 2\tilde{\tau}_m}{2N.T}.k}}{2.E\left\{ \left| N^k \right|^2 \right\}} \right\} \qquad (9)$$

Herein * denotes the complex cojugate and $\Im$ denotes the imaginary part. Substitution from (3) into (9) leads to the conclusion that the weight coefficient A_i has to be equal to SNR_k and the normalisation factor B has to equal $\sum_{k=0}^{N=1} k^2 . SNR_k$. The derived timing error τ_e can be used to control either continuous time or discrete time based synchronisation structures.

In Figure 2 a multi-carrier receiver RX2 is drawn which only differs from the multi-carrier receiver RX1 in Figure 1 in the means used to realise sample timing synchronisation. The serial-to-parallel converter S/P, the fast fourier transformer FFT, the rotation device ROTOR, the clock timing error determination arrangement ARR and the components PHASE, CALC and WEIGHT thereof, the feedback loop FBL, the channel gain device CHANNEL and the channel analyser SNR perform exactly the same functions as the equally labelled functional blocks in Figure 1. Instead of feeding back the clock timing error τ_e Produced by the clock timing error determination arrangement ARR to the skip and duplicate device S/D and the rotation device ROTOR, the clock timing error τ_e in receiver RX2 is fed back to a e voltage controlled crystal oscillator VCXO whose output is coupled to the clock input of the analogue to digital converter A/D. The clock timing error τ_e thus is used to adapt the sample period so that sample timing synchronisation between

the transmitting modem and receiving modem is obtained. The analogue to digital converter A/D, the voltage controlled crystal oscillator VCXO, the rotation device ROTOR, the clock timing error determination arrangement ARR and the feedback loop FBL constitute a synchronisation unit SYNCHRO2 which is an alternative for the synchronisation unit SYNCHRO1 of Figure 1.

Yet another multi-carrier receiver RX3 is drawn in Figure 3. The serial-to-parallel converter S/P, the fast fourier transformer FFT, the rotation device ROTOR, the clock timing error determination arrangement ARR with its components PHASE, WEIGHT and CALC, the feedback loop FBL, the channel gain device CHANNEL and the channel analyse SNR again perform the same role as the equally labelled functional blocks in Figure 1 and Figure 2. The clock timing error τ_e now however is fed back to both an interpolator INT whereto the serial-to-parallel converter S/P is coupled. The interpolator now provide for sample timing synchronisation by interpolating between two samples. The interpolator INT, the rotation device ROTOR, the clock time error determination arrangement ARR and the feedback loop FBL constitute an alternative synchronisation unit SYNCHRO3 for the synchronisation units SYNCHRO1 and SYNCHRO2 drawn in Figure 1 and Figure 2 respectively.

A first remark is that, although the multi-carrier signal in the above described embodiment is transported over a telephone line, the applicability of the present invention is not restricted by the transmission medium via which the signal is transported. In particular, any connection between the transmitting modem and receiving modem RX, e.g. a cable connection, a satellite connection, a radio link through the air, and so on, may be affected by narrowband noise, and thus the synchronisation procedure can be improved according to the present Invention.

The invention also is not only related to ADSL (Asymmetric Digital Subscriber Line) or similar systems wherein DMT (Discrete Multi Tone) modulation is used. A person skilled in the art will be able to adapt the above described embodiment so that it is applicable in any other system wherein a multi-carrier signal is transmitted from a transmitting modem to a receiving modem RX and wherein a plurality of pilot carriers are used for synchronisation purposes during the tracking mode. Systems wherein orthogonal frequency division multiplexing (OFDM) or orthogonally multiplexed quadrature amplitude modulation (OMQAM) is applied for instance are multi-carrier environments wherein the present invention is applicable.

Another remark is that embodiments of the present invention are described above in terms of functional. From the functional description of these blocks, given above, it will be obvious for a person skilled in the art of designing electronic devices how embodiments of these blocks can be manufactured with well-known electronic components. A detailed architecture of the contents of the functional blocks hence is not given.

It is to be noticed that the weights A_0, A_1, ..., A_i, ..., A_{N-1} and the normalisation factor B are calculated above in accordance to the results of a maximum likelihood approach. Although the above weights A_0, A_1, ..., A_i, ..., A_{N-1} and normalisation factor B are to be used in a preferred embodiment of the present invention, the basic principle of the present invention, i.e. the use of transmission quality information for a plurality of pilot carriers to determine the shares of phase information obtained from these pilot carriers in the clock timing error re that is used for synchronisation, is also satisfied when less optimal values are used for the weights A_0, A_1, ..., A_i, ..., A_{N-1} or the normalisation factor B.

It is also noticed that applicability of the present Invention is not restricted to digital environments. A person skilled in the art of electronic design knows that analogue equivalents exist for ail functional blocks described above so that an analogue version of the present invention can be derived from the above described digital embodiments without inventive contribution.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

CLAIMS

1. A method to determine during a tracking mode in a multi-carrier system a clock timing error used for synchronisation purposes, the method including the steps of detecting a phase error for each of a plurality of pilot carriers and calculating the clock timing error from the phase errors, wherein the clock timing error is calculated as a weighted sum of the phase errors whereby, for each phase error, a weight coefficient depends on a signal-to-noise ratio value measured for transmission of a corresponding pilot carrier for which the phase error is measured.

2. A method as claimed in claim 1, wherein the signal-to-noise ratio value is determined during an acquisition mode preceding the tracking mode.

3. A method as claimed in claim 1 or claim 2, wherein the weight coefficient is linearly proportional to the signal-to-noise ratio value.

4. A method as claimed in claim 3, wherein a proportionality factor between the weight coefficient and the signal-to-noise value is linearly dependent on a frequency of the corresponding pilot carrier.

5. A method as claimed in claim 3, wherein the weighted sum is normalised by a linear combination of signal-to-noise ratio values measured for the plurality of pilot carriers.

6. A method as claimed in claim 5, wherein a coefficient in the linear combination depends on a square frequency of a pilot carrier.

7. An arrangement to determine during a tracking mode in a multi-carrier system a clock timing error used for synchronisation purposes, the arrangement including:

- phase error detection means whereto a multi-carrier signal is applied, the phase error detection means being adapted to detect phase errors for each of a plurality of pilot carriers; and
- calculation means, coupled to the phase error detection means, and adapted to calculate the clock timing error from the phase errors,

wherein the arrangement including:

- weight coefficient determination means, having an output coupled to the calculation means and being adapted to receive via an input thereof signal-to-noise ratio values related to the plurality of pilot tones and to determine weight coefficients of the phase errors in the clock timing error from the signal-to-noise ratio values; wherein

- the calculation means is adapted to receive via an input thereof the weight coefficients and to calculate the clock timing error from the weight coefficients and the phase errors as a weighted sum of the phase errors.

8. A method of determining a clock timing error substantially as herein described with reference to the accompanying drawings.

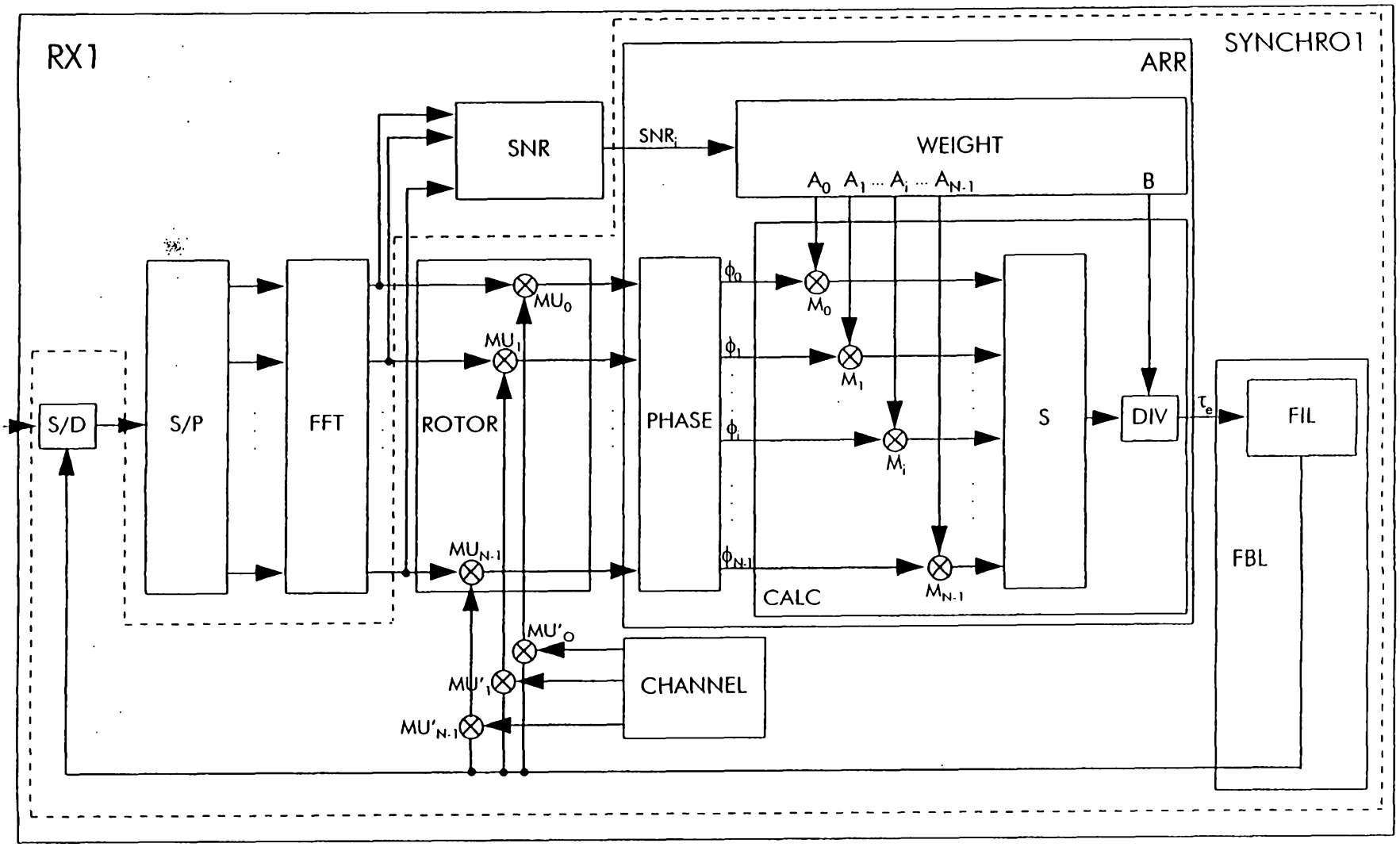
9. A clock timing error detection arrangement substantially as herein described with reference to the accompanying drawings.

Dated this **12th** day of **November 2001**

ALCATEL

by its attorneys

Freehills Carter Smith Beadle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ROTOR
PHASE
CALC
S
DIV
τ_e
FIL
FBL
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MU_1
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MU'_1
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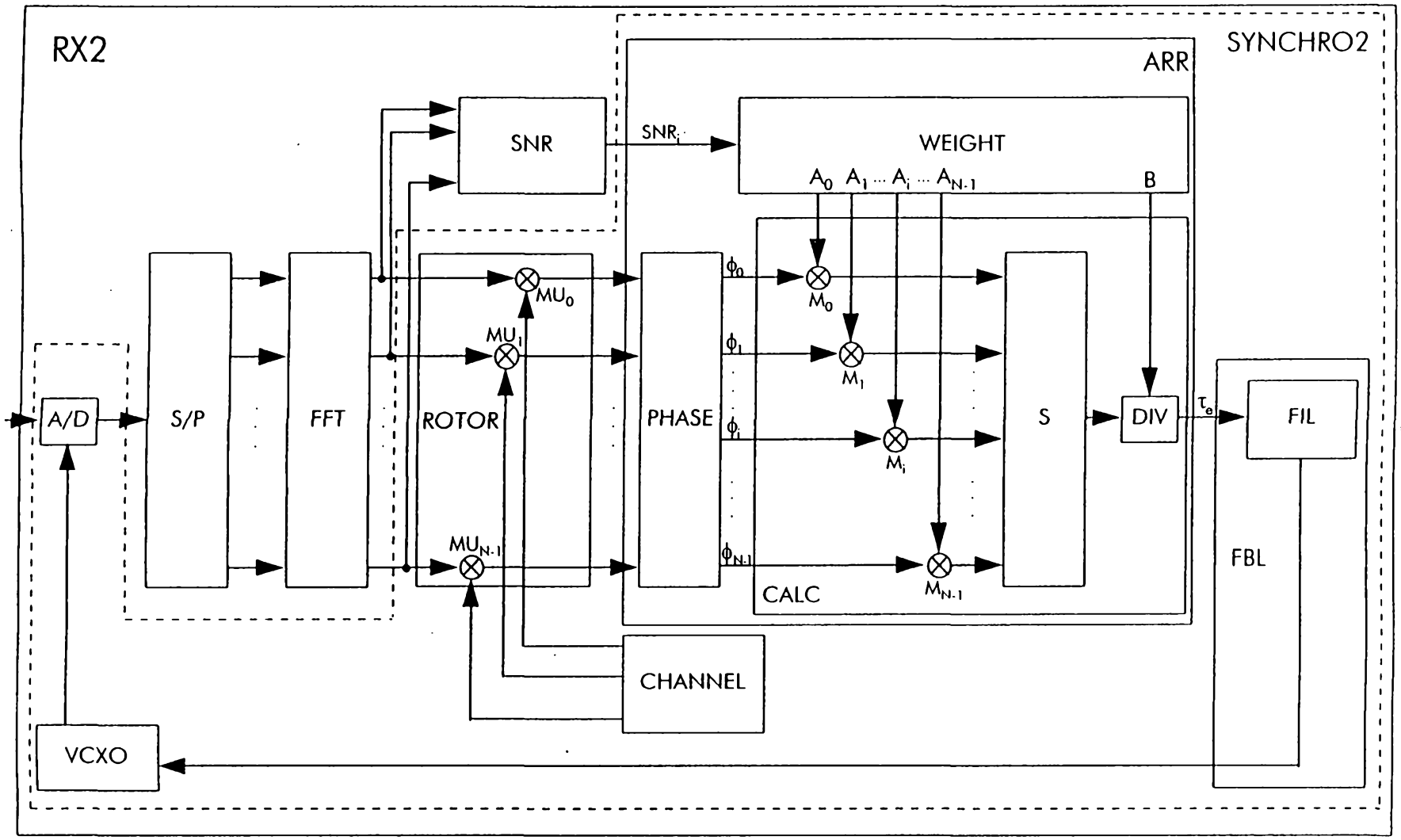
M_i
M_N-1

Fig. 1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A/D
S/P
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ROTOR
MU_0
MU_1
MU_N-1
PHASE
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φ_1
φ_i
φ_N-1
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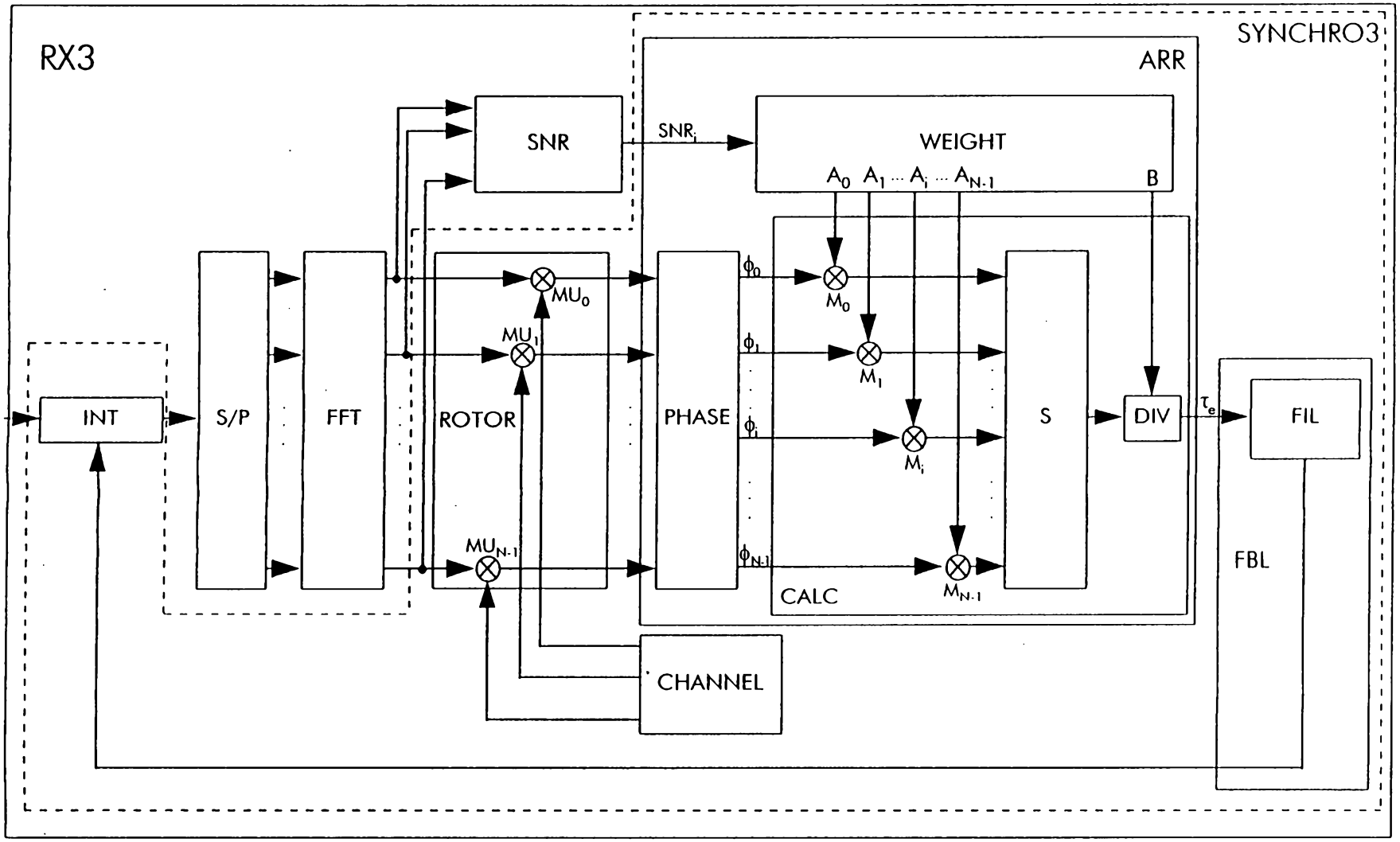
Fig. 2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SYNCHRO3
ARR
SNR
SNR_i
WEIGHT
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B
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S/P
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ROTOR
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CHANNEL

Fig. 3