(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 September 2010 (30.09.2010)

PCT

(10) International Publication Number
WO 2010/110878 A1

(51) International Patent Classification:
C23F 1/08 (2006.01) *H01L 21/3065* (2006.01)

(21) International Application Number:
PCT/US2010/000865

(22) International Filing Date:
24 March 2010 (24.03.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

61/210,990	24 March 2009 (24.03.2009)	US
61/211,573	31 March 2009 (31.03.2009)	US
61/211,614	31 March 2009 (31.03.2009)	US

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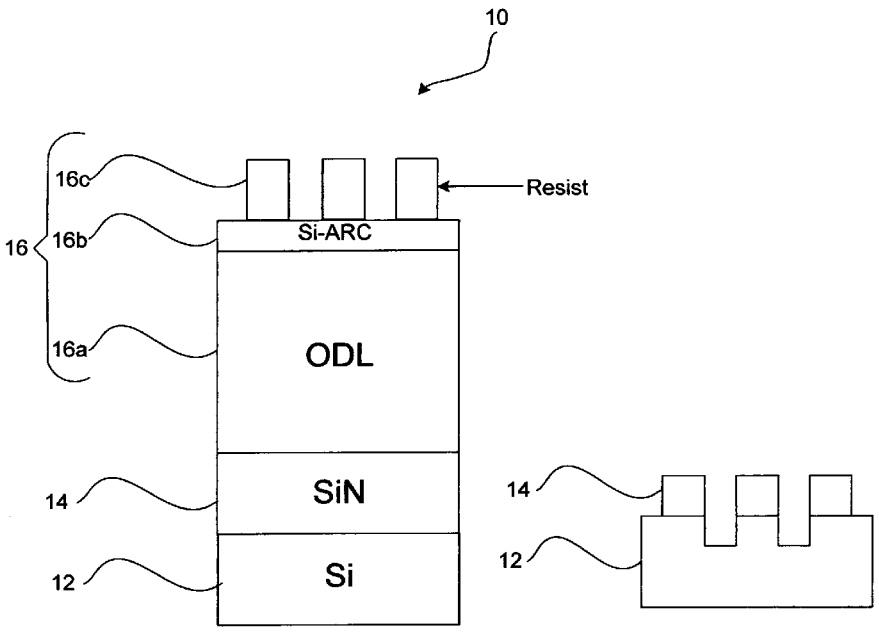
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,

[Continued on next page]

(54) Title: PLASMA ETCHING METHOD

FIG 1



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ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(57) Abstract: A method for processing a substrate to form a desired pattern by an etching process after forming a mask pattern over the substrate includes the steps of forming two layers over the substrate; measuring a width of the mask pattern or an etched pattern of one of the two layers; and adjusting a flow rate of any one of HBr and other gases, used in the etching process, based on the measured width. The two layers may include a silicon nitride layer and an organic dielectric layer.

PLASMA ETCHING METHOD

This application claims priority from United States provisional application Serial No. 61/210,990, filed March 24, 2009, United States provisional application Serial No. 61/211,573, filed March 31, 2009, and United States provisional application Serial No. 61/211,614, filed March 31, 2009, all three entitled "Plasma Etching Method", the contents of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0001]

The present invention relates to semiconductor devices and their manufacturing methods. More specifically, it relates to etching plasma methods for providing high-resolution patterns with a desired critical dimension (CD) value.

BACKGROUND OF THE INVENTION

[0002]

In semiconductor manufacturing process, photolithography technology is used for forming resist patterns. In photolithography technology, a resist solution is first coated on a semiconductor or a liquid crystal display (LCD) substrate. Using a photo mask, the resist film is exposed to a pattern of intense light and then developed. As a result, a desired resist pattern is formed on the semiconductor or the LCD substrate. After forming the desired resist pattern, an etching process will

take place for etching the semiconductor or the LCD substrate.

[0003]

It is known that the processing results in each of the above-mentioned processing steps may not meet a target value, even though they are performed under constant processing conditions, due to existence of unwanted factors such as, for example, the condition of the substrate surface, atmospheric pressure, and fluctuations in temperature and relative humidity.

[0004]

Conventionally, after processing a fixed number of substrates, a substrate is pulled out for inspection. During the inspection various parameters are measured and a decision is made as to whether the processing conditions are appropriate based on the inspection results. Example of those parameters may include a thickness of the resist film after the coating process, a line-width or critical dimension (CD) of the resist pattern after the developing process, accuracy in matching a base pattern with the resist pattern, inconsistencies on the developed surface, a defect on the development, and a line-width or critical dimension (CD) of the etched substrate and a defect on its surface after the etching process.

[0005]

The processing conditions for each process steps may then be amended according to the decision made based on the inspection results. This operation amendment, which is very troublesome, may be performed by an experienced operator. To facilitate the amendment operation, a resist pattern forming process is proposed in Japanese Patent Application Publication No. 2002-190446. In this process a predetermined set of amendment parameters which are related to each

specific measured parameter are first determined. The predetermined set of amendment parameters are then amended according at an automated inspection results.

[0006]

For example, in the case where the line-width or the critical dimension (CD) of an etched substrate is considered as the specific measured parameter, the following amendment parameters may be amended to achieve the target value: 1) the light exposure intensity; 2) the heating time; 3) the developing time; 4) the etching time; and 5) the etching gas composition ratio. However, the above-mentioned publication does not specify how the gas composition ratio may affect the etching process for achieving the desired target value of critical dimension (CD).

[0007]

Further, in Japanese Patent Application Publication No. 2003-209093 a substrate treatment process is disclosed in that a critical dimension (CD) of a resist pattern is precisely measured to form a desired circuit pattern after the etching step. In this process the critical dimension (CD) of the resist pattern is first measured. The measured result is then fed forwarded to an etching processing unit for adjusting the treatment conditions. By setting the optimal treatment conditions, a precise and desired circuit pattern can be obtained after the etching process. This technique provides a feed forward method for etching a desired pattern based on the measured resist film critical dimension (CD). However, similar to the previous publication, it fails to point out the specific conditions with regards to the etching gas types and their composition ratio for achieving the desired critical dimension

(CD).

[0008]

The present invention is proposed in view of the above aforementioned problems. The present invention provides a process for forming high-resolution patterns with a desired critical dimension (CD) using specific type of etching gas and their composition ratio.

SUMMARY OF THE INVENTION

[0009]

In accordance with one aspect of the present invention, there is provided a method for processing a substrate to form a desired pattern by an etching process after forming a mask pattern over the substrate. The method includes the steps of: forming two layers over the substrate, where the two layers include a silicon nitride layer and an organic dielectric layer; measuring a width of the mask pattern or an etched pattern of one of the two layers; and adjusting a flow rate of any one of HBr and other gases based on the measured width. The HBr and the other gases are being used in the etching process.

[0010]

In accordance with a second aspect of the present invention, there is provided a method for processing a substrate to form a desired pattern by an etching process after forming a mask pattern over the substrate, the method includes the steps of: forming three layers over the substrate, the three layers include a silicon nitride layer, an organic dielectric layer and a silicon-contained anti-reflective coating layer; measuring a width of the mask pattern or an etched pattern of one of the three

layers; and adjusting a flow rate of any one of CF_4 and CHF_3 based on the measured width. The CF_4 and CHF_3 are being used in the etching process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

Fig. 1 illustrates schematically an embodiment of a target structure before and after performing a plasma etching process.

Fig. 2 illustrates schematically an alternative embodiment of a target structure and a cross-sectional view of an experimental sample after patterning the silicon nitride (SiN) layer.

Fig. 3 depicts a schematic diagram of an embodiment of a plasma processing device.

Fig. 4 depicts a schematic diagram of an embodiment of a line-width measurement device integrated into a coater developer.

Fig. 5 depicts a schematic diagram of an alternative embodiment of a line-width measurement device integrated into an etching device.

Fig. 6 illustrates an embodiment of a process for adjusting a line-width of patterns where multiple layers are etched.

Fig. 7 depicts a schematic diagram of an alternative embodiment of a stand-alone line-width measurement device.

Fig. 8 illustrates cross-sectional views of experimental samples showing a dense pattern and an isolated pattern after performing a plasma etching process at each specific layer.

Fig. 9 illustrates cross-sectional views of experimental samples and their critical dimension (CD) as a function of over etching (OE) time treatment.

Fig. 10 illustrates cross-sectional views of experimental samples and their critical dimension (CD) as a function of HBr flow rate.

Fig. 11 illustrates cross-sectional views of experimental samples showing a dense pattern and an isolated pattern for various etching gas type.

Fig. 12 illustrates cross-sectional views of experimental samples and their critical dimension (CD) as a function of Ar/HBr/O2 series flow rate.

Fig. 13 illustrates cross-sectional views of experimental samples and their critical dimension (CD).

Fig. 14 illustrates microwave power, RF power, and RF voltage of each mask layer as a function of time.

Fig. 15 illustrates cross-sectional views of experimental samples and their critical dimension (CD).

Fig. 16 illustrates cross-sectional views of experimental samples and their critical dimension (CD).

DETAILED DESCRIPTION OF INVENTION

[0012]

Embodiments of the present invention will be described hereinafter with reference to the accompanying drawings, in which preferred exemplary embodiments of the invention are shown. The ensuing description is not intended to limit the scope, applicability or configuration of the disclosure. Rather, the

ensuing description of the preferred exemplary embodiments will provide those skilled in the art with an enabling description for implementing preferred exemplary embodiments of the disclosure. It should be noted that this invention may be embodied in different forms without departing from the spirit and scope of the invention as set forth in the appended claims.

[0013]

This disclosure relates in general to semiconductor devices and their manufacturing process. More specifically, it relates to etching plasma methods for providing high-resolution patterns with a desired critical dimension (CD) value.

[0014]

Embodiments of the present invention are directed to an etching process for controlling the line-width or the critical dimension (CD) of a silicon (Si) pattern. The silicon (Si) pattern is formed using a silicon nitride (SiN) hard-mask pattern. The silicon nitride (SiN) hard-mask pattern is, in turn, formed using a tri-layer mask pattern. The tri-layer mask pattern includes an organic dielectric layer (ODL). In order to obtain the desired silicon (Si) pattern with a predetermined critical dimension (CD) value, the line-width or the critical dimension (CD) of the silicon nitride (SiN) hard-mask pattern, formed on a silicon (Si) substrate, should be precisely controlled. This is achieved by adding hydrogen bromide (HBr) in a mixed atmosphere of nitrogen and oxygen (N_2/O_2) while patterning the organic dielectric layer (ODL).

[0015]

By adding hydrogen bromide (HBr) and increasing its flow rate, hydrogen (H) concentration is reduced on the surface of the ODL layer due to the extraction of

oxygen (O). As a result, an organic dielectric layer (ODL) with high carbon content is created. The high carbon content of the ODL layer generates carbon-carbon bonds which makes the organic dielectric layer (ODL) more rigid. The rigid property of ODL layer provides a better controllability for obtaining a predetermined value of critical dimension (CD) by reducing horizontal etching rate especially when the CD value is thinner than the target value.

[0016]

Moreover, the high carbon content of the ODL layer generates a plurality of bromide-carbon bonds on the surface of the ODL pattern. As a result, a thin layer of carbon bromide (CBrx) is deposited over the ODL pattern as a side wall protection. This leads to thicken the ODL's critical dimension (CD).

[0017]

According to one embodiment of the present invention, a desired critical dimension (CD) value is carried out by adjusting the hydrogen bromide (HBr) flow rate while performing a main etching (ME) step over the organic dielectric layer (ODL). By increasing the hydrogen bromide (HBr) flow rate, the critical dimension (CD) of ODL pattern tends to increase in value.

[0018]

According to another embodiment, the critical dimension (CD) of ODL pattern may also be adjusted by performing an over etching (OE) step after completing the main etching (ME) step. In the over etching (OE) step, the desired critical dimension (CD) value may be carried out by adjusting the nitrogen to oxygen ratio (N_2/O_2) and adding appropriate amount of hydrogen bromide (HBr).

Accordingly, if the difference between actual CD value and targeted value is relatively greater, adjustment can be done for main etching (ME) process, and when the difference is relatively smaller adjustment can be done for over etching (OE) process.

[0019]

In one embodiment, the critical dimension (CD) value may increase by setting the hydrogen bromide (HBr) flow rate to a fix value while extending the over etching time period. In an alternative embodiment, the critical dimension (CD) value may be thickened by increasing the hydrogen bromide (HBr) flow rate. This leads to a higher composition ratio of hydrogen bromide (HBr) gas to other gases in the overall atmosphere.

[0020]

According to yet another embodiment, the desired critical dimension (CD) value may be carried out in the ODL over etching (OE) step by adjusting the nitrogen to oxygen ratio (N_2/O_2) and adding chlorine (Cl_2) gas.

[0021]

According to yet another embodiment, the desired critical dimension (CD) value may be carried out by adding hydrogen bromide (HBr) in a mixed atmosphere of argon and oxygen (Ar/O_2), instead of nitrogen and oxygen (N_2/O_2), while patterning an organic dielectric layer (ODL). In this embodiment, the critical dimension (CD) of ODL layer may increase by reducing the oxygen (O_2) flow rate.

[0022]

According to an alternative embodiment of the present invention, a desired

pattern with a predetermined critical dimension (CD) value may be achieved while patterning a silicon-contained anti reflective coating (Si-ARC) layer. In this embodiment, the line-width or the critical dimension of the Si-ARC layer may increase or decrease by adjusting a ratio of tetrafluoromethane to trifluoromethane (CF_4/CHF_3) gas.

[0023]

According to yet another embodiment, a desired pattern with a predetermined critical dimension (CD) value may be carried out by adjusting a level of an RF bias power source. In this embodiment, the critical dimension (CD) value is proportional to the applied RF bias level (power). This means the higher the RF bias level is, the thicker is the critical dimension (CD) value. Conversely, a lower RF bias level provides a thinner critical dimension (CD) value.

[0024]

The parameters to be adjusted in the above-mentioned embodiments, such as, for example, the hydrogen bromide (HBr) flow rate in the ODL patterning step, the (CF_4/CHF_3) ratio in the Si-ARC patterning step, and the RF bias level, are determined based on measuring the critical dimension (CD) of a resist pattern or any mask pattern.

[0025]

According to one embodiment, the measured value of the resist pattern in a semiconductor substrate after developing process is used to determine the appropriate setting conditions for performing the following etching step of layers such as, for example, the organic dielectric layer (ODL) or the silicon-contained anti reflective coating (Si-ARC) layer in the same semiconductor substrate.

[0026]

According to another embodiment, the measured value of the resist pattern or the etched pattern of the organic dielectric layer (ODL) or the silicon-contained anti reflective coating (Si-ARC) layer in one semiconductor substrate are used to determine the appropriate setting conditions for performing the etching step in another semiconductor substrate.

[0027]

According to yet another embodiment, the measured value of the etched pattern of the organic dielectric layer (ODL) or the silicon-contained anti reflective coating (Si-ARC) layer in a semiconductor substrate are used to determine the appropriate setting conditions while performing the etching step in the same semiconductor substrate.

[0028]

Referring first to **Fig. 1**, an embodiment of a target structure 10 before and after performing a plasma etching process is shown. As shown in this figure, the target structure 10 may include a silicon (Si) substrate 12, a hard mask silicon nitride (SiN) layer 14, and a tri-layer structure 16. The tri-layer structure 16 includes an organic dielectric layer (ODL) 16a, a silicon-contained anti reflective coating (Si-ARC) layer 16b, and a resist pattern 16c. To control precisely a final silicon (Si) pattern, a hard-mask pattern of the SiN layer 14 should be formed accurately on the Si substrate 12. In order to realize desired shape (CD value or line-width included) of the hard-mask pattern of the SiN layer 14, the hard-mask pattern of the SiN layer 14 can be etched using the tri-layer structure 16 (16a, 16b

and 16c). More specifically, after forming the desired resist pattern 16c, subsequent etching processes will be performed, respectively, for the Si-ARC layer 16b, the ODL layer 16a, and the hard mask silicon nitride (SiN) layer 14, to finally transfer the whole pattern into the silicon (Si) substrate 12 by etching the Si substrate 12 through the pattern of SiN layer 14 as a hard mask. The final silicon (Si) substrate pattern 12 with some remaining residual SiN pattern 14 is also shown in Fig. 1.

[0029]

As described previously, the line-width or critical dimension (CD) of the resist pattern 16c may not meet a desired target value, due to existence of unwanted factors such as, for example, the condition of the substrate surface, atmospheric pressure, and fluctuations in temperature and relative humidity. Therefore, the subsequent etching processes may not provide the desired target pattern of Si-ARC, ODL, SiN and the silicon (Si) substrate 12. To evaluate the above-mentioned point, an experimental sample is first manufactured, based on an alternative target structure. The experimental sample is then subjected to a conventional plasma etching process. In the following, the alternative target structure with its desired target pattern, after performing the plasma etching process, is described in detail.

[0030]

Referring next to Fig. 2, an alternative embodiment of a target structure 20 used for performing a plasma etching process is shown. The target structure 20 is different from the target structure 10 in that an additional silicon dioxide (SiO_2) layer 22 is interposed between the silicon substrate layer 12 and the hard mask silicon nitride (SiN) layer 14. Similar to the target structure 10, a tri-layer structure 16 is formed over the hard mask silicon nitride (SiN) layer 14. In this

embodiment, the desired critical dimension (CD) for the resist pattern 16c is set to be about 40-45nm. It will be appreciated that such a specific example is shown for illustrative purposes and is not intended to be limiting. The desired target pattern, after performing the plasma etching process, is also shown schematically in Fig. 2.

[0031]

A cross-sectional view of the experimental sample after patterning the silicon nitride (SiN) layer 14 is shown in Fig. 2. As shown in this figure, the critical dimension (CD) of the silicon nitride pattern is about 33.4nm, which is about 7nm thinner compared to the desired critical dimension (40-45nm). The measured distance between patterns is about 65.7nm while the measured pattern height is about 49.9nm.

[0032]

In the conventional plasma etching process, most mask material is etched somewhat isotropically. That means the etching proceeds somewhat horizontally as well. Therefore, when the plasma etching process is applied to layer such as, for example, the organic dielectric layer (ODL) 16a, a side etching occurs simultaneously with a vertical etching of the ODL 16a. As a result, a cross-sectional shape of the mask pattern of the ODL 16a becomes far from a desired rectangular shape, instead becomes a tapered skirt shape, for example. Then, the SiN layer 14 etched through the ODL mask will not become a target shape as designed. Ideally, a directional etching with no etching in the horizontal direction is preferred. However, in practice, anisotropic etching with a smaller etching rate in horizontal direction is desirable.

[0033]

As a countermeasure against the lateral etching of the ODL layer 16a and also to control the critical dimension (CD) of the pattern of the SiN layer 14, the present invention provides a plasma over etching (OE) process in which certain amount of hydrogen bromide (HBr) is added into the mixed atmosphere of nitrogen and oxygen (N_2/O_2) while patterning the organic dielectric layer (ODL) 16a. Various processing conditions with regards to the addition of hydrogen bromide (HBr) gas are investigated. These investigations are mainly performed to ascertain the ODL side wall protection mechanism and also to establish a process for controlling critical dimension (CD) while etching. Example of those processing conditions may include the HBr flow rate, the etching time, the etching gas type, bias power applied to the substrate and their composition ratio.

[0034]

On the other hand, several control methods may be used, during the plasma etching process of the present invention, to provide a high-resolution (accurate) pattern with a predetermined critical dimension (CD) on the silicon (Si) substrate 12. Example of those control methods may include a feed-forward control process, a feed-back control process, and a dynamic (in-situ) control process. In the following, each of the above-mentioned control processes will be explained individually in detail.

[0035]

In one embodiment, a feed-forward process control is used for obtaining a pattern with a predetermined critical dimension (CD). In this embodiment, the line-width or the critical dimension (CD) of the resist pattern 16c is first measured

using any commercialized device. An integrated metrology (IM) device with optical measurement, e.g., scatterometory can be adopted. As will be described further below, in some embodiments, the line-width (CD) measurement device is integrated into a coater developer where latent or developed CD value of the photo resist after exposure is measured before the substrate is transferred to an etching device for subsequent etching process. In other embodiments, the CD measurement can be carried out in an IM device combined with the etching device where CD measurement is carried out right before the start of actual etching process. In alternative embodiments, the CD measurement may be conducted by a standalone measurement system instead of IM tool. The detail description of the line-width or CD measurement device will be described further below. After measuring the line-width or the critical dimension (CD) of the resist pattern 16c, a determination is made as to whether the critical dimension (CD) of the resist pattern 16c meets its desired target value. In the case where the critical dimension (CD) of the resist pattern 16c does not meet its desired target value, appropriate setting conditions with regards to a flow rate and type of plasma etching gas are first determined. The setting conditions are then adjusted, in the same semiconductor substrate, for the subsequent etching process of the Si-ARC layer 16b or the ODL layer 16a.

[0036]

In an alternative embodiment, a feed-back process control is used for obtaining a pattern with a predetermined critical dimension (CD). In this alternative embodiment, the line-width or the critical dimension (CD) of the Si-ARC pattern 16b or the ODL layer 16a is first examined. A determination is made as to whether the critical dimension (CD) of the ODL pattern 16a (Si-ARC pattern 16b)

meets its desired target value. In the case where the critical dimension (CD) of the ODL pattern 16a (Si-ARC pattern 16b) does not meet its desired target value, appropriate setting conditions with regards to a flow rate and type of plasma etching gas are determined. The setting conditions are sent to the etching device then adjusted for another semiconductor substrate to provide a predetermined critical dimension (CD) of mask patterns such as the SiN hard mask pattern 14, the ODL pattern 16a, the Si-ARC pattern 16b and the resist pattern 16c, on the silicon (Si) substrate 12.

[0037]

In yet another alternative embodiment, a dynamic process control (in-situ) can be used for obtaining a pattern with a predetermined critical dimension (CD). In this embodiment, the line-width or the critical dimension (CD) of the ODL pattern 16a or the SiN hard mask pattern 14 is first measured during the etching process and the appropriate setting conditions with regard to a flow rate and type of plasma etching gas are adjusted dynamically during the plasma etching process of the ODL layer 16a or the SiN layer 14. In the following, an etching device and a line-width or CD measurement device will be explained individually in detail.

[0038]

Etching device:

Fig. 3 illustrates a schematic diagram of an embodiment of a plasma processing device 30. As shown in this figure, the plasma processing device 30 includes a process vessel 120, a radial line slot plate 300, a substrate holder 140, and a dielectric window 160. The process vessel 120 may include a bottom portion 17, located beneath substrate holder 140 and cylindrical sidewall 18, which extend

upwardly from the circumference of the bottom portion 17. An upper side of the process vessel 120 is open-ended. The dielectric window 160 is placed opposite to the substrate holder 140 and is sealed to the upper side of the process vessel 120 via O rings 20. The plasma processing device 30 further includes a controller, not shown in this figure, to control the processing conditions and overall operation of the device 30.

[0039]

An external microwave generator 15 provides a microwave power of a predetermined frequency, e.g., 2.45 GHz, to the radial line slot plate 300 via a coaxial waveguide 24 and a slow-wave plate 28. The coaxial waveguide 24 may include a central conductor 25 and a circumferential conductor 26. The microwave power is then transmitted to the dielectric window 160 through a plurality of slots 29 provided on the radial line slot plate 300. The microwave from the microwave generator 15 generates an electric field just below the dielectric window 160, which in turn causes excitation of a plasma gas, e.g., nitrogen (N_2) gas or argon (Ar) gas, within the process vessel 120. A concave part 27, provided on an inner side of the dielectric window 160, enables an effective plasma generation inside the process vessel 120.

[0040]

An external high-frequency power supply source 37 is electrically connected to the substrate holder 140 via a matching unit 38 and an electric power supply pole 39. The high-frequency power supply source 37 generates an RF bias power of a predetermined frequency, e.g., 13.56 MHz, for controlling ions energy that are drawn to a substrate. The matching unit 38 matches an impedance of the RF power

supply source 37 to an impedance of the load, e.g., the process vessel 120. An electrostatic chuck 41 is provided on an upper surface of the substrate holder 140 for holding the substrate by an electrostatic absorption power, via a DC power supply source 46.

[0041]

The plasma processing device 30 further includes a reaction gas supply part 13. An enlarged view of the reaction gas supply part 13 is also shown in Fig. 3. As shown in this figure, the reaction gas supply part 13 may include a base injector 61 located at a backward position, inside the dielectric window 160, compared to a lower surface 63 of the dielectric window 160. The reaction gas supply part 13 further includes a base holder 64 which penetrates through the dielectric window 160 in a thickness direction to hold the injector base 61. A plan view of the injector base 61 is also shown in Fig. 3. As shown in this figure, a plurality of supply holes 66 are provided on a flat wall surface 67 which is positioned opposite to the substrate holder 140. The plurality of supply holes 66 are positioned radially at a centre of the flat wall surface 67.

[0042]

The reaction gas supply part 13 further includes a gas duct 68. As shown in Fig. 3, the gas duct 68 penetrates, respectively, through a central conductor 25 from the coaxial waveguide 24, the radial line slot plate 300, and the dielectric window 160, to reach the plurality of supply holes 66. A gas supply system 72 is connected to a gas entrance hole 69 formed at an upper end of the central conductor

25. The gas supply system 72 may include an on-off valve 70 and a flow rate controller 71, e.g., a mass flow controller.

[0043]

Further, the reaction gas may be supplied into the process vessel 120 by two more gas ducts 89 provided on cylindrical sidewall 18. It should be noted that the reaction gas is at least any one of a plasma excitation gas and a material gas. By adjusting the flow rate of the reaction gas supplied from the gas ducts 68 and 89, an optimized dissociation of the material gas may be achieved within the process vessel 120.

[0044]

Line-width or CD measurement device:

A line width of the resist pattern 16c, the silicon-contained anti reflective coating (Si-ARC) layer 16b, the organic dielectric layer (ODL) 16a or the silicon nitride (SiN) layer 14 is measured and calculated using the line width measurement device. This device may be any one of a stand-alone type, one that is integrated into a coater developer, which is called an IM (integrated metrology), or one that is integrated into an etching device. When the line width measurement device is built into the coater developer, a latent image of a resist or a line width of a resist after development can be measured immediately after processing. When the line width measurement device is built into the etching device, the line width can be measured before etching and after etching as well. On the other hand, the line-width or CD measurement may be conducted using a standalone measurement system. In what follows, each of the above-mentioned embodiments will be explained individually in

detail.

[0045]

1) Line-width measurement device integrated into a coater developer:

Fig. 4 illustrates a schematic diagram of an embodiment of a line-width measurement device 402-A integrated into an entire structure of a photo resist forming device 40-A. For the sake of convenience, the entire structure of the photo resist forming apparatus 40-A is simplified. As shown in Fig. 4, the entire structure of the photo resist forming apparatus 40-A may include a coater developer 400-A and an exposure apparatus 420. The coater developer 400-A is attached to the exposure apparatus 420, which can be, in turn, connected to the etching device 440.

[0046]

The photo resist forming apparatus 40-A may include a line-width measurement device 402-A, a plurality of processing units (coating units or developing units) 404-A, and two substrate transfer units 406-A. The plurality of processing units 404-A may further include coating units and/or developing units. The substrate transfer units 406-A have a function of carrying substrates between different adjacent parts in the entire structure of the photo resist forming device 40-A. Further, the substrate transfer units 406-A are structured to be movable upward/downward and back/forth and can be rotated around a vertical axis.

[0047]

A line-width or critical dimension (CD) of a resist pattern is measured after performing a developing process. In the next step, appropriate setting conditions such as, for example, a flow rate of the etching gas is calculated based on the measured line-width. Then, the appropriate setting conditions are feed-forwarded

to the etching device 440 from the coater developer 400-A. In some embodiments the measured raw data may be transmitted from the coater developer 400-A to the etching device 440 and processed to obtain appropriate etching conditions. In these embodiments, the appropriate setting conditions are calculated by the measured raw data using a process condition database, not shown in this figure. The process condition database stores various processing conditions in a memory of computer 442.

[0048]

2) Line-width measurement device integrated into the etching device:

With reference to **Fig. 5**, a schematic diagram of an embodiment of an entire structure of a photo resist forming device 40-B is shown. As shown in this figure, the entire structure of the photo resist forming device 40-B is different form the structure of 40-A in that the line-width measurement device 402-B is integrated into the etching device 440-B, instead of being integrated into the coater developer 400. The other components are basically the same as the structure of 40-A. In this embodiment, all three control methods including: 1) the feed-forward control process, 2) the feed-back control process, and 3) the dynamic (in-situ) control process may be used for controlling the substrate pattern.

[0049]

In the feed-forward control process, after transferring a developed substrate into the etching device 440-B, a line-width of the resist pattern is measured by the line-width measurement device 402-B in the etching device 440-B and appropriate setting conditions such as, for example, a flow rate of the etching gas is calculated based on the measured line-width. Then, the appropriate setting conditions are

adjusted in the etching device 440-B for the etching process.

[0050]

In the feed-back control process, a line-width of an etched pattern is measured by the line-width measurement device 402-B and appropriate setting conditions such as, for example, a flow rate of the etching gas is calculated based on the measured line-width. Therefore, the etching process for another substrate can be optimized by performing the etching process under the appropriate setting conditions.

[0051]

In the dynamic (in-situ) control process, a line-width of an etched pattern is measured by the line-width measurement device 402-B and appropriate setting conditions such as, for example, a flow rate of the etching gas is adjusted dynamically during the etching process. It should be understood that in all the above-mentioned control process, the appropriate setting conditions are calculated by the measured raw data using a process condition database, not shown in Fig. 5, which stores various processing conditions in a memory of computer 442-B.

[0052]

According to one aspect of the present invention, a multilayer structure may need to be etched consecutively. In this embodiment, a line-width of a first patterned layer is first measured. Then, appropriate etching conditions are set for a second layer which is formed beneath the first layer. In the next step, the second layer is etched using the optimized etching conditions. Thereafter, a line-width of the second etched layer is measured, and then appropriate etching conditions are set for a third layer. This process may continue for the number of layer in the

multilayer structure. In this way, the line-width (CD value) of the final etched pattern is closer to the desired target value. The measurement of the line-width (CD value) may be performed by either an IM module equipped outside a chamber or a line width measurement device equipped in the chamber. With this line width measurement device equipped with etch chamber, the CD can be measured after main etching (ME) process and preferred etching conditions for over etching (OE) process can be adjusted to control CD precisely.

[0053]

As an example, the target structure 10 as shown in Fig. 1 may be considered as the multilayer structure. To perform the etching process of each layer according to the process described in paragraph [0052], the following process may be understood with reference to the structure of (**Fig. 6**): First, a CD deviation value per unit time (ΔCD) is obtained for a plurality of HBr/O_2 ratios (conditions) (shown in Fig.12) and stored as a table. Second, a line-width of the Si-ARC layer 16b (CDs) is measured. In the third step, the difference between the measured Si-ARC line-width (CDs) and the line-width target value (CDt) is calculated (CDt-CDs). At last, an optimized flow rate of HBr/O_2 ratio is obtained based on the difference (CDt-CDs) and a time period for over etching (OE) of ODL layer (T), which is obtained in advance for the ODL etching process. The etching is then performed under the optimized HBr/O_2 flow rate. In this way, the final ODL pattern 16a is obtained in a shape close to the target line-width (CDt). Note that in a case where the Si-ARC layer 16b is etched using the photo resist mask 16c, a flow rate of CF_4/CHF_3 is optimized according to the above-mentioned process and the etching is performed under the optimized CF_4/CHF_3 flow rate. CD value can also be adjusted

by etching time with a certain etching conditions (e.g. etching gas flow rate). Further, CD value can be changed by adjusting both flow ratio (flow arte) of the etching gases and etching time.

[0054]

When the difference between the target CDt value and the measured line width of a resist pattern on the Si-ARC layer 16b exceeds a predetermined threshold amount (that is trim capability), flow rate ratios (HBr/O2 and CF4/CHF3 ratios in this specific example) may be optimized in order to obtain the target CDt value when completing both Si-ARC and ODL layers. The predetermined threshold amount may be obtained when one skilled in the art estimates that the target value cannot be reached by the end of the Si-ARC etching process comparing measured resist CD and the target CD value before initiating etching. In this way, the target value for the line-width may be reached when the etching process of two consecutive layers of Si-ARC and ODL are finished. In this embodiment, the flow rate of HBr/O2 and CF4/CHF3 ratios are determined by taking into account various parameters such as, the etching time and the etching shape of each respective layer. In this embodiment, the target value of Si-ARC line-width and the target value of ODL line-width are provided beforehand.

[0055]

3) Stand-alone line-width measurement device

Fig. 7 illustrates a schematic diagram of an embodiment of a stand-alone line-width measurement device 402-C of an entire structure of a photo resist forming device 40-C. As shown in this figure, the entire structure of the photo resist forming device 40-C is different from the structure of 40-A and 40-B in that the

line-width measurement device 402-C is not integrated into any device and functions as a stand-alone measurement device. The other components are basically the same as the structure of 40-A. In this embodiment, a substrate container (generally called FOUP), not shown in Fig. 7, is used. Each substrate may be transported to the container after the developing process or after the etching process and transferred to the line width measurement device 402-C using for example, an automated guided vehicle (AGV). In each substrate, a line-width of each substrate is first measured and then appropriate setting conditions are calculated. The measured CD value and the appropriate setting conditions are transmitted to the etching device 440.

[0056]

Experimental samples:

In order to evaluate the effect of hydrogen bromide (HBr) on side wall protection mechanism and also to establish a process for controlling critical dimension (CD), several experimental samples are manufactured with the same target structure as the one described in Fig. 1 or Fig. 2. The experimental samples are then subjected to the plasma etching process according to the present invention in which appropriate amount of hydrogen bromide (HBr) is added into the mixed atmosphere of nitrogen and oxygen (N_2/O_2) during the over etching (OE) step of organic dielectric layer (ODL). In the following the results of these evaluations will be explained in detail.

[0057]

With reference to Fig. 8, cross-sectional view of two experimental samples are shown after performing the plasma etching process at each specific layer of their

target structure. The first experimental sample features a dense or nested array pattern while the second experimental sample represents an isolated pattern. Cross-sectional views of both patterns are shown respectively on the upper and lower side of the Fig. 8. As shown in this figure, the cross-sectional views are taken after performing the etching step for each mask layer. For both experimental samples, columns 1-5 of these cross-sectional views correspond respectively to resist pattern, Si-ARC pattern, ODL main etching (ME) pattern, ODL over etching (OE) pattern, and the hard mask SiN pattern. Table I summarizes the etching conditions applied to each mask layers.

Table I: Etching conditions used for experimental samples

	Press. (mTorr)	N2 (sccm)	O2 (sccm)	HBr (sccm)	CF4 (sccm)	CHF3 (sccm)	MW (W)	RF (W)	Time (sec)
Si-ARC	100	-	-	-	180	180	2000	300	15
ODL (ME)	10	400	20	-	-	-	3000	200	36
ODL (OE)	10	400	4	60	-	-	3000	200	30
SiN	70	-	-	-	150	170	2000	300	28

[0058]

As shown in Fig. 8, the critical dimension (CD) decreases in the Si-ARC and ODL main etching (ME) step. By adding hydrogen bromide (HBr) into the mixed atmosphere of nitrogen and oxygen (N_2/O_2) during the over etching (OE) step of the ODL layer, the critical dimension of both dense and isolated patterns may increase. As shown in Fig. 8, the critical dimension (CD) of the dense array pattern in the ODL over etching (OE) layer is about 46 nm while the critical dimension (CD) of the isolated pattern is about 115 nm in the same layer. It is thought that this increase

of the critical dimension (CD) is attributed to the deposition of a thin carbon bromide (CBr_x) layer, which functions as a side wall protection against etching.

[0059]

The final critical dimension (CD), after performing the hard mask SiN etching step, is 40nm for the dense pattern and 119 nm for the isolated pattern. A trim capability is a range the critical dimension (CD) of a mask layer thickens or thins after performing an etching step by adjusting gas flow conditions (gas ratio, total flow rate, etc.). Fig. 8 shows that CD value changed both in dense (nested) pattern and in isolated pattern.

[0060]

In what follows the effect of each parameter such as, for example, the HBr flow rate, the time dependency of over etching (OE) step, the etching gas type and composition ratio, on the critical dimension (CD) of the ODL layer is investigated. For this purpose, various experimental samples with dense (nested) and isolated patterns are formed under different etching conditions. Unless described otherwise below, the following etching conditions are used to pattern the ODL layers of each experimental samples: 1) main etching (ME) conditions; a pressure of 10mTorr, a N_2/O_2 flow rate of 400sccm/20sccm, a microwave power of 3kW, an RF power of 200W, and main etching (ME) period of 40 seconds, and 2) over etching (OE) conditions: a pressure of 10mTorr, a N_2/O_2 flow rate of 400sccm/4sccm, a microwave power of 3kW, and an RF power of 200W.

[0061]

To evaluate the dependency of critical dimension (CD) on the over etching time period, two set of experimental samples are manufactured. In each set, three

experimental samples with the same mask pattern are formed. Similar to the previous case, the first set of experimental samples features a dense array pattern while the second set of experimental samples represents an isolated pattern. The main etching (ME) and over etching (OE) of the ODL layer is performed in the plasma processing device 30. The main etching (ME) and over etching (OE) conditions used for patterning the ODL layer are the same as those described in paragraph [0060]. For this evaluation, the HBr flow rate is set to 60sccm. Further, in each set, three experimental samples are patterned under the following over etching (OE) time treatment: 0, 20, and 40 seconds.

[0062]

Fig. 9 represents the cross-sectional views of experimental samples and their critical dimension (CD) as a function of over etching (OE) time treatment. As shown in this figure, the critical dimension (CD) can be made thicker by extending the over etching (OE) time treatment. It is thought that this is mainly due to the fact that the extension of over etching (OE) time period, increases the deposition of the reactive by product, e.g., carbon bromide (CBr_x), over the ODL pattern.

[0063]

Referring next to Fig. 10, cross-sectional views of experimental samples and their critical dimension (CD) as a function of HBr flow rate are shown. Similar to the previous embodiment, two set of experimental samples, each having three samples with similar patterns, are formed. The first set of experimental samples features a dense (nested) array pattern while the second set of experimental samples represents an isolated pattern. The main etching (ME) and over etching (OE) of the ODL layer is performed in the plasma processing device 30. The main etching (ME)

and over etching (OE) conditions used for patterning the ODL layer are the same as those described in paragraph [0060]. For this evaluation, the over etching (OE) time treatment condition is all set to 20 seconds. Further, each of the three experimental samples of each set are, respectively, patterned under the following HBr flow rate condition: 0sccm, 60sccm, and 120sccm.

[0064]

As shown in Fig. 10, the critical dimension (CD) increases with the increase in the HBr flow rate. The mechanism used to control the critical dimension (CD) of ODL layer is thought as follows: by adding hydrogen bromide (HBr) into the mixture of nitrogen and oxygen (N_2/O_2), hydrogen (H) reduces oxygen (O) in the surface of the ODL layer. In other words, oxygen (O) atoms are extracted from the ODL. As a result, an organic dielectric layer (ODL) with high carbon content in its surface is created. So carbon-carbon bonds increase, which makes the organic dielectric layer (ODL) more rigid. The rigidness of ODL layer functions as a side wall protection, which results in prevention of etching.

[0065]

On the other hand, it is also thought that the high carbon content of the ODL layer increases bromide-carbon bonds near the surface of the ODL pattern. It can also be said that a thin layer of carbon bromide (CBr_x) deposited over the ODL pattern functions as a side wall protection, which results in prevention of etching. By increasing the hydrogen bromide (HBr) flow rate, the deposition of carbon bromide (CBr_x) increases due to increase of Br species, which leads, in turn, to increase the ODL's critical dimension (CD). On the other hand, by decreasing HBr flow rate, CD thickening becomes smaller. In this way, a better controllability for

obtaining a predetermined value of critical dimension (CD) can be achieved.

[0066]

The critical dimension (CD) of ODL layer may be controlled using other type of etching gas, such as chlorine (Cl_2) gas. To evaluate how another type of etchant gas may affect the controllability of the critical dimension (CD), two set of experimental samples are manufactured. In each set, two experimental samples with the same mask pattern are formed. Similar to the previous embodiments, the first set of experimental samples features a dense array pattern while the second set of experimental samples represents an isolated pattern. In each set, the first and second experimental samples are first subjected to a main etching (ME) step under the same etching conditions as those described in paragraph [0060]. The first experimental sample of each set is then subjected to an over etching (OE) step by adding hydrogen bromide (HBr) gas into the mixture of nitrogen and oxygen (N_2/O_2). However, the second experimental sample of each set is subjected to an over etching step by adding chlorine (Cl_2) into the mixture of nitrogen and oxygen (N_2/O_2). For this evaluation, both HBr and Cl_2 flow rates are set to 60sccm. Further, the over etching (OE) time treatment condition is set to 20 seconds in each experimental set.

[0067]

Fig. 11 illustrates cross-sectional views of experimental samples for various etching gas type. As shown in this figure, the critical dimension (CD) of the ODL layer in the over etching (OE) step, is increased compared to the main etching (ME) step, for both etching gas type (HBr and Cl_2). Although the exact mechanism for controlling the critical dimension (CD) of the ODL layer in the case of chlorine (Cl_2) gas is unknown, the similar results are obtained with regards to the increase of

critical dimension (CD). However, in this embodiment, some other adverse effects are observed. For example, the underlying hard mask silicon nitride (SiN) layer is shaved such that the height of its mask is decreased (tapered shape).

[0068]

In an alternative embodiment, the desired critical dimension (CD) is carried out by adding hydrogen bromide (HBr) into a mixed atmosphere of argon and oxygen (Ar/O_2). In this alternative embodiment, the argon oxygen ($Ar/HBr/O_2$) series are used to perform the ODL main etching (ME) step. Similar to the previous embodiments, two set of experimental samples each having three samples with similar patterns are formed. The first set of experimental samples features a dense array pattern while the second set of experimental samples represents an isolated pattern. More specifically, a small piece of a substrate (cleaved substrate, also called a coupon) having the structure shown in Fig. 1 is used in this experiment. When the Si-ARC and the ODL main etching (ME) are performed, the coupon is attached on a substrate on which a photo resist is totally coated. When the ODL over etching (OE) is performed, the coupon is attached on another substrate on which a silicon nitride (SiN) is totally deposited. The ODL over etching (OE) is performed for 15 seconds. Table II summarizes the etching conditions at Si-ARC and ODL layers.

Table II: Etching conditions used for experimental samples

	Press. (mTorr)	Ar (sccm)	HBr (sccm)	O2 (sccm)	CF4 (sccm)	CHF3 (sccm)	MW (W)	RF (W)	Time (sec)
Si-ARC	100	-	-	-	150	210	2000	300	15
ODL (ME)	10	100	150	50	-	-	1500	200	51

[0069]

After performing the Si-ARC and ODL main (ME) etching steps, an over etching (OE) step is performed using the plasma processing device 30. The over etching (OE) step of the first, second, and third experimental samples of each set are conducted respectively under the following $Ar/HBr/O_2$ flow rate: 100/150 /20, 100/150/10, and 100/150/5 sccm.

[0070]

Referring next to Fig. 12, cross-sectional views of experimental samples and their critical dimension (CD) as a function of HBr/O_2 ratio are shown. As shown in this figure, the critical dimension (CD) of ODL layer increases with the increase in the HBr/O_2 ratio. In other words, the critical dimension (CD) of ODL layer increases when the oxygen (O_2) flow rate decreases.

[0071]

In the conventional plasma etching process, there has been a problem in that after performing the etching step there exist some variation in pattern shape. In order to avoid this variation in pattern shape, a mask for photolithography purposes is designed by taking into account the variation in the dimension of finished etched pattern. However, the above-mentioned problem cannot be fully avoided by this solution.

[0072]

The plasma etching process of the present invention provides a solution for the above-mentioned problem. By adding hydrogen bromide (HBr) into the mixture of N_2/O_2 or Ar/O_2, it is thought that hydrogen (H) reduces oxygen (O) in the surface of the ODL layer. In other words, oxygen (O) atoms are extracted from the ODL layer.

As a result, an organic dielectric layer (ODL) with high carbon content in its surface is created. So carbon-carbon bonds increase, which makes the organic dielectric layer (ODL) more rigid. The rigidness of ODL layer functions as a side wall protection, which results in prevention of etching.

[0073]

In addition, it is also thought that the high carbon content of the ODL layer increases a plurality of bromide-carbon bonds near the surface of the ODL pattern. As a result, a thin layer of carbon bromide (CBr_x) is deposited over the ODL pattern, which functions as a side wall protection. Therefore, the lateral etching direction of ODL layer may be suppressed. Further, by increasing the hydrogen bromide (HBr) flow rate, the deposition of carbon bromide (CBr_x) increases due to increase of Br species, which increases the ODL's critical dimension (CD). On the other hand, by decreasing HBr flow rate, then CD thickening rate becomes smaller. In this way, a better controllability for obtaining a predetermined value of critical dimension (CD) can be achieved by selecting appropriate HBr flow rate.

[0074]

To evaluate the variation of pattern shape and their critical dimension uniformity, two set of experimental samples, each having different patterns (dense, also called "nested", pattern and isolated pattern), are manufactured. In each set, two experimental samples with similar patterns are formed. Table III summarizes the etching conditions used in each mask layers of experimental samples.

Table III: Etching conditions used for experimental samples

	Ar (sccm)	HBr (sccm)	O2 (sccm)	N2 (sccm)	CF4 (sccm)	CHF3 (sccm)	Press. (mTorr)	MW (W)	RF (W)
Si-ARC	-	-	-	-	180	180	100	3000	Ignition
	-	-	-	-	180	180	100	2000	300
ODL (ME)	250	150	40	-	-	-	10	3000	Ignition
	250	150	40	-	-	-	10	2000	250
ODL (OE)		60	4	400	-	-	10	3000	Ignition
		60	4	400	-	-	10	3000	200

[0075]

For this experiment, the etching time in the Si-ARC and ODL main etching (ME) step are set, respectively, to 16 and 40.8 seconds. In the over etching (OE) step, the etching time for one experimental sample is set to 20 seconds while the etching time for other experimental sample is set to 40 seconds.

[0076]

Fig. 13 illustrates cross-sectional views of experimental samples and their critical dimension (CD). For each experimental sample, the cross-sectional views are taken, respectively, along the center and edge of the substrate, which are defined as "Center" and "Edge" on Fig. 13. As shown in this figure, the critical dimension (CD) does not depend on the over etching (OE) time treatment for all experimental samples. In addition, no variation in pattern shape is observed across all samples.

[0077]

Fig. 14 illustrates the microwave power, RF power, and RF voltage of each mask layer as a function of time. The horizontal axis represents process time, the left vertical axis represents microwave power and RF bias power while the right vertical axis represents RF bias voltage. The data of this experiment, shown in Fig. 14, represents an example in which the etching step for a multilayer structure is

performed consecutively in the same process vessel 120 of the plasma processing device 30. It should be noted that the upper microwave power at the beginning of each process step is applied as a δ (delta) function to ignite the plasma generation process.

[0078]

The RF bias voltage (Lower Vpp) is applied to the substrate holder 140 from the plasma processing device 30 (please refer to Fig. 3). As described previously, this RF bias voltage controls ions energy drawn to the substrate. As shown in Fig. 14, the RF bias voltage drops as the etching process proceeds to the next mask layer. Thereby, the energy of the ions contacting the substrate decreases as the etching process moves forward toward the lower mask layers.

[0079]

Further, another problem observed in the conventional plasma etching process that the resist patterns are formed nonuniformly depending on a region where patterns are isolated or dense (nested). In other words, there exist some variations in pattern shape depending upon whether the resist pattern is isolated, also called roughness, or nested, also called fineness. To avoid the variation in shape of roughness and fineness, a mask for photolithography purposes is designed by considering these variations. However, the above-mentioned problem cannot be fully avoided by this solution. It has also been observed that the variation in shape of roughness and fineness occurs when controlling the critical dimension (CD).

[0080]

The variation in shape of roughness and fineness may be avoided while patterning the silicon-contained anti reflective coating (Si-ARC) layer according to

the process of present invention. In this embodiment, the line-width or the critical dimension (CD) of the final pattern, e.g., the hard mask SiN, is controlled through the Si-ARC layer by adjusting a ratio of tetrafluoromethane to trifluoromethane (CF_4/CHF_3) gas. By adjusting the ratio of CF_4/CHF_3 in the Si-ARC etching step, the critical dimension of Si-ARC pattern may be thickened or thinned such that the final critical dimension (CD) may be controlled within a range of about -2nm to +10nm.

[0081]

The Si-ARC pattern is mainly composed of silicon (Si) and carbon (C) atoms. It is thought that the carbon content of the Si-ARC layer helps to generate a plurality of carbon-fluorine bonds on the surface of the Si-ARC layer. Therefore, by adjusting the ratio of CF_4/CHF_3 in the Si-ARC layer, a thin layer of CF_x series film is deposited over the Si-ARC pattern, due to the bond energy difference between CF_4 gas and CHF_3 gas. As a result, the lateral etching direction of Si-ARC layer may be suppressed and the critical dimension (CD) of the Si-ARC pattern may increase, according to the process of present invention, by adjusting the ratio of CF_4/CHF_3 in the Si-ARC etching step.

[0082]

To evaluate the controllability of the critical dimension (CD) through the etching step of Si-ARC layer and also to investigate the variation in shape of roughness and fineness, various experimental samples are manufactured. Similar to the previous embodiments, two experimental samples, each having different patterns (dense pattern and isolated pattern), are formed. Table IV summarizes the etching conditions used in each mask layers of experimental samples. For this experiment, the etching time in the Si-ARC, ODL main etching (ME) step, ODL over

etching (OE) step, SiN, and ashing step are set, respectively, to 17.7, 40.8, 20, and 30 seconds. Further, the ratio of CF_4/CHF_3 is set to 1 (180/180).

Table IV: Etching conditions used for experimental samples

	Ar (sccm)	HBr (sccm)	O2 (sccm)	N2 (sccm)	CF4 (sccm)	CHF3 (sccm)	Press. (mTorr)	MW (W)	RF (W)
Si-ARC	-	-	-	-	180	180	100	3000	Ignition
	-	-	-	-	180	180	100	2000	300
ODL (ME)	250	150	40	-	-	-	10	3000	Ignition
	250	150	40	-	-	-	10	2000	250
ODL (OE)	-	60	4	400	-	-	10	3000	Ignition
	-	60	4	400	-	-	10	3000	200
SiN	-	-	-	-	150	170	70	3000	Ignition
	-	-	-	-	150	170	70	2000	300
Ash	-	-	370	-	-	-	50	3000	Ignition
	-	-	370	-	-	-	50	2000	0

[0083]

With reference to **Figs. 15**, cross-sectional views of experimental samples and their critical dimension (CD) are shown. As shown in Fig. 15, the vertical profiles are very close to 90 degrees across all experimental samples, showing almost no variation in shape of roughness and fineness. In addition, the critical dimension (CD) of Si-ARC patterns show minimal deviation (±0nm to +2nm) from the desired target pattern across all experimental samples. In this experiment, the desired target pattern for both dense and isolated patterns are set respectively to 45nm and 75nm.

[0084]

The controllability of the critical dimension (CD) through the etching step of Si-ARC layer and also the variation in shape of roughness and fineness are also investigated when the ratio CF_4/CHF_3 varies for each experimental sample. Again,

two set of experimental samples, each having different patterns (dense pattern and isolated pattern), are manufactured. In each set, three experimental samples are formed. The etching conditions used in each mask layers of experimental samples are the same as those summarized in Table IV. However, in each set of experimental sample, the ratio of CF_4/CHF_3 is set respectively to (210/150), (180/180), and (150/210) for the first, second, and third experimental samples.

[0085]

Referring next to **Fig. 16**, cross-sectional views of experimental samples and their critical dimension (CD) are shown. As shown in this figure, the vertical profiles are very close to 90 degrees across all experimental samples, showing almost no variation in shape of roughness and fineness. In addition, the critical dimension (CD) of Si-ARC patterns show minimal deviation (-3nm to +12nm) from the initial target pattern across all experimental samples. The maximum deviation across the patterns is +2nm. In this experiment, the initial target pattern for both dense and isolated patterns is set respectively to 45nm and 75nm.

[0086]

While the principles of the disclosure have been described above in connection with specific apparatuses/devices and methods, it is to be clearly understood that this description is made only by way of example and not as limitation on the scope of the invention.

CLAIMS

What is claimed is:

1. A method for processing a substrate to form a desired pattern by an etching process after forming a mask pattern over the substrate, the method comprising the steps of:

forming two layers over the substrate, the two layers comprising a silicon nitride layer and an organic dielectric layer;

measuring a width of the mask pattern or an etched pattern of one of the two layers; and

adjusting a flow rate of any one of HBr and other gases based on the measured width, HBr and the other gases being used in the etching process.

2. The method as recited in claim 1, further comprising a step of etching one of the two layers of the same substrate under the adjusted flow rate based on the measured width of the mask pattern.

3. The method as recited in claim 1, further comprising a step of etching one of the two layers of another substrate under the adjusted flow rate based on the measured width of the mask pattern or the etched pattern.

4. The method as recited in claim 1, further comprising a step of etching one of the two layers of the same substrate under the adjusted flow rate based on the

measured width of the etched pattern, wherein the measuring step and the adjusting step are performed during the etching process.

5. The method as recited in claim 1, wherein the adjusting step comprises increasing a flow rate ratio of HBr to the other gases when the measured width is smaller than a desired width and decreasing the flow rate ratio of HBr to the other gases when the measured width is greater than the desired width.

6. The method as recited in claim 2, wherein the organic dielectric layer is etched in the etching step.

7. The method as recited in claim 6, wherein the adjusting step comprises increasing an etching time when the measured width is smaller than a desired width and decreasing the etching time when the measured width is greater than the desired width.

8. The method as recited in claim 6, wherein the etching step includes a main etching and an over etching following the main etching, and the HBr is used in the over etching.

9. The method as recited in claim 8, wherein the adjusting step comprises increasing an over etching time when the measured width is smaller than a desired width and decreasing the over etching time when the measured width is greater than the desired width.

10. The method as recited in claim 1, wherein the adjusting step comprises increasing a RF bias power applied to the substrate when the measured width is smaller than a desired width and decreasing the RF bias power when the measured width is greater than the desired width.

11. The method as recited in claim 1, wherein the other gases comprises N_2 and O_2.

12. The method as recited in claim 1, wherein the other gases comprises Ar and O_2.

13. A method for processing a substrate to form a desired pattern by an etching process after forming a mask pattern over the substrate, the method comprising the steps of:

forming three layers over the substrate, the three layers comprising a silicon nitride layer, an organic dielectric layer and a silicon-contained anti-reflective coating layer;

measuring a width of the mask pattern or an etched pattern of one of the three layers; and

adjusting a flow rate of any one of CF_4 and CHF_3 based on the measured width, CF_4 and CHF_3 being used in the etching process.

14. The method as recited in claim 13, further comprising a step of etching one of the three layers of the same substrate under the adjusted flow rate based on the measured width of the mask pattern.

15. The method as recited in claim 13, further comprising a step of etching one of the three layers of another substrate under the adjusted flow rate based on the measured width of the mask pattern or the etched pattern.

16. The method as recited in claim 13, further comprising a step of etching one of the three layers of the same substrate under the adjusted flow rate based on the measured width of the etched pattern, wherein the measuring step and the adjusting step are performed during the etching process.

17. The method as recited in claim 13, further comprising a step of etching the silicon-contained anti-reflective coating layer under the adjusted flow rate based on the measured width of the mask pattern.

18. The method as recited in claim 13, wherein the adjusting step comprises increasing a flow rate ratio of CF_4 to CHF_3 when the measured width is greater than a desired width and decreasing the flow rate ratio of CF_4 to CHF_3 when the measured width is smaller than the desired width.

19. The method as recited in claim 13, wherein the adjusting step comprises increasing a RF bias power applied to the substrate when the measured width is

smaller than a desired width and decreasing the RF bias power when the measured width is greater than the desired width.

FIG 1

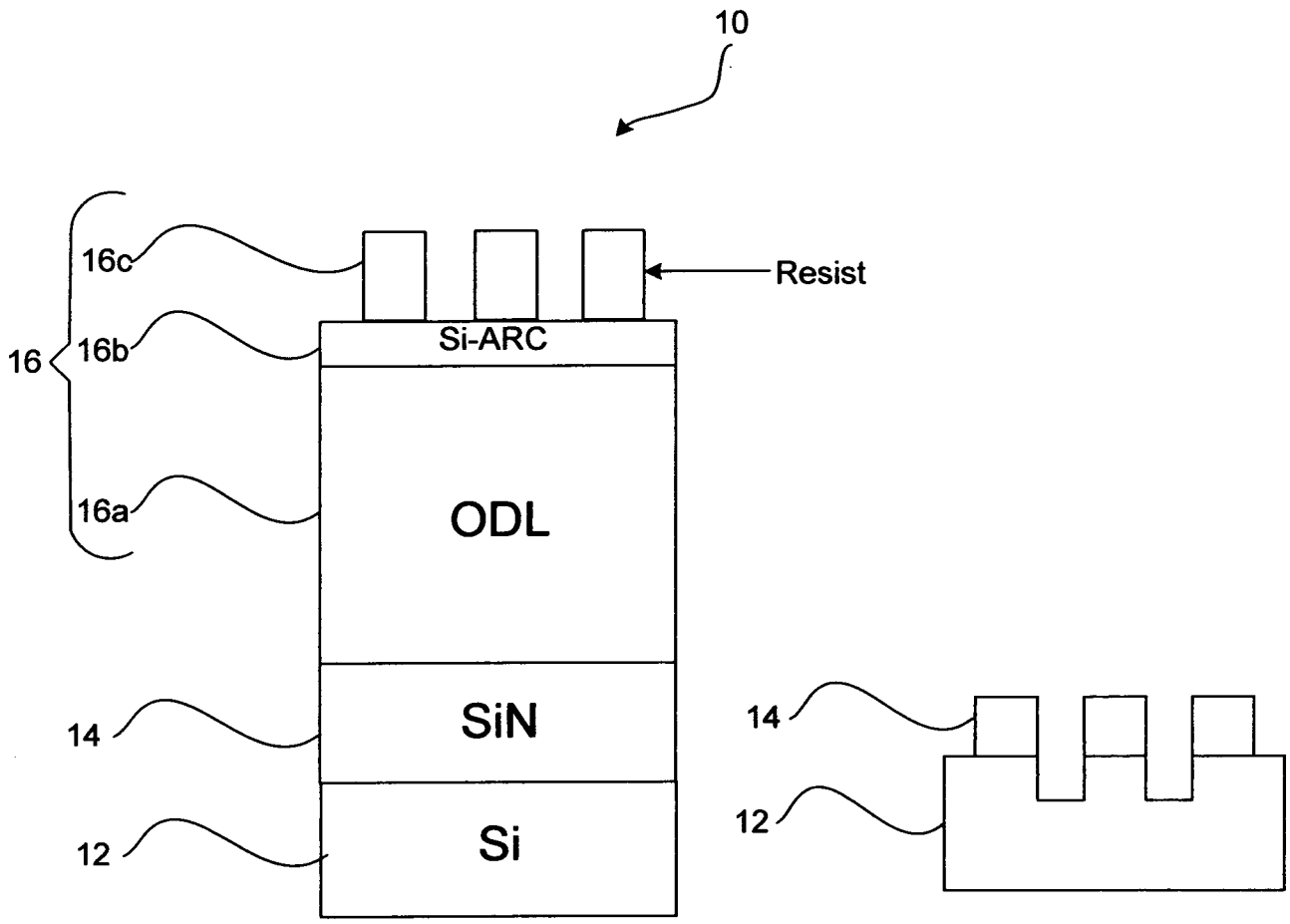


FIG 2

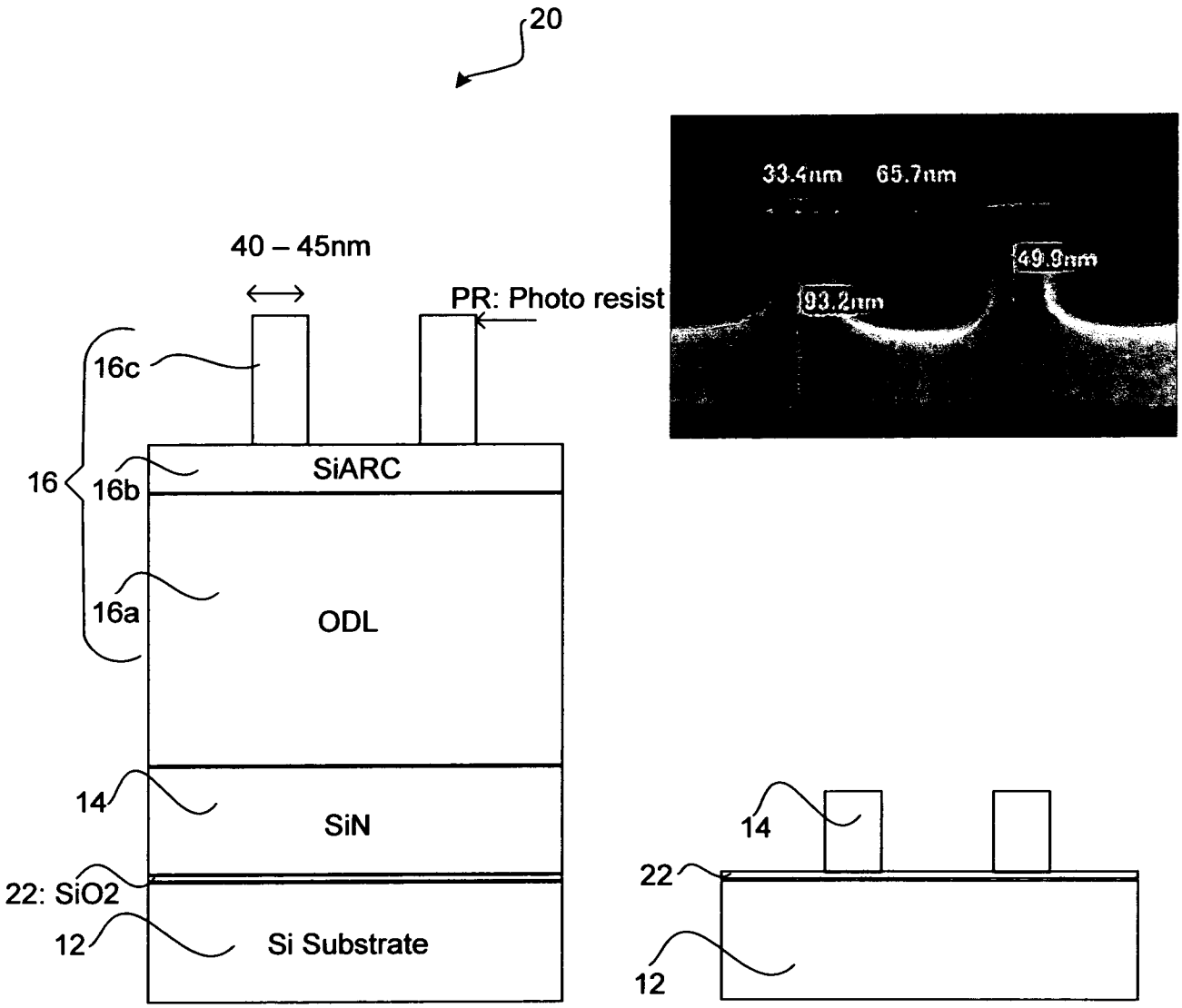
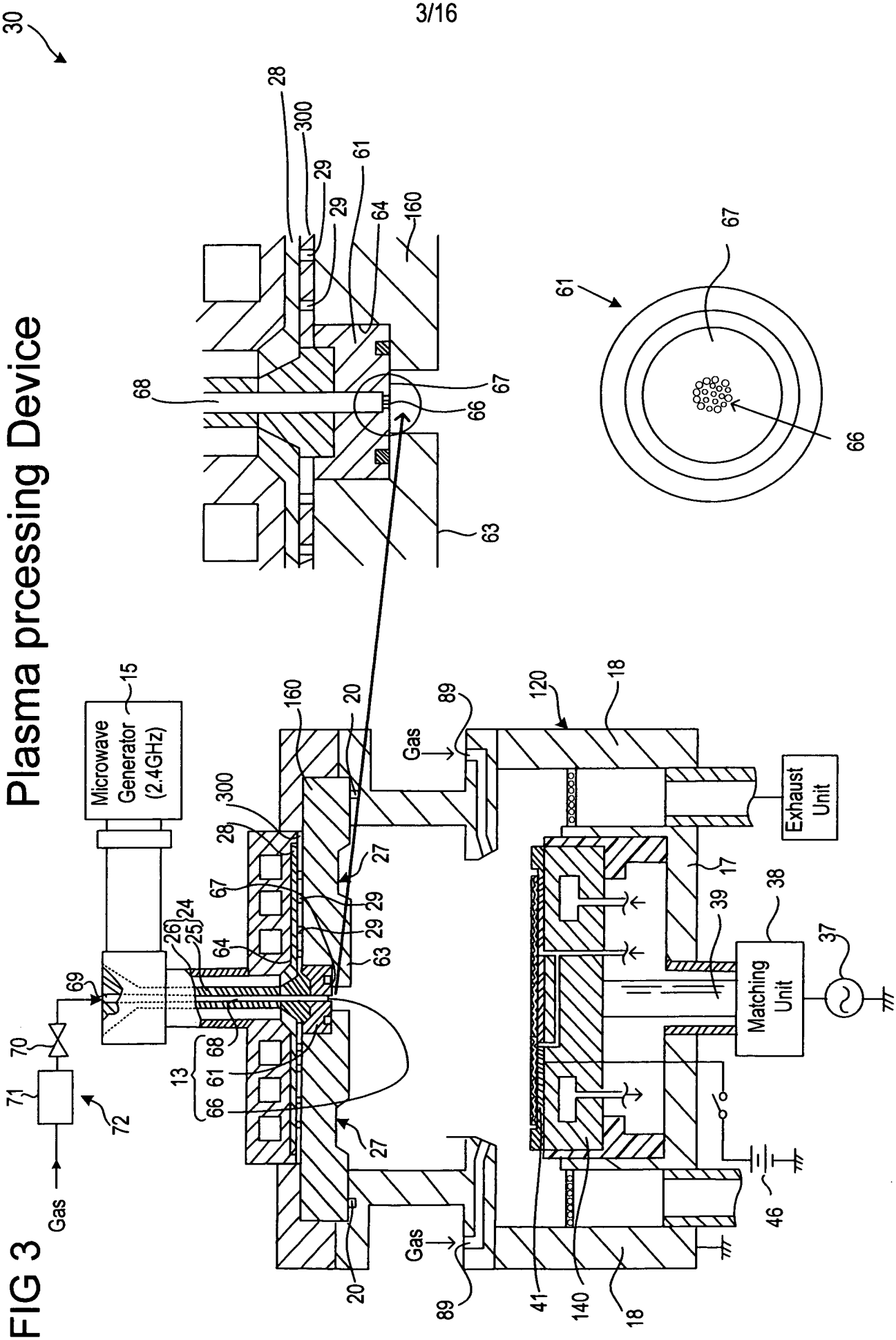

20
33.4nm
65.7nm
49.9nm
93.2nm
40 – 45nm
PR: Photo resist
16c
16
16b
SiARC
16a
ODL
14
SiN
22: SiO2
12
Si Substrate
14
22
12

FIG 3


Plasma prcessing Device
30
Microwave Generator (2.4GHz)
15
Gas
69
70
71
72
13
68
66
61
67
64
63
29
28
300
160
20
27
89
120
18
Exhaust Unit
17
38
39
Matching Unit
37
46
41
140
24
25
26

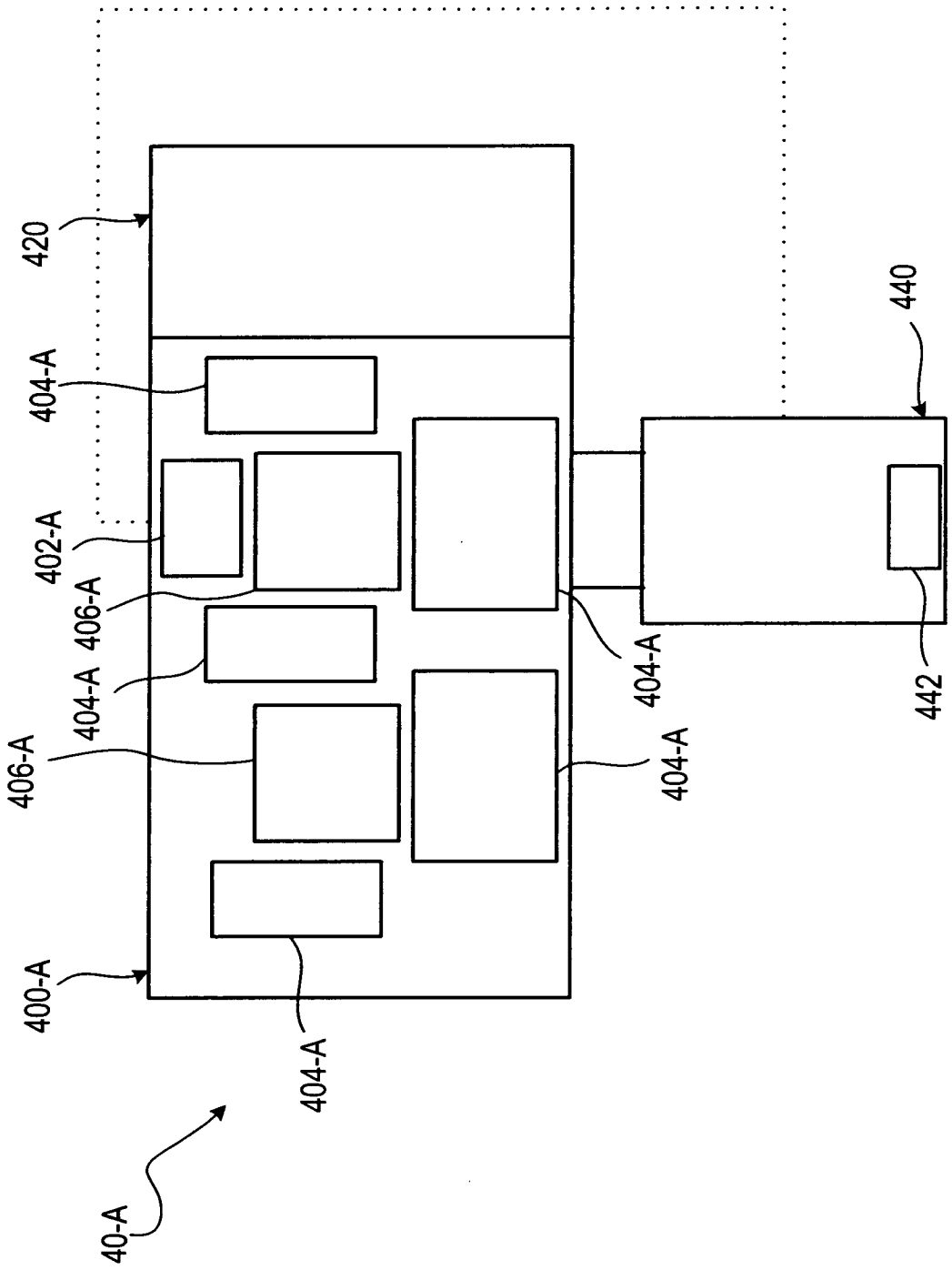


FIG 4

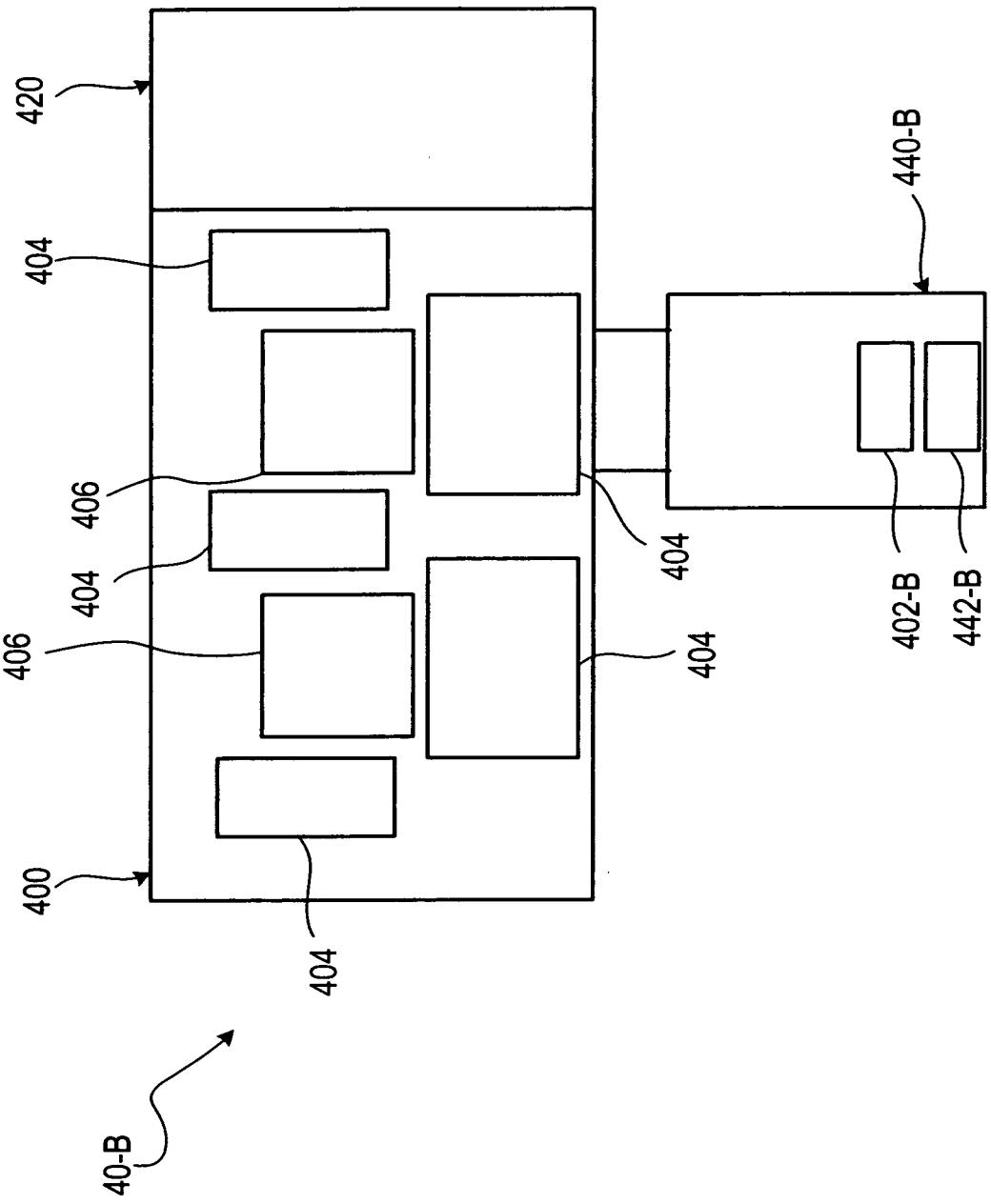
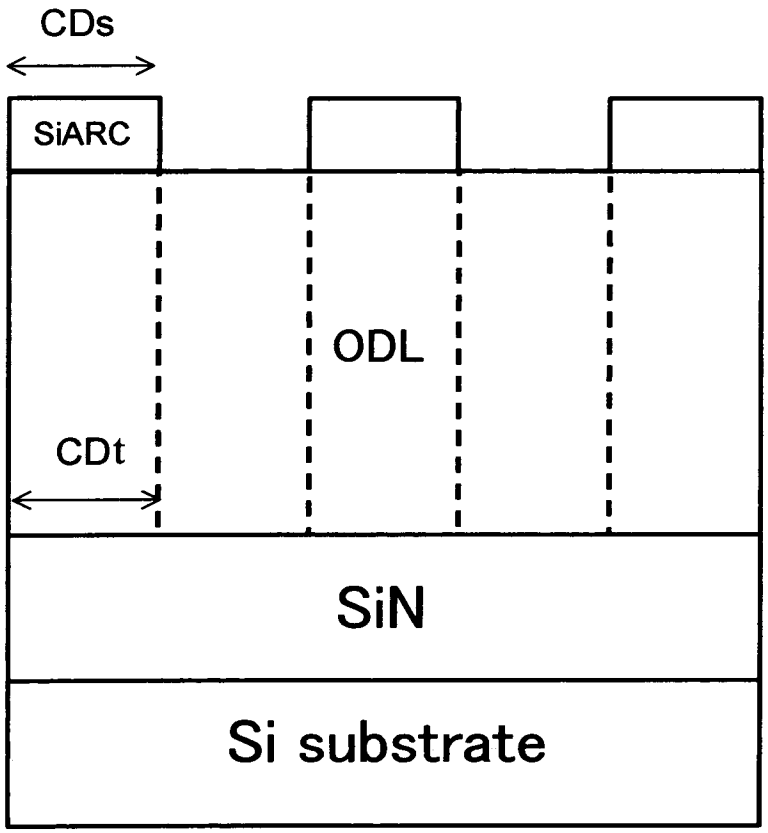


FIG 5

FIG 6



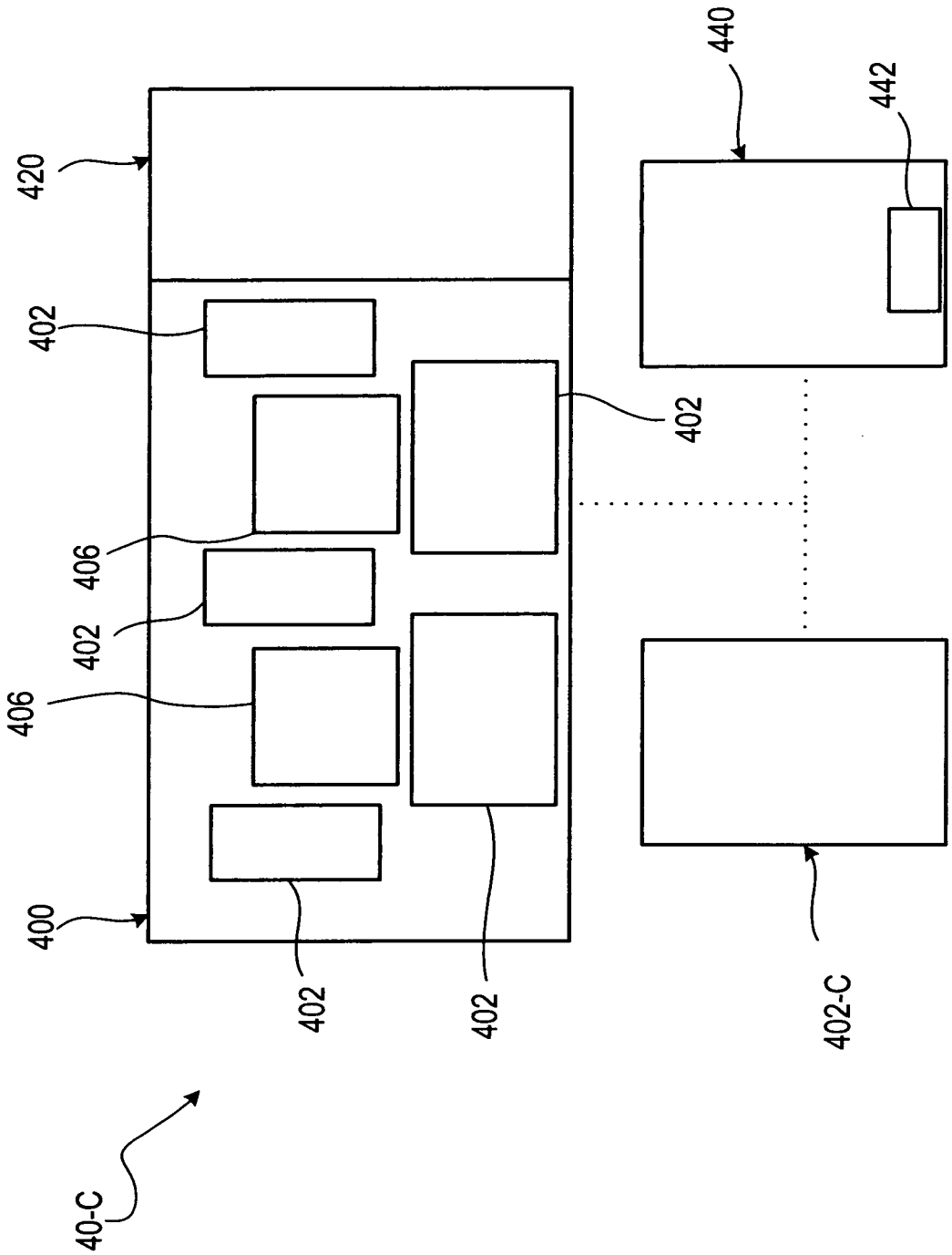


FIG 7

FIG 8

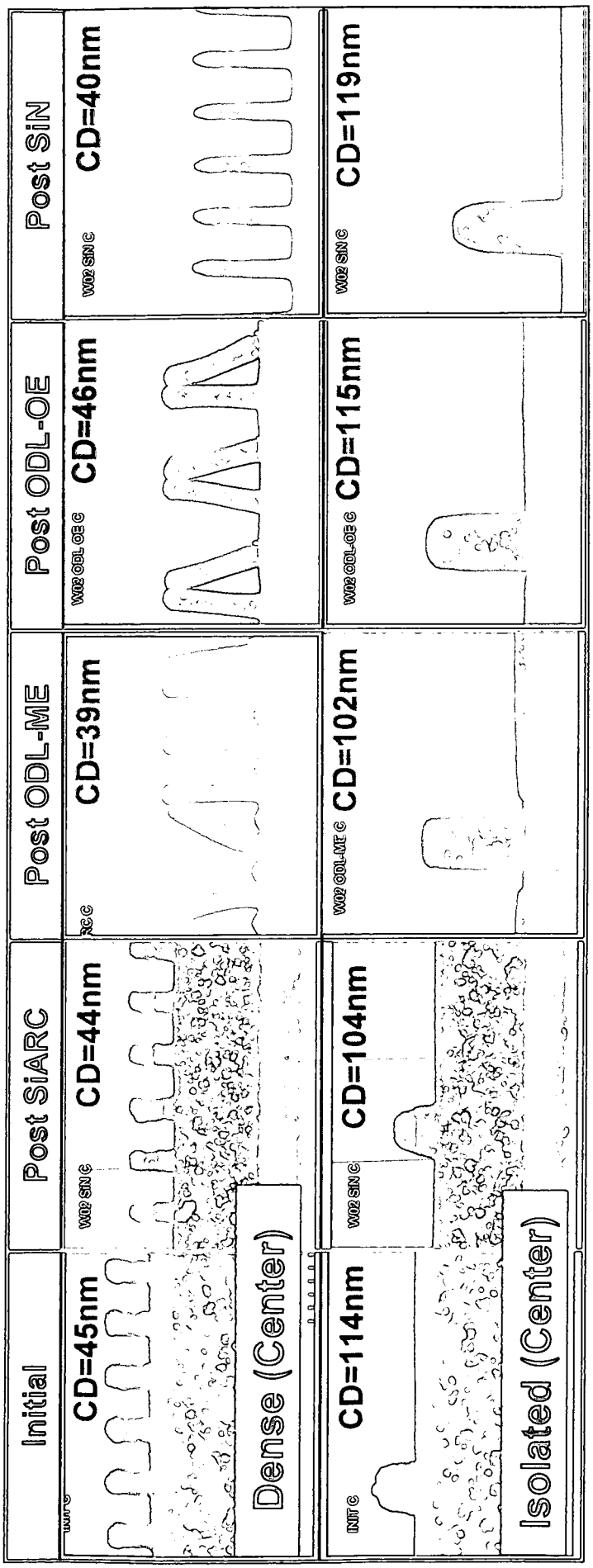

Initial
Post SiARC
Post ODL-ME
Post ODL-OE
Post SiN
CD=45nm
CD=44nm
CD=39nm
CD=46nm
CD=40nm
Dense (Center)
CD=114nm
CD=104nm
CD=102nm
CD=115nm
CD=119nm
Isolated (Center)

FIG 9

ODL-OE Time Dependency

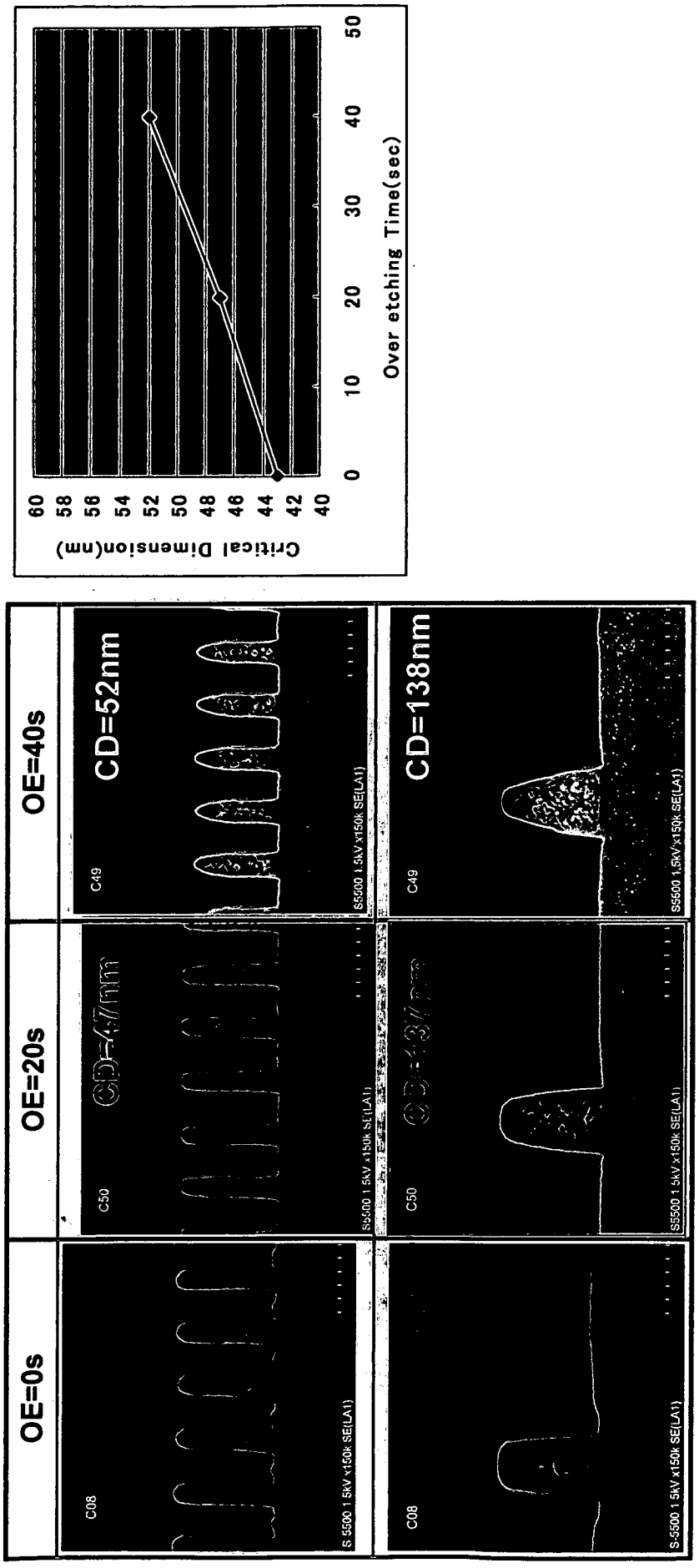
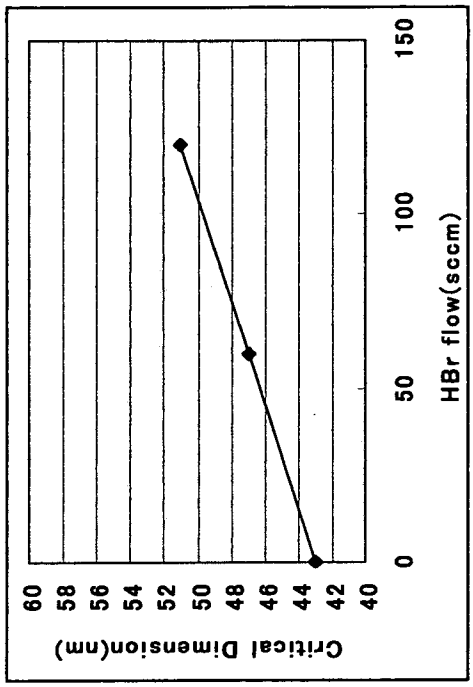


FIG 10

HBr Flow Dependency



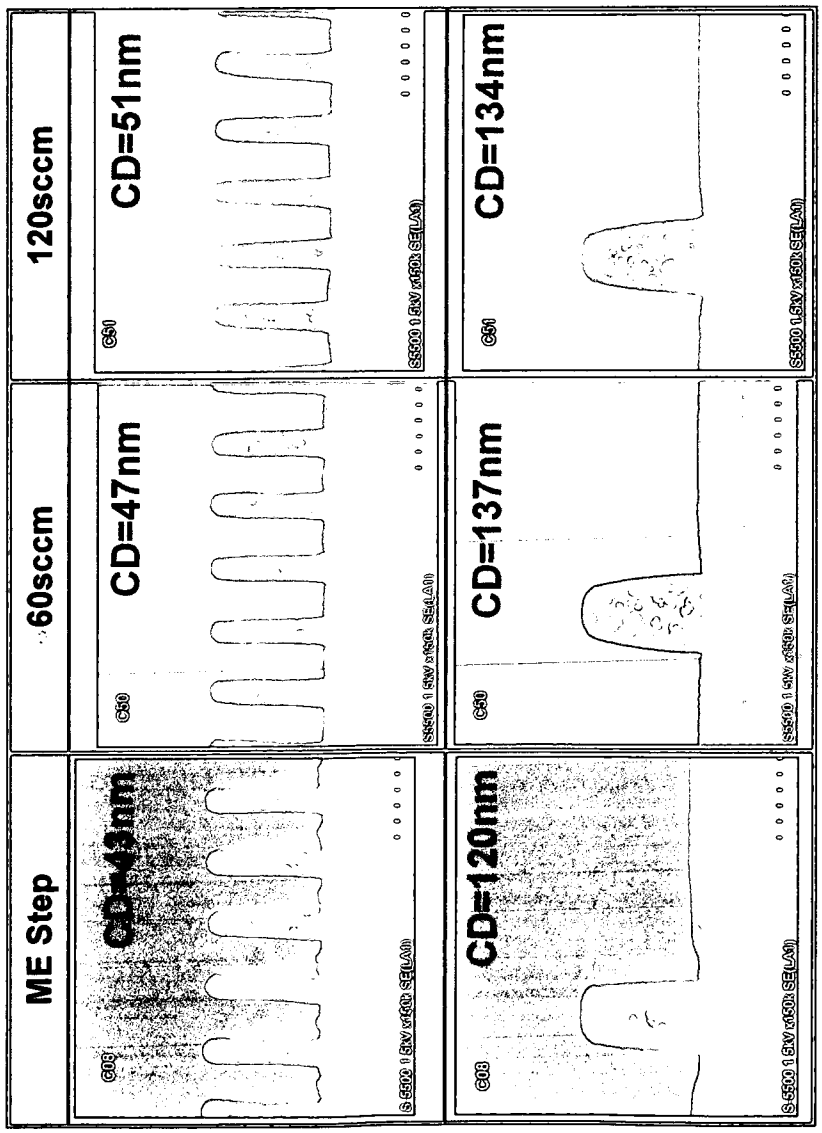


FIG 11

Etching Gas Type

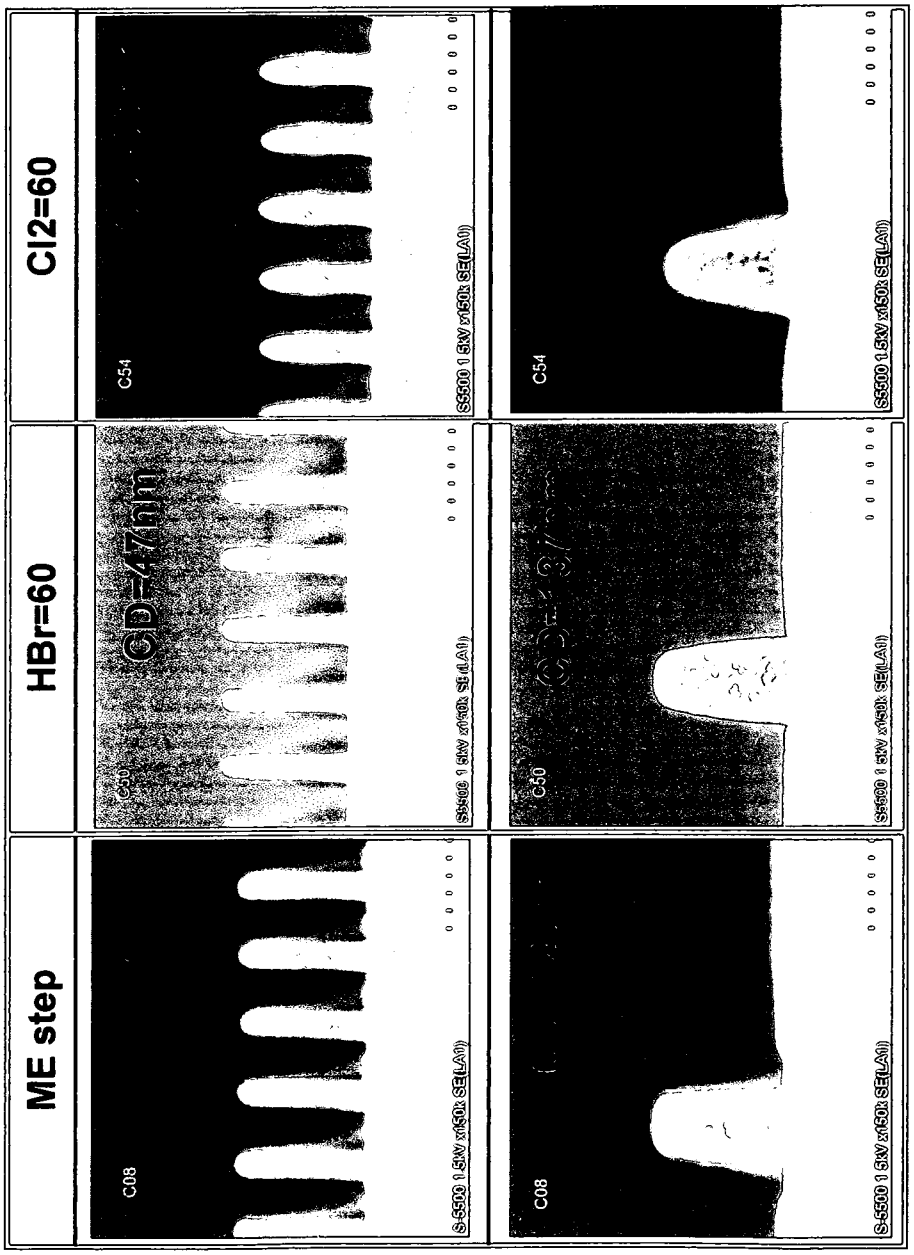


FIG 12

ODL-OE (Ar/HBr/O2 Series)

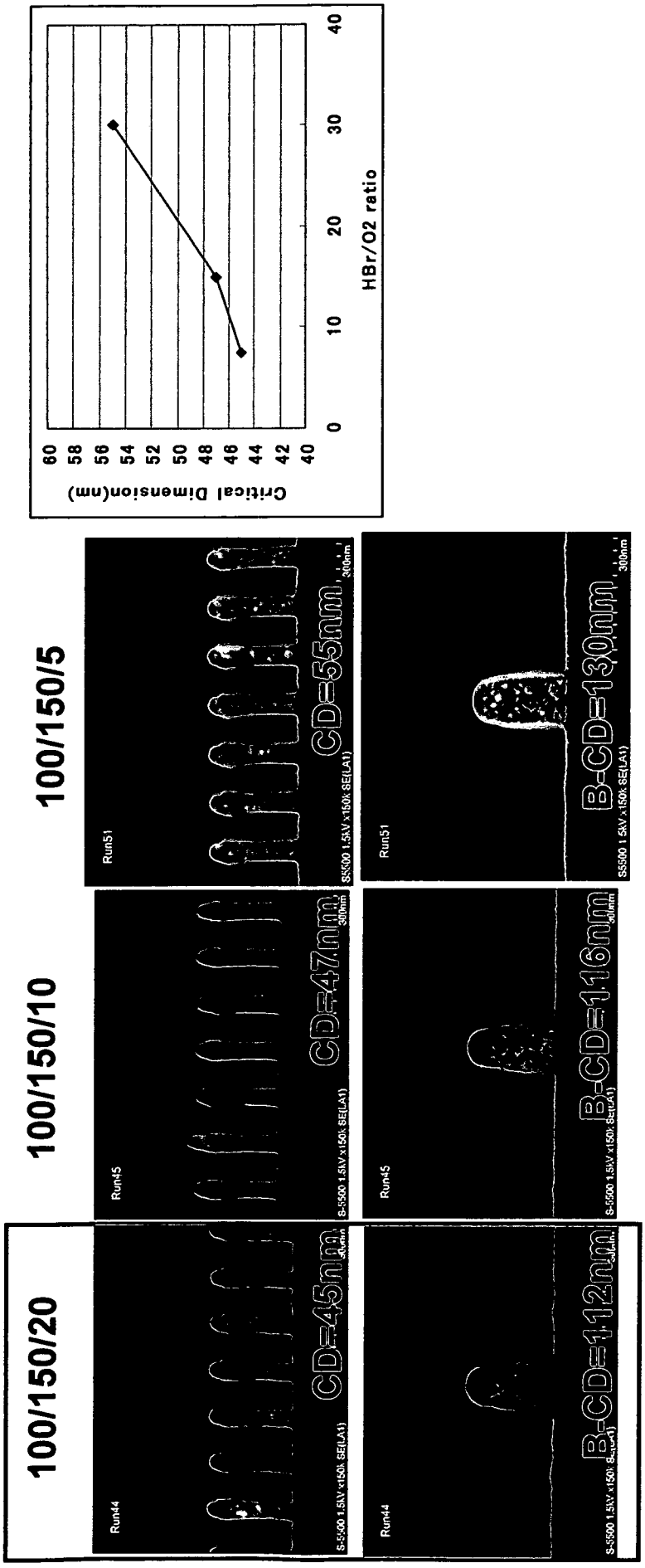


FIG 13

ODL-OE Time Dependent

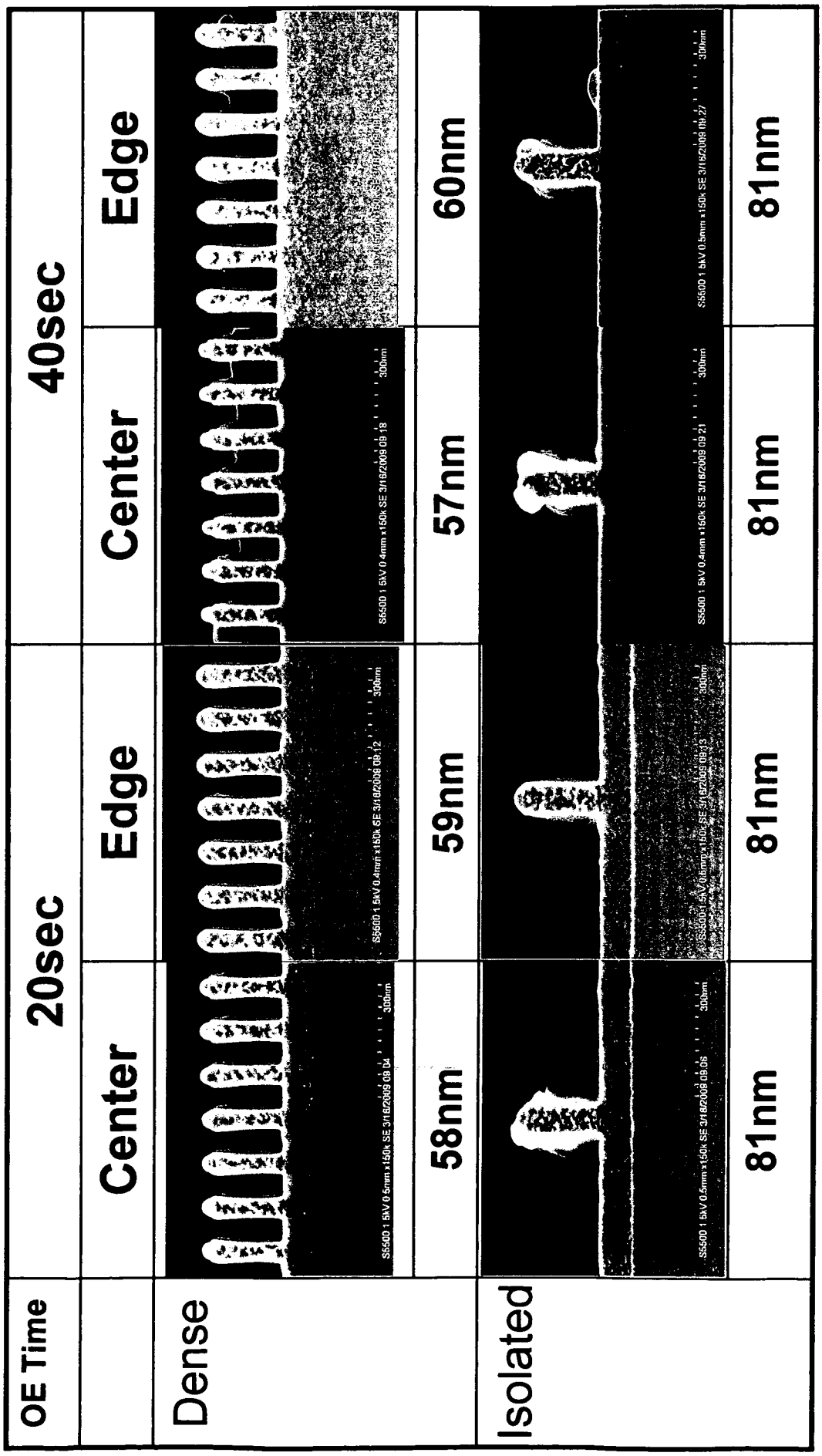


FIG 14

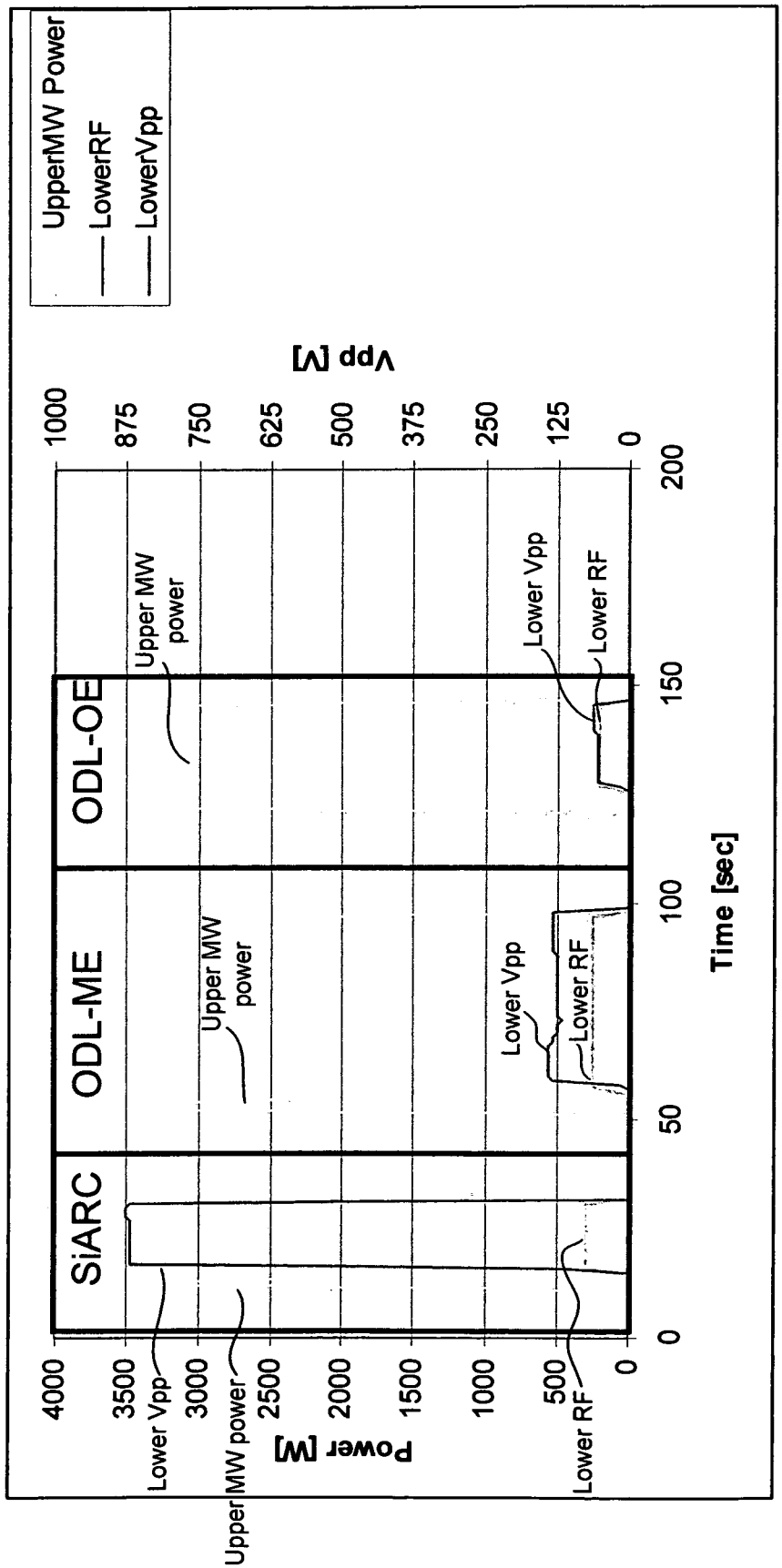

UpperMW Power
LowerRF
LowerVpp
Vpp [V]
1000
875
750
625
500
375
250
125
0
SiARC
ODL-ME
ODL-OE
Upper MW power
Lower Vpp
Lower RF
Power [W]
4000
3500
3000
2500
2000
1500
1000
500
0
Lower Vpp
Upper MW power
Lower RF
0
50
100
150
200
Time [sec]

FIG 15

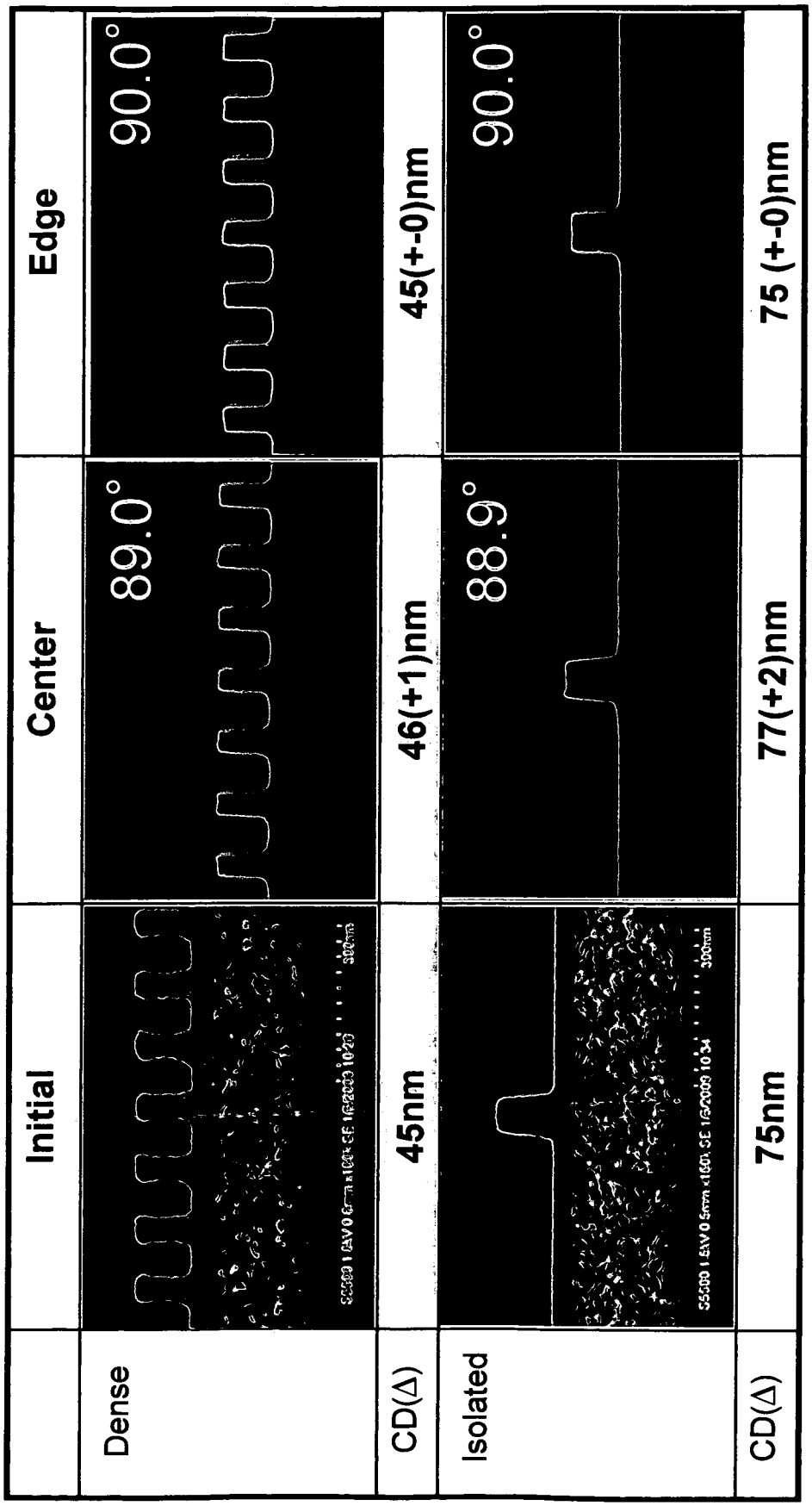
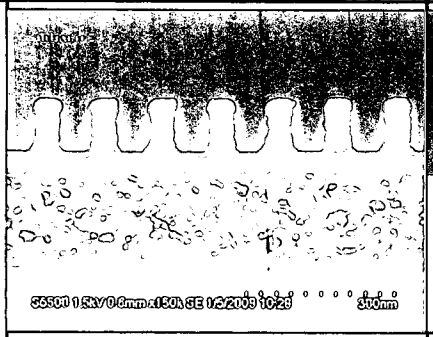
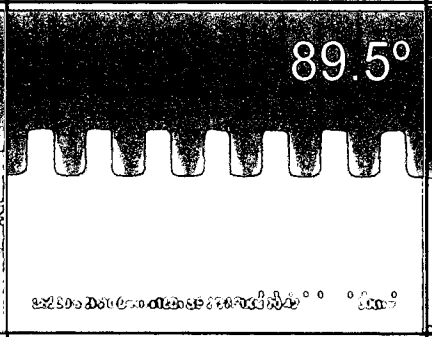
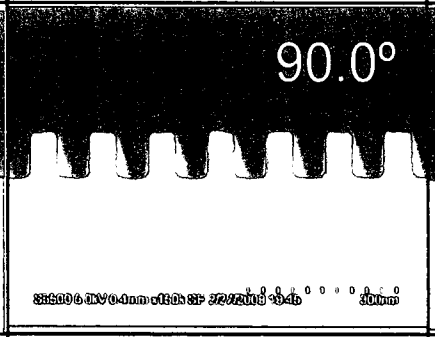
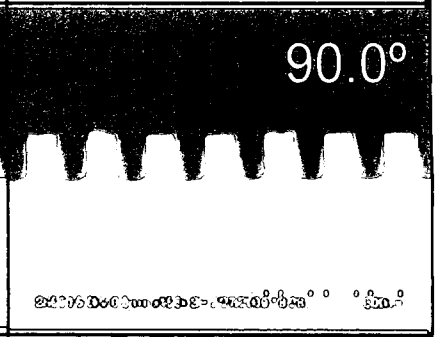
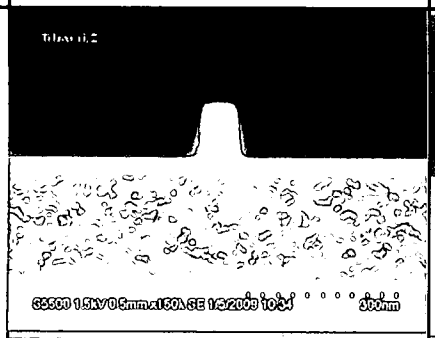
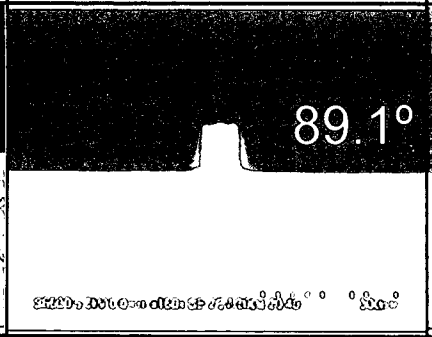
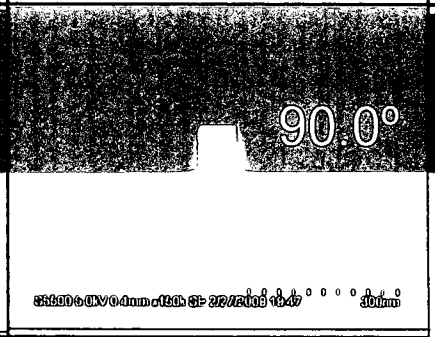
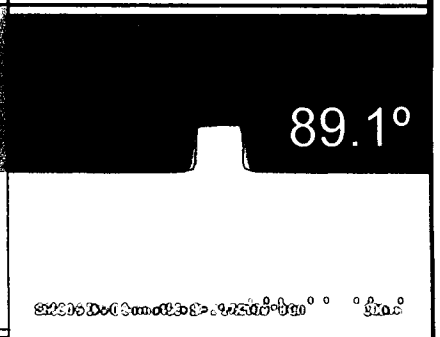

Initial
Center
Edge
Dense
89.0°
90.0°
CD(Δ)
45nm
46(+1)nm
45(+-0)nm
Isolated
88.9°
90.0°
CD(Δ)
75nm
77(+2)nm
75 (+-0)nm

FIG 16

CD Controllability

CF4/CHF3	Initial	-(210/150)	±0(180/180)	+(150/210)
Dense				
	45nm	42nm(-3nm)	45nm(±0nm)	55nm(+10nm)
Isolated				
	75nm	73nm(-1nm)	75nm (±0nm)	87nm(+12nm)
Isolated/ Dense Δ		+2nm	0nm	+2nm

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 10/00865

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - C23F 1/08; H01L 21/3065 (2010.01)
USPC - 156/345.48; 156/345.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - C23F 1/08; H01L 21/3065 (2010.01)
USPC - 156/345.48; 156/345.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
156/345.46 (keyword-limited: see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Google, Google Patents, PUBWEST(PGPB, USPT, USOC, EPAB, JPAB)
Search Terms Used: semiconductor, substrate, (mask or mask pattern and photoresist and ARC or silicon nitride), (CD or critical dimension), control, (laser or light and interference), plasma, (etching and trimming), etching near5 adjusting.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,423,457 B1 (BELL) 23 July 2002 (23.07.2002), Abstract, col 5, ln 46 - ln 57, col 7, ln 3 - ln 11, col 7, ln 33 - ln 37, Figure 1, col 7, ln 33 - ln 36.	1, 2, 4, 6, 10, 12 --- 3, 5, 7-9, 11, 13-19
Y	US 7,094,613 B2 (MUI et al) 22 August 2006 (22.08.2006), col 7, ln 41 - ln 54, claim 5, claim 6, Figure 1, col 2, ln 4 - ln 18, col 3, ln 22 - ln 37, Figure 2A, col 7, ln 63 to col 8, ln 2.	3, 5, 7-9, 11, 15, 18
Y	US 6,914,010 B2 (JEONG et al) 05 July 2005 (05.07.2005), col 7, ln 48 - ln 58.	13-19
Y	US 5,854,136 A (HUANG et al) 29 December 1998 (29.12.1998), Abstract.	8, 9

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 May 2010 (11.05.2010)	03 JUN 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)