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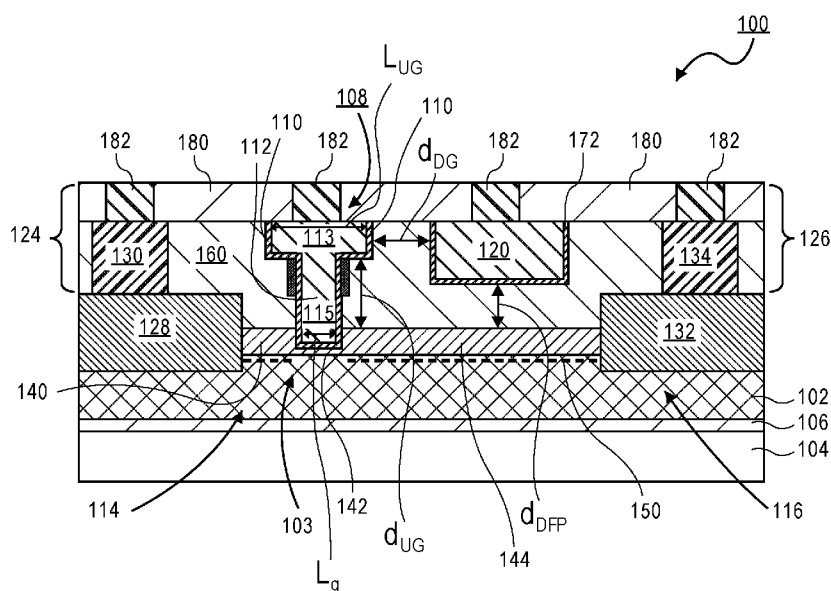


FIG. 1

(57) **Abstract:** Gallium nitride (GaN) transistors with drain field plates and their methods of fabrication are described. In an example, a transistor includes a gallium nitride (GaN) layer above a substrate, a gate structure over the GaN layer, a source region on a first side of the gate structure, a drain region on a second side of the gate structure, the second side opposite the first side, and a drain field plate above the drain region, wherein the drain field plate is not electrically coupled to the gate structure or the source region.

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GALLIUM NITRIDE TRANSISTORS WITH DRAIN FIELD PLATES AND THEIR METHODS OF FABRICATION

TECHNICAL FIELD

5 Embodiments of the present disclosure relate to semiconductor integrated circuits and more particularly to GaN transistors with drain field plates.

BACKGROUND

RF power amplifiers (RF PAs) are needed to transmit RF signals between mobile devices
10 and base stations located at far distances away, such as greater than 1 mile. The efficiency of these RF PAs is a key determinant of battery life in mobile handsets and power consumption (cost) in RF base stations. Good linearity of the RF power amplifier is required for modern communication standards such as 4G LTE and future 5G standards. RF PAs typically operate at several dB back-off from its saturated mode in order to meet the linearity requirements. Thus,
15 the efficiency suffers and in most PAs, it may degrade by a factor of 2-3X.

Due to its wide bandgap and high critical breakdown electric field, gallium nitride (GaN) transistors are considered for high voltage applications such as power converters, RF power amplifiers, RF switch and high voltage applications. Simple transistor architecture, namely, having a single gate, source and drain, falls short of realizing the full potential of GaN in
20 achieving the maximum breakdown voltage as dictated by its material properties. This is because the drain electric field concentrates at the edge of the gate and causes premature breakdown.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a transistor having a drain field plate in accordance with embodiments
25 of the present disclosure.

Fig. 2 illustrates a GaN transistor having a drain field plate and having multiple gates in accordance with embodiments of the present disclosure.

Figs. 3A-3K illustrate a method of forming a transistor having a source field plate and a drain field plate in accordance with embodiments of the present disclosure.

30 Fig. 4 illustrates a circuit comprising a first transistor and a second transistor each having a drain field plate, in accordance with embodiments of the present disclosure.

Fig. 5 is a chart illustrating the performance advantage of a GaN transistor having a drain field plate in accordance with embodiments of the present disclosure.

35 Fig. 6 illustrates a computing device in accordance with one implementation of the disclosure.

Fig. 7 illustrates an interposer that includes one or more embodiments of the disclosure.

EMBODIMENTS OF THE DISCLOSURE

Gallium nitride (GaN) transistors with drain field plates are described. In the following description, numerous specific details are set forth, such as specific material and tooling regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as single or dual damascene processing, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, “below”, “bottom”, and “top” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

Embodiments described herein may be directed to back end of line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

Embodiments described below may be applicable to FEOL processing and structures,

BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

Embodiments of the present disclosure relate to gallium nitride (GaN) transistors having drain field plates. In embodiments, the transistors of the present disclosure have a gallium nitride (GaN) layer disposed above a substrate. A gate structure is disposed above the GaN layer. A source region and a drain region are disposed on opposite sides of the gate structure.

The drain field plate may be biased to an electrical potential which is different than a gate voltage and/or VSS offering a greater degree of control of the drain field. The transistors of the present disclosure may enable new circuit architectures, such as a cross-coupled pairs.

Additionally, the distance the drain field plate extends above the drain can be independently adjusted to improve the affect the field plate has on the drain field distribution, and hence

increase breakdown voltage and linearity. In an embodiment, the transistor is operated in an enhancement mode. In an embodiment the gate structure may have a “T” shape in order to reduce the electrical resistance of the gate structure. In an embodiment, the transistor may include a second gate structure or multiple gate structures disposed between the gate structure and the drain field plate to provide a multigate switch for, for example, an RF voltage divider.

Fig. 1 illustrates as transistor 100 having a drain field plate in accordance with embodiments of the present disclosure. Transistor 100 includes a GaN layer 102 disposed above a substrate 104. A buffer layer 106 may be disposed between GaN layer 102 and substrate 104. A gate structure 108 is disposed above GaN layer 102 as illustrated in Fig. 1. Gate structure 108 may include a gate dielectric 110, such as a high k gate dielectric, such as but not limited to hafnium oxide (e.g., HfO_2) and aluminum oxide (e.g., Al_2O_3), and a gate electrode 112, such as a metal gate electrode. A source region 114 and a drain region 116 are disposed on opposite sides of gate structure 108 as illustrated in Fig. 1.

Transistor 100 includes a drain field plate 120 located above drain region 116. Drain field plate 120 is separated from drain region 116 by a distance (d_{DFP}) as illustrated in Fig. 1.

Drain field plate 120 may be separated from gate structure 108 by a distance d_{DG} .

In an embodiment, source region 114 includes a source contact 124 and drain region 116 includes a drain contact 126. Source contact 124 may include a source semiconductor contact 128 and a source metal contact 130, and drain contact 126 may include a drain semiconductor contact 132 and a drain metal contact 134. In an embodiment as illustrated in Fig. 1, source semiconductor contact 128 and drain semiconductor contact 132 are formed from a III-N semiconductor, such as but not limited to indium gallium nitride (InGaN). In an embodiment,

the III-N semiconductor has an N⁺ conductivity, such as, for example, greater than 1×10^{18} atoms/cm³. In an embodiment, the source metal contact 130 and the drain metal contact 134 comprise a metal, such as but not limited to tungsten. In an embodiment, drain field plate 120 is located laterally between drain metal contact 134 and gate structure 108 as shown in Fig. 1.

5 Transistor 100 may include as polarization layer 140 disposed on GaN layer 102. Polarization layer 140 may be formed from a group III-N semiconductor, such as but not limited to aluminum indium nitride (AlInN), aluminum indium gallium nitride (AlInGa₂N) and indium gallium nitride (InGa₂N). In an embodiment, polarization layer 140 is sufficiently thick in order to create a two-dimensional electron gas (2DEG) effect or layer 150 in the top surface of GaN layer 102 as illustrated in Fig. 1. In an embodiment, polarization layer 140 has a portion 142
10 beneath gate structure 108 which is thinner than portion 144 above source region 114 and drain region 116 so that a 2DEG layer or effect is not created in gallium nitride layer 102 beneath gate structure 108 as shown in Fig. 1. In an embodiment, polarization layer 140 is completely removed from under gate structure 108 and gate structure 108 is disposed directly on GaN layer
15 102. In an embodiment polarization layer 140 is multilayer film comprising a lower AlN film and an upper AlInN for example. In an embodiment, transistor 100 is operated in an enhancement mode.

Drain field plate 120 and gate structure 108 are disposed within dielectric layer 160 as illustrated in Fig. 1. In an embodiment, the top surface of drain field plate 120, is coplanar with
20 the top surface of gate structure 108 as illustrated in Fig. 1. In an embodiment, the top surface of dielectric layer 160 is coplanar with the top surface of gate structure 108, and drain field plate 120 as illustrated in Fig. 1. In an embodiment, the top surface of source metal contact 130 and the top surface of drain metal contact 134 are coplanar with the top surface of gate structure 108 and the top surface of drain field plate 120.

25 Transistor 100 has a gate length (L_g) in a first direction extending between the source region 114 and the drain region 116 as shown in Fig. 1. A channel region is located in GaN layer 102 beneath gate structure 108 and between source region 114 and drain region 116. Transistor 100 has a gate width (G_w) in a direction perpendicular (in and out of the page) to the gate length (L_g) direction. In an embodiment, transistor 100 has a gate width (G_w) between 10
30 microns – 100 microns. In an embodiment, drain field plate 120 extends the entire gate width (G_w) of transistor 100. In an embodiment gate structure 108 has a “T” shape as illustrated in Fig. 1. Gate structure may include an upper gate portion 113 and a lower gate portion 115. Upper gate portion 113 is distal from GaN layer 102 while lower gate portion 115 is nearer GaN layer 102. In an embodiment, lower gate portion 115 has a length (L_g) in the gate length
35 direction which defines the gate length (L_g) of transistor 100. In an embodiment, upper gate portion 113 has length (L_{ug}) in the gate length direction which is at least two times, and in other

embodiments at least three times, greater than the gate length (L_g) of lower gate portion 115. In an embodiment, as shown in Fig. 1 upper gate portion 113 extends a distance (d_{UG}) above drain region 116 which is greater than the distance d_{DFP} that drain field plate 120 extends above drain region 116. A recessed drain field plate may provide better control of the drain field. In an embodiment, a recessed drain field plate may exert a depletion effect on the 2DEG in the extended drain region. In an embodiment, upper gate portion 113 extends a distance (d_{UG}) above drain region 116 which is the same distance d_{DFP} that drain field plate 120 extends above drain region 116. In an embodiment, gate dielectric 110 is disposed along the sidewalls and bottom of upper gate portion 113 and along the sidewalls and bottom of lower gate portion 115 as illustrated in Fig. 1.

In an embodiment, drain field plate 120 may be biased separately from a gate voltage (V_g) applied to gate structure 108. In an embodiment, drain field plate 120 may be biased to a potential different than V_{ss} or ground. In an embodiment, drain field plate 120 may be biased differently than the voltage applied to source region 114. In an embodiment, drain field plate 120 may be biased differently than a voltage applied to drain region 116. In an embodiment, drain field plate 120 is not electrically connected to drain region 116.

In an embodiment, a pair of insulative spacers 170 are disposed along opposite sides of gate structure 108 as illustrated in Fig. 1. In an embodiment, insulative spacers 170 do not extend the entire height of gate structure 108. In an embodiment, insulative spacers 170 do not contact polarization layer 140 or GaN layer 102. In an embodiment, spacers 170 are formed beneath upper gate portion 113 and on sidewalls of lower gate portion 115 as illustrated in Fig. 1. In an embodiment, insulative spacers 170 are formed from an insulative material, such as but not limited to, silicon nitride and silicon oxynitride, which is different from the dielectric material of dielectric layer 160.

In an embodiment, a second dielectric layer 180 is disposed over dielectric layer 160. A plurality of conductive vias 182 may be disposed in dielectric 180 to enable independent electrical connections to and control of source region 114, drain region 116, drain field plate 120 and gate structure 108.

In an embodiment, a high k dielectric 172, such as but not limited to hafnium oxide (e.g., HfO_2) and aluminum oxide (e.g., Al_2O_3) may be disposed on the sidewalls and bottom surface of drain field plate 120 as illustrated in Fig. 1. In an embodiment, high k dielectric 172 is the same high k dielectric material as gate dielectric layer 110 of gate structure 108.

Fig. 2 illustrates a GaN transistor 200 having a drain field plate and multiple gates. Transistor 200 includes a second gate structure 202 above GaN layer 102 and between gate structure 108 and drain field plate 120 as illustrated in Fig. 2. Second gate structure 202 may be recessed into polarization layer 140 so that a 2DEG layer of effect is not formed under second

gate structure 202 as illustrated in Fig. 2. Gate structure 202 may include a gate dielectric 210, such as a high k gate dielectric and a gate electrode 212 as described with respect to gate structure 108. In an embodiment, insulating spacers 220 may be disposed on opposite sidewalls of gate structure 202 as illustrated in Fig. 2. Insulative spacers 220 may not extend the entire height of gate structure 202 as illustrated in Fig. 2. In an embodiment, the second gate structure 202 has a larger gate length (Lg2) than the gate length (Lg) of gate structure 108. That is, in an embodiment, Lg2 is greater than Lg. In an embodiment, Lg2 is equal to Lg. In an embodiment, second gate structure 202 may have a “T” shape including an upper gate portion 213 and a lower gate portion 215 as illustrated in Fig. 2.

In an embodiment, two or more additional gate structures 202 may be disposed over GaN layer 102 and between gate structure 108 and drain field plate 120. In an embodiment, gate structure 108 and each of the additional gate structures 202 may be bias separately. In an embodiment, the multiple gates act as an RF voltage divider allowing each gate to be biased with a lower DC voltage. A single gate NMOS transistor may require a large negative gate voltage (Vg) to keep the transistor in an “OFF” state. In an embodiment, transistor 200 may be used in a cascoded power amplifier circuit. Transistor 200 may improve gain by reducing source resistance of the second gate. Having two gate electrodes may protect the corresponding gate oxides from increased voltages.

Figs. 3A-3K illustrate a method of forming a transistor having a drain field plate in accordance with embodiments of the present disclosure. A gallium nitride (GaN) layer 302 may be disposed above a substrate 304, such as but not limited to a monocrystalline silicon substrate, a silicon carbide substrate, and aluminum oxide (Al₂O₃) substrate. As shown in Fig. 3A, a polarization layer 306, such as but not limited to aluminum gallium nitride (AlGaN), aluminum indium gallium nitride (AlInGaN) and indium gallium nitride (InGaN) may be disposed on GaN layer 302. Polarization layer may be formed to a thickness, such as greater than 10 nm, sufficient to create a 2DEG layer 305 or effect in the top surface of GaN layer 302 as illustrated in Fig. 3A. In an embodiment, polarization layer 306 is a III-N semiconductor, such as but not limited to aluminum gallium indium nitride (Al_xGa_{1-x-y}In_yN, where 0 < x ≤ 1, 0 < y ≤ 1) which is formed to a sufficient thickness to create a two dimensional electron gas (2-DEG) layer 305 in the top portion of GaN layer 302. In an embodiment, polarization layer 306 consists of multiple layers, such as AlN/Al_{0.2}Ga_{0.8}N/Al_{0.83}In_{0.17}N, where the AlN is to the bottommost layer. In an embodiment, the polarization layer 306 has a thickness of approximately 10 nanometers. In an embodiment, the top surface of GaN layer 302 is the (0001) plane or the c-plane of GaN. In an embodiment, polarization layer 306 is lattice matched to GaN layer 302.

A buffer layer 308 may be disposed between substrate 304 and GaN layer 302. Buffer layer 308 may contain one or more layers having a lattice constant between the lattice constant

of substrate 304 and GaN layer 302.

In a specific embodiment, substrate 304 is a monocrystalline silicon substrate, buffer layer 308 includes an aluminum nitride layer having a thickness between 100-300 nm disposed on the monocrystalline silicon substrate and a graded aluminum gallium nitride layer with a higher aluminum concentration near the aluminum nitride layer. Integrated circuits, for example, a system-on-chip (SOC) or a microprocessor, may be formed from silicon transistors, such as nonplanar transistors, fabricated on portions of silicon substrate 304 not covered by the GaN layer 302. In another embodiment, substrate 304 is a silicon carbide (SiC) substrate and buffer layer 308 comprises aluminum nitride having a thickness, for example, between 100-300 nm. Polarization layer 306, buffer layer 308, GaN layer 302 may be epitaxially deposited by any well-known technique, such as but not limited to chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), and sputtering.

Fig. 3B illustrates the formation of a hard mask block 308 on the structure of Fig. 3A. Hard mask block 310 defines a source contact location 312, and a drain contact location 314.

Hard mask block 310 may be formed of any suitable material, such as silicon nitride. Hard mask material 310 may be formed by blanket depositing a hard mask material, by for example, CVD or sputtering, and then patterning the hard mask material, by for example, lithographic patterning and etching.

Fig. 3C illustrates the formation of a source semiconductor contact 316 and a drain semiconductor contact 318 on the structure of Fig. 3B. In an embodiment, source semiconductor contact 316 and drain semiconductor contact 318 are formed from a group III-N semiconductor, such as but not limited to InGaN. In an embodiment, source semiconductor contact 316 and drain semiconductor contact 318 are doped to an N⁺ conductivity level with silicon. In an embodiment, source semiconductor contact 316 and drain semiconductor contact 318 are selectively epitaxially deposited by, for example, chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD). In an embodiment, source semiconductor contact 316 and drain semiconductor contact 318 are single crystalline or near single crystalline semiconductor. In an embodiment, source semiconductor contact 316 and drain semiconductor contact 318 are formed from a III-N semiconductor having a smaller band gap than GaN. In an embodiment, source semiconductor contact 316 and drain semiconductor contact 318 are formed in a pair of recesses etched through polarization layer 306 and into GaN layer 302 as illustrated in Fig. 3C. Source semiconductor contact 316 and drain semiconductor contact 318 disposed in trenches in GaN layer 302 may apply stress to the channel region of the fabricated transistor in order to improve device performance.

Fig. 3D illustrates a formation of a partial gate trench 320 in a dielectric layer 322. Dielectric layer 322 may be any well-known dielectric, such as but not limited to silicon oxide

and carbon doped silicon oxide. A partial gate trench 320 may be formed by first forming a patterned photoresist mask 324 over dielectric 322 which has an opening 326 which defines the location desired for a subsequently formed gate structure. Partial gate trench 320 may then be formed by, for example, etching in alignment with opening 326. Partial gate trench 320 does not extend to polarization layer 306 or GaN layer 302 as illustrated in Fig. 3B. In an embodiment, partial gate trench 320 may define the location and gate length (L_g) of a lower gate portion of a subsequently formed T gate structure. Additionally, it is to be appreciated, that if multiple gate structures are desired for the fabrication of a multigate transistor, such as transistor 200 illustrated in Fig. 2, multiple partial gate trenches 320 may be etched into dielectric 322 at this time.

Fig. 3E illustrates the formation of a spacer/hard mask material 330 and a patterned photoresist resist layer 332. In an embodiment, spacer/hard mask material 330 is blanket deposited over the top surface of dielectric 322, along the sidewalls of partial gate trench 320 and onto the bottom surface of partial gate trench 320 as illustrated in Fig. 3E. In an embodiment, spacer/hard mask material layer 330 is formed of a material, such as but not limited to silicon nitride, which may be selectively etched with respect to dielectric 322. A photoresist layer may then be deposited over spacer/hard mask layer 330 and patterned to provide a patterned photoresist layer 332 having opening 336 which defines a drain field plate location and an opening 338 which defines an upper gate portion location as shown in Fig. 3E. Additionally, the location of opening 336 relative to the location of opening 338 may define the distance (d_{DG}) at which a subsequently formed “T” gate structure and drain field plate are separated from one another.

In an embodiment, opening 338 defining the upper gate portion may be wider than the opening of the partial gate trench 320 as illustrated in Fig. 3E, so that a gate electrode may be formed which has a “T” shaped gate structure. A “T” shaped gate structure may provide a low resistance gate structure.

Fig. 3F illustrates the patterning of spacer/hard mask layer 330 of the structure of Fig. 3E. As illustrated in Fig. 3F, spacer/hard mask layer 330 is removed from drain field plate location 336 and upper gate portion location 338 by, for example, etching to form a patterned spacer/hard mask layer 339 as illustrated in Fig. 3F. Additionally, the spacer/hard mask layer 330 located on the bottom of the partial gate trench 320 is removed while leaving insulating spacers 340 along sidewalls of partial gate trench 320 as illustrated in Fig. 3F. An anisotropic dry etch process may be used to remove exposed portions of spacers/hard mask layer 330 from horizontal surfaces while leaving spacer/hard mask layer 330 on vertical sidewalls to form spacers 340 as illustrated in Fig. 3F.

Fig. 3G illustrates the formation of a drain field plate trench 342 and an upper gate

portion trench 343 formed in the structure of Fig. 3F. The drain field plate trench 342 and the upper gate portion trench 343 may be formed by etching dielectric layer 322 in alignment with patterned spacer/hard mask layer 339 as illustrated in Fig. 3G. The formation of upper gate portion trench 343 may also etch away a top portion of spacers 340 as illustrated in Fig. 3G. In an embodiment, the process used to form drain field plate trench 342 and upper gate portion trench may also be used to etch the dielectric layer 322 beneath the partial gate trench 320 to form lower gate portion trench 344 of the subsequently formed gate structure as illustrated in Fig. 3G. In an embodiment, lower gate portion trench 344 is partially etched into polarization layer 306 to create a recessed polarization layer 348 beneath lower gate portion trench 344. In an embodiment, recessed polarization layer 348 is of an insufficient thickness, such as less than two nanometers, to create a 2DEG layer or effect in the top surface of GaN layer 302 as illustrated in Fig. 3G. In an embodiment, lower gate portion trench 344 is formed completely through polarization layer 306 and exposes GaN layer 302.

The depth at which the upper gate portion trench 343 is formed in dielectric layer 322 may define the distance d_{UG} which the upper gate extends above the source and drain region. The depth at which drain field plate trench 342 is formed in dielectric layer 322 may define the distance d_{DFP} which the drain field plate extends above a drain region 352. In an embodiment, upper gate portion and drain field plate trench 342 have the same depth so that the upper gate portion is separated from the source and drain regions 350 and 352 by the same distance that the drain field plate is separated from the drain region 352 (i.e., $d_{UG}=d_{DFP}$).

In an embodiment, it may be desirable to have the drain field plate extend a different distance above the drain region than the distance at which the upper gate portion extends above the source and drain regions (i.e., d_{UG} does not equal d_{DFP}). For example, as illustrated in Fig. 3H, the drain field plate trench 342 may be etched an additional time to remove an additional portion 402 of dielectric material 322 to create a deeper trench. A patterned photoresist mask 410 may be disposed over upper gate portion trench 343, as shown in Fig. 3H, to protect it from further etching. In an embodiment, a material 420, such as a sacrificial light absorbing material (SLAM), may be blanket deposited and planarized to fill upper gate trench portion 343 and lower gate trench portion 344 and drain field plate trench 342 prior to the formation of patterned photoresist mask 410 in order to provide a planar surface upon which to form patterned photoresist mask 410 and improve lithography.

Fig. 3I illustrates the formation of a drain field plate 364 and a gate structure 365. In an embodiment, upper gate portion trench 343 and lower gate portion trench 344 are filled with a gate dielectric layer 366 and a gate electrode material 368 as illustrated in Fig. 3I. In an embodiment, the gate dielectric is a high k gate dielectric, such as but not limited to hafnium oxide (e.g., HfO_2), zirconium oxide (ZrO_2) and aluminum oxide (e.g., Al_2O_3). In an

embodiment, the gate dielectric layer is deposited by, for example, atomic layer deposition so that the gate dielectric layer forms on the bottom and sidewalls of upper gate portion trench 343 as well as along sidewalls and bottom lower gate portion trench 344. In an embodiment, the gate dielectric 366 is in contact with sidewall spacers 340 disposed along sidewalls of lower gate portion trench 343. A gate electrode material 368, such as but not limited to titanium aluminide (TiAl), titanium nitride (TiN), or any other suitable metal or metals may be deposited by, for example, ALD or CVD on gate dielectric 366.

In an embodiment, the deposition process used to fill upper gate portion trench 343 and upper gate portion trench 344 is also used to fill drain field plate trench 342 as illustrated in Fig. 3I. Accordingly, the bottom and sidewalls of drain field plate trench 342 may be lined with gate dielectric layer 366 and filled with a gate electrode material 368 as illustrated in Fig. 3I. In an embodiment, gate dielectric 366 and gate electrode 368 are blanket deposited over dielectric layer 322 and into and filling drain field plate trench 342, upper gate portion trench 343 and lower gate portion trench 344. Excess gate electrode material 368 and gate dielectric layer 366 disposed on the top surface of dielectric layer 322 may be removed by a planarization process, such as but not limited to chemical mechanical polishing. The planarization process may make the top surface of the drain field plate 364 and the gate structure 360 as well as dielectric layer 322 all coplanar with one another as illustrated in Fig. 3H.

Fig. 3J illustrates the formation of a source metal contact 372 and a drain metal contact 374 in dielectric layer 322 and in contact with the source semiconductor contact 316 and drain semiconductor contact 318, respectively. Source metal contact 372 and drain metal contact 374 may be formed by etching a plurality of openings in dielectric layer 322 to expose source semiconductor contact 316 and drain semiconductor contact 318. A contact metal such as but not limited to tungsten may then be deposited into the openings and polished back so that the top surfaces of source metal contact 372 and drain metal contact 374 are coplanar with gate structure 365 and drain field plate 364 as illustrated in Fig 3J.

Fig. 3K illustrates the formation of a second dielectric layer 380 over the dielectric layer 322 and the formation of a plurality of via contacts 382 in the dielectric layer 380. In this way the source region, the drain region, gate structure 365, and drain field plate 364 may all be independently biased or controlled.

Fig. 4 illustrates a circuit 400, having a first transistor 410 and a second transistor 420. First transistor 410 and second transistor 420 may be transistors having a drain field plate as illustrated and described with respect to transistors 100 and 200 of Figs. 1 and 2, respectively. In an embodiment, transistor 410 has a source region 412, a drain region 414, a gate structure 416, and a drain field plate 418. Transistor 410 may include a body contact tap 419. Second transistor 420 has a source region 422, a drain region 424, a gate structure 426, and a drain field

plate 428. Second transistor 420 may have a body contact tap 429.

A first capacitor 430 has a first electrode coupled to drain field plate 418 of first transistor 410 and a second electrode coupled to drain 424 of second transistor 420. A second capacitor 432 has a first electrode coupled to drain field plate 428 of second transistor 420 and a second electrode coupled to drain 414 of first transistor 410.

Circuit 400 includes a crossover 450 wherein the electrical connection 452 coupling drain 414 of first transistor 410 to drain field plate 428 of the second transistor 420 crosses over or under the electrical connection 454 coupling the drain 424 of second transistor 420 to drain field plate 418 of the first transistor 410, without making an electrical connection thereto. In an embodiment, source 412 of the first transistor 410 and source 422 of the second transistor 420 are coupled to ground as illustrated in Fig. 4.

In an embodiment of the present disclosure, a differential input signal is provided between the gate 416 of first transistor 410 and the gate 426 of second transistor 420. In an embodiment, a differential output signal is outputted from drain 514 of first transistor 410 and drain 424 of second transistor 420. In an embodiment, circuit 400 is a cross-coupled power amplifier (PA).

Fig. 5 is a chart illustrating the performance advantage of a GaN transistor, such as transistor 100, having a drain field plate. Chart 500 has the drain breakdown voltage (BVD(V)) on the X-axis and the equivalent ON resistance (R_{ON} Ohms- μ m) on the Y-axis. Plot 502 shows the performance of a GaN transistor with a drain field plate and plot 504 shows the performance of a similar GaN transistor without a field plate. Plot 506 shows the performance in a silicon transistor. As shown in chart 500 of Fig. 5, a GaN transistor having a field plate shows an approximately 2X improvement in drain breakdown voltage relative to a GaN transistor without a field plate.

Implementations of embodiments of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various

implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein
5 may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k
10 dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide,
15 titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

The gate electrode layer is formed on the gate dielectric layer and may consist of at least
20 one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not
25 limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as
30 hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall
35 portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a

planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

Fig. 6 illustrates a computing device 600 in accordance with one implementation of the

disclosure. The computing device 600 houses a board 702. The board 602 may include a number of components, including but not limited to a processor 604 and at least one communication chip 606. The processor 604 is physically and electrically coupled to the board 602. In some implementations the at least one communication chip 706 is also physically and electrically coupled to the board 602. In further implementations, the communication chip 606 is part of the processor 604.

Depending on its applications, computing device 600 may include other components that may or may not be physically and electrically coupled to the board 602. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 606 enables wireless communications for the transfer of data to and from the computing device 600. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 606 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 600 may include a plurality of communication chips 606. For instance, a first communication chip 606 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 606 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 604 of the computing device 600 includes an integrated circuit die packaged within the processor 604. In some implementations of the disclosure, the integrated circuit die of the processor includes one or more devices, such as GaN transistors with source and drain field plates built in accordance with implementations of the disclosure. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 606 also includes an integrated circuit die packaged within the communication chip 606. In accordance with another implementation of the disclosure, the integrated circuit die of the communication chip includes one or more devices, such as GaN transistors with source and drain field plates built in accordance with implementations of the disclosure.

In further implementations, another component housed within the computing device 700 may contain an integrated circuit die that includes one or more devices, such as GaN transistors with source and drain field plates built in accordance with implementations of the disclosure.

In various implementations, the computing device 600 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 600 may be any other electronic device that processes data.

Fig. 7 illustrates an interposer 700 that includes one or more embodiments of the disclosure. The interposer 700 is an intervening substrate used to bridge a first substrate 702 to a second substrate 704. The first substrate 702 may be, for instance, an integrated circuit die. The second substrate 704 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 700 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 700 may couple an integrated circuit die to a ball grid array (BGA) 706 that can subsequently be coupled to the second substrate 704. In some embodiments, the first and second substrates 702/704 are attached to opposing sides of the interposer 700. In other embodiments, the first and second substrates 702/704 are attached to the same side of the interposer 700. And in further embodiments, three or more substrates are interconnected by way of the interposer 700.

The interposer 700 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 708 and vias 710, including but not limited to through-silicon vias (TSVs) 712. The interposer 700 may further include embedded devices 814, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-

frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 700. In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer 700.

5 Thus, embodiments described herein include GaN transistors with source and drain field plates.

 The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for,
10 the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

 These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather,
15 the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

 Example embodiment 1: A transistor includes a gallium nitride (GaN) layer above a substrate, a gate structure over the GaN layer, a source region on a first side of the gate structure, a drain region on a second side of the gate structure, the second side opposite the first side, and a
20 drain field plate above the drain region wherein the drain field plate is not electrically coupled to the gate structure or to the source region or to the drain region.

 Example embodiment 2: The transistor of example embodiment 1 wherein a voltage applied to the drain field plate is different from a gate voltage applied to the gate structure and is different than V_{ss} .

25 Example embodiment 3: The transistor of example embodiment 1 wherein a voltage applied to the drain field plate is V_{ss} .

 Example embodiment 4: The transistor of example embodiment 1, 2 or 3 wherein the drain field plate has a top surface, wherein the top surface of the drain field plate is substantially coplanar with a top surface of the gate structure.

30 Example embodiment 5: The transistor of example embodiment 1, 2, 3 or 4 wherein the gate structure has a T gate structure.

 Example embodiment 6: The transistor of example embodiment 1, 2, 3, 4 or 5 further comprising a drain metal contact wherein the drain field plate is located laterally between the drain metal contact and the gate structure.

35 Example embodiment 7: The transistor of example embodiment 1, 2, 3, 4, 5 or 6 further comprising a first spacer on a source side of the gate structure and a second spacer on the drain

side of the gate structure.

Example embodiment 8: The transistor of example embodiment 1, 2, 3, 4, 5, 6 or 7 further comprising a second gate structure, the second gate structure over the GaN layer and between the gate structure and the drain field plate.

5 Example embodiment 9: A system includes a board, the board including a processor and a communication chip, wherein one of the processor or the communications chip has a transistor including a gallium nitride (GaN) layer above a substrate, a gate structure over the GaN layer, a source region on a first side of the gate structure, a drain region on a second side of the gate structure, the second side opposite the first side, and a drain field plate above the drain region,
10 where the drain field plate is not electrically coupled to the gate structure or to the source region or to the drain region.

Example embodiment 10: The system of example embodiment 9 wherein the drain field plate has a top surface, wherein the top surface of the drain field plate is substantially coplanar with a top surface of the gate structure.

15 Example embodiment 11: The system of example embodiment 9 or 10 further comprising a first spacer on a source side of the gate structure and a second spacer on a drain side of the gate structure.

Example embodiment 12: The system of example embodiment 9, 10 or 11 further comprising a second gate structure, the second gate structure over the GaN layer and between
20 the gate structure and the drain field plate.

Example embodiment 13: A method of forming a transistor includes forming a gate trench in a dielectric layer above a GaN layer, the gate trench having opposite sidewalls, the gate trench having a first depth. The method also includes forming a drain field plate trench in the dielectric layer, and increasing the trench depth of the gate trench to a second depth, and filling
25 the gate trench and the drain field plate trench with a conductor.

Example embodiment 14: The method of example embodiment 13 further comprising forming a hard mask over the dielectric layer and on the sidewalls of the gate trench and in the bottom of the gate trench prior to forming the drain field plate trench.

Example embodiment 15: The method of example embodiment 14 further comprising
30 forming a first sidewall spacer from the hard mask on a source side of the gate trench and a second sidewall spacer from the hard mask on a drain side of the gate trench.

Example embodiment 16: The method of example embodiment 13, 14 or 15 further comprising forming a polarization layer on the GaN layer.

Example embodiment 17: The method of example embodiment 13, 14, 15 or 16 further
35 comprising forming a source semiconductor contact on a first side of the gate structure and a drain semiconductor contact on a second opposite side of the gate structure.

Example embodiment 18: The method of example embodiment 17, wherein the source semiconductor contact and the drain semiconductor contact comprise indium, gallium and nitrogen.

5 Example embodiment 19: The method of example embodiment 13, 14, 15, 16, 17 or 18 further comprising forming a second gate trench in the dielectric layer, the second gate trench between the gate trench and the drain field plate trench.

10 Example embodiment 20: A circuit includes a first transistor having a gallium nitride (GaN) layer above a substrate, a first gate structure over the GaN layer, a first source region on a first side of the first gate structure, a first drain region on a second side of the first gate structure, the second side opposite the first side, and a first drain field plate above the first drain region. The circuit also includes a second transistor having a second gate structure over the GaN layer, a second source region on a first side of the second gate structure, a second drain region on a second side of the second gate structure, the second side opposite the first side, and a second drain field plate above the second drain region. The circuit also includes a first capacitor
15 coupled between the first drain field plate of the first transistor and the second drain of the second transistor, and a second capacitor coupled between the second drain field plate of the second transistor and the first drain of the first transistor.

Example embodiment 21: The circuit of example embodiment 20, wherein the first drain field plate is not electrically coupled to the first gate structure or the first source.

20 Example embodiment 22: The circuit of example embodiment 20 or 21, wherein the second drain field plate is not electrically coupled to the second gate structure or the second source.

CLAIMS

What is claimed is:

1. A transistor comprising:
5 a gallium nitride (GaN) layer above a substrate;
a gate structure over the GaN layer;
a source region on a first side of the gate structure;
a drain region on a second side of the gate structure, the second side opposite the first side; and
10 a drain field plate above the drain region wherein the drain field plate is not electrically coupled to the gate structure or to the source region or to the drain region.
2. The transistor of claim 1 wherein a voltage applied to the drain field plate is different from a gate voltage applied to the gate structure and is different than V_{ss} .
15
3. The transistor of claim 1 wherein a voltage applied to the drain field plate is V_{ss} .
4. The transistor of claim 1 wherein the drain field plate has a top surface, wherein the top surface of the drain field plate is substantially coplanar with a top surface of the gate structure.
20
5. The transistor of claim 1 wherein the gate structure has a T gate structure.
6. The transistor of claim 1 further comprising:
a drain metal contact wherein the drain field plate is located laterally between the drain
25 metal contact and the gate structure.
7. The transistor of claim 1 further comprising a first spacer on a source side of the gate structure and a second spacer on the drain side of the gate structure.
- 30 8. The transistor of claim 1 further comprising a second gate structure, the second gate structure over the GaN layer and between the gate structure and the drain field plate.
9. A system comprising:
a board, the board including a processor and a communication chip, wherein one of the
35 processor or the communications chip has a transistor comprising:
a gallium nitride (GaN) layer above a substrate;

a gate structure over the GaN layer;
a source region on a first side of the gate structure;
a drain region on a second side of the gate structure, the second side opposite the first side; and

5 a drain field plate above the drain region, where the drain field plate is not electrically coupled to the gate structure or to the source region or to the drain region.

10. The system of claim 9 wherein the drain field plate has a top surface, wherein the top surface of the drain field plate is substantially coplanar with a top surface of the gate structure.

10

11. The system of claim 10 further comprising a first spacer on a source side of the gate structure and a second spacer on a drain side of the gate structure.

12. The system of claim 10 further comprising a second gate structure, the second gate structure over the GaN layer and between the gate structure and the drain field plate.

15

13. A method of forming a transistor comprising:

forming a gate trench in a dielectric layer above a GaN layer, the gate trench having opposite sidewalls, the gate trench having a first depth;

20 forming a drain field plate trench in the dielectric layer, and increasing the trench depth of the gate trench to a second depth;

filling the gate trench and the drain field plate trench with a conductor.

14. The method of claim 13 further comprising forming a hard mask over the dielectric layer and on the sidewalls of the gate trench and in the bottom of the gate trench prior to forming the drain field plate trench.

25

15. The method of claim 14 further comprising forming a first sidewall spacer from the hard mask on a source side of the gate trench and a second sidewall spacer from the hard mask on a drain side of the gate trench.

30

16. The method of claim 13 further comprising forming a polarization layer on the GaN layer.

35 17. The method of claim 13 further comprising forming a source semiconductor contact on a first side of the gate structure and a drain semiconductor contact on a second opposite side of the

gate structure.

18. The method of claim 17 wherein the source semiconductor contact and the drain semiconductor contact comprise indium, gallium and nitrogen.

5

19. The method of claim 13 further comprising forming a second gate trench in the dielectric layer, the second gate trench between the gate trench and the drain field plate trench.

20. A circuit, comprising:

10

a first transistor, comprising:

a gallium nitride (GaN) layer above a substrate;

a first gate structure over the GaN layer;

a first source region on a first side of the first gate structure;

a first drain region on a second side of the first gate structure, the second side

15

opposite the first side; and

a first drain field plate above the first drain region;

a second transistor, comprising:

a second gate structure over the GaN layer;

a second source region on a first side of the second gate structure;

20

a second drain region on a second side of the second gate structure, the second side opposite the first side; and

a second drain field plate above the second drain region;

a first capacitor coupled between the first drain field plate of the first transistor and the second drain of the second transistor; and

25

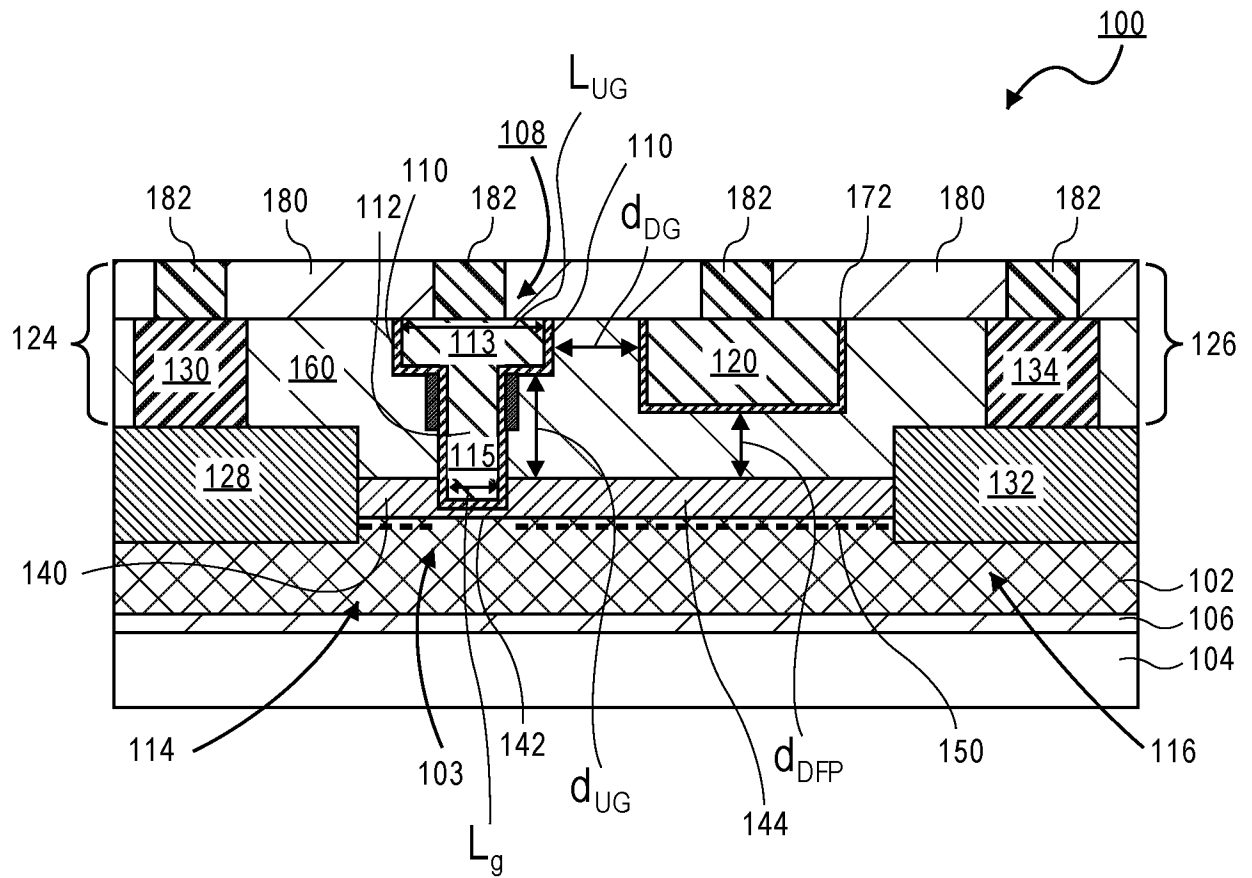
a second capacitor coupled between the second drain field plate of the second transistor and the first drain of the first transistor.

21. The circuit of claim 20 wherein the first drain field plate is not electrically coupled to the first gate structure or the first source.

30

22. The circuit of claim 20 wherein the second drain field plate is not electrically coupled to the second gate structure or the second source.

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**FIG. 1**

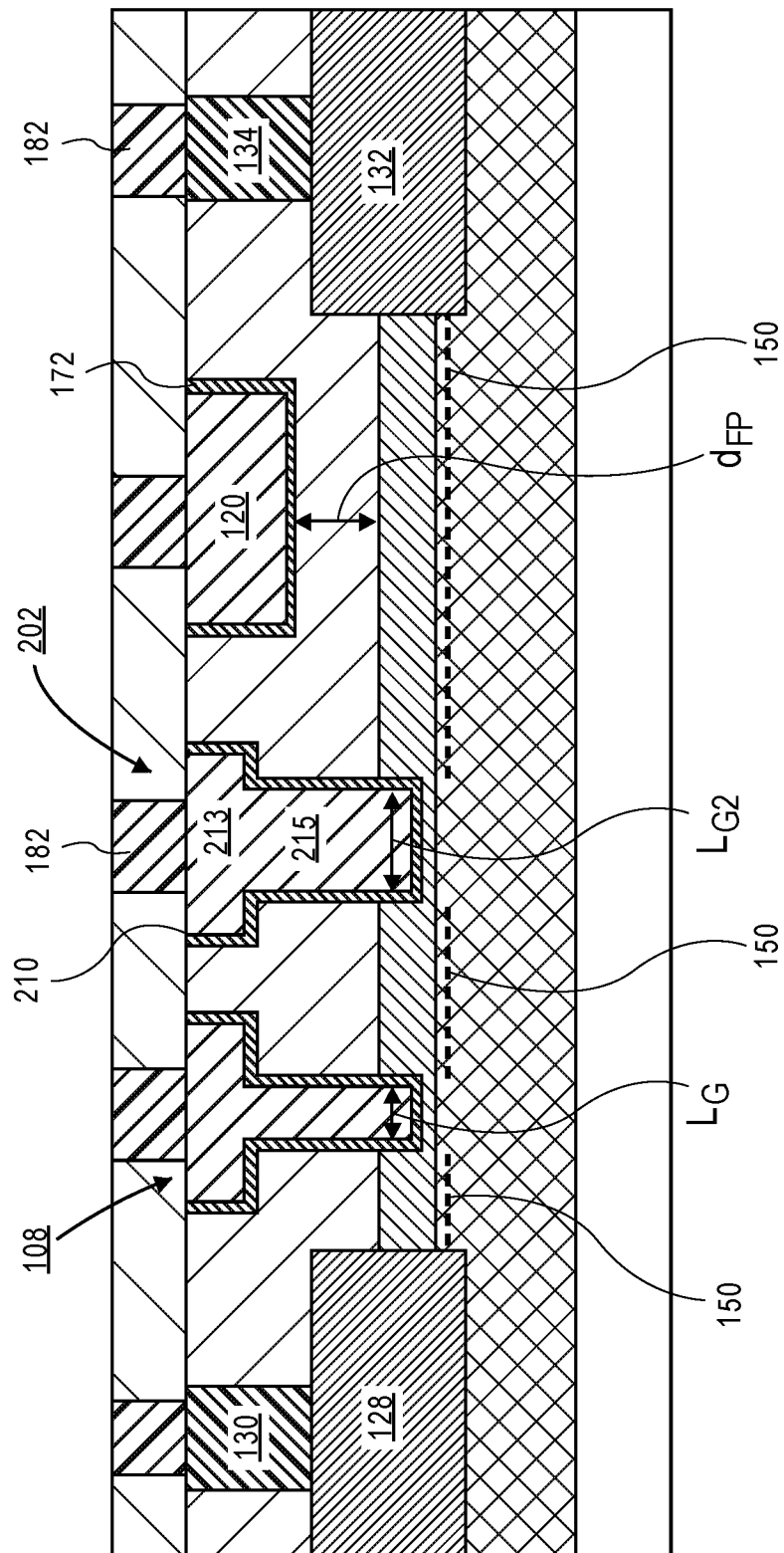


FIG. 2

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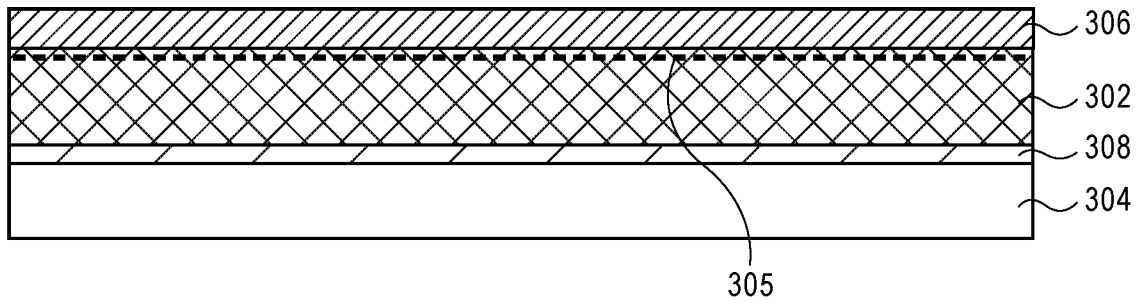


FIG. 3A

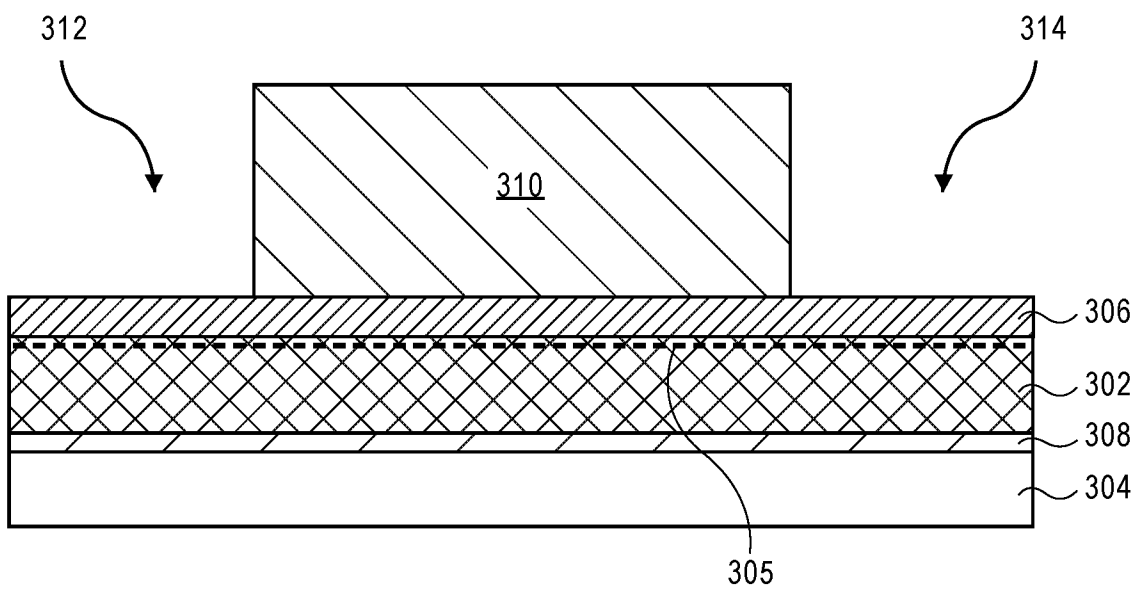


FIG. 3B

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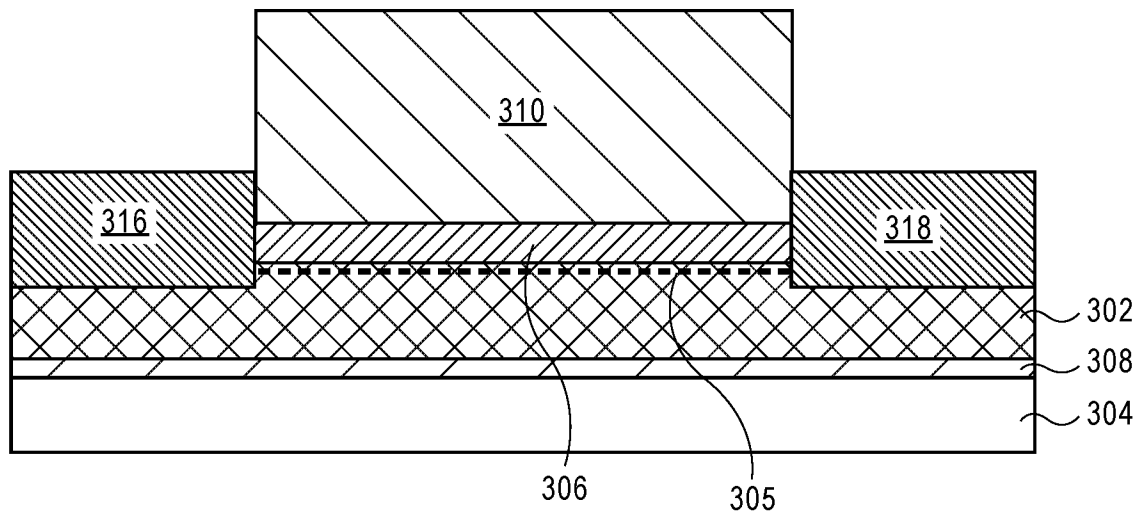


FIG. 3C

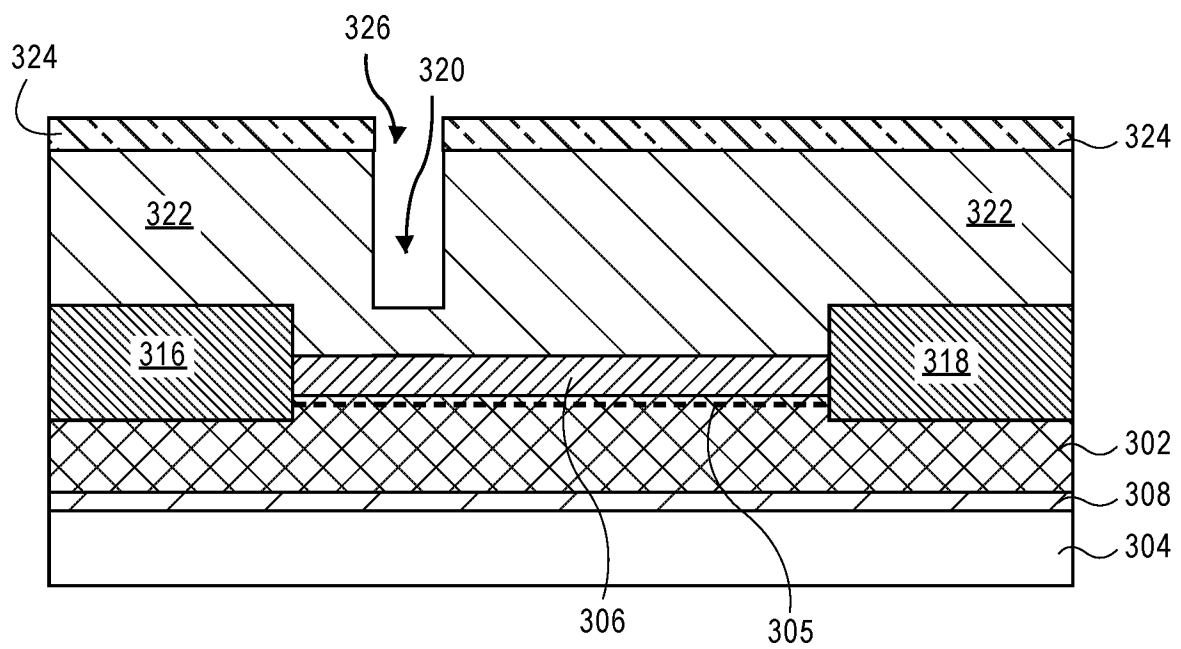


FIG. 3D

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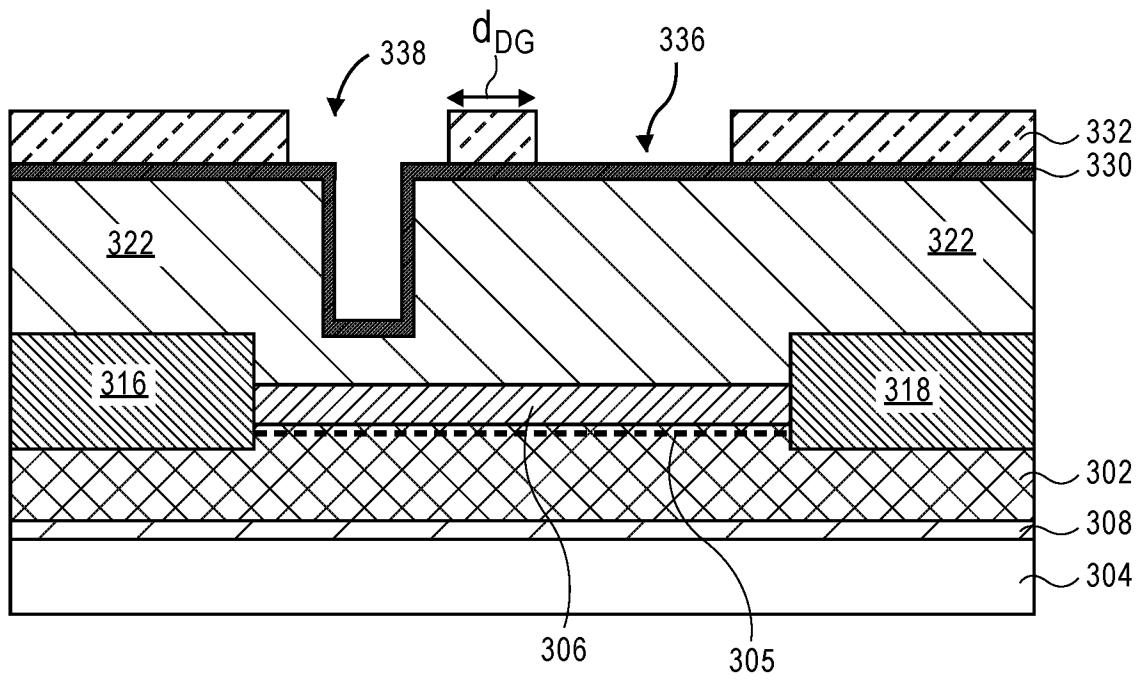


FIG. 3E

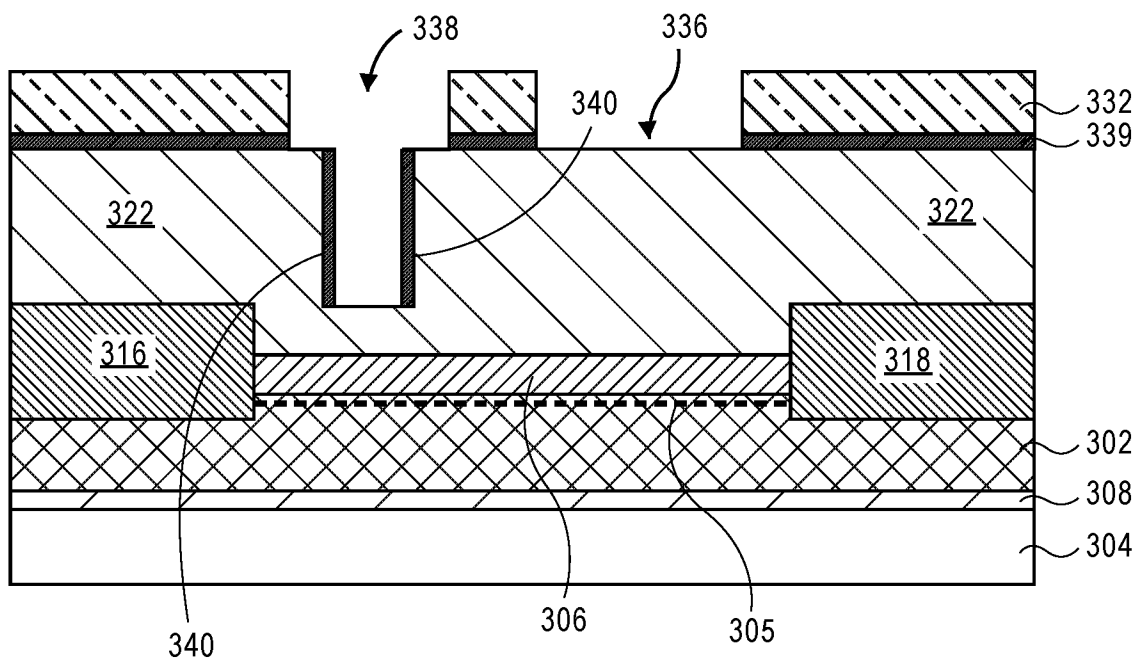


FIG. 3F

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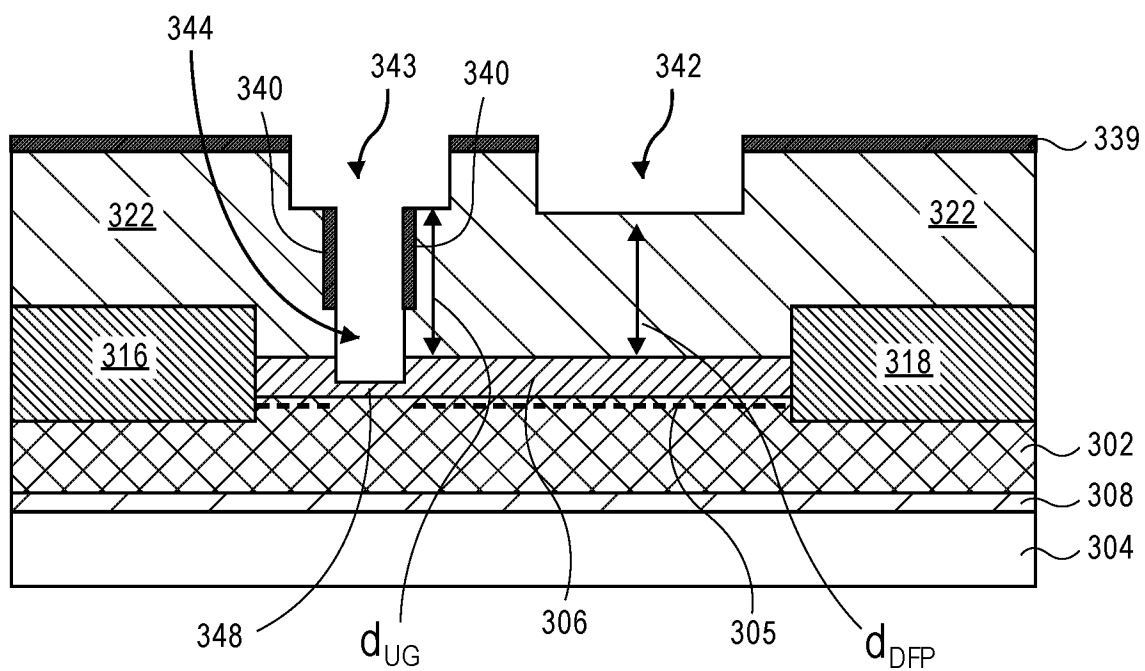


FIG. 3G

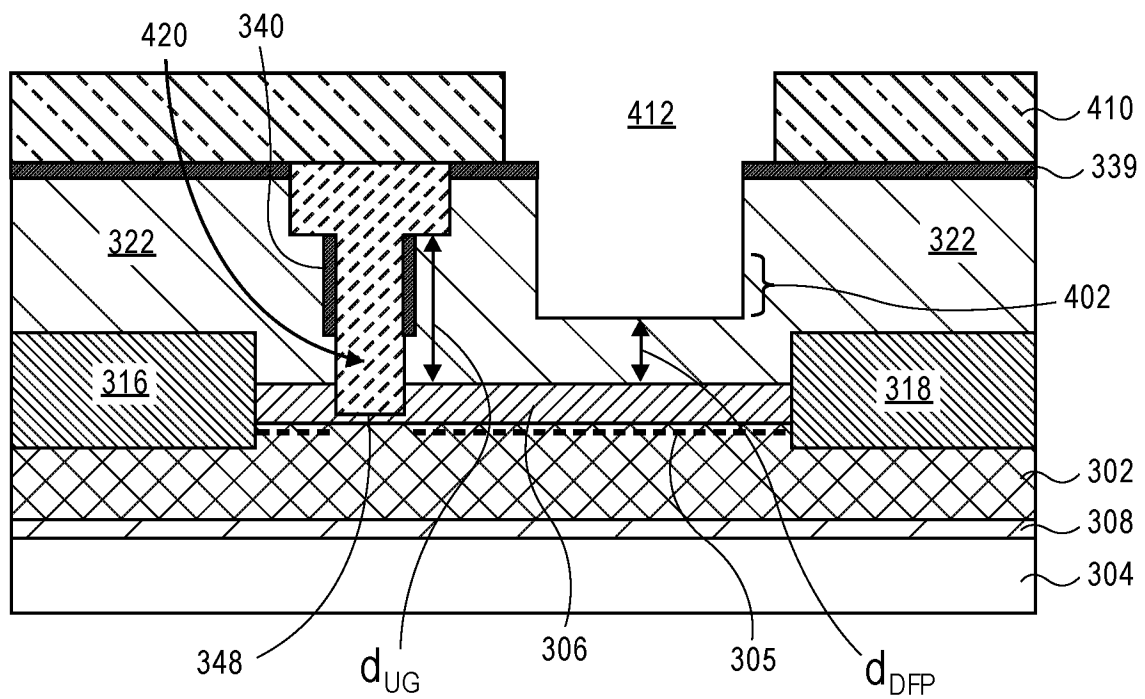
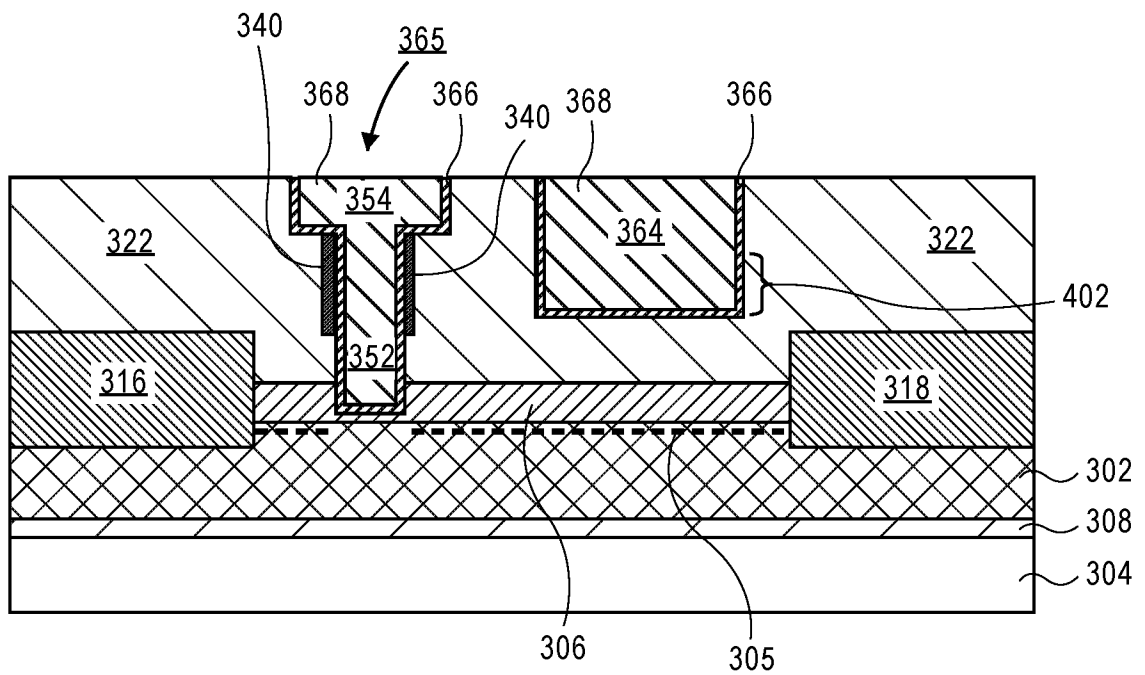
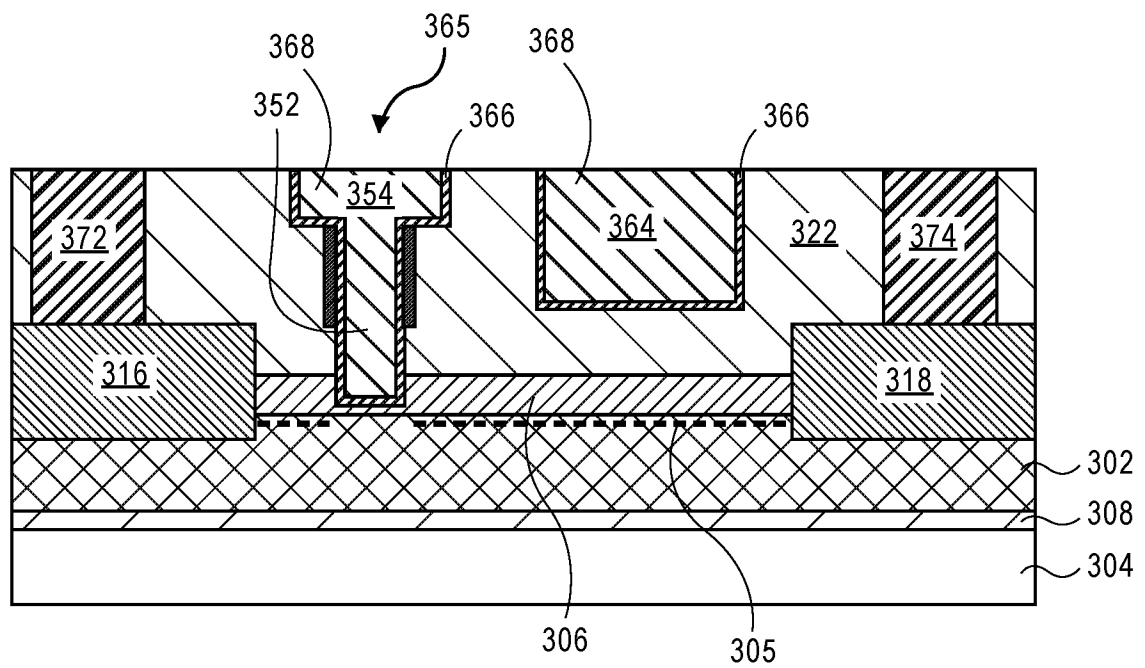


FIG. 3H

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**FIG. 3I****FIG. 3J**

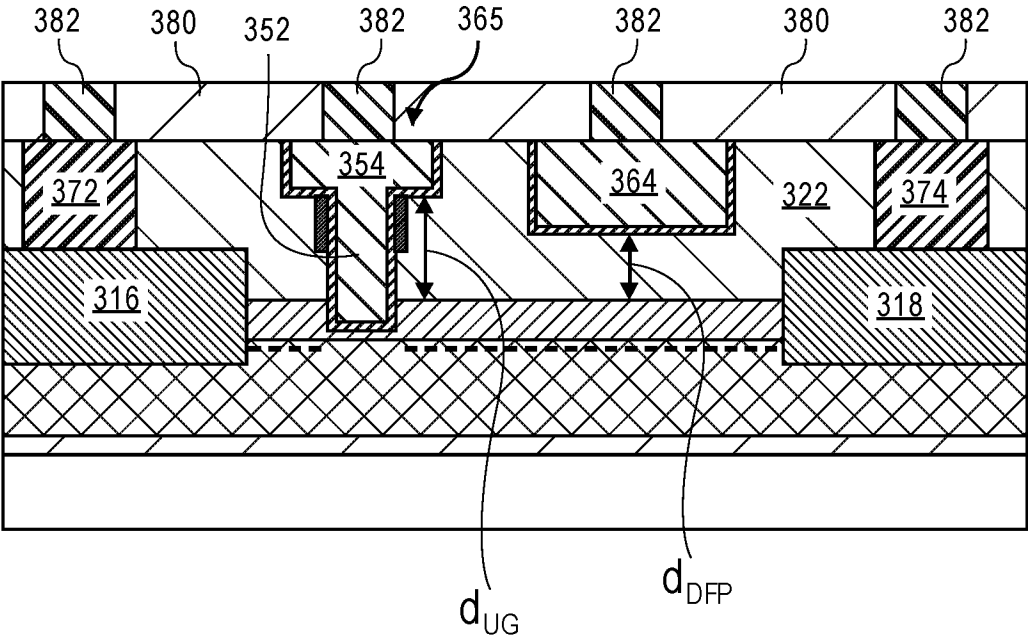
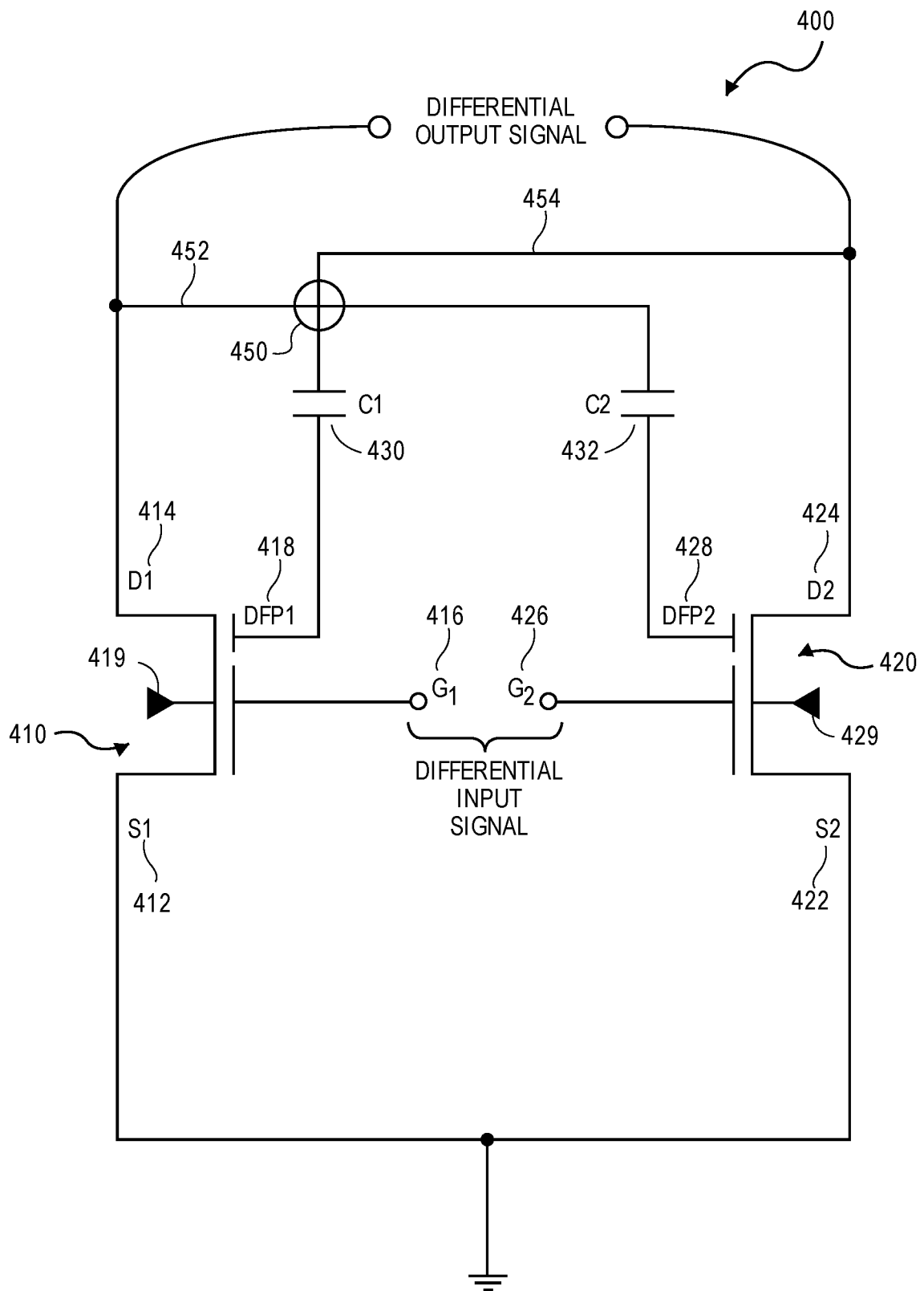


FIG. 3K

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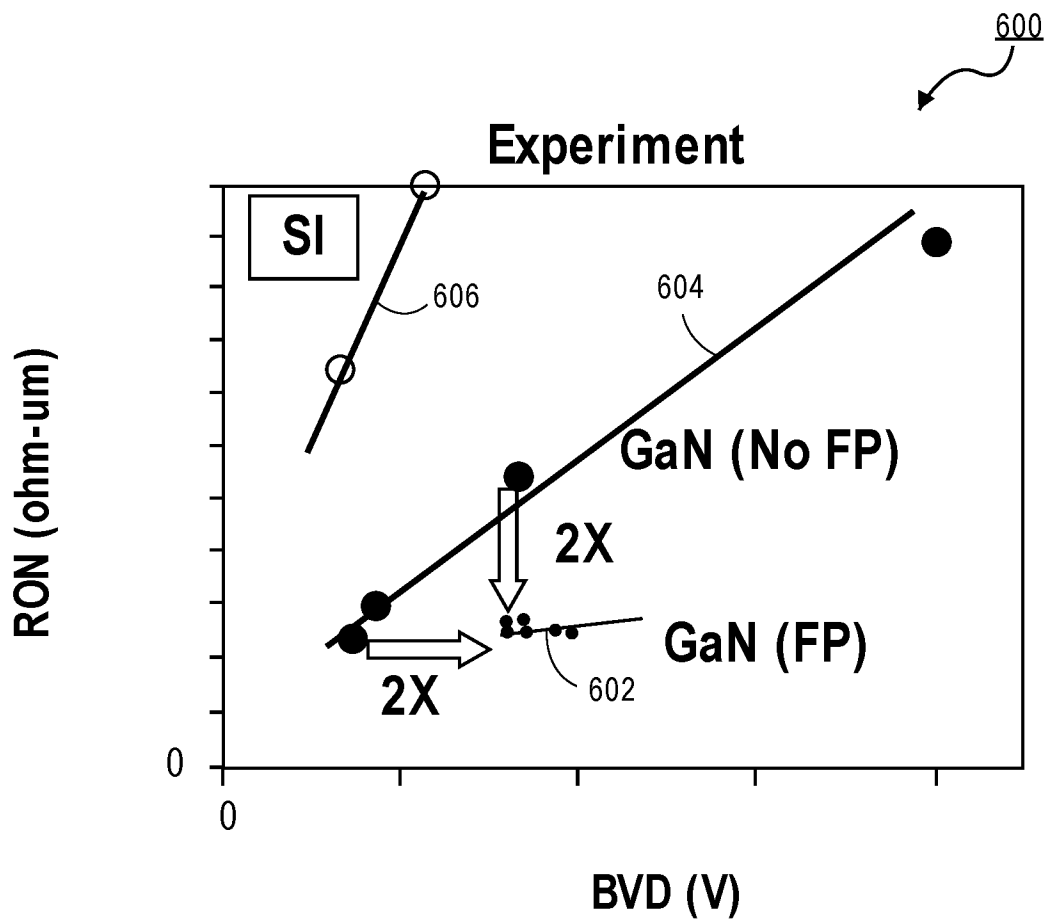


FIG. 5

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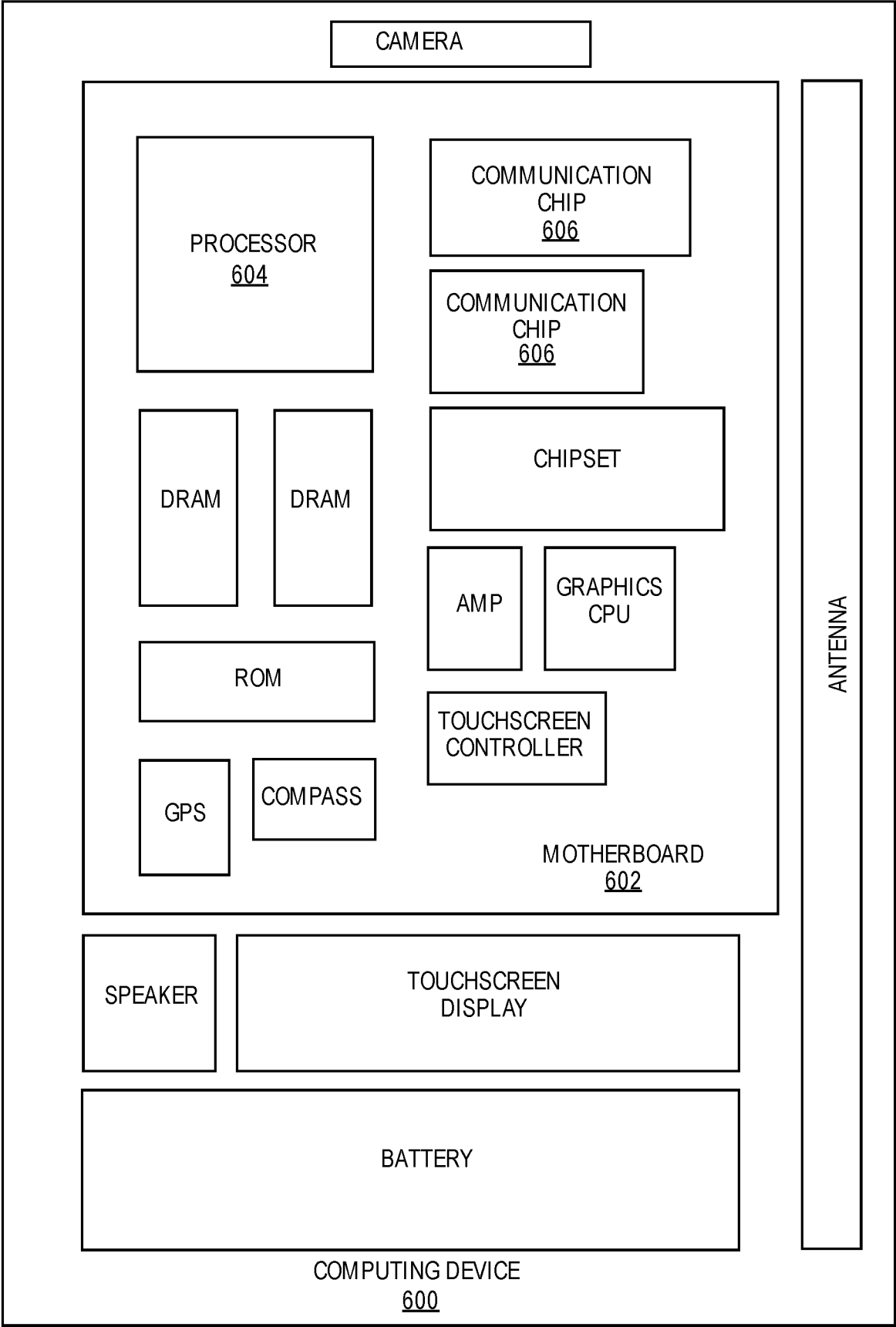


FIG. 6

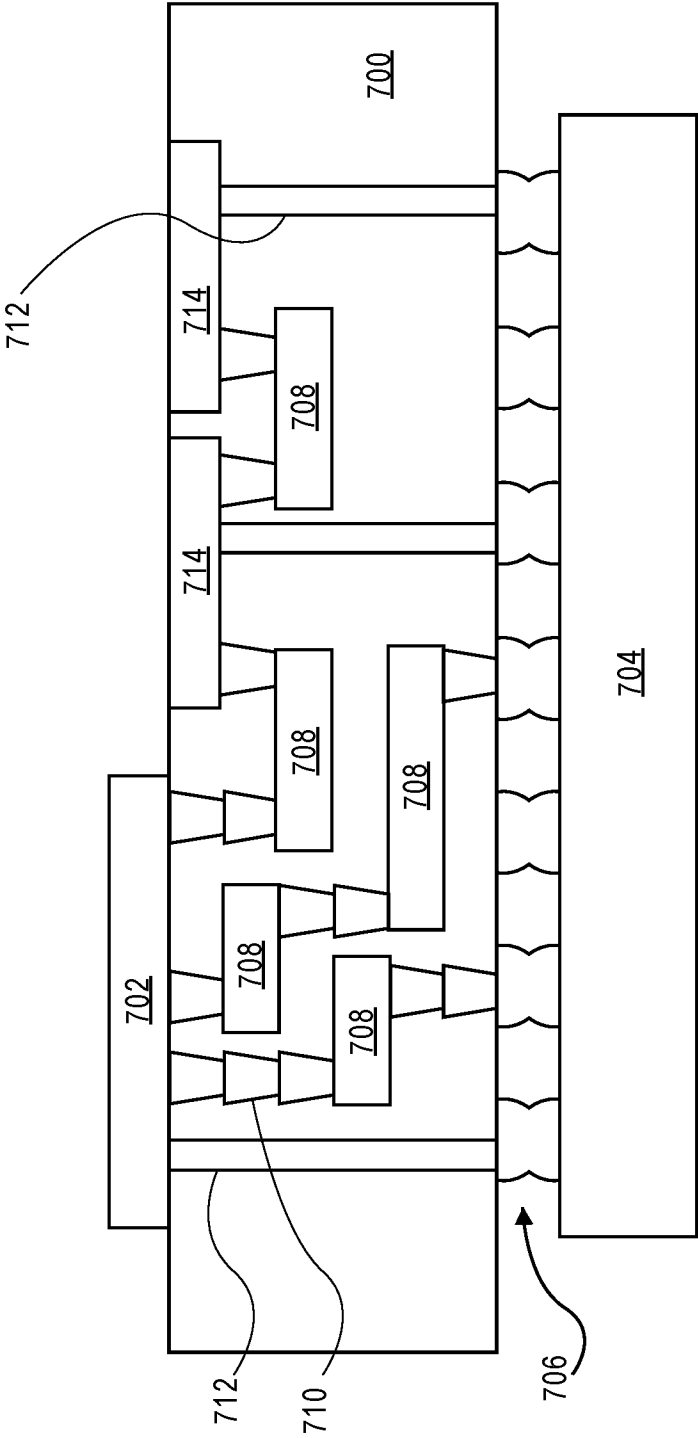


FIG. 7

A. CLASSIFICATION OF SUBJECT MATTER**H01L 29/778(2006.01)i, H01L 29/423(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/778; H01L 21/768; H01L 29/08; H01L 29/78; H01L 21/338; H01L 29/40; H01L 29/06; H01L 29/10; H01L 29/423

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, drain field plate, gate structure, dielectric layer, trench

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2017-0200794 A1 (NXP USA, INC.) 13 July 2017	1-7,9-11
A	See paragraphs [0019]-[0032], [0070]-[0071], claim 19 and figures 1-2A.	8,12-22
Y	US 2015-0179793 A1 (TEXAS INSTRUMENTS INCORPORATED) 25 June 2015	1-7,9-11
	See paragraphs [0022]-[0051] and figures 1, 8.	
A	US 2017-0194491 A1 (GLOBALFOUNDRIES SINGAPORE PTE. LTD.) 06 July 2017	1-22
	See paragraphs [0013]-[0040] and figure 1b.	
A	US 2016-0315188 A1 (GLOBALFOUNDRIES SINGAPORE PTE. LTD.) 27 October 2016	1-22
	See claim 1 and figures 1a-1d.	
A	JP 2008-078601 A (KOREA ADVANCED INST OF SCIENCE & TECHNOL) 03 April 2008	1-22
	See claim 1 and figure 1.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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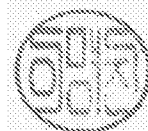
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017-0200794 A1	13/07/2017	US 2017-0077245 A1 US 9647075 B2	16/03/2017 09/05/2017
US 2015-0179793 A1	25/06/2015	US 2016-0300946 A1 US 9397211 B2	13/10/2016 19/07/2016
US 2017-0194491 A1	06/07/2017	US 2017-0309745 A1 US 9698260 B1	26/10/2017 04/07/2017
US 2016-0315188 A1	27/10/2016	SG 10201503305 A US 9741845 B2	29/11/2016 22/08/2017
JP 2008-078601 A	03/04/2008	KR 10-0782430 B1 US 2008-0073670 A1 US 2009-0261384 A1 US 7696535 B2	05/12/2007 27/03/2008 22/10/2009 13/04/2010