(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 September 2015 (17.09.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/138469 A1

(51) International Patent Classification:
G11C 11/22 (2006.01) *G11C 7/06* (2006.01)

(21) International Application Number:
PCT/US2015/019734

(22) International Filing Date:
10 March 2015 (10.03.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/950,351 10 March 2014 (10.03.2014) US
14/252,551 14 April 2014 (14.04.2014) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH,

[Continued on next page]

(54) Title: CIRCUIT AND METHOD FOR IMPRINT REDUCTION IN FRAM MEMORIES

(57) Abstract: In described examples, a method of operating a memory circuit includes writing true data (01) to a plurality of bits (B_0, B_1). A first data state (0) is written to a signal bit (B_i) indicating the true data. The true data is read, and complementary data (10) is written to the plurality of bits (B_0, B_1). A second data state (1) is written to the signal bit (B_i) indicating the complementary data.

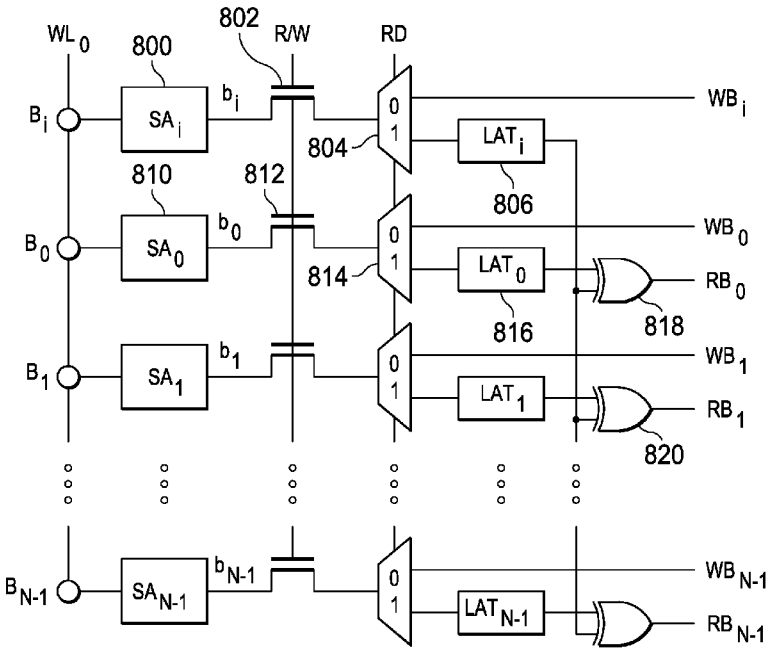

FIG. 8A

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GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

CIRCUIT AND METHOD FOR IMPRINT REDUCTION IN FRAM MEMORIES

BACKGROUND

[0001] Nonvolatile memory circuits, such as electrically erasable programmable read only memories (EEPROM) and flash EEPROMs, have been widely used for several decades in various circuit applications including computer memory, automotive applications, and video games. Each of these nonvolatile memory circuits has at least one nonvolatile memory element, such as a floating gate, silicon nitride layer, programmable resistance, or other nonvolatile memory element that maintains a data state when an operating voltage is removed. However, many new applications require the access time and packing density of previous generation nonvolatile memories, and low power consumption for battery powered circuits. One nonvolatile memory technology that is particularly attractive for these low power applications is the ferroelectric memory cell, which uses a ferroelectric capacitor for a nonvolatile memory element. A major advantage of these ferroelectric memory cells is that they require approximately three orders of magnitude less energy for write operations than previous generation floating gate memories. Furthermore, they do not require high voltage power supplies for programming and erasing charge stored on a floating gate. Thus, circuit complexity is reduced and reliability increased.

[0002] The term ferroelectric is something of a misnomer, because modern ferroelectric capacitors contain no ferrous material. Typical ferroelectric capacitors include a dielectric of ferroelectric material formed between two closely-spaced conducting plates. One well-established family of ferroelectric materials, known as perovskites, has a general formula ABO_3. This family includes lead zirconate titanate (PZT) having a formula $Pb(Zr_xTi_{1-x})O_3$. This material is a dielectric with a desirable characteristic, in which a suitable electric field will displace a central atom of the lattice. This displaced central atom, either titanium or zirconium, remains displaced after the electric field is removed, thereby storing a net charge. Another family of ferroelectric materials is strontium bismuth titanate

(SBT) having a formula $SbBi_2Ta_2O_9$. SBT has several advantages over PZT. Memories fabricated from either ferroelectric material have a destructive read operation. Accordingly, the act of reading a memory cell destroys the stored data, so it must be rewritten before the read operation is terminated.

[0003] FIG. 1 shows a conventional one-transistor, one-capacitor (1T1C) ferroelectric memory cell. The ferroelectric memory cell is similar to a 1T1C dynamic random access memory (DRAM) cell, except for ferroelectric capacitor 100. The ferroelectric capacitor 100 is connected between plate line 110 and storage node 112. Access transistor 102 has a current path connected between bit line 108 and storage node 112. A control gate of access transistor 102 is connected to word line 106 to control reading and writing of data to the ferroelectric memory cell. This data is stored as a polarized charge corresponding to cell voltage V_{CAP}. Capacitance of bit line BL is represented by capacitor C_{BL} 104.

[0004] In FIG. 2, a hysteresis curve corresponds to the ferroelectric capacitor 100. The hysteresis curve includes net charge Q or polarization along the vertical axis and applied voltage along the horizontal axis. By convention, the polarity of the ferroelectric capacitor voltage is defined as shown in FIG. 1. Accordingly, a stored "0" is characterized by a positive voltage at the plate line terminal with respect to the access transistor terminal. A stored "1" is characterized by a negative voltage at the plate line terminal with respect to the access transistor terminal. A "0" is stored in a write operation by applying a voltage Vmax across the ferroelectric capacitor. This stores a saturation charge Qs in the ferroelectric capacitor. However, the ferroelectric capacitor includes a linear component in parallel with a switching component. Therefore, when the electric field is removed, the linear component discharges, but the residual charge Qr remains in the switching component. The stored "0" is rewritten as a "1" by applying –Vmax to the ferroelectric capacitor. This charges the linear and switching components of the ferroelectric capacitor to a saturation charge of –Qs. The stored charge reverts to –Qr when the voltage across the ferroelectric capacitor is removed. Coercive points V_C and $-V_C$ are minimum voltages on the hysteresis curve that will degrade a stored data state. For example, application of V_C across a ferroelectric capacitor will degrade a stored "1" even though it is not sufficient to store a "0". Thus, it is particularly

important to avoid voltages near these coercive points unless the ferroelectric capacitor is being accessed. Moreover, power supply voltage across a ferroelectric capacitor must exceed these coercive voltages during a standby or sleep mode avoid data loss.

[0005] FIG. 3 shows a typical write sequence for a ferroelectric memory cell as in FIG. 1. Initially, the bit line (BL), word line (WL), and plate line (PL) are all low. The upper row of hysteresis curves illustrates a write "1", and the lower row represents a write "0". Either a "1" or "0" is initially stored in each example memory cell. The write "1" is performed when the bit line BL and word line WL are high and the plate line PL is low. This places a negative voltage across the ferroelectric capacitor and charges it to –Qs. When plate line PL goes high, the voltage across the ferroelectric capacitor is 0 V, and the stored charge reverts to –Qr. At the end of the write cycle, both bit line BL and plate line PL go low, and stored charge –Qr remains on the ferroelectric capacitor. Alternatively, the write "0" occurs when bit line BL remains low and plate line PL goes high. This places a positive voltage across the ferroelectric capacitor and charges it to Qs representing a stored "0". When plate line PL goes low, the voltage across the ferroelectric capacitor is 0 V, and the stored charge reverts to Qr representing a stored "0".

[0006] A read operation is illustrated at FIG. 4 for the ferroelectric memory cell at FIG. 1. The upper row of hysteresis curves illustrates a read "0". The lower row of hysteresis curves illustrates a read "1". Word line WL and plate line PL are initially low. Bit lines BL are precharged low. At time t_0, bit line precharge signal PRE goes low, permitting the bit lines BL to float. At time t_1, word line WL goes high. At time t_2, plate line PL goes high. This permits each memory cell to share charge with a respective bit line. A stored "1" will share more charge with parasitic bit line capacitance C_{BL} and produce a greater bit line voltage than the stored "0" as shown at time t_3. A reference voltage (not shown) is produced at each complementary bit line of an accessed bit line. This reference voltage is between the "1" and "0" voltages. Sense amplifiers are activated at time t_3 to amplify the difference voltage between the accessed bit line and the complementary bit line. When respective bit line voltages are fully amplified, the read "0" curve cell charge has increased from Qr to Qs. By way of comparison, the read "1" data state has changed from a stored "1" to a stored "0".

Thus, the read "0" operation is nondestructive, but the read "1" operation is destructive. At time t_4, plate line PL goes low and applies –Vmax to the read "1" cell, thereby storing -Qs. At the same time, zero voltage is applied to the read "0" cell, and charge Qr is restored. At the end of the read cycle, signal PRE goes high and precharges both bit lines BL to zero volts or ground. Thus, zero volts is applied to the read "1" cell, and –Qr is restored.

[0007] Referring to FIG. 5, a pulse sensing read operation is illustrated for a ferroelectric memory circuit. The read operation begins at time t_0 when precharge signal PRE goes low, permitting the bit lines BL to float. Word line WL and plate line PL are initially low, and bit lines BL are precharged low. At time t_1, word line WL goes high, thereby coupling a ferroelectric capacitor to a respective bit line. Then plate line PL goes high at time t_2, thereby permitting each memory cell to share charge with the respective bit line. The ferroelectric memory cells share charge with their respective bit lines BL and develop respective difference voltages. Here, V_1 represents a data "1", and V_0 represents a data "0". Plate line PL then goes low prior to time t_3, and the common mode difference voltage goes to near zero. The difference voltage available for sensing is the difference between: one of V_1 and V_0 at time t_3; and a reference voltage (not shown) which lies approximately midway between voltages V_1 and V_0 at time t_3. The difference voltage is amplified at time t_3 by respective sense amplifiers, and full bit line BL voltages are developed while the plate line PL is low. Thus, the data "1" cell is fully restored while plate line PL is low and the data "1" bit line BL is high. Subsequently, the plate line PL goes high while the data "0" bit line BL remains low. Thus, the data "0" cell is restored. The plate line PL goes low at time t_4, and precharge signal PRE goes high at time t_5. The high level of precharge signal PRE precharges the bit lines to ground or Vss. The word line WL goes low at time t_6, thereby isolating the ferroelectric capacitor from the bit line and completing the pulse sensing cycle.

[0008] Each of the foregoing read, write, and restore operations of the ferroelectric memory induce retained polarization domains within the ferroelectric capacitor 100. This is particularly true when a maximum electric field is applied to the ferroelectric capacitor at +/– Vmax. This phenomenon is often referred to as imprinting and may degrade the memory cell (FIG. 1) signal margin when reading an opposite data state. For example, when a "0" is

frequently written to the memory cell followed by writing a "1", residual charge may remain more positive than –Qr (FIG. 2), thereby degrading the "1" signal margin. Likewise, when a "1" is frequently written to the memory cell followed by writing a "0", residual charge may remain more negative than Qr, thereby degrading the "0" signal margin.

SUMMARY

[0009] In described examples, a method of operating a memory circuit includes writing true data to a plurality of bits, and writing a first data state to a signal bit indicating the true data. The true data is read, and complementary data is written to the plurality of bits. A second data state is written to the signal bit indicating the complementary data.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a circuit diagram of a conventional ferroelectric memory cell.

[0011] FIG. 2 is a hysteresis curve of the ferroelectric capacitor 100 of FIG. 1.

[0012] FIG. 3 is a timing diagram of a write operation to the ferroelectric memory cell of FIG. 1.

[0013] FIG. 4 is a timing diagram of a read operation from the ferroelectric memory cell of FIG. 1.

[0014] FIG. 5 is a timing diagram of a pulse sense read cycle.

[0015] FIG. 6A is a schematic diagram of a column of 1T1C ferroelectric memory cells of the example embodiments.

[0016] FIG. 6B is a schematic diagram of a column of 2T2C ferroelectric memory cells of the example embodiments.

[0017] FIG. 7A is a schematic diagram of an inverting sense amplifier circuit of the example embodiments that may be used with the ferroelectric memory circuits of FIGS. 6A and 6B.

[0018] FIG. 7B is a timing diagram of operation of the inverting sense amplifier circuit of FIG. 7A.

[0019] FIG. 8A is a schematic diagram of a memory circuit of the example embodiments, showing conditional inversion of a data word.

[0020] FIG. 8B is a truth table of operation of the circuit of FIG. 8A.

[0021] FIG. 8C is a schematic diagram of a memory circuit of the example embodiments, showing conditional inversion of a data word with error checking and correction (ECC).

[0022] FIG. 9 is a schematic diagram of an exclusive OR (XOR) gate that may be used with the memory circuits of FIGS. 8A and 8C.

[0023] FIG. 10 is a block diagram of a wireless telephone as an example of a portable electronic device which could advantageously employ the example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0024] The example embodiments provide significant advantages in imprint reduction of a memory circuit. The example embodiments may be applied to any memory circuit, such as static random access memory circuits, resistive random access memory circuits, magnetic random access memory circuits, or any other memory circuit that may develop a biased signal margin after multiple asymmetric read or write operations.

[0025] FIG. 6A is a schematic diagram of a column of one-transistor, one-capacitor (1T1C) ferroelectric memory cells according to a first embodiment. A ferroelectric memory array includes plural columns of memory cells arranged in parallel. The memory array also includes plural rows of memory cells defined by N parallel word lines WL_0 through WL_{N-1}. The memory cells are arranged in pairs and coupled to adjacent word lines and complementary bit lines BL and /BL. For example, word line WL_0 is connected to a control terminal of access transistor 606. Access transistor 606 has a current path coupled between complementary bit line /BL and ferroelectric capacitor 608. Ferroelectric capacitor 608 is coupled to a common plate line terminal PL. Word line WL_1 is connected to a control terminal of access transistor 602. Access transistor 602 has a current path coupled between bit line BL and ferroelectric capacitor 604. Ferroelectric capacitor 604 is also coupled to a common plate line terminal PL. The column further includes a bit line precharge circuit having two n-channel transistors arranged to precharge bit lines BL and /BL to VSS or ground in response to a high level of precharge signal PRE.

[0026] A bit line reference circuit is arranged to apply voltage VREF to one of bit lines BL and /BL during a read operation. For example, if a memory cell connected to bit line BL is selected, complementary bit line /BL receives reference voltage VREF in response to a

high level of control signal /RFW. Likewise, if a memory cell connected to bit line /BL is selected, bit line BL receives reference voltage VREF in response to a high level of control signal RFW. Sense amplifier 600 amplifies a difference voltage between bit lines BL and /BL during a read operation in response to control signals SAEN and /SAEN (not shown in FIG. 6A). These control signals activate sense amplifier 600, which applies the amplified data signal to data lines DL and /DL via n-channel read/write transistors in response to a high level of control signal R/W.

[0027] FIG. 6B is a schematic diagram of a column of two-transistor, two capacitor (2T2C) ferroelectric memory cells according to a second embodiment. Here and in the following discussion, the same reference numerals indicate substantially the same elements. A ferroelectric memory array includes plural columns of memory cells arranged in parallel. The memory array also includes plural rows of memory cells defined by N parallel word lines WL_0 through WL_{N-1}. In the 2T/2C embodiment, the memory cells are arranged in pairs and coupled to a respective word line and complementary bit lines BL and /BL. For example, word line WL_0 is connected to control terminals of access transistors 610 and 614. Access transistor 610 has a current path coupled between bit line BL and ferroelectric capacitor 612. Access transistor 614 has a current path coupled between complementary bit line /BL and ferroelectric capacitor 616. Ferroelectric capacitors 612 and 616 are coupled to a common plate line terminal PL. During a read operation, charge on each of ferroelectric capacitors 612 and 616 is applied to respective bit lines BL and /BL via access transistors 610 and 614, thereby providing a greater signal margin than the 1T1C memory cell.

[0028] FIG. 7A is a schematic diagram of an inverting sense amplifier circuit 600 of the example embodiments that may be used with the ferroelectric memory circuits of FIGS. 6A and 6B. The sense amplifier circuit includes a sense amplifier having P-channel transistors 716 and 720 arranged in a cross-coupled configuration with N-channel transistors 718 and 722. An N-channel sense amplifier enable (SAEN) transistor 724 is coupled between a common source terminal of N-channel transistors 718 and 722 and power supply terminal VSS. A P-channel complementary sense amplifier enable (/SAEN) transistor 700 is coupled between a common source terminal of P-channel transistors 716 and 720 and power supply

terminal VDD. N-channel switching transistor 712 is coupled between a common drain terminal of transistors 716 and 718 and bit line BL. N-channel switching transistor 714 is coupled between a common drain terminal of transistors 708 and 710 and complementary bit line /BL. Switching transistors 712 and 714 are controlled by bit line multiplex signal BLMUX. A first inverter, formed by P-channel transistor 706 and N-channel transistor 704, has an input terminal coupled to the common drain terminal of transistors 716 and 718 and an output terminal coupled to bit line BL. A second inverter, formed by P-channel transistor 710 and N-channel transistor 708, has an input terminal coupled to the common drain terminal of transistors 720 and 722 and an output terminal coupled to complementary bit line /BL. The first and second inverters are enabled by P-channel transistor 702 and control signal /BLRSTR together with N-channel transistor 724 and control signal SAEN.

[0029] Operation of the inverting sense amplifier circuit 600 of FIG. 7A is explained with reference to the timing diagram of FIG. 7B. Initially, all signals of FIG. 7B are low, except for complementary sense amplifier enable signal /SAEN and complementary bit line restore signal /BLRSTR. Bit lines BL and /BL are precharged to VSS. At time t0, word line WL goes high to select a row of memory cells. Here, word line WL may be any of word lines WL_0 through WL_{N-1} of FIGS. 6A or 6B. At time t1, plate line signal PL pulses high to read data from a selected memory cell and produce a difference voltage between bit lines BL and /BL. Bit line multiplex signal BLMUX also goes high to turn on switching transistors 712 and 714, thereby coupling bit lines BL and /BL to the sense amplifier. At time t2, when the difference voltage is sufficiently developed at the sense amplifier, complementary sense amplifier enable signal /SAEN goes low to turn on P-channel transistor 700 and apply a positive voltage from power supply VDD to the common source terminal of P-channel transistors 716 and 720. This positive voltage provides some initial amplification of the difference voltage. At time t3, control signal BLMUX goes low to turn off switching transistors 712 and 714, thereby isolating bit lines BL and /BL from the sense amplifier. Sense amplifier enable signal SAEN goes high to turn on N-channel transistor 724 and enable the inverters formed by transistors 704 through 710. N-channel transistor 724 couples the common source terminal of transistors 718 and 722 to power supply terminal VSS,

thereby further amplifying the difference voltage at the sense amplifier. At time t4, read/write signal R/W goes high to apply the amplified difference voltage to data lines DL and /DL (FIGS. 6A or 6B). Complementary bit line restore signal /BLRSTR goes low to turn on P-channel transistor 702 and apply power supply voltage VDD to the common source terminal of P-channel inverter transistors 706 and 710. Inverters formed by transistors 704 through 710 subsequently write an inverted data signal to the selected memory cell. For example, a memory cell on bit line BL that produced a positive difference voltage with respect to complementary bit line /BL ("1") would be rewritten as a negative voltage on bit line BL with respect to complementary bit line /BL ("0"). This is because the first inverter, formed by transistors 704 and 706, inverts the original data signal on bit line BL. Likewise, the second inverter, formed by transistors 708 and 710, inverts the original data signal on complementary bit line /BL.

[0030] The inverting sense amplifier circuit 600 (FIG. 7A) is highly advantageous for several reasons. First, the original data signal read from each memory cell is unconditionally rewritten as an opposite data state. This greatly reduces imprinting within the memory cells by annealing polarized domains of the ferroelectric capacitor. Second, there is no speed penalty in the inverting sense amplifier, because read/write signal R/W is activated as soon as the difference voltage is sufficiently amplified and applied to data lines DL and /DL. Third, the sense amplifier formed by transistors 704 through 710 does not directly restore bit lines BL and /BL. The amplified difference voltage is inverted and driven onto bit lines BL and /BL by respective first (704-706) and second (708-710) inverters. This additional buffering by the first and second inverters reduces the load on the sense amplifier, so it can more easily drive data lines DL and /DL. Finally, because the capacitive load of bit lines (BL, /BL) and data lines (DL, /DL) is divided between the inverters and sense amplifier, respectively, transistor sizes may be reduced, so only a small area penalty occurs.

[0031] FIG. 8A is a schematic diagram of a memory circuit of the example embodiments, showing conditional inversion of a data word. From the previous discussion, inverting sense amplifier circuit 600 unconditionally inverts data read from a selected memory cell and restores the inverted data to the selected memory cell. Therefore, in response to a

determination of whether data from the inverting sense amplifier is original or inverted data, the data is conditionally inverted. This determination is made by signal bit or inverting bit (B_i). The memory circuit of FIG. 8A includes a row of ferroelectric memory cells B_i and B_0 through B_{N-1} that are selected by word line WL_0. Data from each ferroelectric memory cell is amplified during a read operation by a respective sense amplifier. For example, signal bit B_i is amplified by inverting sense amplifier circuit 800 to produce amplified signal bit b_i. Signal bit b_i is applied to multiplex circuit 804 via read/write (R/W) transistor 802. Multiplex circuit 804 subsequently applies signal bit b_i from a respective data line to latch circuit 806 in response to a high level ("1") of control signal RD. Latch circuit 806 latches signal bit b_i and applies it to one terminal of each exclusive OR (XOR) gate corresponding to a data column such as XOR gates 818 and 820. Alternatively, during a write operation, write signal bit WB_i is applied through multiplex circuit 804 in response to a low level of control signal RD to read/write transistor 802, sense amplifier circuit 800, and a respective bit line BL or /BL.

[0032] Data signals from other ferroelectric memory cells of the row operate in a similar manner. For example, data bit B_0 is amplified by inverting sense amplifier circuit 810 to produce amplified data bit b_0. Data bit b_0 is applied to multiplex circuit 814 via read/write (R/W) transistor 812. Multiplex circuit 814 subsequently applies data bit b_0 from a respective data line to latch circuit 816 in response to a high level ("1") of control signal RD. Latch circuit 816 latches data bit b_0 and applies it to one terminal of XOR gate 818. Alternatively, during a write operation, write data bit WB_0 is applied through multiplex circuit 814 in response to a low level of control signal RD to read/write transistor 812, sense amplifier circuit 810, and a respective bit line BL or /BL.

[0033] Operation of the memory circuit of FIG. 8A is explained with reference to the truth table of FIG. 8B. The left column of the truth table indicates a previous logical operation, such as a READ or WRITE operation. Each row of the truth table shows the logical values of signals identified in FIG. 8A after the logical operation. In particular, the first row indicates initial values after a first write. Signal bit B_i is 0, and data bits B_0 and B_1 are 01, respectively. Signal bit b_i, amplified data bits b_0 and b_1, and read bits RB_0 and RB_1 are "do not care" values as indicated by "X." After a first read operation in the second row, signal bit

b_i, amplified data bits b_0 and b_1, and read bits RB_0 and RB_1 are 00101, respectively. Signal bit b_i has the same value as memory cell signal bit B_i after the initial write operation in the first row. The 0 value of signal bit b_i indicates amplified data bits b_0 and b_1 (01) are not to be inverted. An XOR of the 0 signal bit b_i with amplified data bits b_0 and b_1 (01) produces a 01 output at respective XOR gates 818 and 820. Thus, read bits RB_0 and RB_1 are 01, respectively. Memory cell signal bit B_i and memory cell data bits B_0 and B_1 in the second row are each rewritten in an inverted state (110) by a respective inverting sense amplifier as previously explained.

[0034] After a second read operation in the third row, signal bit $b_{i,,}$ amplified data bits b_0 and b_1, and read bits RB_0 and RB_1 are 11001, respectively. Signal bit b_i and amplified data bits b_0 and b_1 have the same value as memory cell signal bit B_i and memory cell data bits B_0 and B_1 in the second row. These are inverted data states from the original write data of the first row (001). The 1 value of signal bit b_i indicates amplified data bits b_0 and b_1 (10) must be inverted. An XOR of the 1 signal bit b_i with amplified data bits b_0 and b_1 (10) produces a 01 output at respective XOR gates 818 and 820. Thus, read bits RB_0 and RB_1 are 01, respectively. Memory cell signal bit B_i and memory cell data bits B_0 and B_1 are each rewritten in an inverted state (001) by a respective inverting sense amplifier as previously explained.

[0035] The third and fourth read operations are the same as previously explained. In each row, read data bits RB_0 and RB_1 are 01 as originally written to the memory cell data bits in the first row. Each even-numbered read operation rewrites the original data (001) into the memory cell signal and data bits. However, each odd-numbered read rewrites inverted data (110) into the memory cell signal and data bits. As previously discussed, this is highly advantageous for several reasons. First, the original data signal read from each memory cell is unconditionally rewritten as an opposite data state. This greatly reduces imprinting within the memory cells by annealing polarized domains of the ferroelectric capacitor. Second, there is no significant speed penalty in the read path, because the XOR gate is also used for buffering the amplified data bits b_0 and b_1 in the read data path. The read/write signal R/W is activated as soon as the difference voltage is sufficiently amplified and applied to data lines

DL and /DL without additional gate delays. Third, the write data path is unaffected, because a multiplex circuit is required to distinguish between read and write data. Finally, implementation is accomplished with minimum additional circuit complexity of the inverting sense amplifier circuit 600 and XOR gates such as 818-820.

[0036] FIG. 8C is a schematic diagram of a memory circuit of the example embodiments, showing conditional inversion of a data word with error checking and correction or error correction code (ECC). The circuit is similar to the circuit of FIG. 8A, except that ECC circuit 830 is added between read/write transistors (such as 802 and 812) and multiplex circuits (such as 804 and 814). The ECC circuit may use a single-error correction, double-error detection (SECDED) Hamming code, which was invented by Richard Hamming in 1950. The Hamming code adds parity bits to the data bits and is effective for detecting double-bit errors and correcting single-bit errors. The ECC circuit 830 preferably includes a code corresponding to a desired word size. For each valid code word C, a valid inverted code word ~C may be used for SECDED with an inverted data word. Here, a valid code word is one that performs a specific error detection and correction operation, such as SECDED on a data word.

[0037] Other codes may be used in the ECC circuit to perform SECDED, as is known in the art, so long as they satisfy the property that both code words C and ~C are valid. Moreover, cyclic error-correcting codes such as BCH codes may be used in ECC circuit 830 to correct multiple bit errors in a single data word, such as double-error correction and triple-error detection (DECTED). BCH codes were first invented in 1959 by Alexis Hocquenghem and later independently invented in 1960 by Raj Bose and D.K. Ray-Chaudhuri. The BCH code name is derived from the inventors' initials. BCH codes are known in the art and used in satellite communications, compact disk players, DVD, disk drives, solid-state drives, and two-dimensional bar codes.

[0038] FIG. 9 is a schematic diagram of an exclusive OR (XOR) gate 818 that may be used with the memory circuits of FIGS. 8A and 8C. Here, A and B are the two XOR input signals, and Y is the output signal. The XOR gate includes: a left branch formed by series-connected transistors 902 through 908; and a right branch formed by series-connected

transistors 910 through 916. Inverter 900 receives the B input signal and generates complementary input signal /B. In operation, when input signal B is high, transistors 904 and 906 are both off and disable the left branch. The high state of B and the corresponding low state of /B turn on N-channel transistor 914 and P-channel transistor 912, respectively. The right branch then operates as a simple inverter having input signal A. Thus, when B is high, Y is the inverse of A. Alternatively, when B is low and /B is high, transistors 912 and 914 are both off and disable the right branch. The low state of B and the corresponding high state of /B turn on P-channel transistor 904 and N-channel transistor 906, respectively. Transistors 910 and 916 operate as a first inverter to produce complementary signal /A at the control gate of transistors 902 and 908. Transistors 902 and 908 then operate as a simple inverter having input signal /A. Thus, when B is low, Y is equal to A.

[0039] FIG. 10 is a block diagram of a wireless telephone as an example of a portable electronic device that could advantageously employ the example embodiments in a nonvolatile memory array. The wireless telephone includes antenna 1000, radio frequency transceiver 1002, base band circuits 1010, microphone 1006, speaker 1008, keypad 1020, and display 1022. The wireless telephone is preferably powered by a rechargeable battery (not shown) known in the art. Antenna 1000 permits the wireless telephone to interact with the radio frequency environment for wireless telephony in a manner known in the art. Radio frequency transceiver 1002 both transmits and receives radio frequency signals via antenna 1000. The transmitted signals are modulated by the voice/data output signals received from base band circuits 1010. The received signals are demodulated and supplied to base band circuits 1010 as voice/data input signals. An analog section 1004 includes an analog to digital converter 1024 connected to microphone 1006 to receive analog voice signals. The analog to digital converter 1024 converts these analog voice signals to digital data and applies them to digital signal processor 1016. Analog section 1004 also includes a digital to analog converter 1026 connected to speaker 1008. Speaker 1008 provides the voice output to the user. Digital section 1010 is embodied in one or more integrated circuits and includes a microcontroller unit 1018, a digital signal processor 1016, nonvolatile memory circuit 1012, and volatile memory circuit 1014. Nonvolatile memory circuit 1012 may include read only

memory (ROM), ferroelectric memory (FeRAM or FRAM), FLASH memory, or other nonvolatile memory known in the art. Volatile memory circuit 1014 may include dynamic random access memory (DRAM), static random access memory (SRAM), or other volatile memory circuits known in the art. Microcontroller unit 1018 interacts with keypad 1020 to receive telephone number inputs and control inputs from the user. Microcontroller unit 1018 supplies the drive function to display 1022 to display numbers dialed, the current state of the telephone such as battery life remaining, and received alphanumeric messages. Digital signal processor 1016 provides real time signal processing for transmit encoding, receive decoding, error detection and correction, echo cancellation, and voice band filtering. Both microcontroller unit 1018 and digital signal processor 1016 interface with nonvolatile memory circuit 1012 for program instructions and user profile data. Microcontroller unit 1018 and digital signal processor 1016 also interface with volatile memory circuit 1014 for signal processing, voice recognition processing, and other applications.

[0040] The example embodiments may be applied to any memory circuit, such as static random access memory circuits, resistive random access memory circuits, magnetic random access memory circuits, or any other memory circuit that may develop a biased signal margin after multiple asymmetric read or write operations.

[0041] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of operating a memory circuit, the method comprising:

writing data to a plurality of bits;

writing a first data state to a signal bit indicating the data;

reading the data from the plurality of bits;

writing complementary data to the plurality of bits; and

writing a second data state to the signal bit indicating the complementary data.

2. The method of claim 1, wherein the steps of writing include writing to a row of memory cells.

3. The method of claim 1, wherein the plurality of bits includes error checking and correction (ECC) bits and data bits.

4. The method of claim 3, wherein the ECC bits include a plurality of valid code words C, wherein each code word C has a valid complementary code word ~C.

5. The method of claim 4, wherein the ECC bits include one of a single-error correction, double-error detection (SECDED) and a double-error correction, triple-error detection (DECTED) code.

6. The method of claim 1, comprising:

applying the data to plural output terminals in response to the first data state;

inverting the complementary data in response to the second data state; and

applying the inverted complementary data to the output terminals.

7. The method of claim 1, comprising latching data from the plurality of bits and the signal bit in response to the step of reading.

8. The method of claim 1, comprising performing an exclusive OR of the signal bit with each bit of the plurality of bits.

9. The method of claim 1, comprising:

performing an exclusive OR of the signal bit with each bit of the plurality of bits.

10. An inverting sense amplifier circuit, comprising:

a memory cell;

a sense amplifier;

a first switching transistor coupled between the sense amplifier and the memory cell; and

a first inverter having an input terminal coupled to the sense amplifier and having an output terminal coupled to the memory cell.

11. The circuit of claim 10, wherein the memory cell is a one-transistor, one-capacitor (1T1C) memory cell.

12. The circuit of claim 10, wherein the memory cell is a two-transistor, two-capacitor (2T2C) memory cell.

13. The circuit of claim 10, comprising:

a second switching transistor coupled to the sense amplifier; and

a second inverter having an input terminal coupled to the sense amplifier and having an output terminal coupled to the second switching transistor.

14. The circuit of claim 10, comprising:

a bit line coupled between the memory cell and the sense amplifier; and

a word line coupled to the memory cell.

15. The circuit of claim 10, wherein the memory cell is a ferroelectric memory cell.

16. The circuit of claim 10, wherein the memory cell is one of a static random access memory (SRAM) cell, a magnetic random access memory (MRAM), and a resistive random access memory (RRAM) cell.

17. A system, comprising:

a processor circuit;

an input device coupled to the processor circuit;

an output device coupled to the processor circuit; and

an inverting sense amplifier circuit including: a memory cell; a sense amplifier; a switching transistor coupled between the memory cell and the sense amplifier; and an inverter having an input terminal coupled to the sense amplifier and having an output terminal coupled to the memory cell.

18. The system of claim 17, wherein the memory cell is a one-transistor, one-capacitor (1T1C) memory cell.

19. The system of claim 17, wherein the memory cell is a two-transistor, two-capacitor (2T2C) memory cell.

20. The system of claim 17, wherein the memory cell is a ferroelectric memory cell.

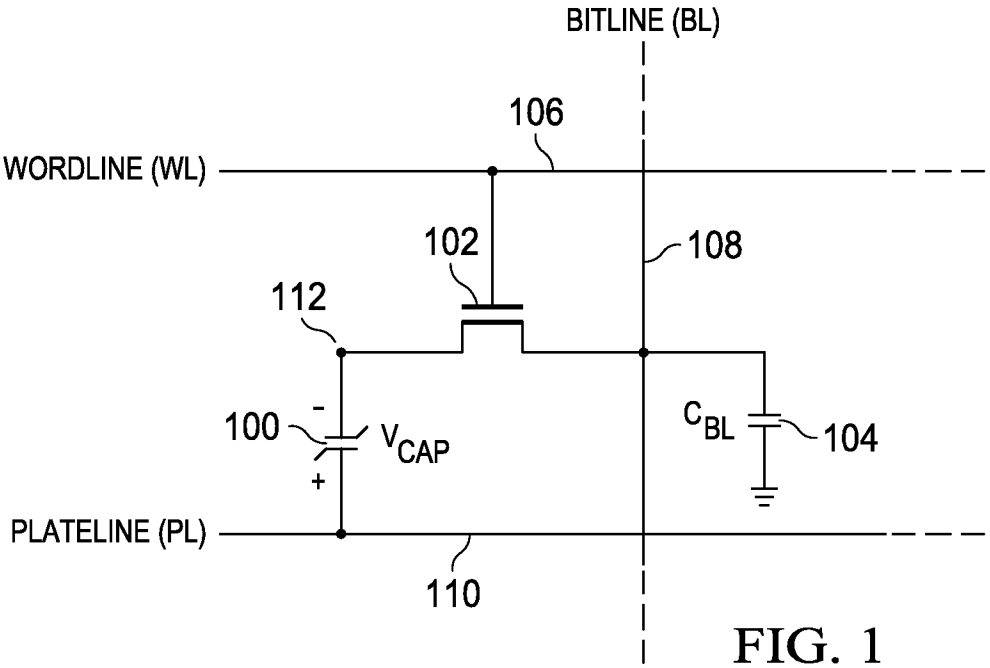

FIG. 1
(PRIOR ART)

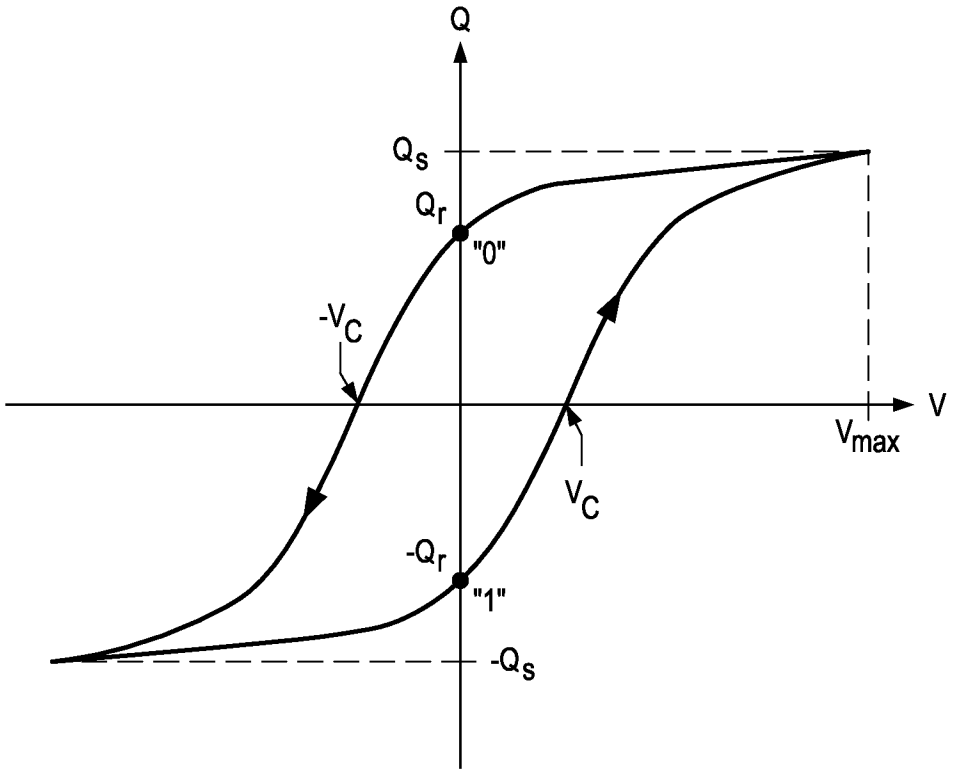

FIG. 2
(PRIOR ART)

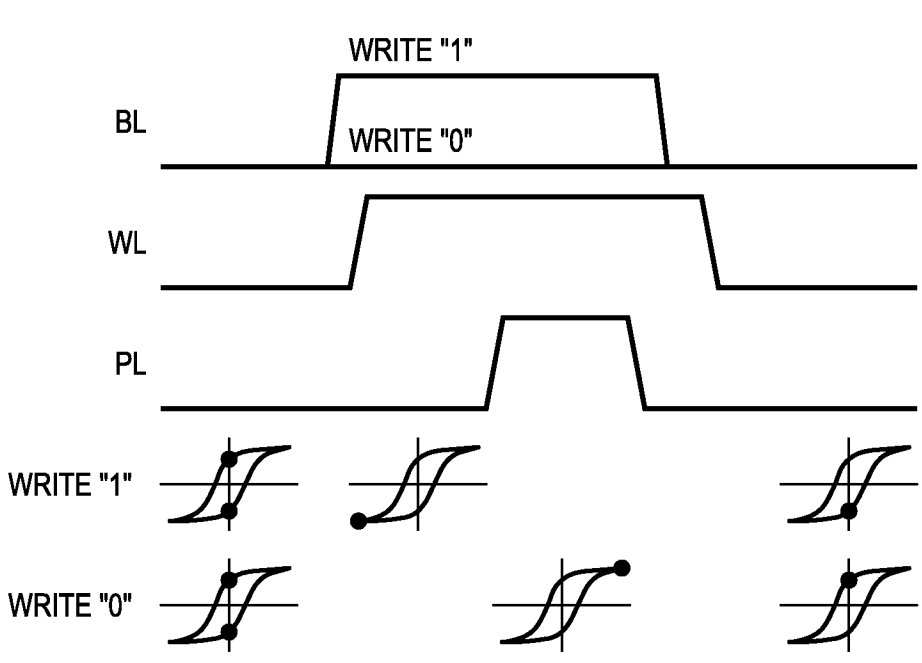

FIG. 3
(PRIOR ART)

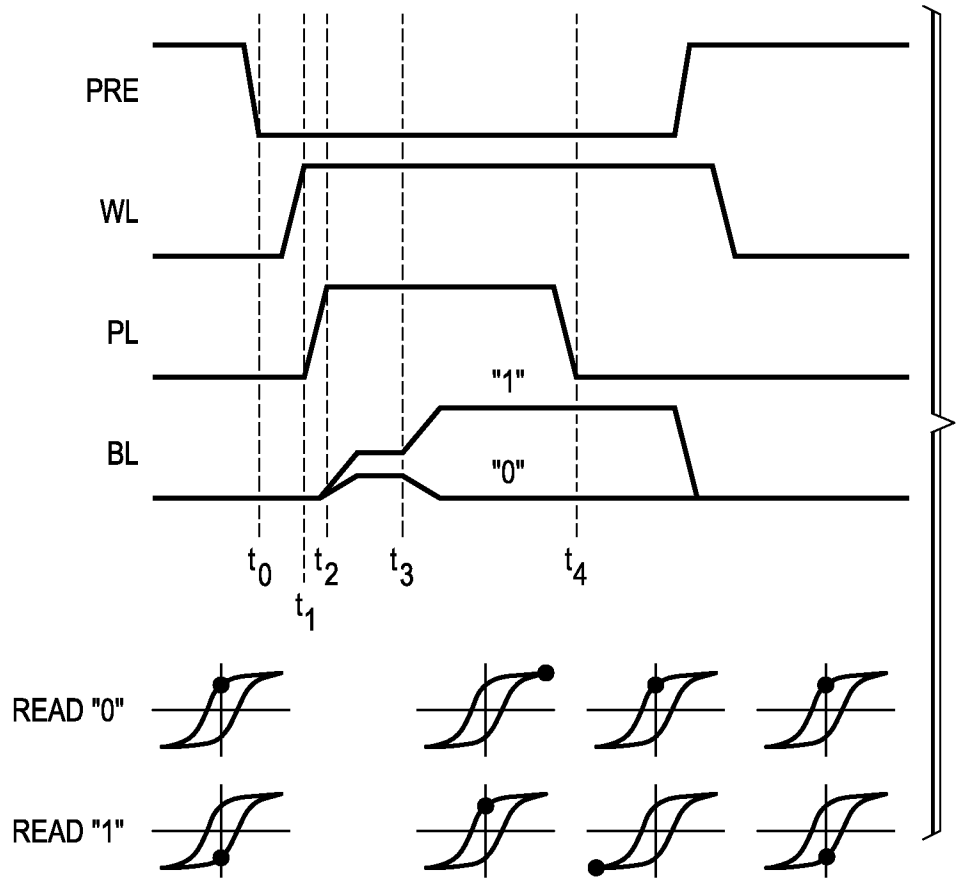

FIG. 4
(PRIOR ART)

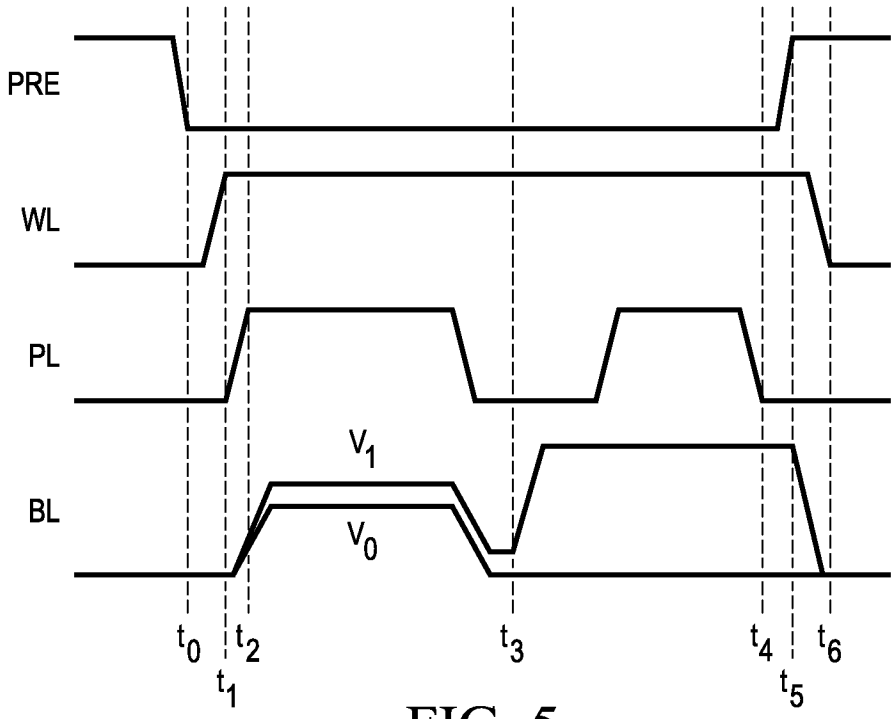

FIG. 5
(PRIOR ART)

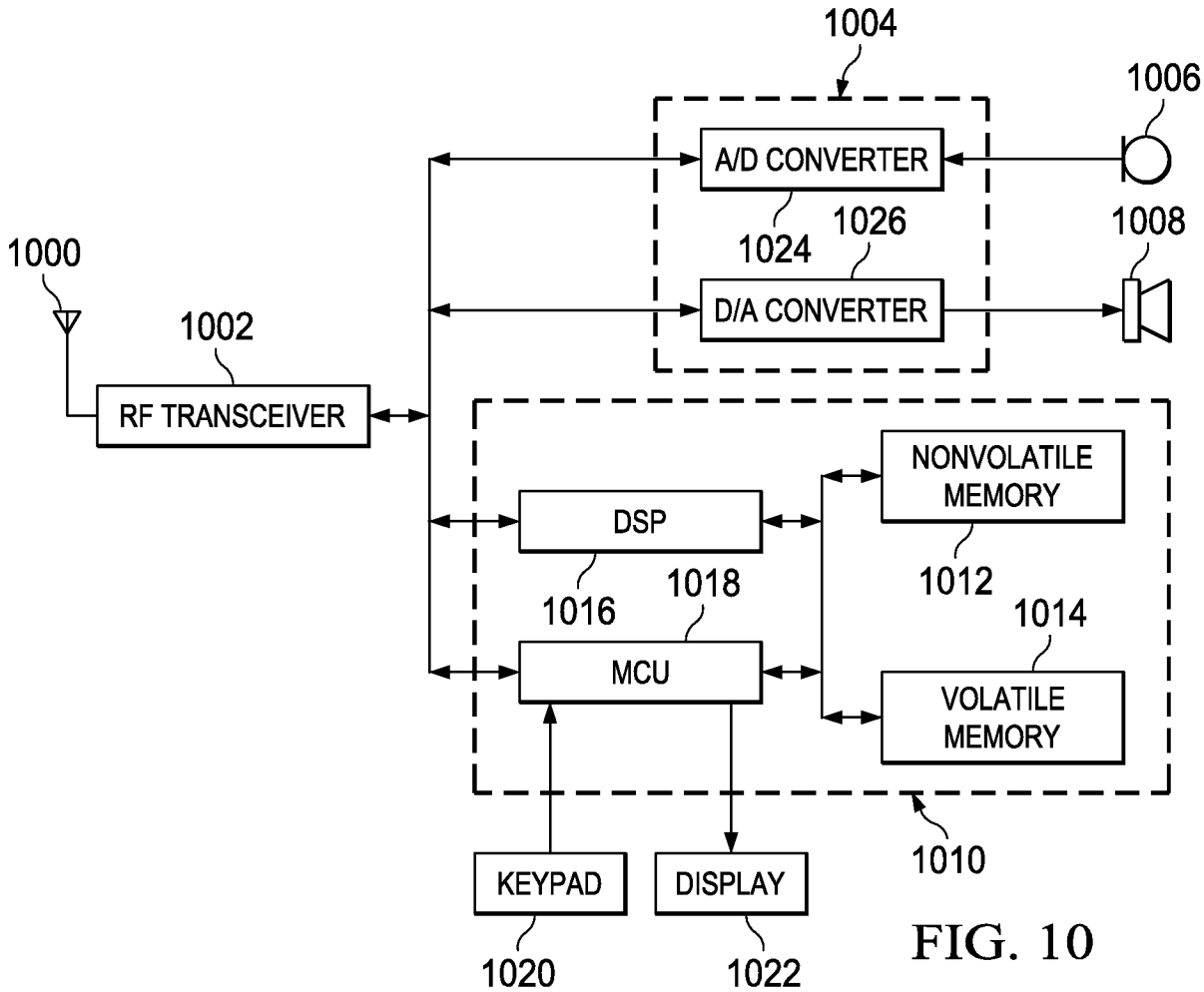

FIG. 10

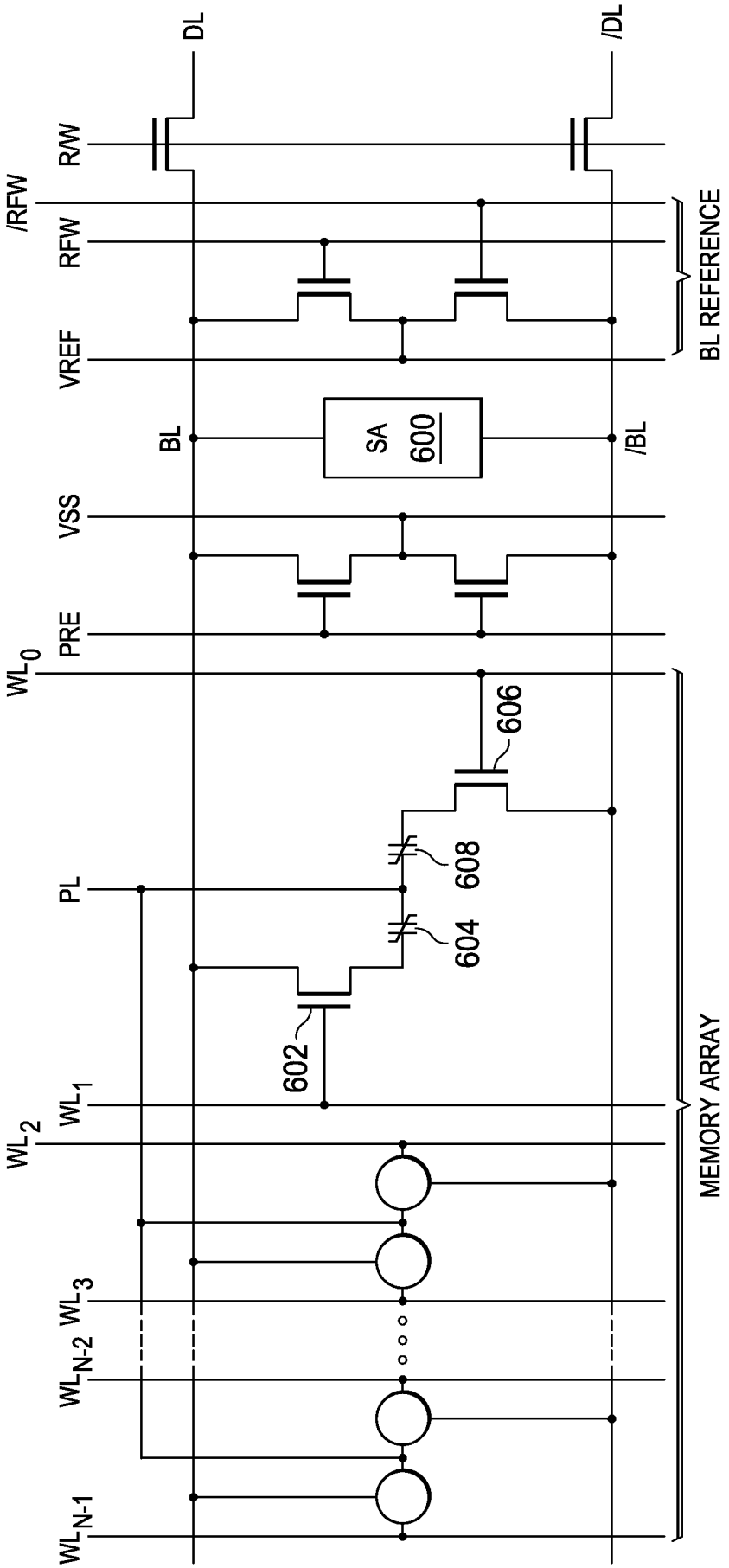
DL
/DL
R/W
/RFW
RFW
VREF
BL REFERENCE
BL
SA
600
/BL
VSS
PRE
WL0
606
608
PL
604
602
WL1
WL2
WL3
WLN-2
WLN-1
MEMORY ARRAY

FIG. 6A

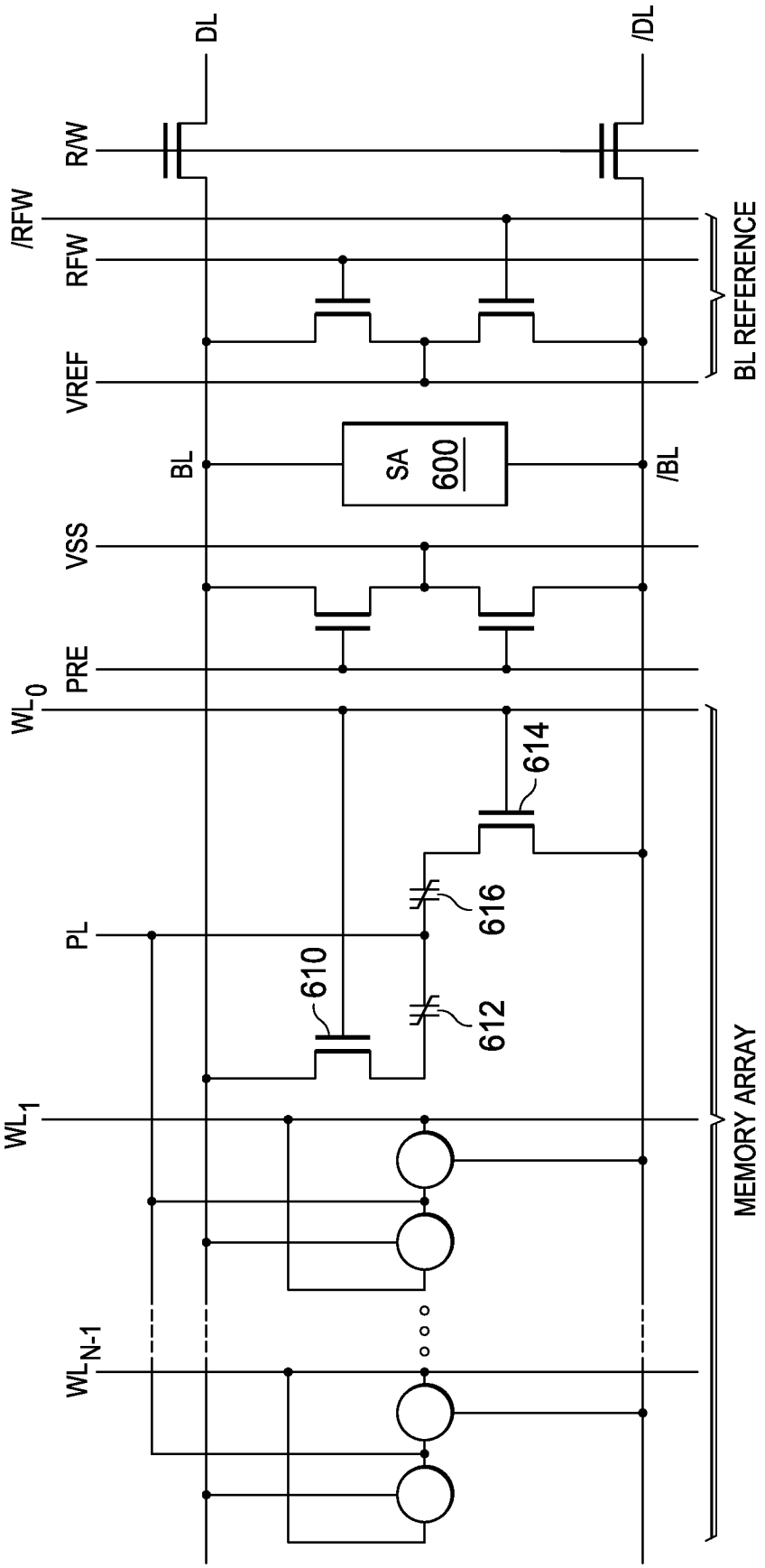
DL
/DL
R/W
/RFW
RFW
VREF
BL REFERENCE
BL
SA
600
/BL
VSS
PRE
WL0
614
616
PL
610
612
WL1
MEMORY ARRAY
WLN-1

FIG. 6B

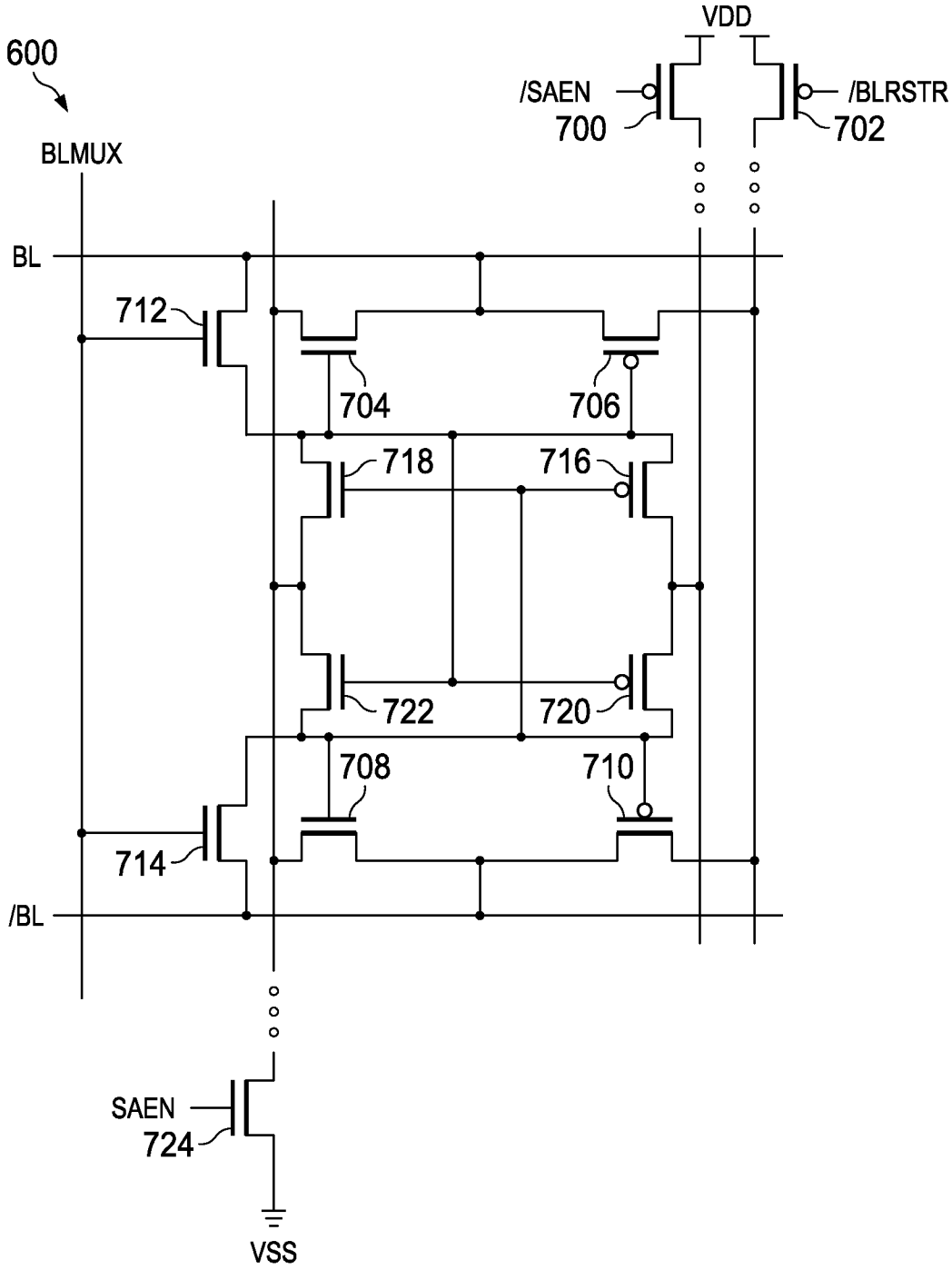
600
VDD
/SAEN
700
/BLRSTR
702
BLMUX
BL
712
704
706
718
716
722
720
708
710
714
/BL
SAEN
724
VSS

FIG. 7A

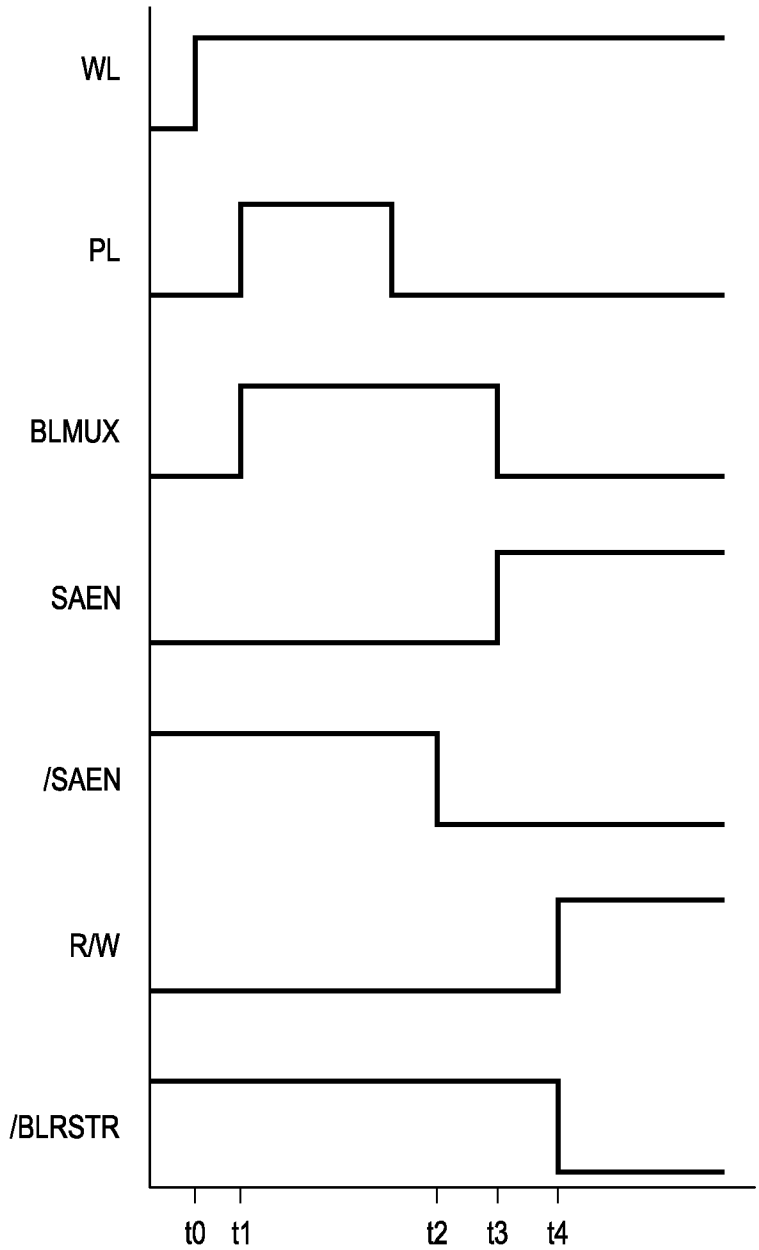

FIG. 7B

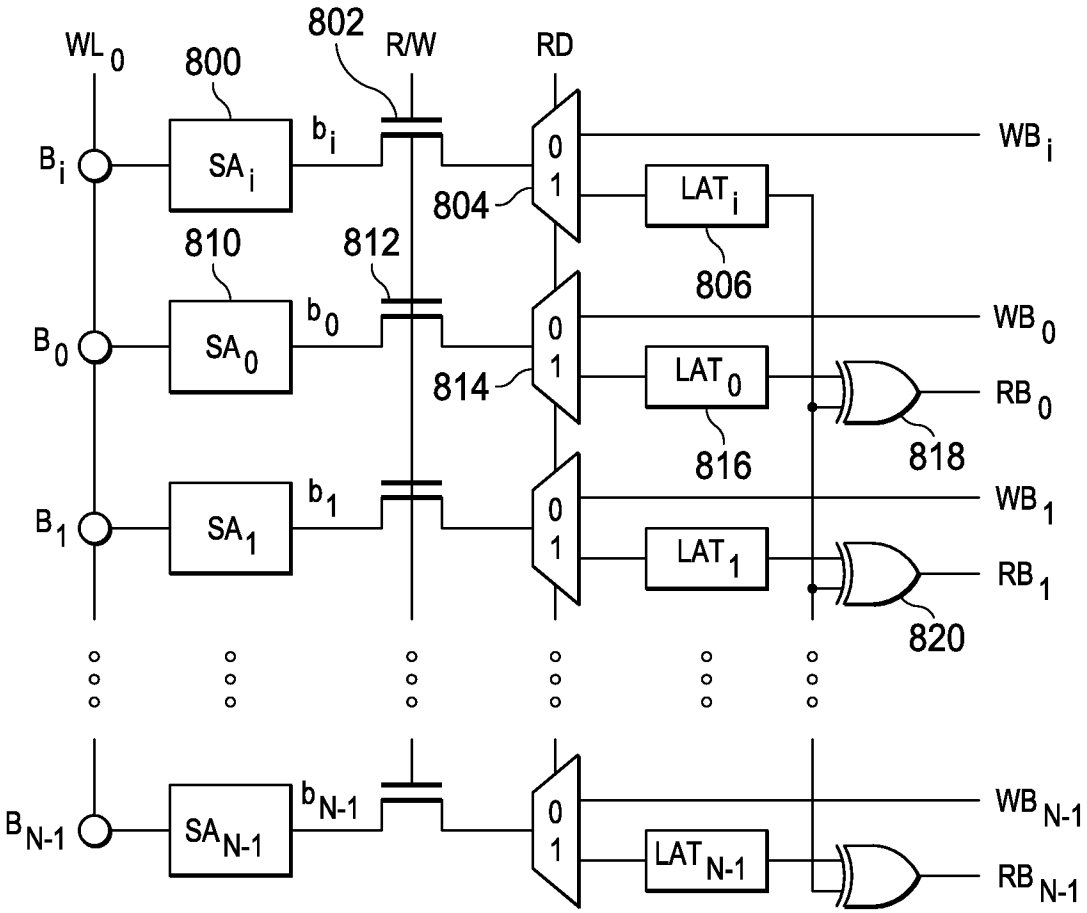

FIG. 8A

LOGIC STATE	B_i	B_0	B_1	b_i	b_0	b_1	RB_0	RB_1
AFTER WRITE	0	0	1	X	X	X	X	X
AFTER 1ST READ	1	1	0	0	0	1	0	1
AFTER 2ND READ	0	0	1	1	1	0	0	1
AFTER 3RD READ	1	1	0	0	0	1	0	1
AFTER 4TH READ	0	0	1	1	1	0	0	1

FIG. 8B

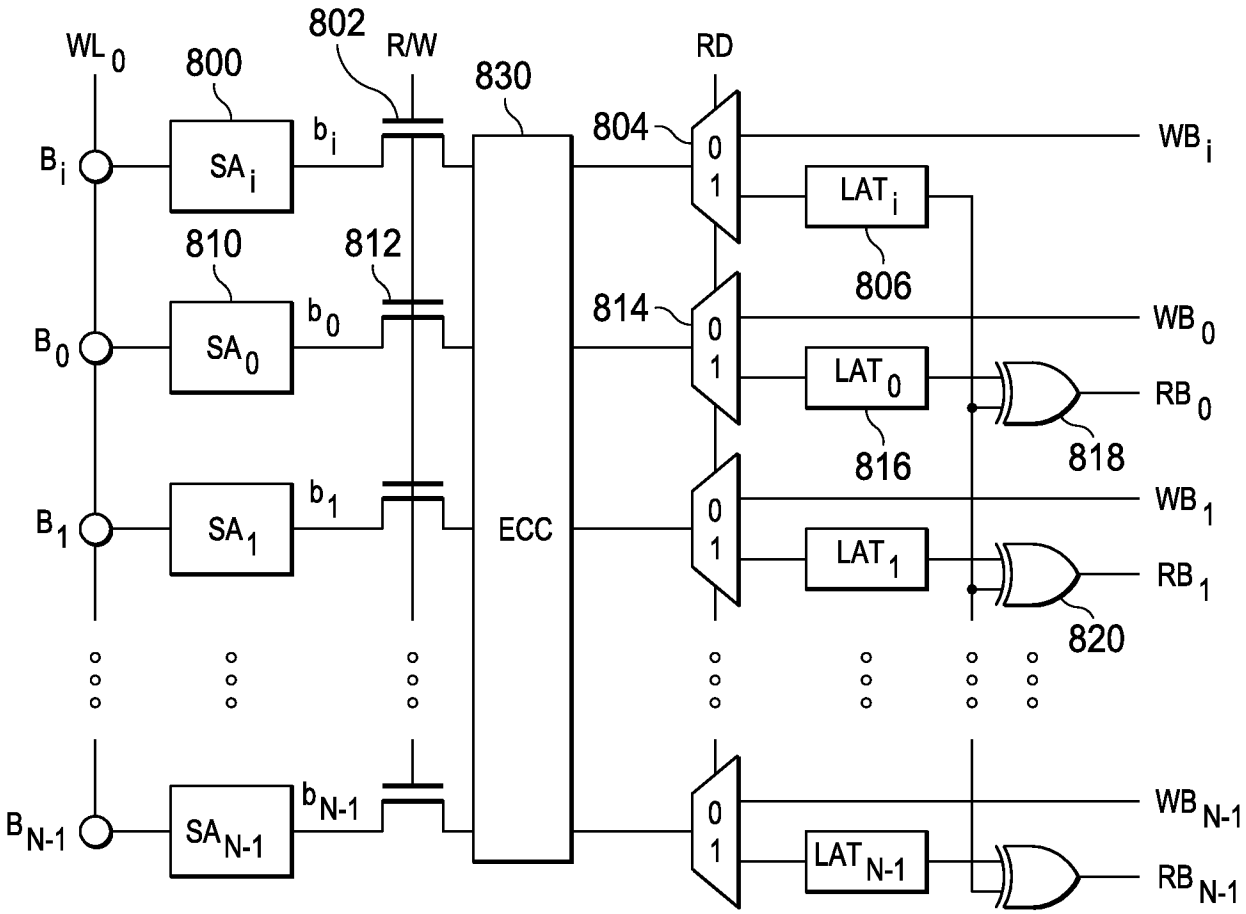
WL 0
800
802
R/W
830
RD
804
WB i
B i
SA i
b i
LAT i
806
810
812
814
WB 0
B 0
SA 0
b 0
LAT 0
RB 0
816
818
B 1
SA 1
b 1
ECC
WB 1
LAT 1
RB 1
820
B N-1
SA N-1
b N-1
WB N-1
LAT N-1
RB N-1

FIG. 8C

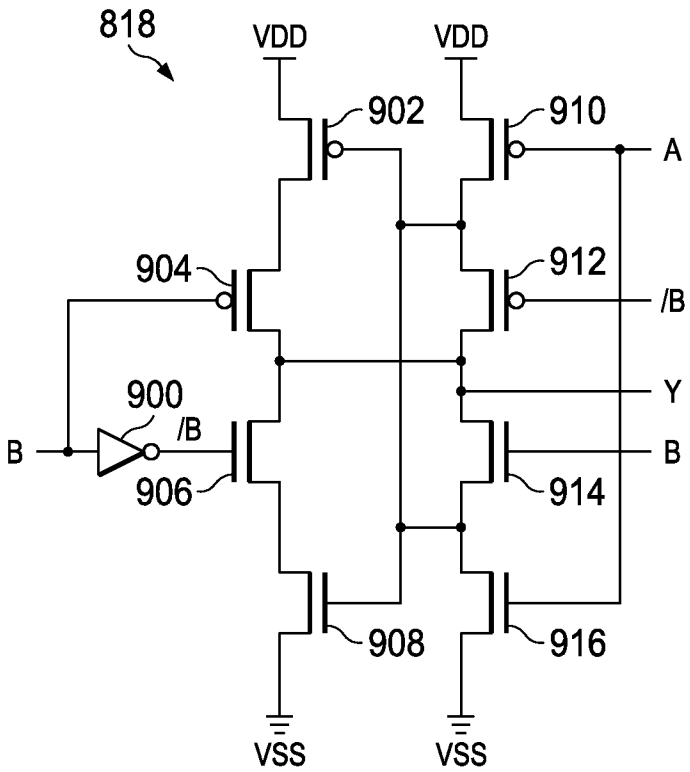
818
VDD
VDD
902
910
A
904
912
/B
900
/B
Y
B
B
906
914
908
916
VSS
VSS

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/019734

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/22 *(2006.01)*
G11C 7/06 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/00,11/21,11/22,11/34,11/40,11/401,11/4063,11/407,11/409,11/4091, 7/00,7/06,7/10, 29/00,29/04,29/08,29/12,29/38,29/42, G11B 9/00,9/02, H01G 7/00,7/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6590798 B1 (TEXAS INSTRUMENTS INCORPORATED) 08.07.2003, abstract, col. 1, lines 15-30, col. 2, line 47 - col. 3, line 3, col. 4, lines 43-56, col. 5, lines 26-66, col. 6, lines 28-32, 58-61, col. 7, lines 9-23, col. 8, line 39 - col. 9, line 32, col.10, lines 54-67, col. 11, lines 35, 36	1, 2, 6, 7, 10-15, 17-20
Y		3-5, 8, 9, 16
Y	US 2007/0022360 A1 (NIVRUTI RAI et al.) 25.01.2007, paragraphs [0018], [0022], [0028], [0040]-[0044], [0049]	3-5, 16
Y	US 2003/0112651 A1 (CEM BASCERI et al.) 19.06.2003, paragraphs [0026], [0028]	8, 9
A	US 5745403 A (RAMTRON INTERNATIONAL CORPORATION) 28.04.1998	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 June 2015 (26.06.2015)	02 July 2015 (02.07.2015)

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