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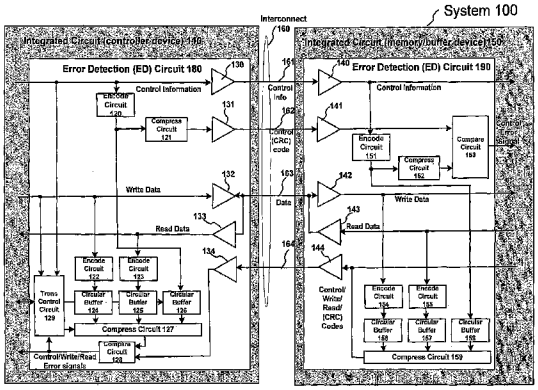
(54) **Title:** SYSTEM TO DETECT AND IDENTIFY ERRORS IN CONTROL INFORMATION, READ DATA AND/OR WRITE DATA



(57) **Abstract:** An integrated circuit, such as an integrated circuit memory or buffer device, method and system, among other embodiments, generate a plurality of error codes, such as CRC codes, corresponding to control information, write data and read data transactions, respectively. The plurality of separately generated CRC codes is logged or stored in respective storage circuits, such as circular buffers. The stored plurality of CRC codes corresponding to each transaction then may be used to determine whether an error occurred during a particular transaction and thus whether a retry of the particular transaction is issued. The integrated circuit includes a compare circuit to compare a CRC code generated by the integrated circuit with a CRC code provided by a controller device. A CRC code corresponding to read data is transferred to a controller device using a data mask signal line that is not being used during a read transaction. The CRC code generated by the integrated circuit then may be compared to a CRC code generated by the controller device to determine whether an error occurred. The controller device generates and stores a plurality of CRC codes, corresponding to control information, write data and read data. The controller device then compares the CRC codes generated by the controller device with CRC codes generated and stored in the integrated circuit to determine whether an error has occurred during a particular transaction.

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System to Detect And Identify Errors In Control Information, Read Data And/Or Write Data

FIELD OF THE INVENTION

The present invention generally relates to integrated circuit devices and/or high speed signaling of such devices.

BACKGROUND OF THE RELATED ART

In chip communications, errors may occur in transferring information between integrated circuits. For example, noise, crosstalk and/or inter-symbol interference may alter a signal resulting in erroneously received information. An integrated circuit may have an error detection circuit and/or software for detecting erroneously received and/or transmitted information. For example, an integrated circuit may have a checksum and/or parity-checking scheme to detect when erroneous information is received. Further, an integrated circuit may have an error checking and correcting ("ECC") scheme (ECC is also known as error correction code) that not only detects errors in information, but also corrects the error in the information.

However, when large amounts of information are transferred between integrated circuits, complicated error detection and correction schemes may require too much bandwidth and may introduce latencies that degrade system performance. Further, in certain applications, errors in information on one interconnect (e.g. control or address) may result in other information being erroneously transferred or received and thus it may be difficult to determine what the root cause of the error was.

BRIEF DESCRIPTION OF THE DRAWING

Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings, which like reference numerals refer to similar elements.

Fig. 1 illustrates a system 100 having error detecting circuits according to an embodiment.

Figs. 2A-B is a flow chart that illustrates a method 200 to detect different types of errors according to an embodiment.

Fig. 3 illustrates an integrated circuit memory device 300 having an error detection circuit according to an embodiment.

Fig. 4 illustrates an integrated circuit buffer device 400 having an error detection circuit according to an embodiment.

Fig. 5 illustrates a memory system 500 that detects errors according to an embodiment.

Fig. 6 illustrates a device 600 including a plurality of integrated circuit memory devices and a buffer device having error detection circuits according to an embodiment.

DETAILED DESCRIPTION

An integrated circuit, such as an integrated circuit ("IC") memory or buffer device, method, and/or system, among other embodiments, generates a plurality of error codes, such as cycle redundancy checking ("CRC") codes, corresponding to control information, write data and read data transactions. The plurality of separately generated CRC codes corresponding to control information, write data and read data is logged, or stored in respective storage circuits, such as circular buffers. The stored plurality of CRC codes corresponding to each transaction may be used to determine whether an error occurred during a particular transaction and thus whether a retry of the particular transaction, or

multiple retries, is issued. The integrated circuit includes a compare circuit to compare a CRC code generated by the integrated circuit with a CRC code provided by a controller device. A CRC code corresponding to control information is transferred to a controller device using a data mask signal line that is not being used during a read transaction. The CRC code generated by the integrated circuit then may be compared to a CRC code generated by the controller device to determine whether an error occurred in the control information. The controller device generates and stores a plurality of CRC codes, corresponding to control information, write data and read data. The controller device then compares the CRC codes generated by the controller device with CRC codes generated and stored in the integrated circuit to determine whether an error has occurred during a particular transaction.

An integrated circuit includes a first encode circuit to encode a first code representing write data, a second encode circuit to encode a second code representing read data and a third encode circuit to encode a third code representing control information. The control information includes address information and/or a memory command for accessing a storage array. A first, second and third compression circuit compresses the first, second and third codes to provided compressed first, second and third codes. In another embodiment, a single compression circuit compresses the first, second and third codes to provide a single compressed code. The first and second compressed codes are output to a controller device for detecting errors in transferred write and read data. A compare circuit compares the third compressed code that represents control information with a compressed code from a controller device to determine whether an error occurred in transferring the control information.

In a method embodiment of operating an integrated circuit, a first code that represents write data to be stored in a storage array is

generated and stored. A second code that represents read data obtained from a storage array is generated and stored. A third code that represents control information used to access the storage array is generated and stored. A fourth code from a controller device is compared with the third code to generate an error signal. A signal indicating retrying a memory transaction is generated in response to the error signal.

In a method embodiment of operating an integrated circuit, the first code is transferred to a controller device that compares the first code to a code generated by the controller device to generate an error signal that represents an occurrence of erroneous write data. The second code is transferred to a controller device that compares the second code to a code generated by the controller device to generate an error signal that represents an occurrence of erroneous read data. The third code is transferred to a controller device that compares the third code to a code generated by the controller device to generate an error signal that represents an occurrence of erroneous control information. A retry of read data, write data and/or control information may then be initiated in response to the corresponding error signals.

In a system embodiment, a controller device includes a first, second and third circuit to store first, second and third codes that represent write data to be stored in a storage array, read data obtained from the storage array and control information used to access the storage array. An integrated circuit includes a fourth, fifth and sixth circuit to store fourth, fifth and sixth codes that represent write data to be stored in a storage array, read data obtained from the storage array and control information used to access the storage array. The controller device includes a compare circuit to compare 1) the third code with the sixth code to determine when to retry a memory command or retransfer control information, 2) the first code with the fourth code to determine

when to retransfer the write data from the controller device to the IC memory device, and 3) the second code with the fifth code to determine when to retransfer the read data from the IC memory device to the controller device.

Fig. 1 illustrates a system 100 including an IC 110, such as a controller device or other master device, coupled to an IC 150, such as an IC memory device or buffer device, by an interconnect 160. ICs 110 and 150 include error detection ("ED") circuits 180 and 190, respectively, for detecting hierarchal types of errors when there is a limited amount of available bandwidth for transferring information between the ICs 110 and 150. For example, errors in different types of memory transactions or operations may be detected by using corresponding error codes stored in ICs 110 and 150. A memory transaction may include providing control information, such as address information and/or memory commands, to access a storage array in an IC memory device. Also, a memory transaction may include providing write data to be stored in a storage array of the IC memory device. A memory transaction may also include accessing, by a memory controller, read data from the storage array of the IC memory device. ED circuits 180 and 190 are able to detect whether an error occurred in the control information, write data and/or read data, singly or in combination.

ED circuit 190 includes receivers 140, 141 and 142 coupled to an interconnect 160 that includes signal lines or paths 161-164. Receiver 140 is coupled to a signal line 161 that carries control information and receiver 141 is coupled to a signal line 162 that carries mask information during a write operation, or other signal line that has available bandwidth when providing error information or CRC codes. In an embodiment, signal line 162 is included with other signal lines that transfer write and/or read data, such as signal line 163. Receiver 142 is coupled to signal line 163 that carries data information, such as write data to be

stored in a storage array or read data stored in a storage array. Transmitter 143 is coupled to signal line 163 while transmitter 144 is coupled to signal line 164. Signal line 164 may be included in a serial data bus, such as a SMBus bus, that provides CRC codes from ED circuit 190 to IC 110. In an alternate embodiment, signal line 164 is a signal line that has available bandwidth when providing error information. In another embodiment, signal line 164 is a signal line that has available bandwidth used during a typical memory operation, such as transferring read and/or write data.

Control information is provided by receiver 140 to encode circuit 151 that encodes the control information into an error code. Encode circuit 151 then outputs the encoded control information to circular buffer 158 and compression (compress) circuit 152. Compression circuit 152 compresses the encoded control information or CRC code for control information. Compare circuit 153 compares an error code from IC 110 via receiver 141 with a compressed encoded control information from compression circuit 152 in order to determine when an error occurs in the control information. When the received code from IC 110 does not match or is not equal to the code from compression circuit 152, compare circuit 153 generates an error signal indicating that an error occurred in control information. The error signal from compare circuit 153 causes IC 150 to generate a retry signal to IC 110 which then retries or repeats sending the control information on signal line 161.

In another embodiment, an error signal is provided in an IC buffer device that rejects and/or ignores any subsequent read data and/or write data (to and/or from the IC buffer device) until the error is corrected by, for example, resending the control information (to or from) the IC buffer device. Ignoring or rejecting incoming write and/or read data is done in order to avoid any possible data contamination due to receiving erroneous control information. If data is contaminated or erroneous due

to receiving erroneous control information, future transactions may be interpreted incorrectly.

Control information from receiver 140 may be provided to IC memory core, such as column decoder circuit 302 and/or row decoder 303, to access storage arrays in IC memory device 300 as illustrated in Fig. 3 and described below. In another embodiment, control information is provided to request an address circuit 440 in IC buffer device 400 as illustrated in Fig. 4 and described below.

Similarly, write data from receiver 142 is provided to encode circuit 154 that encodes the write data to obtain an error code or CRC code. The encoded write data may then be stored in a circular buffer 156 and compressed by compression circuit 159. In response to a request by IC 110, periodically or during a testing/maintenance operation, compression circuit 159 provides an encoded and compressed write data error code to transmitter 144 which transmits the code representing write data, via signal line 164, to IC 110. As described below, IC 110 then may compare the code representing the write data from IC 150 with an internally generated and stored code representing the write data transmitted to IC 150 to determine when an error occurred in transferring the write data. Retry or retransfer of the write data may be provided by controller 110 on line 163 in response to determining that an error occurred in the transfer of the write data or in response to a write error signal output from compare circuit 128.

Write data from receiver 142 may be provided to a memory core, such as sense amplifiers 306, to store the write data in IC memory device 300 as illustrated in Fig. 3 and described below. In another embodiment, write data is provided to interfaces 420a-b in IC buffer device 400 as illustrated in Fig. 4 and described below.

Read data is provided to transmitter 143 and encode circuit 155 that encodes the read data to obtain an error code or CRC code. The

encoded read data is then stored in circular buffer 157 and compressed by compression circuit 159. In response to a request by IC 110, periodically or during a testing/maintenance operation, compression circuit 159 provides an encoded and compressed read data to transmitter 144 that transmits the code representing read data, via signal line 164, to IC 110. As described below, IC 110 then may compare the code representing the read data from IC 150 with an internally generated and stored code representing the read data transmitted to IC 150 to determine when an error occurred in transferring the read data or in response to a read error signal output from compare circuit 128.

In another embodiment, control information, read data and write data are obtained from circular buffers 156-158 and, rather than compressed and transferred singly, are compressed simultaneously to provide a combined compressed code that is output from transmitter 144. This combined compressed code from ED circuit 190 then may be compared with a simultaneously combined compressed code from compression circuit 127 by compare circuit 128 to generate an error signal in ED circuit 180.

Read data provided to transmitter 143 may be provided from a memory core, such as sense amplifiers 306, to obtain stored read data in a storage array of IC memory device 300 as illustrated in Fig. 3 and described below. In another embodiment, read data is provided from interfaces 420a-b in IC buffer device 400 (via multiplexers 430a-b) as illustrated in Fig. 4 and described below.

ED circuit 190 using circular buffer 158, compress circuit 159 and transmitter 144 may likewise provide stored encoded control information via receiver 140 to IC 110.

IC 110 includes transmitters 130, 131 and 132 coupled to interconnect 160. In particular, control information is provided to transmitter 130 that is coupled to signal line 161 and encode circuit 120.

Control information or a control transaction is also input to transaction control circuit 129. Encoded control information is then output from encode circuit 120 to compression circuit 121 and circular buffer 126. Compression circuit 121 then provides the code representing the control information or CRC code to transmitter 131 that transmits the code on signal line 162. Write data is provided to transmitter 132, transaction control circuit 129 and encode circuit 122. Encode circuit 122 then outputs a code representing write data to be stored into circular buffer 124. Likewise, read data received from receiver 133 that is coupled to signal line 163 is provided to encode circuit 123 that outputs a code representing the read data received from receiver 133. The code is then input to circular buffer 125.

Transaction control circuit 129 stores recent transactions and controls the output of circular buffers 124, 125 and 126 to compression circuit 127. Transaction control circuit 129 also controls the output of compression circuit 127 to compare circuit 128 that compares codes representing control information, write data and read data generated in IC 110 to codes representing control information, write data and read data received from IC 150 via receiver 134. As described below, IC 110 accesses stored transactions in transaction control circuit 129 and circular buffers 124-126 and 156-158 in retransmitting information, such as control information, write data and/or read data, which caused an error signal to be output from compare circuit 128. When there is no error signal output (or alternatively a pass signal is output) after a comparison by compare circuit 128, stored transactions may be cleared or erased.

IC 110 may compare the code representing the write data from IC 150 (via receiver 134) with an internally generated and stored code representing the write data (stored in circular buffer 124) to output an error signal from compare circuit 128 when an error occurred in

transferring the write data. IC 110 may also compare the code representing the read data from IC 150 (via receiver 134) with an internally generated and stored code representing the read data (stored in circular buffer 125) to output an error signal from compare circuit 128 when an error occurred in transferring the read data. IC 110 also may compare the code representing the control information from IC 150 (via receiver 134) with an internally generated and stored code representing the control information (stored in circular buffer 126) to output an error signal from compare circuit 128 when an error occurred in transferring the control information. Compare circuit 128 outputs an error signal when the codes from compression circuit 127 does not match or does not equal the code received from receiver 134.

Control information may be retried or retransmitted from transmitter 130 when an error signal for the control information is output from compare circuit 128. In particular, integrated circuit 110 accesses transaction control circuit 129 to determine what stored transaction to retry. Integrated circuit 110 also accesses circular buffers 124-126 and 156-157 to determine which specific transaction failed or is erroneous. Write data may be retried or retransmitted from transmitter 132 when an error signal for write data is output from compare circuit 128. Read data may be retried or retransmitted from transmitter 143 in IC 150 when an error signal for read data is output from compare circuit 128. In an embodiment, IC 110 provides control information to transmitter 130 in order to retry or retransfer read data that was determined to be erroneous.

Circular buffers 124-126 and 156-158, singly or in combination, are storage circuits to sequentially write and read binary information. A circular buffer may use pointers to identify current locations in the storage circuit for the next binary information to be written to or read from.

Encode circuits 120, 122-123, 151 and 154-155, singly or in combination, are circuits to encode a first set of binary information into a second set of binary information or a code. Encode circuits may encode binary information, such as control information, read data and/or write data, into an ECC that enables errors to be detected. For example, a 64-bit word read from a storage array or to be stored in the storage array may be encoded into a 6-bit ECC which is appended and transferred with the 64-bit word. An ECC is a polynomial, such as a 4-bit, 6-bit, 16-bit or 32-bit polynomial. In other embodiments, N-bit polynomials are used. The resulting polynomial is known as a cycle redundancy checking code ("CRC code" or a "CRC-4" for a 4-bit polynomial or "CRC-6" for a 6-bit polynomial, and so on). CRC-Ns may be defined by the International Telecommunication Union-Telecommunication Standardization Sector ("ITU-TS") are used. A CRC-16 may detect all single and double-bite errors and may ensure detection of a significant number of possible errors. One or more encode circuits 120, 122-123, 151 and 154-155 may include a plurality of XOR gates to output a CRC code.

Transmitters 130-132 and 143-144, singly or in combination, may include output driver circuits to output respective signals onto interconnect 160. The output driver circuit may be pull-up, pull-down and/or push-pull type output driver circuits.

Multiple compression circuits may replace compression circuit 159 and/or 127. A single encode circuit may replace multiple encode circuits.

Figs. 2A-B illustrate method 200 embodiments for operating an integrated circuit, such as ICs 110 and/or 150. In embodiments, logic blocks illustrated in Figs. 2A-B are carried out by hardware, software or a combination thereof. In embodiments, logic blocks illustrated in Figs. 2A-B illustrate actions or steps. In embodiments, the circuits illustrated in

Fig.1, singly or in combination, carry out the logic blocks illustrated in Figs. 2A-B. Other logic blocks that are not shown may be included in various embodiments. Similarly, logic blocks that are shown may be excluded in various embodiments. Also, while method 200 is described in sequential logic blocks, steps of logic blocks of method 200 are completed very quickly or almost instantaneously.

Method 200 begins at logic blocks 201 and 202 where a determination is made whether an error occurred in a memory transaction. The memory transaction may be the transfer of read data. A code representing the read data from IC 150 via receiver 134 may be compared (using compare circuit 128) with a code representing read data via circular buffer 125 and compression circuit 127. Alternatively, a single combined compressed code representing control information, read data and write data may be provided from a memory device and/or buffer device and compared to another internally generated combined compressed code representing control information, read data and write data to determine whether an error occurred in a memory transaction. The determination whether an error is detected may be performed by hardware in a controller device, such as a controller device 501 shown in Fig. 5 and/or buffer device 600 shown in Fig. 6. When an error in the read data and/or compressed combined code is not detected, a buffer storing prior transaction is cleared and memory operations continue as illustrated by logic block 211. Transaction control circuit 129 includes a transaction queue or storage circuit that may be cleared or erased. Otherwise, control transfers to logic block 203 where memory transactions are stopped when an error in the read data and/or compressed combined code is detected. Halting or stopping memory transactions may be performed by a controller device, such as an embedded processor that executes firmware, or by a separate processor that is interrupted in response to an error signal. As illustrated by logic

blocks 204-205, codes in circular buffers 124, 125 and 126 are then compared with codes from IC 150 via receiver 134 in order to determine whether an error occurred in the transfer of write data (which was then read in logic block 201 and subsequently determined erroneous), read data or control information, such as address information. A determination is made whether an error occurred in the transfer of address information or write/read data as illustrated by logic block 206. When an error occurs in the address, all memory transactions after the failed transfer of the address information are reissued or retried as illustrated by logic block 208. Otherwise, a determination is made whether an error occurred in the transfer of write data or read data as illustrated in logic block 207. When an error occurs in the transfer of the read data as determined by logic block 207, read data is retried or retransmitted as illustrated by logic block 209. When an error occurred in the transfer of the write data as determined by logic block 207, write data is retried or retransmitted as illustrated by logic block 210. Other errors are checked as illustrated in logic block 212. When other errors are detected, control transfers to logic block 202. Otherwise, control transfers to logic block 213 that illustrates clearing a transaction buffer that stores recent transaction information. Memory transactions are resumed as illustrated in logic block 214 and method 200 ends.

Fig. 3 illustrates an integrated circuit memory device 300 having an ED circuit 190 included in an interface 310. Integrated circuit memory device 300 includes N storage arrays (memory banks) 304 in a memory core 301 having column decoder circuit 302 and row decoder circuit 303. Each memory bank 304 may include a storage array or plurality of storage cells.

Integrated circuit memory device 300 receives control information, such as memory operation commands and address information, from ED circuit 190 in a memory transaction. Control information may include a

request packet that represents one or more signals asserted at particular bit windows on particular signal lines.

Row decoder circuit 303 and column decoder circuit 302 are used to access data stored in storage arrays 304 in response to control signals received by way of row decoder circuit 303 and column decoder circuit 302. Row decoder circuit 303 and column decoder circuit 302 may generate control signals in response to commands and addresses received by IC memory device 300 at ED circuit 190. For example, data stored in a plurality of storage cells, such as row 305, is sensed using sense amplifiers 306 in response to a row command. Row 305 is identified by a row address provided to row decoder circuit 303. A subset of the data sensed in sense amplifiers 306 is selected in response to a column command provided to column decoder circuit 302. The subset of the data is identified by a column address provided to column decoder circuit 302.

Fig. 4 illustrates an IC buffer device 400 having an ED circuit 190 in interface 410. As described above, ED circuit 190 receives and/or outputs CRC codes corresponding to different types of memory transactions for IC buffer device 400. As described in detail below, IC buffer device 400 may be disposed on a memory module, housed in a common package along with IC memory devices or dies, or situated on a motherboard, for example, main memory in a personal computer or server. The IC buffer device 400 may also be used in an embedded memory subsystem, for example such as one found on a computer graphics card, video game console or a printer.

Fig. 4 illustrates interface 410 that receives control information, write data and CRC codes from interconnect 160. A multiplexed combination of control information, write data and CRC codes intended for IC memory devices coupled to IC buffer device 400 may be received via interface 410, which may, for example extract the control information.

For example, memory commands and address information may be decoded and separated from multiplexed information on interconnect 160 and provided to request and address circuit 440 from interface 410. Write data may be provided to interfaces 420a-b by way of interface 410 and read data from IC memory devices may be received at one or more interfaces 420a-b and provided to interface 410 via multiplexers 430a-b.

Interface 410, and in particular ED circuit 190, receives a CRC code from a controller device or other IC buffer device. Interface 410 along with request and address circuit 440 may route or forward one or more CRC codes intended for another IC from one interconnect coupled to interface 410 to another interconnect coupled to interface 410 (or on the same interconnect). CRC codes generated by ED circuit 190 in interface 410 may be accessed by way of one or more interconnects coupled to interface 410.

A clock signal and other information, may be received on interconnect 160 or by other interconnects, such as a serial bus. Interface 410 may include a transmit circuit or transmitters and a receiver circuit or receivers (or in combination referred to as transceivers) to output and receive signals on interconnect 160. Similarly, interfaces 420a and 420b receive and transmit control information, read data and write data to and from IC memory devices via interconnects 421 and 422, respectively. Interfaces 420a-b may include transmitters and receivers to output and receive signals on interconnects 421 and 422. Transmitters and receivers in interfaces 410 and 420a-b, singly or in combination, may be dedicated to or shared with particular signal lines in the interconnects 421 and 422.

Transmitters and receivers in interfaces 420a-b may transmit and receive signals having a first type of standard signaling characteristic (or protocol), such as a DDR3 signal; while interface 410 includes

transmitters and receivers that transmit and receive signals having a second type of standard signaling characteristic, such as a DDR2 signal.

Interfaces 420a-b may include transmitters to transfer control information on a unidirectional interconnect; while transmitters and receivers for write and read data transfer the write and read data on a bidirectional interconnect.

Multiplexers 430a and 430b may perform bandwidth-concentrating operations, between interface 410 and interfaces 420a and 420b, as well as route data from an appropriate source (i.e. target a subset of interconnects, internal data cache) to an appropriate destination. Bandwidth concentration may involve combining the (smaller) bandwidth of each interconnect in a multiple interconnect to match the (higher) overall bandwidth utilized in a smaller group of interconnects. Bandwidth concentration typically utilizes multiplexing and demultiplexing of throughput between the multiple interconnects and smaller group of interconnects. IC buffer device 400 may utilize the combined bandwidth of interfaces 420a and 420b to match the bandwidth of interface 410.

Cache 460 may be incorporated onto IC buffer device 400. Cache 460 may improve memory access time by providing storage of most frequently referenced write and/or read data and associated tag addresses with lower access latency characteristics than those of the IC memory devices. In an embodiment, cache 460 may replace circular buffers 156-158 of ED circuit 190 as shown in Fig. 1.

Computation circuit 465 may include a processor or controller unit, a compression/decompression engine, and so on, to further enhance the performance and/or functionality of IC buffer device 400. In an embodiment, computation circuit 465 is used to compress binary information in replacement of one or more compression circuits 152 and 159 of ED circuit 190 shown in Fig.1.

Clock circuit 470 includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown). Clock alignment circuits may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship. Clock circuit 470 may include a phase lock loop circuit or a delay lock loop circuit. Clock alignment circuits may provide an internal clock signal having a temporal relationship with transferred or received control information, read data and/or write data as will as CRC codes.

Transmitters in interfaces 420a-b (as well as interface 410) may transmit a differential signal that includes encoded clock information and receivers may receive a differential signal that includes encoded clock information. For example, clock circuit 470 extracts the clock information encoded with the data received by the receiver. Furthermore, clock information is encoded with data transmitted by the transmitter. For example, clock information may be encoded onto a data signal, by ensuring that a minimum number of signal transitions occur in a given number of data bits.

Serial interface 474 is an interface to receive serial information from a controller or other configuration circuit. The serial information may include initialization signals for IC buffer device 400 or a memory module. Serial interface 474 may be used by IC 110 (or a controller device) to obtain CRC codes output from compression circuit 159 in ED circuit 190.

Fig. 5 illustrates a memory system 500 including a controller device 501 having an ED circuit 180 coupled to a plurality of memory modules 520a-n. The plurality of memory modules 520a-n include connectors 522a-n to transfer signals between a plurality of respective IC buffer devices 525a-n having respective ED circuits 190a-n and

interconnects 530a-n. In response, IC buffer devices 525a-n transfer signals between a plurality of IC memory devices 521a-h and IC buffer devices 525a-n using interconnects 421 and 422. In an embodiment, at least one ED circuit in the plurality of ED circuits 190a-n corresponds to ED circuit 190 shown in Fig. 1.

Controller device 501 and memory modules 520a, 520b and 520n are coupled by interconnects 530a, 530b and 530n. Interconnect 530a corresponds to interconnect 160 shown in Figs. 1 and 4. Interconnects 530a, 530b and 530n may include respective point-to-point links to transfer control information and write data using unidirectional differential signals from controller device 501 to IC buffer device 525a and from IC buffer device 525a to IC buffer device 525b and so on. Similarly, interconnects 530b and 530a also include respective point-to-point links to transfer read data using unidirectional differential signals from IC buffer device 525b to IC buffer device 525a and from IC buffer device 525a to controller device 501 in response to received control information.

In an embodiment, a point-to-point link denotes one or a plurality of signal lines, each signal line having only two transceiver connection points, each transceiver connection point coupled to a transmitter, a receiver or transceiver circuit. For example, a point-to-point link may include a transmitter coupled at or near one end and a receiver coupled at or near the other end.

One or more interconnects 530a, 530b and 530n may include different types of bus or point-to-point link architectures. Interconnects may also have different types of signaling and clocking type architectures. Embodiments having different link architectures include simultaneous bi-directional links, time-multiplexed bi-directional links and multiple unidirectional links. Voltage or current mode signaling may be employed in any of these link or bus architectures.

One or more memory modules in memory modules 520a-n may be dual-in-line memory modules ("DIMM") having a standard DIMM form factor. A memory module may be included in a single unitary package, as in a "system in package" ("SIP"). In one type of SIP embodiment, a memory module may include a series of integrated circuit dies (i.e., memory devices and buffer device) stacked on top of one another and coupled via conductive interconnect. Solder balls or wire leads may be employed as the connector interface such that the memory module may be fixedly attached to a printed circuit board substrate. A connector interface may also be of a physically separable type that includes, for example, male and female portions such that a memory module is detachable from the rest of a system. Another SIP embodiment may include a number of memory devices and a buffer device disposed, in a two dimensional arrangement, on a common substrate plane and situated inside a single package housing.

A clock source 510 may provide one or more clock signals on interconnect 533 to controller device 501 and memory modules 520a-n. One or more signal lines in interconnect 533 may be coupled to clock circuit 470 of IC buffer devices 525a-n. A clock source 510 may be a clock generator to provide a clock signal. Clock source 510 may be included in controller device 501. Clock signals from clock source 510 may be used to provide temporal relationships between control information, read data and write data as well as CRC codes transferred between controller 501 and memory modules 520a-n, singly or in combination.

Interconnect 531 couples controller device 501 to memory modules 520a-n. Interconnect 531 may be a serial bus coupled to serial interface 474 of IC buffer devices 525a-n.

Returning to the embodiments illustrated by Fig. 1, ICs 110 and 150 may be housed in packages that include a plurality of conducting

contacts, such as pins and/or balls, for coupling to interconnect 160. A plurality of contacts, solder balls or pins may be included in an interface to provide electrical connections between an interface and a substrate. In an embodiment, the interface may be removable from a connector or substrate. In an embodiment, ICs 110, 150 and associated interconnects are in one integrated monolithic circuit and/or package housing both ICs 110 and 150.

Fig. 6 is a block diagram illustrating a device 600 having a plurality of integrated circuit memory devices (or dies) 300a-d and a buffer device (or die) 400 having error detection circuits 180/190. One or more integrated circuit memory devices 300a-d may correspond to integrated circuit memory device 300 shown in Fig. 3 and buffer device 400 may correspond to integrated circuit buffer device 400 shown in Fig. 4. Buffer device 400 includes error detection circuit 190, including circular buffers 156-158, to determine whether an error occurred in transferring control information, write data and/or read data over interconnect 160 from or to a controller device 110. Similarly, buffer device 400 may also include error detection circuit 180 which is used in detecting errors in transferring control information, write data and/or read data between buffer device 400 and one or more memory devices 300a-d, that may include error detection circuit 190.

Here, data (read and/or write) may be transferred between the plurality of integrated circuit memory devices 300a-d and buffer device 400 on interconnect 606 (Read/Write data). Interconnect 606 is an interconnect situated internal to device 600 and may be a bus for providing bidirectional data signals between a plurality of integrated circuit memory devices 300a-d and buffer device 400. An example of bidirectional data signals includes signals traveling from one or more of integrated circuit memory devices 300a-d to buffer device 400 and also signals traveling from buffer device 400 to one or more of integrated

circuit memory devices 300a-d. Interconnect 605 is an interconnect internal to device 600 and may be a bus for providing unidirectional control/address/clock signals from a buffer 400 to a plurality of integrated circuit memory devices 300a-d. In an example of a unidirectional bus, signals travel in only one direction, i.e., in this case, from only buffer device 400 to one or more of integrated circuit memory devices 300a-d. Interconnect 605 may include individual control signal lines, for example, a row address strobe line, column address strobe line, etc., and address signal lines. Interconnect 605 may include a fly-by clock line to transfer a clock signal from buffer device 400 to integrated circuit memory devices 300a-d. Interconnect 605 may transfer a clock signal from one or more integrated circuit memory devices 300a-d to buffer device 400.

Interconnect 160 may be coupled to device 600 and in particular buffer device 400. Interconnect 160 transfers unidirectional control/address/clock signals and bidirectional or unidirectional data signals between buffer device 400 and a controller device 110. Other interconnect and external connect topologies may also be used for device 600 in alternate embodiments. For example, buffer device 600 may be coupled to a single multi-drop control bus, a split multi-drop control bus, or a segmented multi-drop bus.

In an embodiment, buffer device 400 communicates with a serial presence detect device ("SPD") 602 to store and retrieve parameters and configuration information regarding device 600 and/or memory modules 520a-n. In an embodiment, an SPD 602 is a non-volatile storage device. Interconnect 604 couples SPD 602 to buffer device 400. In an embodiment, interconnect 604 is an internal signal path for providing bidirectional signals between SPD 602 and buffer device 400.

SPD 602 may be an EEPROM device. However, other types of SPD 602 are possible, including but not limited to a manual jumper or switch settings, such as pull-up or pull-down resistor networks tied to a

particular logic level (high or low), which may change state when a memory module is added or removed from a system.

In an embodiment, device 600 has two separate power sources. Power source V1 supplies power to one or more memory devices (memory devices 300a-d). Power source V2 supplies power to one or more buffers (buffer device 400). In an embodiment, the buffer device 400 has internal power regulation circuits to supply power to the memory devices 300a-d.

Returning to Fig. 4, a storage array 304 includes a two dimensional array of storage cells. Storage cells of a storage array may be dynamic random access memory ("DRAM") cells, static random access memory ("SRAM") cells, FLASH cells, ferroelectric RAM ("FRAM") cells, magnetoresistive or magnetic RAM ("MRAM") cells, or other equivalent types of memory storage cells. IC memory device 300 may be a double data rate SDRAM ("DDR") IC memory device or later generation IC memory device (e.g., "DDR2" or "DDR3"). In an alternate embodiment, IC memory device 300 is an XDR™ DRAM IC memory device or Direct Rambus® DRAM ("DRDRAM") memory device.

In embodiments shown in Fig. 1, IC 110 is a master device, which may be an integrated circuit device that contains other interfaces or functionality, for example, a Northbridge chip of a chip set. The master device may be integrated on a microprocessor or a graphics processor unit ("GPU") or visual processor unit ("VPU"). The master device may be implemented as a field programmable gate array ("FPGA"). The ICs 110 and 150 may be included in various systems or subsystems such as personal computers, graphics cards, set-top boxes, cable modems, cell phones, game consoles, digital television sets (for example, high definition television ("HDTV")), fax machines, cable modems, digital versatile disc ("DVD") players or network routers.

Signals described herein may be transmitted or received between and within devices/circuits by electrical conductors and generated using any number of signaling techniques including without limitation, modulating the voltage or current level of an electrical signal. The signals may represent any type of control and timing information (e.g. commands, address values, clock signals, and configuration information) as well as data. Also, a single signal illustrated may represent a plurality of signals on respective signal lines in an embodiment.

In embodiments, interconnects described herein include a plurality of conducting elements or signal paths such as a plurality of wires and/or metal traces/signal lines. Multiple signal paths may replace a single signal path illustrated in the figures and a single signal path may replace multiple signal paths illustrated in the figures. An interconnect may include a bus and/or point-to-point connection. Interconnects may include control and data signal lines. In an alternate embodiment, interconnects include only data signal lines or only control signal lines. In still other embodiments, interconnects are unidirectional (signals that travel in one direction) or bidirectional (signals that travel in two directions) or combinations of both unidirectional signal lines and bidirectional signal lines.

It should be noted that the various circuits disclosed herein may be described using computer aided design tools and expressed (or represented) as data and/or instructions embodied in various computer-readable media, in terms of their behavior, register transfer, logic component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to: formats supporting behavioral languages such as C, Verilog, and HLDL; formats supporting register level description languages like RTL; formats supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF,

MEBES; and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, non-volatile storage media in various forms (e.g., optical, magnetic or semiconductor storage media) and carrier waves that may be used to transfer such formatted data and/or instructions through wireless, optical, or wired signaling media or any combination thereof. Examples of transfers of such formatted data and/or instructions by carrier waves include, but are not limited to, transfers (uploads, downloads, e-mail, etc.) over the Internet and/or other computer networks via one or more data transfer protocols (e.g., HTTP, FTP, SMTP, etc.). When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits may be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, netlist generation programs, place and route programs and the like, to generate a representation or image of a physical manifestation of such circuits. Such representation or image may thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

The foregoing description of the preferred embodiments has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the embodiments to the precise forms disclosed. Modifications and variations will be apparent to practitioners skilled in the art. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, thereby enabling others skilled in the art to understand the invention for various embodiments and with the various modifications as are suited to the particular use contemplated. It is

intended that the scope of the invention be defined by the following claims and their equivalents.

What is claimed is:

1. An integrated circuit device comprising:

a first storage circuit to store a first code that represents write data to be stored in a storage array;

a second storage circuit to store a second code that represents read data obtained from the storage array; and

a third storage circuit to store a third code that represents control information used to access the storage array.

2. The integrated circuit device of claim 1, wherein the integrated circuit device is a buffer device to transfer write data from a controller device to an integrated circuit memory device including the storage array and to transfer read data from the integrated circuit memory device to the controller device.

3. The integrated circuit device of claim 1, wherein the integrated circuit is an integrated circuit memory device including the storage array to store the write data.

4. The integrated circuit device of claim 1, wherein the control information includes address information for accessing a row of the storage array and a memory command.

5. The integrated circuit device of claim 1 further comprising:

a first encode circuit to provide the first code in response to the write data;

a second encode circuit to provide the second code in response to the read data; and

a third encode circuit to provide the third code in response to the control information.

6. The integrated circuit device of claim 1 further comprising:

a compression circuit to provide a first compressed code in response to the third code; and

a comparison circuit to compare the first compressed code with a code that is received to determine whether an error has occurred.

7. The integrated circuit device of claim 1, wherein the first, second and third storage circuits include first, second and third circular buffers to store a first plurality of codes representing write data, a second plurality of codes representing read data, and a third plurality of codes representing control information.

8. The integrated circuit of claim 1, wherein the first, second and third codes are cycle redundancy checking codes.

9. A method for operation of an integrated circuit device, the method comprising:

generating a first code that represents write data to be stored in a storage array;

storing the first code;

generating a second code that represents read data obtained from the storage array;

storing the second code;

generating a third code that represents control information used to access the storage array; and

storing the third code.

10. The method of claim 9, further comprising:

receiving a fourth code from a controller device;

comparing the fourth code with the third code to generate an error signal; and

retrying a memory transaction in response to the error signal.

11. The method of claim 10, wherein the fourth code is received from a signal line used to transfer mask information.

12. The method of claim 10, wherein the control information includes an address for accessing a row of the storage array.

13. The method of claim 9, further comprising:

transferring the first code to a controller device that compares the first code with a fourth code to generate an error signal indicating an occurrence of erroneous write data;

transferring the second code to a controller device that compares the second code with a fifth code to generate an error signal indicating an occurrence of erroneous read data;

transferring the third code to a controller device that compares the third code with a sixth code to generate an error signal indicating an occurrence of erroneous control information.

14. The method of claim 13, further comprising:

retrying transferring the write data in response to the error signal indicating an occurrence of erroneous write data;

retrying transferring the read data in response to the error signal indicating an occurrence of erroneous read data; and

retrying transferring control information in response to the error signal indicating an occurrence of erroneous control information.

15. The method of claim 9, wherein the integrated circuit device is a buffer device to transfer write data from a controller device to an integrated circuit memory device including the storage array and to transfer read data from the integrated circuit memory device to the controller device.

16. The method of claim 9, wherein the first, second and third codes are cycle redundancy checking codes.

17. A method for operation of an integrated circuit memory device, the method comprising:

generating a code indicating an error occurred in an access of the integrated circuit memory device;

determining a type of error that occurred in an access of the integrated circuit memory device; and

retrying an access of the integrated circuit memory device in response to the type of error.

18. The method of claim 17, wherein the access of the integrated circuit memory device includes providing control information to the integrated circuit memory device, the control information including an address to a storage array of the integrated circuit memory device.

19. The method of claim 17, wherein the access of the integrated circuit memory device includes providing write data to

be stored in a storage array of the integrated circuit memory device.

20. The method of claim 17, wherein the access of the integrated circuit memory device includes providing read data from a storage array of the integrated circuit memory device.

21. The method of claim 17, wherein generating the code includes compressing the code.

22. The method of claim 17, wherein the determining includes reading a code representing control information from a first storage circuit disposed on the integrated circuit memory device having a storage array, reading a code representing a write data from a second storage circuit disposed on the integrated circuit memory device and reading a code representing read data from a third storage circuit disposed on the integrated circuit memory device.

23. The method of claim 17, wherein a type of error is selected from one of an error in the control information transferred to the integrated circuit memory device, an error in the write data to be stored in a storage array of the integrated circuit memory device and an error in the read data obtained from the storage array of the integrated circuit memory device.

24. A system, comprising:

a controller including,

a first storage circuit to store a first code that represents write data to be stored in a storage array;

a second storage circuit to store a second code that represents read data obtained from the storage array;

a third storage circuit to store a third code that represents control information used to access the storage array; and

an integrated circuit including,

a fourth storage circuit to store a fourth code that represents write data to be stored in a storage array;

a fifth storage circuit to store a fifth code that represents read data obtained from the storage array;

a sixth storage circuit to store a sixth code that represents control information used to access the storage array.

25. The system of claim 24, wherein the controller device includes a compare circuit to compare the third code with the sixth code to determine when to retry a memory command.

26. The system of claim 25, wherein the compare circuit compares the first code with the fourth code to determine when to retransfer the write data from the controller device to the integrated circuit.

27. The system of claim 25, wherein the compare circuit compares the second code with the fifth code to determine when to retransfer the read data from the integrated circuit to the controller device.

28. The system of claim 24, wherein the controller device and the integrated circuit is coupled by a serial interconnect, wherein

the third, fourth and fifth codes are transferred to the controller device on the serial interconnect.

29. The system of claim 24, wherein the first, second, third, fourth and fifth codes are cycle redundancy checking codes.

30. Machine-readable media including information that represents an apparatus, the represented apparatus comprising:

a first storage circuit to store a first code that represents write data to be stored in a storage array;

a second storage circuit to store a second code that represents read data obtained from the storage array; and

a third storage circuit to store a third code that represents control information used to access the storage array.

31. An integrated circuit comprising:

an interface to transfer write data, read data and control information; and

means for encoding the write data, read data and control information into an error code representing write data, read data, and control information and,

the means for encoding including determining whether an error occurred in transferring one of the write data, read data and control information in response to the error code.

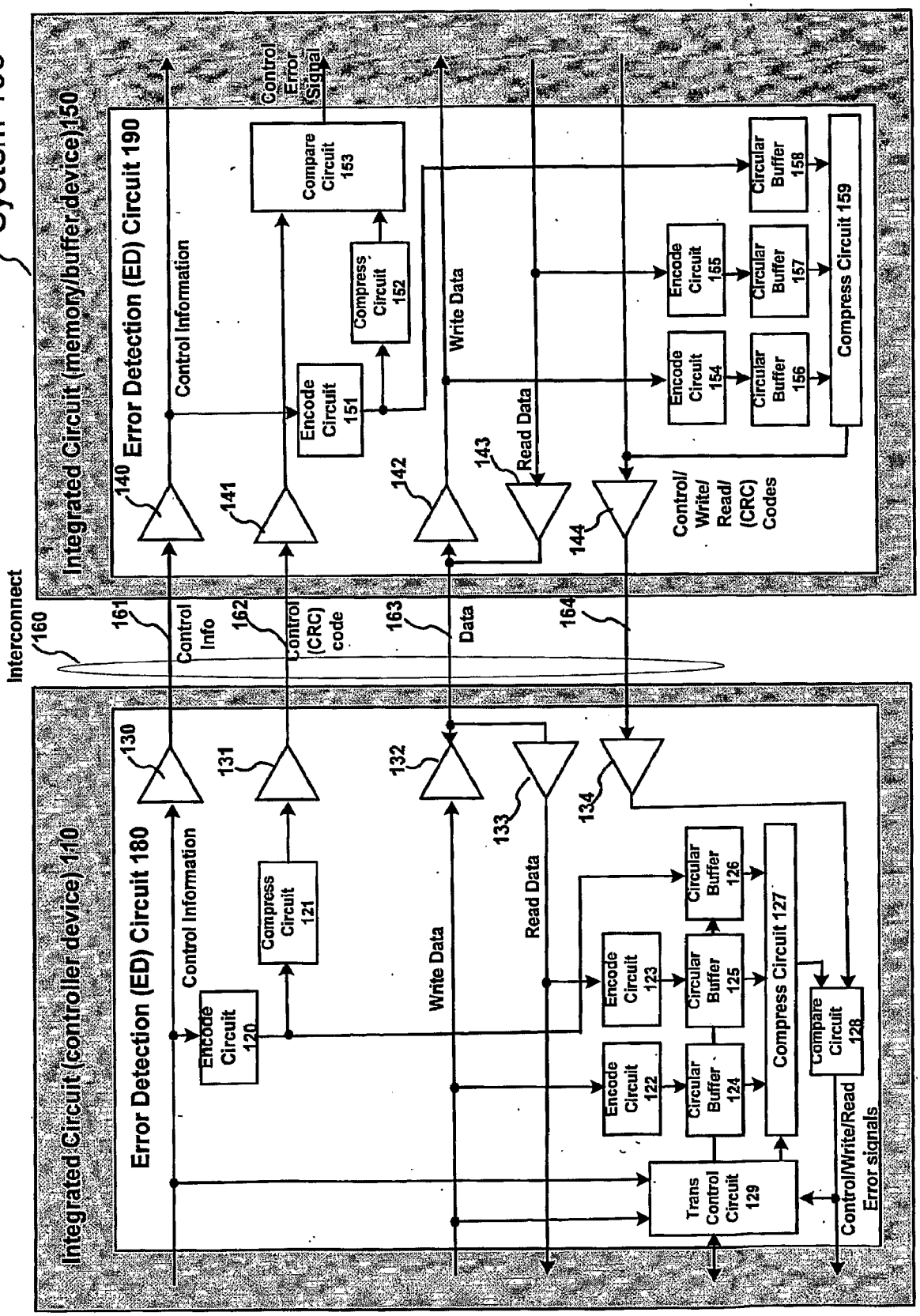
System 100
Integrated Circuit (memory/buffer device) 150
Error Detection (ED) Circuit 190
Control Information
Control Error Signal
Compare Circuit 153
Compress Circuit 152
Encode Circuit 151
Write Data
Read Data
Encode Circuit 154
Encode Circuit 155
Circular Buffer 156
Circular Buffer 157
Circular Buffer 158
Compress Circuit 159
Control/ Write/ Read/ (CRC) Codes
140
141
142
143
144
Interconnect 160
161 Control Info
162 Control (CRC) code
163 Data
164
Integrated Circuit (controller device) 110
Error Detection (ED) Circuit 180
Control Information
Encode Circuit 120
Compress Circuit 121
Write Data
Read Data
Encode Circuit 122
Encode Circuit 123
Circular Buffer 124
Circular Buffer 125
Circular Buffer 126
Compress Circuit 127
Compare Circuit 128
Trans Control Circuit 129
Control/Write/Read Error signals
130
131
132
133
134

Fig. 1

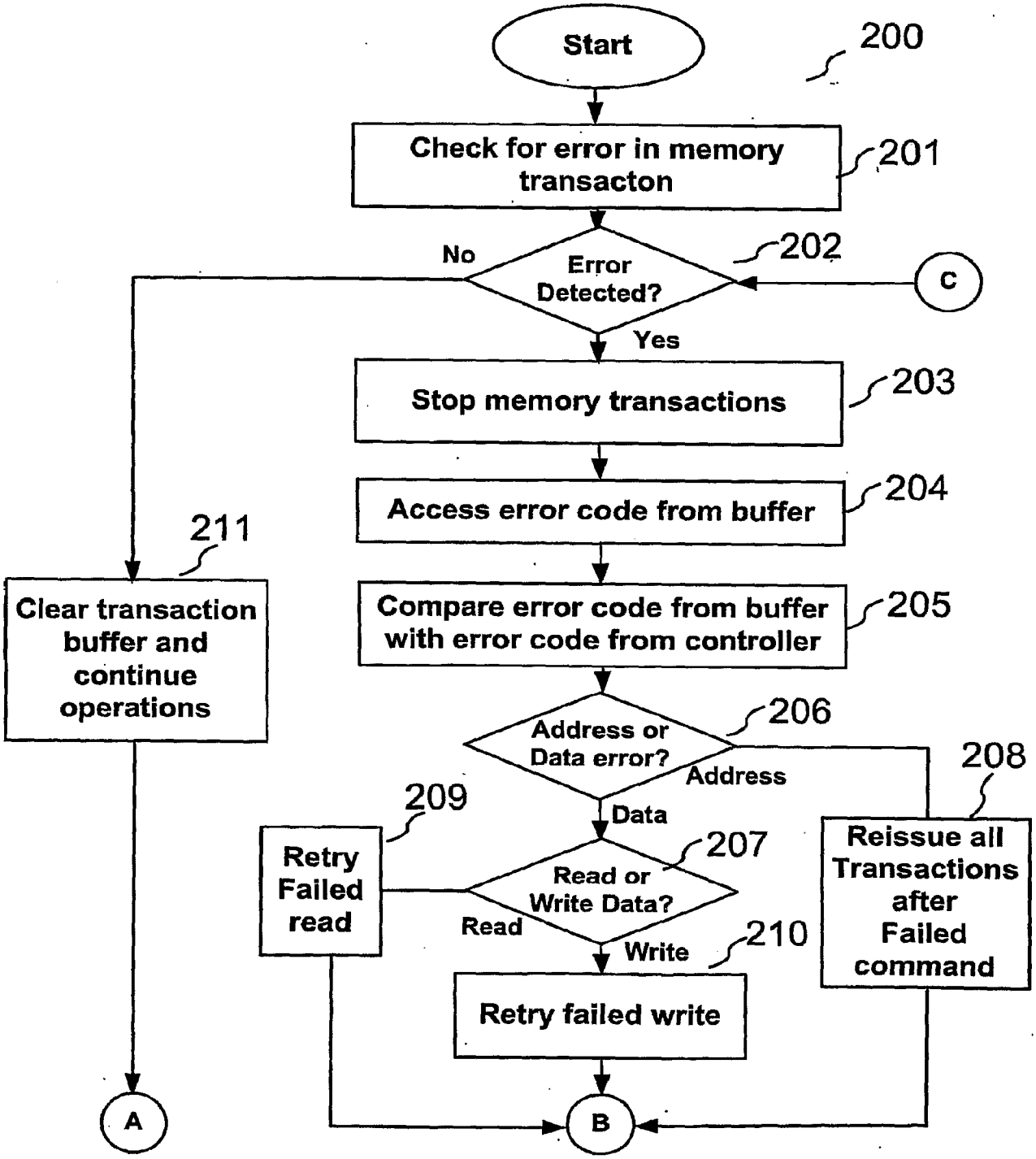
Start
200
Check for error in memory transacton
201
No
Error Detected?
202
C
Yes
Stop memory transactions
203
Access error code from buffer
204
211
Clear transaction buffer and continue operations
Compare error code from buffer with error code from controller
205
Address or Data error?
206
Address
208
Data
209
Retry Failed read
Read or Write Data?
207
Read
Write
210
Reissue all Transactions after Failed command
Retry failed write
A
B

Fig. 2A

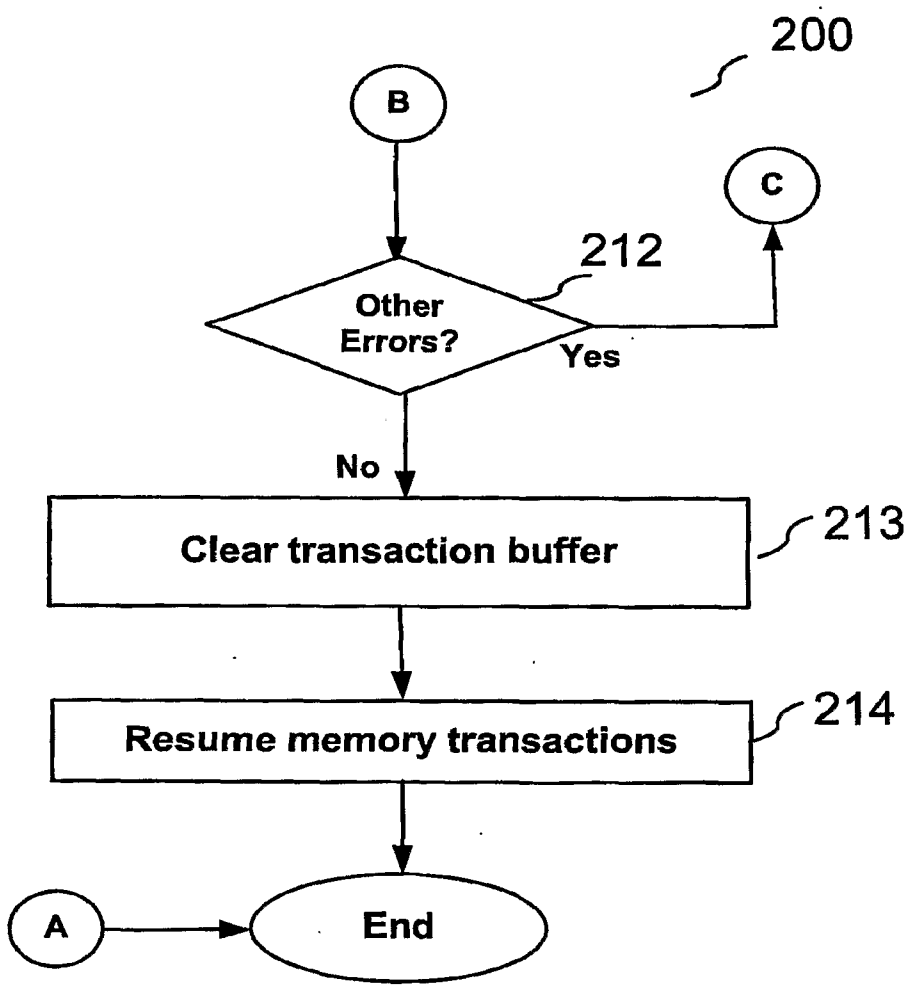
200
B
C
212
Other Errors?
Yes
No
Clear transaction buffer
213
Resume memory transactions
214
A
End

Fig. 2B

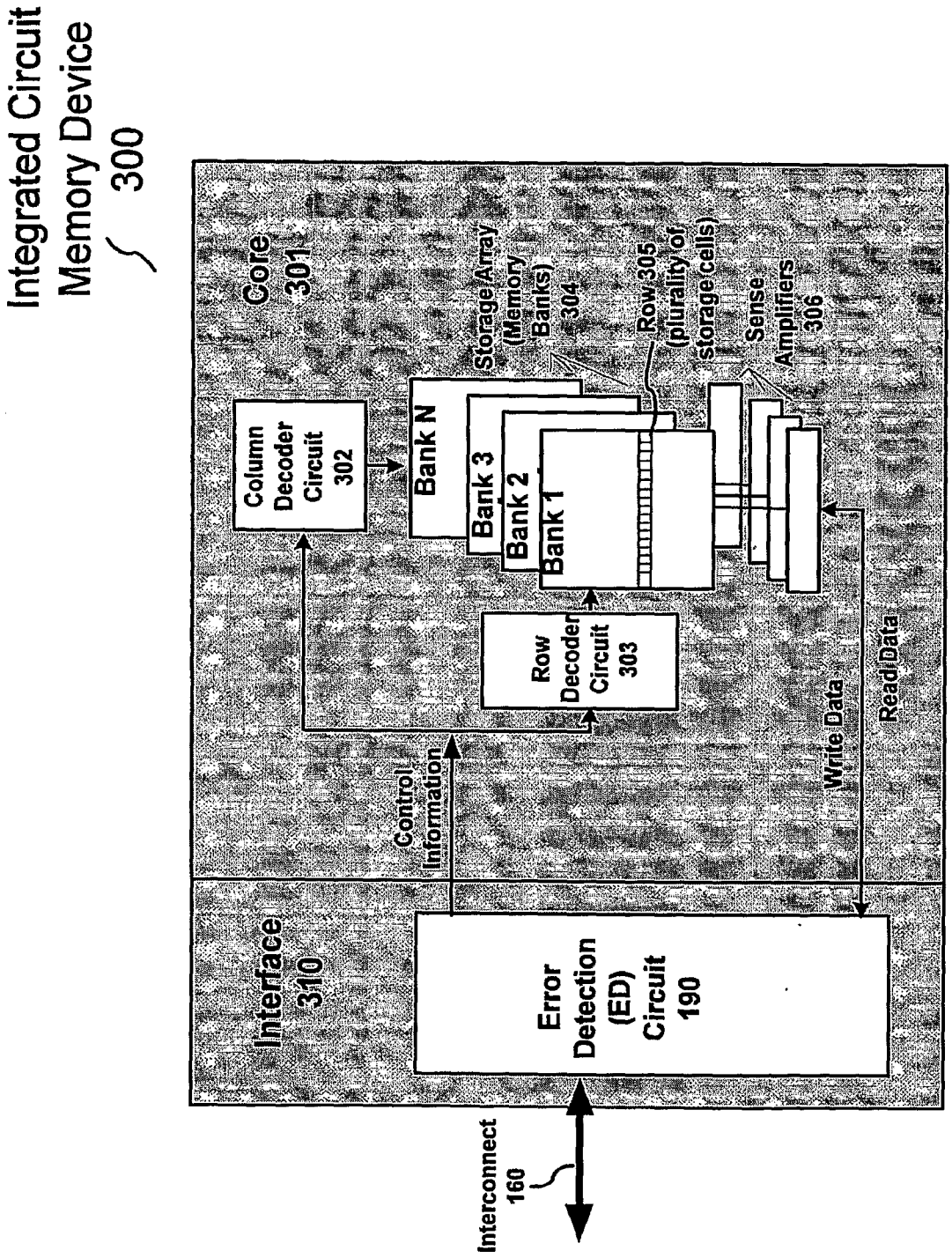
Integrated Circuit Memory Device 300
Core 301
Storage Array (Memory Banks) 304
Row 305 (plurality of storage cells)
Sense Amplifiers 306
Column Decoder Circuit 302
Bank N
Bank 3
Bank 2
Bank 1
Row Decoder Circuit 303
Control Information
Write Data
Read Data
Interface 310
Error Detection (ED) Circuit 190
Interconnect 160

Fig. 3

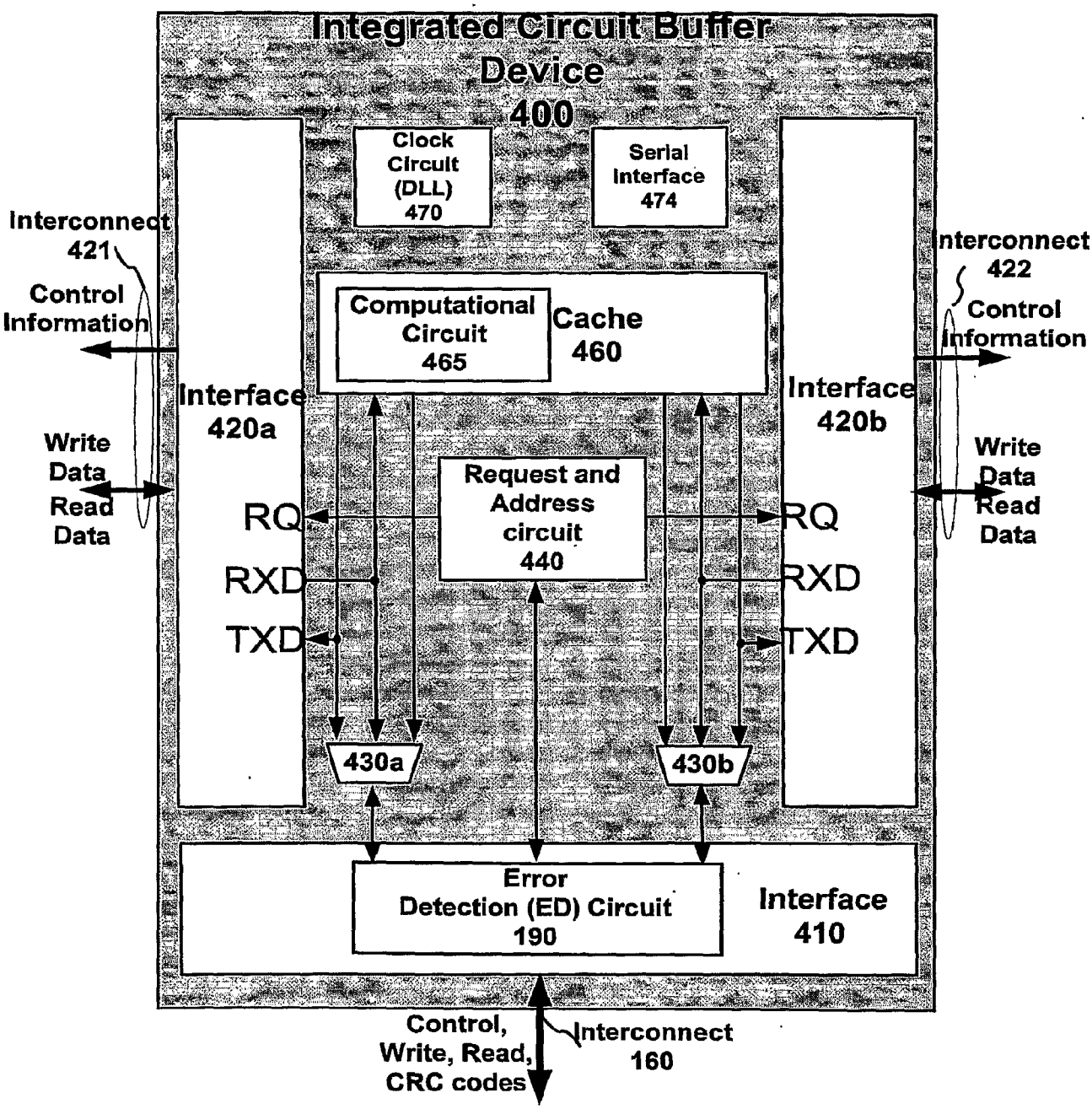
Integrated Circuit Buffer Device 400
Clock Circuit (DLL) 470
Serial Interface 474
Interconnect 421
Control Information
Write Data Read Data
Computational Circuit 465
Cache 460
Interface 420a
Request and Address circuit 440
RQ
RXD
TXD
Interface 420b
Interconnect 422
Control Information
Write Data Read Data
430a
430b
Error Detection (ED) Circuit 190
Interface 410
Control, Write, Read, CRC codes
Interconnect 160

Fig. 4

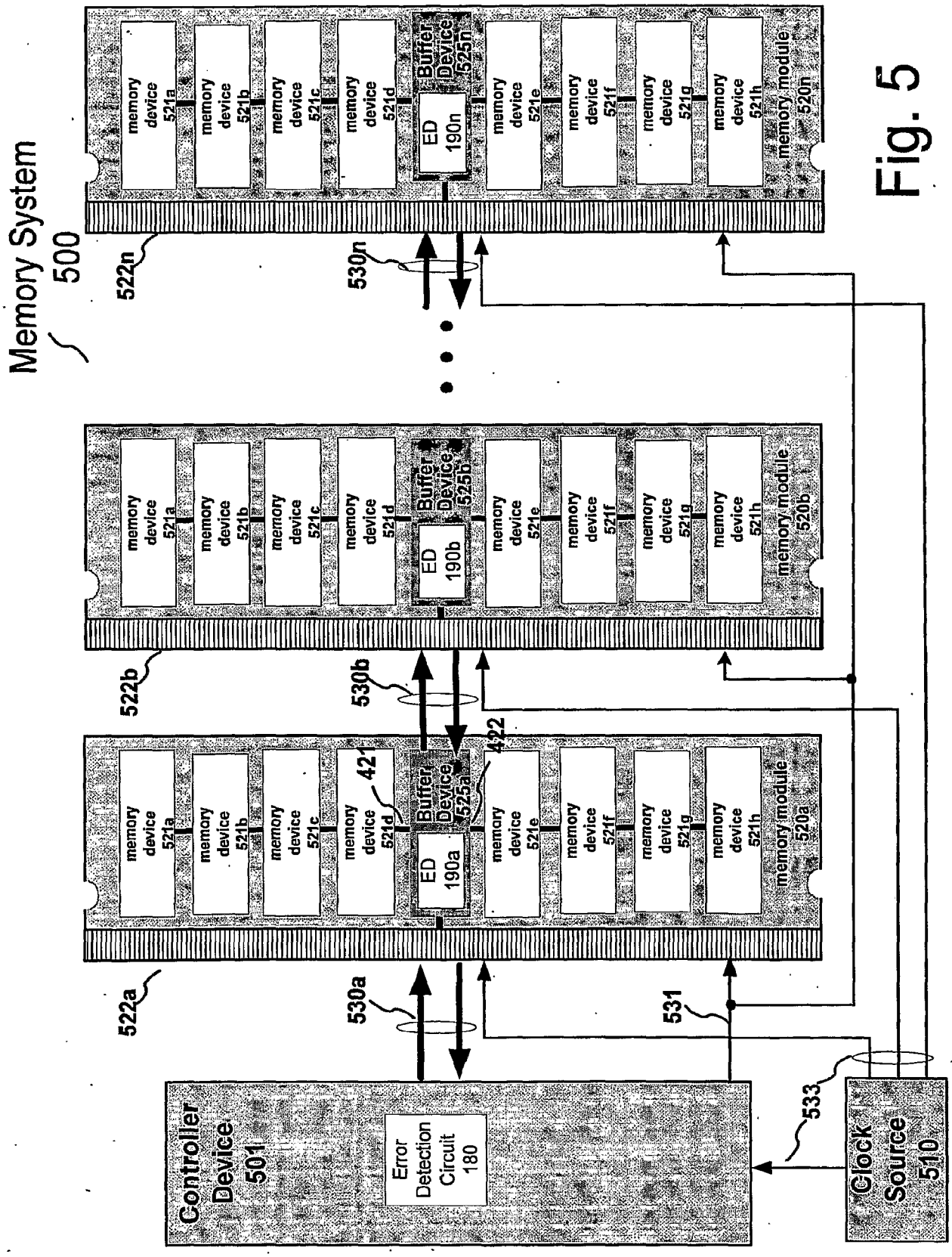
Memory System
500
Controller Device
501
Error Detection Circuit
180
Clock Source
510
memory module
520a
520b
520n
memory device
521a
521b
521c
521d
521e
521f
521g
521h
Buffer Device
525a
525b
525n
ED
190a
190b
190n
421
422
522a
522b
522n
530a
530b
530n
531
533

Fig. 5

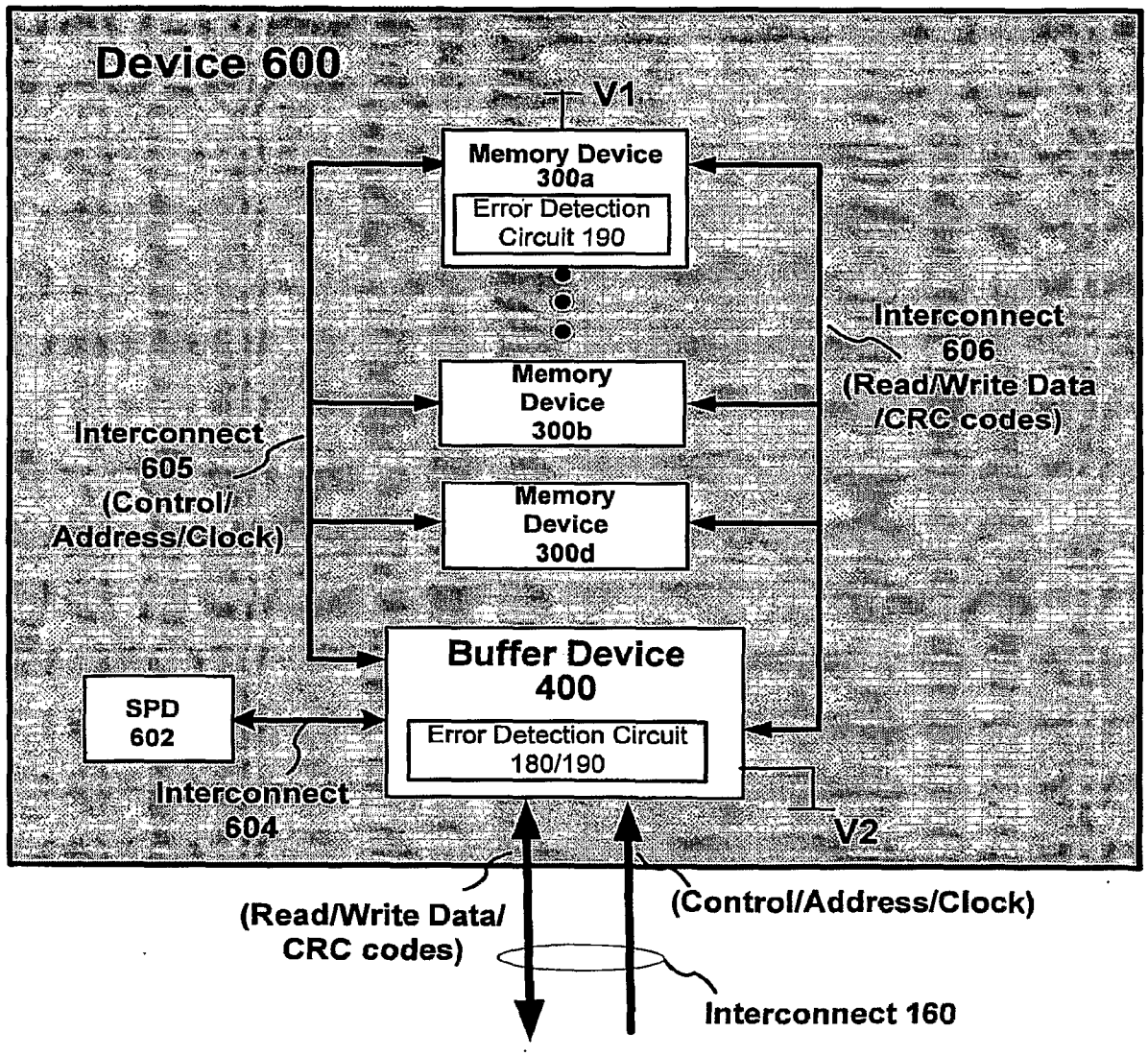
Device 600
V1
Memory Device 300a
Error Detection Circuit 190
Memory Device 300b
Memory Device 300d
Interconnect 606 (Read/Write Data /CRC codes)
Interconnect 605 (Control/ Address/Clock)
Buffer Device 400
Error Detection Circuit 180/190
SPD 602
Interconnect 604
V2
(Read/Write Data/ CRC codes)
(Control/Address/Clock)
Interconnect 160

Fig. 6