Title: INTEGRATED DEVICE COMPRISING HIGH DENSITY INTERCONNECTS AND REDISTRIBUTION LAYERS

Abstract: An integrated device (e.g., integrated package) that includes a base portion for the integrated device, a first die (206) coupled to a first surface of the base portion, and an underfill (222) between the first die and the base portion. The base portion includes a dielectric layer (202), and a set of redistribution metal layers (230-260). In some implementations, the integrated device further includes an encapsulation material (220) that encapsulates the first die. In some implementations, the integrated device further includes a second die (208) coupled to the first surface of the base portion. In some implementations, the integrated device further includes a set of interconnects (280) on the base portion, the set of interconnects coupling the first die and the second die. In some implementations, the first die includes a first set of interconnect pillars (216) and the second die includes a second set of interconnect pillars (218).
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INTEGRATED DEVICE COMPRISING HIGH DENSITY INTERCONNECTS AND REDISTRIBUTION LAYERS

CROSS-REFERENCE TO RELATED APPLICATION


BACKGROUND

Field

[0002] Various features relate to an integrated device that includes high density interconnects and redistributions layers.

Background

[0003] FIG. 1 illustrates a conventional integrated package 100 that includes a substrate 102, a first die 106, a second die 108, a first set of solder balls 116, a second set of solder bails 118, and a third set of solder balls 120. The first die 106 is coupled to the substrate 102 through the first set of solder balls 116. The second die 108 is coupled to the substrate 102 through the second set of solder bails 118. The third set of solder bails 120 is coupled to the substrate 102. Typically, the third set of solder balls 120 is coupled to a printed circuit board (PCB) (not shown).

[0004] Conventional integrated packages, such as the one described in FIG. 1, have certain limitations and downsides. For example, the substrate 102 of the integrated package 100 of FIG. 1 is typically made of an organic laminate (e.g., rigid or flexible), or a silicon (Si) interposer. The use of such materials as a substrate creates design problems when attempting to manufacture low profile integrated package. That is, these materials create substantial design penalty due to their manufacturing limitations. In particular, these materials make it impossible or cost-prohibitive to provide a low profile integrated package.

[0005] Moreover, the use of solder bails as a coupling method between a die and a substrate limits the density of the connection that can exist between a die and a substrate, as the minimum spacing required between solder balls is often greater than the minimum spacing required between traces and/or vias on a substrate.
[0006] In addition, during the manufacturing process of an integrated device, tool alignment tolerances and the shifting of dies can cause inaccuracy in the placement of dies on a substrate. To account for these issues, big landing pads must be provided to ensure that there is proper connection of the dies. These big landing pads can take up valuable space in the integrated device and add unnecessarily cost to the manufacturing of an integrated device.

[0007] Therefore, there is a need for a cost effective integrated package that has a low profile but also takes up a little real estate as possible. Ideally, such an integrated package will also provide higher density connections with the dies.

SUMMARY

[0008] Various features, apparatus and methods described herein provide an integrated device that includes high density interconnects redistribution layers.

[0009] A first example provides an integrated device that includes a base portion for the integrated device, a first die coupled to a first surface of the base portion, and an underfill between the first die and the base portion. The base portion includes a dielectric layer, and a set of redistribution metal layers.

[0010] According to an aspect, the integrated device further includes an encapsulation material that encapsulates the first die.

[0011] According to one aspect, the integrated device further includes a second die coupled to the first surface of the base portion. In some implementations, the integrated device further includes a set of interconnects on the base portion, the set of interconnects electrically coupling the first die and the second die. In some implementations, the first die includes a first set of interconnect pillars and the second die includes a second set of interconnect pillars. The set of interconnects is coupled to the first set of interconnects pillars and the second set of interconnect pillars while bypassing a bump pad and/or landing pad. In some implementations, the set of interconnects has a first pitch that is about 40 microns (µm) or less. In some implementations, the underfill is also between the second die and the base portion.

[0012] According to an aspect, the first die is a first wafer level die.

[0013] According to an aspect, the first die includes a first set of interconnect pillars, the first die is coupled to the set of redistribution metal layers through the first set of interconnect pillars. In some implementations, the first set of interconnect pillars has a first pitch that is about 40 microns (µm) or less.
According to one aspect, the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

A second example provides an apparatus that includes a base portion for an integrated device. The base portion includes a dielectric layer, and a redistribution means. The apparatus further includes a first die coupled to a first surface of the base portion, and a means for encapsulating an area between the first die and the base portion.

According to an aspect, the apparatus further includes an encapsulation means that encapsulates the first die.

According to one aspect, the apparatus further includes a second die coupled to the first surface of the base portion. In some implementations, the apparatus further includes a set of interconnects on the base portion. The set of interconnects electrically couples the first die and the second die. In some implementations, the first die includes a first set of interconnect pillars. The second die includes a second set of interconnect pillars. The set of interconnects is coupled to the first set of interconnects pillars and the second set of interconnect pillars while bypassing a landing pad. In some implementations, the set of interconnects includes a first pitch that is about 40 microns (μm) or less.

According to an aspect, the first die is a first wafer level die.

According to one aspect, the first die includes a first set of interconnect pillars. The first die is coupled to the redistribution means through the first set of interconnect pillars.

According to an aspect, the first set of interconnect pillars includes a first pitch that is about 40 microns (μm) or less.

According to one aspect, the apparatus is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

A third example provides a method for providing an integrated device. The method forms a base portion for the integrated device, where forming the base portion includes forming a dielectric layer, and forming a set of redistribution metal layers. The method provides a first die on a first surface of the base portion. The method forms an underfill between the first die and the base portion.
According to an aspect, the method further forms an encapsulation material that encapsulates the first die.

According to one aspect, the method provides a second die on the first surface of the base portion. In some implementations, the method forms a set of interconnects on the base portion. The set of interconnects electrically coupling the first die and the second die. In some implementations, the first die includes a first set of interconnect pillars and the second die includes a second set of interconnect pillars. The set of interconnects is coupled to the first set of interconnects pillars and the second set of interconnect pillars while bypassing a landing pad. In some implementations, the set of interconnects includes a first pitch that is about 40 microns (μm) or less.

According to an aspect, the first die is a first wafer level die.

According to one aspect, the first die includes a first set of interconnect pillars. The first die is coupled to the set of redistribution metal layers through the first set of interconnect pillars. In some implementations, the first set of interconnect pillars includes a first pitch that is about 40 microns (μm) or less.

According to an aspect, the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

**DRAWINGS**

Various features, nature and advantages may become apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

FIG. 1 illustrates a profile view of a conventional integrated device.

FIG. 2 illustrates an example of an integrated device.

FIG. 3 illustrates an example of a die.

FIG. 4 illustrates an example of a die that includes a through substrate via.

FIG. 5 illustrates an example of an integrated device.

FIG. 6 illustrates an example of an integrated device.

FIG. 7A illustrates part of an exemplary sequence for providing/manufacturing an integrated device.

FIG. 7B illustrates part of an exemplary sequence for providing/manufacturing an integrated device.
FIG. 7C illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 7D illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 8A illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 8B illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 8C illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 8D illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 9 illustrates an exemplary method for providing / manufacturing an integrated device.

FIG. 10A illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 10B illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 10C illustrates part of an exemplary sequence for providing / manufacturing an integrated device.

FIG. 11 illustrates various electronic devices that may integrate a semiconductor device, a die, an integrated circuit and/or PCB described herein.

DETAILED DESCRIPTION

In the following description, specific details are given to provide a thorough understanding of the various aspects of the disclosure. However, it will be understood by one of ordinary skill in the art that the aspects may be practiced without these specific details. For example, circuits may be shown in block diagrams in order to avoid obscuring the aspects in unnecessary detail. In other instances, well-known circuits, structures and techniques may not be shown in detail in order not to obscure the aspects of the disclosure.

Overview
Some novel features pertain to an integrated device (e.g., integrated package) that includes a base portion for the integrated device, a first die (e.g., first wafer level die) coupled to a first surface of the base portion, and an underfill between the first die and the base portion. The base portion includes a dielectric layer, and a set of redistribution metal layers. In some implementations, the integrated device further includes an encapsulation material that encapsulates the first die. In some implementations, the integrated device further includes a second die (e.g., second wafer level die) coupled to the first surface of the base portion. In some implementations, the integrated device further includes a set of interconnects on the base portion, the set of interconnects electrically coupling the first die and the second die. In some implementations, the first die includes a first set of interconnect pillars and the second die includes a second set of interconnect pillars. The set of interconnects is coupled to the first set of interconnects pillars and the second set of interconnect pillars while bypassing a landing pad (e.g., bump pad). In some implementations, the set of interconnects has a first pitch of about 40 microns \((\mu m)\) or less. In some implementations, the underfill is also between the second die and the base portion.

Exemplary **Integrated Device That Includes Redistribution Layers**

FIG. 2 conceptually illustrates an example of a side view of an integrated device (e.g., semiconductor device, integrated package) that includes several dies. Specifically, FIG. 2 illustrates an integrated device 200 (e.g., integrated package) that includes a dielectric layer 202, a first set of solder balls 204, a first die 206, a second die 208, an encapsulation material 220, and an underfill 222. Different implementations may use different materials for the encapsulation material 220. For example, the encapsulation material 220 may include one of at least a mold, an epoxy and/or a polymer fill. The dies (e.g., first die 206, second die 208) may represent different types of dies, such as memory dies, and/or processors. In some implementations, the first die 206 and/or the second die 208 are wafer level dies. Dies are further described in detail below with reference to FIGS. 3-4.

The dielectric layer 202 may include one dielectric layer or several dielectric layers. In some implementations, the dielectric layer 202 is an insulation layer. FIG. 2 illustrates that the dielectric layer 202 includes a set of metal layers. In particular, the dielectric layer 202 includes a first set of redistribution interconnects 230, a first under bump metallization (UBM) layer 232, a second set of redistribution interconnects 240, a
second under bump metallization (UBM) layer 242, a third set of redistribution interconnects 250, a third under bump metallization (UBM) layer 252, a fourth set of redistribution interconnects 260, a fourth under bump metallization (UBM) layer 262, and a fifth set of redistribution interconnects 280. In some implementations, the first, second, third, and fourth sets of redistribution interconnects 230, 240, 250, and 260 are redistribution layers h₁ the dielectric layer 202. The redistribution layers may include vias. Different implementations may have different number of redistribution metal layers (e.g., 1, 2 or more metal layers).

The fifth set of redistribution interconnects 280 is a metal layer on the dielectric layer 202 (e.g., on surface of dielectric layer 202). In some implementations, the first, second, third, and fourth sets of redistribution interconnects 230, 240, 250, and 260 have respectively, a first pitch, a second pitch, a third pitch, and a fourth pitch. In some implementations, the fifth set of redistribution interconnects 280 has a fifth pitch that is different than the first pitch, the second pitch, the third pitch, and/or the fourth pitch. In some implementations, the fifth pitch is less than the first pitch, the second pitch, the third pitch, and/or the fourth pitch. The fifth set of redistribution interconnects 280 is coupled to the first set of interconnects 216 and the second set of interconnects 218. In some implementations, the fifth set of redistribution interconnects 280 includes a set of high density interconnects. In some implementations, the fifth set of interconnects 280 includes a first pitch that is about 40 microns (μm) or less.

The first die 206 is coupled to a first surface of the dielectric layer 202 through the first set of interconnects 216. In some implementations, the first set of interconnects 216 are metal pillars (e.g., metal layers). In some implementations, the metal pillars are copper pillars. In some implementations, the first die 206 is electrically coupled to at least one of the set of solder bails 204 through the first set of interconnects 216, the first set of redistribution interconnects 230, the first UBM layer 232, the second set of redistribution interconnects 240, and/or the second UBM layer 242.

The second die 208 is coupled to the first surface of the dielectric layer 202 through the second set of interconnects 218. In some implementations, the second set of interconnects 218 are metal pillars (e.g., metal layers). In some implementations, the metal pillars are copper pillars. In some implementations, the second die 208 is electrically coupled to at least one of the set of solder bails 204 through the second set of interconnects 218, the third set of redistribution interconnects 250, and/or the third UBM layer 252.
As shown in FIG. 2, the first die 206 may be electrically coupled to the second die 208 through the fifth set of redistribution interconnects 280. FIG. 2 also illustrates that the first set of interconnects 216 and the second set of interconnects 218 are encapsulated by the underfill 222. The underfill 222 is optional in some instances.

FIG. 3 conceptually illustrates an example of a die 300 (which is a form of an integrated device). For purpose of clarity, FIG. 3 illustrates a generalization of a die. As such, not all the components of a die are shown in FIG. 3. In some implementations, the die 300 may correspond to at least one of the dies 206, and/or 208 of FIG. 2. As shown in FIG. 3, the die 300 (e.g., integrated device) includes a substrate 301, several lower level metal layers and dielectric layers 302, a set of interconnects 311-316 (e.g., bumps, pillar interconnects), and an encapsulation material 320 (e.g., mold, epoxy, polymer fill). In some implementations, the encapsulation material 320 may be optional.

The die 300 includes a front side region (e.g., active region) and a back side region. In some implementations, the die 300 is wafer level die.

In some implementations, the die 300 may also include pads, a passivation layer, a first insulation layer, a first under bump metallization (UBM) layer, and a second under bump metallization (UBM) layer. In such instances, the pad may be coupled to the lower level metal layers and dielectric layers 302. A passivation layer may be positioned between the lower level metal layers and dielectric layers 302 and the encapsulation material 320. A first bump layer may be coupled to the pad and one of the interconnects 311-316.

In some implementations, a die may also include one or more through substrate vias (TSVs). FIG. 4 conceptually illustrates an example of a die 400 (which is a form of an integrated device) that includes at least one TSV. For purpose of clarity, FIG. 4 illustrates a generalization of a die. As such, not all the components of a die are shown in FIG. 4. In some implementations, the die 400 may correspond to at least one of the dies 206, and/or 208 of FIG. 2. As shown in FIG. 4, the die 400 (e.g., integrated device) includes a substrate 401, several lower level metal layers and dielectric layers 402, a set of interconnects 411-416 (e.g., bumps, pillar interconnects), and an encapsulation material 420 (e.g., mold, epoxy, polymer fill). In some implementations, the encapsulation material 420 may be optional.

The die 400 includes a front side region (e.g., active region) and a back side region. In some implementations, the die 400 is wafer level die.
As shown in FIG. 4, the die 400 includes a first through substrate via (TSV) 421, a second TSV 422, a third TSV 423, and a fourth TSV 424. The first TSV 421 and the second TSV 422 traverse the substrate 401 and the lower level metal layers and dielectric layers 402. That is, the first TSV 421 and the second TSV 422 traverse the active region (e.g., front side) and the back side region of the die 400. The third TSV 433 and the fourth TSV 434 traverse the substrate 401. That is, the third TSV 433 and the fourth TSV 434 traverse the active region (e.g., front side) of the die 400.

In some implementations, the die 400 may also include pads, a passivation layer, a first insulation layer, a first under bump metallization (UBM) layer, and a second under bump metallization (UBM) layer. In such instances, the pad may be coupled to the lower level metal layers and dielectric layers 402. A passivation layer may be positioned between the lower level metal layers and dielectric layers 402 and the encapsulation material 420. A first bump layer may be coupled to the pad and one of the interconnects 411-416.

FIG. 5 conceptually illustrates an example of a side view of an integrated device (e.g., semiconductor device, integrated package) that includes several dies. Specifically, FIG. 5 illustrates a integrated device 500 (e.g., integrated package) that includes a dielectric layer 502, a first set of solder balls 504, a first die 506, a second die 508, an encapsulation material 520, and an underfill 522. Different implementations may use different materials for the encapsulation material 520. For example, the encapsulation material 520 may include one of at least a mold, an epoxy and/or a polymer fill. The dies (e.g., first die 506, second die 508) may represent different types of dies, such as memory dies, and/or processors. In some implementations, the first die 506 and/or the second die 508 are wafer level dies. Dies are described in detail with reference to FIGS. 3-4.

The dielectric layer 502 may include one dielectric layer or several dielectric layers. In some implementations, the dielectric layer 502 is an insulation layer. FIG. 5 illustrates that the dielectric layer 502 includes a set of metal layers. In particular, the dielectric layer 502 includes a first set of redistribution interconnects 530, a first under bump metallization (UBM) layer 532, a second set of redistribution interconnects 540, a second under bump metallization (UBM) layer 542, a third set of redistribution interconnects 550, a third under bump metallization (UBM) layer 552, a fourth set of redistribution interconnects 560, a fourth under bump metallization (UBM) layer 562, and a fifth set of redistribution interconnects 580. In some implementations, the first,
second, third, fourth, and fifth set of redistribution interconnects 530, 540, 550, 560, and 580 are redistribution layers. The redistribution layers may include vias. Different implementations may have different number of redistribution metal layers (e.g., 1, 5 or more metal layers).

[0065] The first die 506 is coupled to a first surface of the dielectric layer 502 through a first set of interconnects 516. In some implementations, the first set of interconnects 516 are metal pillars (e.g., metal layers). In some implementations, the metal pillars are copper pillars. In some implementations, the first die 506 is electrically coupled to at least one of the set of solder bails 504 through the first set of interconnects 516, the first set of redistribution interconnects 530, the first UBM layer 532, the second set of redistribution interconnects 540, and/or the second UBM layer 542.

[0066] The second die 508 is coupled to the first surface of the dielectric layer 502 through a second set of interconnects 518. In some implementations, the second set of interconnects 518 are metal pillars (e.g., metal layers). In some implementations, the metal pillars are copper pillars. In some implementations, the second die 508 is electrically coupled to at least one of the set of solder bails 504 through the second set of interconnects 518, the third set of redistribution interconnects 550, and/or the third UBM layer 552.

[0067] As shown in FIG. 5, the first die 506 may be electrically coupled to the second die 508 through the fifth set of redistribution interconnects 580. FIG. 5 also illustrates that the first set of interconnects 516 and the second set of interconnects 518 is encapsulated by the underfill 522. The underfill 522 is optional in some instances.

[0068] FIG. 6 conceptually illustrates an example of a side view of an integrated device (e.g., semiconductor device, integrated package) that includes several dies. Specifically, FIG. 6 illustrates a integrated device 600 (e.g., integrated package) that includes a dielectric layer 602, a first set of solder balls 604, a first die 606, a second die 608, and an encapsulation material 620. Different implementations may use different materials for the encapsulation material 620. For example, the encapsulation material 620 may include one of at least a mold, an epoxy and/or a polymer fill. The dies (e.g., first die 606, second die 608) may represent different types of dies, such as memory dies, and/or processors. In some implementations, the first die 606 and/or the second die 608 are wafer level dies. Dies are described in detail with reference to FIGS. 3-4.

[0069] The dielectric layer 602 may include one dielectric layer or several dielectric layers. In some implementations, the dielectric layer 602 is an insulation layer. FIG. 6
illustrates that the dielectric layer 602 includes a set of metal layers. In particular, the dielectric layer 602 includes a first set of redistribution interconnects 630, a first under bump metallization (UBM) layer 632, a second set of redistribution interconnects 640, a second under bump metallization (UBM) layer 642, a third set of redistribution interconnects 650, a third under bump metallization (UBM) layer 652, a fourth set of redistribution interconnects 660, a fourth under bump metallization (UBM) layer 662, and a fifth set of redistribution interconnects 680. In some implementations, the first, second, third, and fourth sets of redistribution interconnects 630, 640, 650, and 660 are redistribution layers. The redistribution layers may include vias. Different implementations may have different number of redistribution metal layers (e.g., 1, 6 or more metal layers).

[0070] The first die 606 is coupled to a first surface of the dielectric layer 602 through a first set of interconnects 616. In some implementations, the first set of interconnects 616 are metal pillars (e.g., metal layers). In some implementations, the metal pillars are copper pillars. In some implementations, the first die 606 is electrically coupled to at least one of the set of solder bails 604 through the first set of interconnects 616, the first set of redistribution interconnects 630, the first UBM layer 632, the second set of redistribution interconnects 640, and/or the second UBM layer 642.

[0071] The second die 608 is coupled to the first surface of the dielectric layer 602 through a second set of interconnects 618. In some implementations, the second set of interconnects 618 are metal pillars (e.g., metal layers). In some implementations, the metal pillars are copper pillars. In some implementations, the second die 608 is electrically coupled to at least one of the set of solder bails 604 through the second set of interconnects 618, the third set of redistribution interconnects 650, and/or the third UBM layer 652.

[0072] As shown in FIG. 6, the first die 606 may be electrically coupled to the second die 608 through the fifth set of redistribution interconnects 680.

[0073] Having described several integrated devices, a sequence for providing / manufacturing an integrated device (e.g., semiconductor device) will now be described below.

Exemplary Sequence for Providing / Manufacturing an Integrated Device That Includes a Redistribution Layer
In some implementations, providing an integrated device (e.g., integrated package) that includes redistribution layers includes several processes. FIGS. 7A-7D illustrate an exemplar™ sequence for providing an integrated device. In some implementations, the sequence of FIGS. 7A-7D may be used to provide / manufacture the integrated device of FIGS. 2 and/or 5-6, and/or other integrated devices described in the present disclosure.

It should also be noted that the sequence of FIGS. 7A-7D may be used to provide / manufacture integrated devices that also include circuit elements. It should further be noted that the sequence of FIGS. 7A-7D may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device that includes several dies.

In some implementations, the process of FIGS. 7A-7D illustrates a novel process that provides an integrated device with high density interconnects (e.g., pitch between interconnects is about 40 microns or less) and/or an integrated device that bypasses the use of unnecessary big landing pads (e.g., big bump pads).

As shown in stage 1 of FIG. 7A, a carrier (e.g., carrier 700), a first set of interconnects 702 (e.g., first set of traces) and a second set of interconnects 704 (e.g., second set of traces) are provided. In some implementations, the carrier is a substrate. Different implementations may use different materials for the carrier (e.g., silicon substrate, glass substrate, ceramic substrate).

At stage 2, several dies are provided on the carrier. As shown in stage 2, a first die 712 and a second die 714 are provided on the earner 700. Specifically, the front sides (active sides) of the first die 712 and the second die 714 are coupled to the carrier 700. Examples of dies are described in FIGS. 3-4. The first die 712 includes a first set of interconnects 722 (e.g., bumps, copper pillar). The second die 714 includes a second set of interconnects 724 (e.g., bumps, copper pillar). As shown at stage 2, the first set of interconnects 722 of the first die 712 is coupled to the first set of interconnects 702 of the carrier 700. Similarly, the second set of interconnects 724 of the second die 714 is coupled to the second set of interconnects 704 of the earner 700. In some implementations, the first die 712 and/or the second die 714 are wafer level dies.

At stage 3, an underfill 730 is provided on the carrier 700. In some implementations, the underfill 730 is provided such that the underfill 730 covers the first set of interconnects 702, the second set of interconnects 704, the first set of interconnects 722, and the second set of interconnects 724.
interconnects 722, and the second set of interconnects 724. In some implementations, providing the underfill 730 is optional.

[0080] At stage 4, an encapsulation material 740 is provided. The encapsulation material 740 substantially or completely surrounds or encapsulates the first die 712 and the second die 714.

[0081] At stage 5, as shown in FIG. 7B, the integrated device is flipped and coupled to a temporary carrier 742. That is, the encapsulation material 740 is coupled to the temporary carrier 742. Different implementations may use different materials (e.g., substrate, silicon, glass, ceramic) for the carrier 742. In some implementations, an adhesive layer (not shown) may be used to couple the encapsulation material 740 of the integrated device to the temporary carrier 742. Different implementations may use different materials for the adhesion layer. In some implementations, the temporary carrier 742 is a bonding tape.

[0082] At stage 6, a first surface of the integrated device is removed (e.g., polished, grinded). In this example, the surface that includes the carrier 700 is removed (e.g., polished, grinded). In some implementations, polishing the integrated device may include polishing and/or grinding the carrier 700, the first set of interconnects 702, the second set of interconnects 704, the first set of interconnects 722, the second set of interconnects 724, the underfill 730, and/or the encapsulation material 740. In some implementations, polishing the integrated device may leave behind portions of the first set of interconnects 702, the second set of interconnects 704, the first set of interconnects 722, the second set of interconnects 724, the underfill 730, and/or the encapsulation material 740.

[0083] At stage 7, a first dielectric layer 750 and several redistribution interconnects (e.g., redistribution interconnects 751-755) are provided on the front side of the first die 712 and the second die 714. Specifically, several interconnects are provided on the first set of interconnect 722 and the second set of interconnects 724. In some implementations, the redistribution interconnects 751-755 are formed on a first redistribution metal layer. In some implementations, the redistribution interconnects 755-755 may include at least one via. In some implementations, the redistribution interconnects 751-755 bypasses the use of unnecessary landing pads (e.g., big bump pads) when coupling to the first set of interconnect 722 and/or the second set of interconnects 724. In some implementations, the redistribution interconnects 751-755
are directly coupled to the first set of interconnect 722 and/or the second set of interconnects 724.

[0084] At stage 8, as shown in FIG. 7C, a second dielectric layer 760 and several redistribution interconnects (e.g., redistribution interconnects 761-764) are provided on the first dielectric layer 750 and the redistribution interconnects 751-754. In some implementations, the redistribution interconnects 761-764 are formed on a second redistribution metal layer. In some implementations, the redistribution interconnects 761-764 may include at least one via.

[0085] At stage 9, a third dielectric layer 770 and several redistribution interconnects (e.g., redistribution interconnects 771-774) are provided on the second dielectric layer 760 and the redistribution interconnects 761-764. In some implementations, the redistribution interconnects 771-774 is formed on a third redistribution metal layer. In some implementations, the redistribution interconnects 771-774 may include at least one via.

[0086] At stage 10, at least one under bump metallization (UBM) layer is provided. Specifically, a first under bump metallization (UBM) layer 781, a second UBM layer 782, a third UBM layer 783, and a fourth UBM layer 784 are provided. The UBM layers are provided on the fourth dielectric layer 780. In some implementations, providing the UBM layer is optional.

[0087] At stage 11, as shown in FIG. 7D, at least one solder ball is provided on the UBM layer. Specifically, a first solder ball 791 is coupled to the first UBM layer 781, a second solder ball 792 is coupled to the second UBM layer 782, a third solder ball 793 is coupled to the third UBM layer 783, and a fourth solder ball 794 is coupled to the fourth UBM layer 784. Stage 11 illustrates the set of dielectric layers 790. In some implementations, the set of dielectric layers 790 includes the dielectric layers 750, 760, 770 and 780. In some implementations, the solder ball may be coupled to the redistribution interconnects instead of a UBM layer.

[0088] At stage 12, a portion of the integrated device is removed (e.g., polished). As shown at stage 12, at least a portion of the carrier 742 is removed (e.g., entire carrier 742 is removed). In some implementations, at least a portion of the encapsulation material 740 is also removed.

Exemplary Sequence for Providing / Manufacturing an Integrated Device That includes a Redistribution Layer
In some implementations, providing an integrated device (e.g., integrated package) that includes redistribution layers includes several processes. FIGS. 8A-8D illustrate an exemplary sequence for providing an integrated device. In some implementations, the sequence of FIGS. 8A-8D may be used to provide / manufacture the integrated device of FIGS. 2 and/or 5-6, and/or other integrated devices described in the present disclose.

It should also be noted that the sequence of FIGS. 8A-8D may be used to provide / manufacture integrated devices that also include circuit elements. It should further be noted that the sequence of FIGS. 8A-8D may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device that includes several dies.

In some implementations, the process of FIGS. 8A-8D illustrates a novel process that provides an integrated device with high density interconnects (e.g., pitch between interconnects is about 40 microns or less) and/or an integrated device that bypasses the use of unnecessary big landing pads (e.g., big bump pads).

As shown in stage 1 of FIG. 8A, a carrier (e.g., carrier 800), a first set of interconnects 802 (e.g., first set of traces) and a second set of interconnects 804 (e.g., second set of traces) are provided. In some implementations, the carrier is a substrate. Different implementations may use different materials for the carrier (e.g., silicon substrate, glass substrate, ceramic substrate).

At stage 2, several dies are provided on the carrier. As shown in stage 2, a first die 812 and a second die 814 are provided on the carrier 800. Specifically, the front side (active side) of the first die 812 and the second die 814 are coupled to the carrier 800. Examples of dies are described in FIGS. 3-4. The first die 812 includes a first set of interconnects 822 (e.g., bumps, copper pillar). The second die 814 includes a second set of interconnects 824 (e.g., bumps, copper pillar). As shown at stage 2, the first set of interconnects 822 of the first die 812 is coupled to the first set of interconnects 802 of the carrier 800. Similarly, the second set of interconnects 824 of the second die 814 is coupled to the second set of interconnects 804 of the carrier 800. In some implementations, the first die 812 and/or the second die 814 are wafer level dies.

At stage 3, an underfill 830 is provided on the carrier 800. In some implementations, the underfill 830 is provided such that the underfill 830 covers the first set of interconnects 802, the second set of interconnects 804, the first set of
interconnects 822, and the second set of interconnects 824. In some implementations, providing the underfill 830 is optional.

[0095] At stage 4, an encapsulation material 840 is provided. The encapsulation material 840 substantially or completely surrounds or encapsulates the first die 812 and the second die 814.

[0096] At stage 5, as shown in FIG. 8B, the integrated device is flipped and coupled to a temporary carrier 842. That is, the encapsulation material 840 is coupled to the temporary carrier 842. Different implementations may use different materials (e.g., substrate, silicon, glass, ceramic) for the carrier 842. In some implementations, an adhesive layer (not shown) may be used to couple the encapsulation material 840 of the integrated device to the temporary carrier 842. Different implementations may use different materials for the adhesion layer. In some implementations, the temporary carrier 842 is a bonding tape.

[0097] At stage 6, a first surface of the integrated device is removed (e.g., polished, grinded). In this example, the surface that includes the carrier 800 is removed (e.g., polished, grinded). In some implementations, polishing the integrated device may include polishing and/or grinding the carrier 800, the first set of interconnects 802, the second set of interconnects 804, the first set of interconnects 822, the second set of interconnects 824, the underfill 830, and/or the encapsulation material 840. In some implementations, polishing the integrated device may leave behind portions of the first set of interconnects 802, the second set of interconnects 804, the first set of interconnects 822, the second set of interconnects 824, the underfill 830, and/or the encapsulation material 840.

[0098] In some implementations, polishing the integrated device includes creating at least one cavity (e.g., cavities 825) in the integrated device. For example, the cavity 825 may be created in the underfill 830 and/or the encapsulation material 840.

[0099] At stage 7, a metal layer is provided in the cavity 825. The metal layer defines an interconnect from a set of interconnects 826. When several cavities are created, several metal layers may be provided in some implementations. The set of interconnects 826 electrically couples the first set of interconnects 822 and the second set of interconnects 824. In some implementations, the set of interconnects 826 electrically couples the first die 812 and the second die 814. In some implementations, the set of interconnects 826 bypasses the use of unnecessary landing pads (e.g., big bump pads) when coupling to the first set of interconnects 822 and/or the second set of
interconnects 824. In some implementations, the set of interconnects 826 is directly coupled to the first set of interconnects 822 and the second set of interconnects 824. In some implementations, the set of interconnects 826 is coupled to the side surface of the first set of interconnects 822 and the side surface of the second set of interconnects 824. In some implementations, the set of interconnects 826 is coupled to the top surface of the first set of interconnects 822 and the top surface of the second set of interconnects 824. In some implementations, the set of interconnects 826 are high density interconnects. In some implementations, a pitch of the set of interconnects 826 is about 40 microns (μm) or less.

[00100] At stage 8, a first dielectric layer 850 and several redistribution interconnects (e.g., redistribution interconnects 851-854) are provided on the front side of the first die 812 and the second die 814. Specifically, several interconnects are provided on the first set of interconnect 822 and the second set of interconnects 824. In some implementations, the redistribution interconnects 851-854 are formed on a first redistribution metal layer. In some implementations, the redistribution interconnects 855-854 may include at least one via. In some implementations, the redistribution interconnects 851-854 bypasses the use of unnecessary landing pads (e.g., big bump pads) when coupling to the first set of interconnect 822 and/or the second set of interconnects 824. In some implementations, the redistribution interconnects 851-854 are directly coupled to the first set of interconnects 822 and/or the second set of interconnects 824.

[00101] At stage 9, as shown in FIG. 8C, a second dielectric layer 860 and several redistribution interconnects (e.g., redistribution interconnects 861-864) are provided on the first dielectric layer 850 and the redistribution interconnects 851-854. In some implementations, the redistribution interconnects 861-864 is formed on a second redistribution metal layer. In some implementations, the redistribution interconnects 861-864 may include at least one via.

[00102] At stage 10, a third dielectric layer 870 and several redistribution interconnects (e.g., redistribution interconnects 871-874) are provided on the second dielectric layer 860 and the redistribution interconnects 861-864. In some implementations, the redistribution interconnects 871-874 is formed on a third redistribution metal layer. In some implementations, the redistribution interconnects 871-874 may include at least one via.
[00103] At stage 11, at least one under bump metallization (UBM) layer is provided. Specifically, a first under bump metallization (UBM) layer 881, a second UBM layer 882, a third UBM layer 883, and a fourth XIBM layer 884 are provided. The UBM layers are provided on the fourth dielectric layer 880. In some implementations, providing the UBM layer is optional.

[00104] At stage 12, as shown in FIG. 8D, at least one solder ball is provided on the XIBM layer. Specifically, a first solder ball 891 is coupled to the first UBM layer 881, a second solder ball 892 is coupled to the second UBM layer 882, a third solder ball 893 is coupled to the third UBM layer 883, and a fourth solder ball 894 is coupled to the fourth UBM layer 884. Stage 12 illustrates the set of dielectric layers 890. In some implementations, the set of dielectric layers 890 includes the dielectric layers 850, 860, 870 and 880. In some implementations, the solder ball may be coupled to the redistribution interconnects instead of the UBM layer.

[00105] At stage 13, a portion of the integrated device is removed (e.g., polished). As shown at stage 12, at least a portion of the carrier 842 is removed (e.g., entire carrier 842 is removed). In some implementations, at least a portion of the encapsulation material 840 is also removed.

[00106] Having described a sequence for providing / manufacturing an integrated device (e.g., semiconductor device), a method for providing / manufacturing an integrated device (e.g., semiconductor device) will now be described below.

Exemplary Method for Providing / Manufacturing an Integrated Device

[00107] FIG. 9 illustrates an exemplary method for providing an integrated device (e.g., integrated package). In some implementations, the method of FIG. 9 may be used to provide / manufacture the integrated device of FIGS. 2 and/or 5-6, and/or other integrated devices (e.g., die package) described in the present disclose.

[00108] The method provides (at 805) a first carrier (e.g., carrier 800) and interconnects (e.g., traces). In some implementations, the first carrier is a sacrificial carrier. In some implementations, the first carrier is a substrate. Different implementations may use different materials for the first carrier (e.g., silicon substrate, glass substrate, ceramic substrate).

[00109] The method then provides (at 910) at least one integrated device (e.g., die) on the carrier. In some implementations, providing (at 810) at least one integrated device includes providing a first die on the first carrier and providing a second die on
the first carrier. In some implementations, the dies that are provided are wafer level dies. Examples of providing at least one die is shown in FIG. 8A (see e.g., stage 2).

[00110] The method optionally provides (at 815) an underfill and an encapsulation material. In some implementations, the underfill is provided between the dies and the first carrier. In some implementations, the interconnects 802, 804, 822, and 824 are covered by the underfill. In some implementations, the encapsulation material substantially or completely surrounds or encapsulates the dies (e.g., first die 812, the second die 814).

[00111] The method couples (at 920) the integrated device that includes the first carrier and the first and second dies, to a second carrier. In some implementations, the second carrier is a temporary carrier. Different implementations may use different materials for the second carrier. In some implementations, the second carrier is a bonding tape.

[00112] The method further removes (at 925) at least a portion of the integrated device. In some implementations, removing at least a portion of the integrated device includes removing (e.g., polishing, grinding) at least the first carrier, portions of the underfill, potions of the encapsulation layer, and/or the interconnects (e.g., interconnects 802, 804, 822, 824). In some implementations, after removing a portion of the integrated device, at least one metal layer may be provided in a cavity. In some implementations, the metal layer in the cavity may define an interconnect (e.g., high density interconnect between two dies).

[00113] The method further provides (at 930) at least one dielectric layer (e.g., dielectric layers 850, 860, 870, 880). Different implementations may use different materials for the dielectric layers. For example, first and second insulation layers (which are a form of a dielectric layer) may be a Poiybenzoxazole (FbO) layer and/or a polymer layer.

[00114] The method also provides (at 935) several metal redistribution layers. In some implementations, providing several redistribution layers includes providing several redistribution interconnects (e.g., redistribution interconnects 851-854) and/or vias. It should be noted that in some implementations, the method of providing (at 930) at least one dielectric layer, and providing (at 935) the metal redistribution layers may be performed sequentially back and forth. That is, in some implementations, the method may provide a first dielectric layer, a first redistribution layer, a second dielectric layer, a second redistribution layer, and so on and so forth.
The method then optionally provides (at 940) an under bump metallization (UBM) layer. In some implementations, providing (at 940) the UBM layer includes coupling the UBM layer to a metal redistribution layer. In some implementations, the UBM layer is a copper layer. The method further provides (at. 945) a solder bail on the UBM layer.

The method further removes (at 950) at least a portion of the integrated device. In some implementations, removing a portion of the integrated device includes removing (e.g., polishing, grinding) at least a portion of the carrier 842. In some implementations, at least a portion of the encapsulation material 840 is also removed.

Exemplary Sequence for Providing /Manufacturing Redistribution Layers

In some implementations, providing an integrated device that includes redistribution layers includes several processes. FIGS. 10A-10C illustrate an exemplary sequence for providing an integrated device that includes several redistribution layers. In some implementations, the sequence of FIGS. 10A-10C may be used to provide /manufacture the integrated device of FIGS. 2 and/or 5-6, and/or other integrated devices (e.g., dies) described in the present disclose. It should also be noted that the sequence of FIGS. 10A-10C may be used to provide /manufacture integrated devices that also include circuit elements. It should further be noted that the sequence of FIGS. 10A-10C may combine one or more stages in order to simplify and/or clarify the sequence for providing an integrated device that includes redistribution layers. FIGS. 10A-10C a more specific process for providing one or more redistribution layers.

As shown in stage 1 of FIG. 10A, a substrate (e.g., substrate 1001) is provided. In some implementations, the substrate 1001 is a wafer. Different implementations may use different materials for the substrate (e.g., silicon substrate, glass substrate, ceramic substrate).

In addition, at stage 1, several lower level metal layers and dielectric layers (e.g., lower level metal and dielectric layers 1002) are provided on the substrate 1001. Different implementations may provide different number of lower level metal layers and dielectric layers (e.g., M1 metal layer, M2 metal layer, M3 metal layer, M4 metal layer, M5 metal layer, M6 metal layer, M7 metal layer).

In some implementations, circuits, routes and/or interconnects are also provided. However, for the purpose of simplification and clarity, circuits, routes and/or interconnects are not shown in the lower level metal layers and dielectric layers 1002.
Moreover, at stage 1, at least one pad (e.g., pads 1004, 1025, 1029) is provided on the lower level metal layers and dielectric layers 1002. In some implementations, the pad 1004 is coupled to one of the lower level metal layer (e.g., the top lower level metal layer, M7 metal layer). In some implementations, the pad 1004 is an aluminum pad. However, different implementations may use different materials for the pad 1004. Different implementations may use different processes for providing the pad on the lower level metal layers and dielectric layers 1002. For example, in some implementations, a lithography and/or etching process may be use to provide the pad 1004 on the lower level metal layers and dielectric layers 1002.

Additionally, at stage 1, a passivation layer (e.g., passivation layer 1006) is provided on the lower level metal layers and dielectric layers 1002. Different implementations may use different materials for the passivation layer 1006. As shown in stage 4, the passivation layer 1006 is provided on the lower level metal layers and dielectric layers 1002 such that at least a portion of the pad 1004 is exposed.

At stage 2, a first insulation layer (e.g., first insulation layer 1008) is provided on the passivation layer 1006 and the pads 1004, 1025 and 1029. In some implementations, the first insulation layer 1008 is a dielectric layer. Different implementations may use different materials for the first insulation layer 1008. For example, the first insulation layer 1008 may be a Polybenzoxazole (PBO) layer or a polymer layer.

At stage 3, several cavities (e.g., cavity, trench) is provided / created in the first insulation layer 1008. As further shown in stage 3, the cavity 1009 is created over the pad 1004. Similarly, a cavity 1011 is created over the pad 1025, and a cavity 1013 is created over the pad 1029. Different implementations may create the cavities (e.g., cavity 1009) differently. For example, the cavity 1009 may be provided / created by etching the first insulation layer 1008.

At stage 4 of FIG. 10B, a first metal redistribution layer is provided. Specifically, a first metal redistribution layer 1010 is provided over the pad 1004 and the first insulation layer 1008. As shown in stage 4, the first metal redistribution layer 1010 is coupled to the pad 1004. The first metall redistribution layer 1010 also includes a first metal layer 1030 and a second metal layer 1032. That is, in some implementations, the first metal layer 1030 and the second metal layer 1032 is on the same layer as the first metal redistribution layer 1010. In some implementations, the first and second
metal layers 1030 and 1032 are vias. In some implementations, the first metal redistribution layer 1010 is a copper layer.

[00126] At stage 5, several insulation layers and several redistribution layers are provided. Specifically, a second insulation layer 1014 and a third insulation layer 1016 are provided. Moreover, a second metal redistribution layer 1020 is provided. In addition, several metal layers (1040, 1050, 1042, 1052) are provided. In some implementations, the metal layers are part of the redistribution layers. In some implementations, some of the metal layers include vias. For example, metal layers 1042, and 1052 are vias and metal layers 1040 and 1050, are traces in some implementations.

[00127] At stage 6, a cavity 1017 is provided in the insulation layer 1016. The cavity 1017 in the insulation layer 1016 is over a portion of the second metal redistribution layer 1020 (e.g., interconnect).

[00128] At stage 7 of FIG. 10, an under bump metallization (XJBM) layer is provided. Specifically, an under bump metallization (UBM) layer 1070 is provided in the cavity 1017 of the insulation layer 1016. In some implementations, the UBM layer 1070 is a copper layer.

[00129] At stage 8, a solder ball is provided on the UBM layer. Specifically, a solder ball 1080 is coupled to the UBM layer 1070.

Exemplary Electronic Devices

[00130] FIG. 11 illustrates various electronic devices that may be integrated with any of the aforementioned semiconductor device, integrated circuit, die, interposer or package. For example, a mobile telephone 1102, a laptop computer 1104, and a fixed location terminal 1106 may include an integrated circuit (IC) 1100 as described herein. The IC 1100 may be, for example, any of the integrated circuits, dice or packages described herein. The devices 1102, 1104, 1106 illustrated in FIG. 11 are merely exemplary. Other electronic devices may also feature the IC 1100 including, but not limited to, mobile devices, hand-held personal communication systems (PCS) units, portable data units such as personal digital assistants, GPS enabled devices, navigation devices, set top boxes, music players, video players, entertainment units, fixed location data units such as meter reading equipment, communications devices, smartphones, tablet computers or any other device that stores or retrieves data or computer instructions, or any combination thereof.
[00131] One or more of the components, steps, features, and/or functions illustrated in FIGS. 2, 3, 4, 5, 6, 7A-7D, 8A-8D, 9, 1OA-1OC and/or 11 may be rearranged and/or combined into a single component, step, feature or function or embodied in several components, steps, or functions. Additional elements, components, steps, and/or functions may also be added without departing from the disclosure. It should also be noted that FIGS. 2, 3, 4, 5, 6, 7A-7D, 8A-8D, 9, 1OA-1OC and/or 11 and its corresponding description in the present disclosure is not limited to dies and/or ICs. In some implementations, 2, 3, 4, 5, 6, 7A-7D, 8A-8D, 9, 1OA-1OC and/or 11 and its corresponding description may be used to manufacture, create, provide, and/or produce integrated devices. In some an integrated device may include a die package, an integrated circuit (IC), a wafer, a semiconductor device, and/or an interposer.

[00132] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any implementation or aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects of the disclosure. Likewise, the term "aspects" does not require that all aspects of the disclosure include the discussed feature, advantage or mode of operation. The term "coupled" is used herein to refer to the direct or indirect coupling between two objects. For example, if object A physically touches object B, and object B touches object C, then objects A and C may still be considered coupled to one another—even if they do not directly physically touch each other.

[00133] Also, it is noted that the embodiments may be described as a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be re-arranged. A process is terminated when its operations are completed.

[00134] The various features of the disclosure described herein can be implemented in different systems without departing from the disclosure. It should be noted that the foregoing aspects of the disclosure are merely examples and are not to be construed as limiting the disclosure. The description of the aspects of the present disclosure is intended to be illustrative, and not to limit the scope of the claims. As such, the present teachings can be readily applied to other types of apparatuses and many alternatives, modifications, and variations will be apparent to those skilled in the art.
CLAIMS

WHAT I CLAIMED IS:

1. An integrated device comprising:
   a base portion for the integrated device, the base portion comprising;
   a dielectric layer; and
   a set of redistribution metal layers;
   a first die coupled to a first surface of the base portion; and
   an underfill between the first die and the base portion.

2. The integrated device of claim 1, further comprising an encapsulation material that encapsulates the first die.

3. The integrated device of claim 1, further comprising a second die coupled to the first surface of the base portion.

4. The integrated device of claim 3, further comprising a set of interconnects on the base portion, the set of interconnects electrically coupling the first die and the second die.

5. The integrated device of claim 4, wherein the first die comprises a first set of interconnect pillars and the second die comprises a second set of interconnect pillars, the set of interconnects being coupled to the first set of interconnect pillars and the second set of interconnect pillars while bypassing a landing pad.

6. The integrated device of claim 4, wherein the set of interconnects comprises a first pitch that is about 40 microns (µm) or less.

7. The integrated device of claim 1, wherein the first die is a first wafer level die.

8. The integrated device of claim 1, wherein the first die comprises a first set of interconnect pillars, the first die being coupled to the set of redistribution metal layers through the first set of interconnect pillars.
9. The integrated device of claim 8, wherein the first set of interconnect pillars comprises a first pitch that is about 40 microns (µm) or less.

10. The integrated device of claim 1, wherein the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

11. An apparatus comprising:
   a base portion for an integrated device, the base portion comprising:
   a dielectric layer; and
   a redistribution means;
   a first die coupled to a first surface of the base portion; and
   a means for encapsulating an area between the first die and the base portion.

12. The apparatus of claim 11, further comprising an encapsulation means that encapsulates the first die.

13. The apparatus of claim 11, further comprising a second die coupled to the first surface of the base portion.

14. The apparatus of claim 13, further comprising a set of interconnects on the base portion, the set of interconnects electrically coupling the first die and the second die.

15. The apparatus of claim 14, wherein the first die comprises a first set of interconnect pillars and the second die comprises a second set of interconnect pillars, the set of interconnects being coupled to the first set of interconnect pillars and the second set of interconnect pillars while bypassing a landing pad.

16. The apparatus of claim 14, wherein the set of interconnects comprises a first pitch that is about 40 microns (µm) or less.

17. The apparatus of claim 11, wherein the first die is a first wafer level die.
18. The apparatus of claim 11, wherein the first die comprises a first set of interconnect pillars, the first die being coupled to the redistribution means through the first set of interconnect pillars.

19. The apparatus of claim 18, wherein the first set of interconnect pillars comprises a first pitch that is about 40 microns (µm) or less.

20. The apparatus of claim 11, wherein the apparatus is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.

21. A method for providing an integrated device, comprising:
   forming a base portion for the integrated device, wherein forming the base portion comprises:
   forming a dielectric layer; and
   forming a set of redistribution metal layers;
   providing a first die on a first surface of the base portion; and
   forming an underfill between the first die and the base portion.

22. The method of claim 21, farther comprising forming an encapsulation material that encapsulates the first die.

23. The method of claim 21, further comprising providing a second die on the first surface of the base portion.

24. The method of claim 23, further comprising forming a set of interconnects on the base portion, the set of interconnects electrically coupling the first die and the second die.

25. The method of claim 24, wherein the first die comprises a first set of interconnect pillars and the second die comprises a second set of interconnect pillars,
the set of interconnects being coupled to the first set of interconnects pillars and the second set of interconnect pillars while bypassing a landing pad.

26. The method of claim 24, wherein the set of interconnects comprises a first pitch that is about 40 microns ($\mu$m) or less.

27. The method of claim 21, wherein the first die is a first wafer level die.

28. The method of claim 21, wherein the first die comprises a first set of interconnect pillars, the first die being coupled to the set of redistribution metal layers through the first set of interconnect pillars.

29. The method of claim 28, wherein the first set of interconnect pillars comprises a first pitch that is about 40 microns ($\mu$m) or less.

30. The method of claim 21, wherein the integrated device is incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, and/or a laptop computer.
**FIG. 3**

**FIG. 4**
FIG. 7B
FIG. 8A
900 Provide a first carrier and interconnects (e.g., traces)

905 Provide at least one integrated device (e.g., die) in/on the carrier (e.g., provide first and second dies)

910 Provide underfill and/or encapsulation layer (e.g., mold)

915 Couple to a second carrier (e.g., temporary carrier)

920 Remove (e.g., polish) first carrier

925 Provide at least one dielectric layer

930 Provide several metal redistribution layers

935 Provide at least one under bump metallization (UBM) layer (optional)

940 Provide at least one solder ball on UBM layer

945 Remove at least the second carrier

950

FIG. 9
FIG. 10A
FIG. 10C
A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/538
ADD. H01L21/56
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td></td>
<td>paragraphs [0006], [0037], [0056], [0075], [0076]; figures 14,15</td>
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<td></td>
<td>paragraphs [0035], [0055], [0056], [0062]; figures 8,10</td>
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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:
  *A* document defining the general state of the art which is not considered to be of particular relevance
  *E* earlier application or patent but published on or after the international filing date
  *L* document which may throw doubts on priority claim(s) on which is cited to establish the publication date of another citation or other special reason (as specified)
  *O* document referring to an oral disclosure, use, exhibition or other means
  *P* document published prior to the international filing date but later than the priority date claimed

  *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
  *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
  *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
  *A* document member of the same patent family

Date of the actual completion of the international search: 27 May 2015
Date of mailing of the international search report: 21/08/2015

Name and mailing address of the ISA:
European Patent Office, P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer:
Manook, Rhoda
INTERNATIONAL SEARCH REPORT

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. □ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. □ Claims Nos.:
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. □ Claims Nos.:
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. □ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. □ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. □ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☑ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

   1, 2, 7, 10-12, 17, 20-22, 27, 30

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.
<table>
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This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 2, 7, 10-12, 17, 20-22, 27, 30

   The subject matter of common to both independent product claim 1 and independent product claim 11 and independent method claim 21 is not new compared to the teaching of document US 2011/316156 (D1) and cannot therefore serve as a common concept (Rule 13(1) PCT) for these claims 2, 3, 7, 8, 10 and 12, 13, 17, 18, 20 and 22, 23, 27, 28 and 30 which are directly dependent upon these claims. See the attached party al search report for this reason ng.

   Group 1: directed towards the subject matter of claims 1-2, 11-12, 21-22, 7, 17, 27, 10, 20, 30 (c.f. claims 2, 12, 22)

   Re. claims 2 and 22 D1 also discloses an encapsulated material (150; para. 76) that encapsulates the first die (124).

   Re. claims 12 D1 also discloses further comprising an encapsulated material on means (150; para. 76) that encapsulates the first die (124).

   These features are already known from document D1 and its subject matter therefore cannot form special technical features.

   Although the technical features of the dependent claims 7, 17, 27 and 10, 20 and 30 are not the same, they could be searched without any effort and are thus included in the first searched group of claims.

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2. claims: 3-6, 13-16, 23-26

   Group 2: directed towards the subject matter of claims 3-6, 13-16 and 23-26 (c.f. claims 3, 13 and 23)

   Re. claims 3, 13 and 23 the special technical features surpass us to the known claims 1, 11 and 21 are: further comprising a second die coupled to the first surface of the base port on.

   Thus the objective problem of claims 3, 13 and 23 to be solved can be construed as: defining the integrated device for higher density whilst maintaining a thin package.

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3. claims: 8, 9, 18, 19, 28, 29

   Group 3: directed towards the subject matter of claims 8-9, 18-19, 28-29 (c.f. claims 9, 19, 29)

   Re. claims 8, 18 and 28 the technical features are already disclosed by document D1: the first die comprises a first set of interconnect pillars, the first die being coupled to the set of redi stri but on metal layers through the first set of interconnect pillars.

   These features are already known from document D1 and its subject matter of claims 8, 18 and 28 therefore cannot form special technical features.

   Re. claims 9, 19 and 29 the special technical features with
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respect to the known document D1 wherein the first set of
interconnect pillars comprises a first pitch of about 40
microns or less.
Thus the objective problem of claims 9, 19 and 29 to be
solved can be construed as: defining the integrated device
to ensure a large number of electrical interconnects can
connect to an individual die.

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