

Oct. 22, 1946.

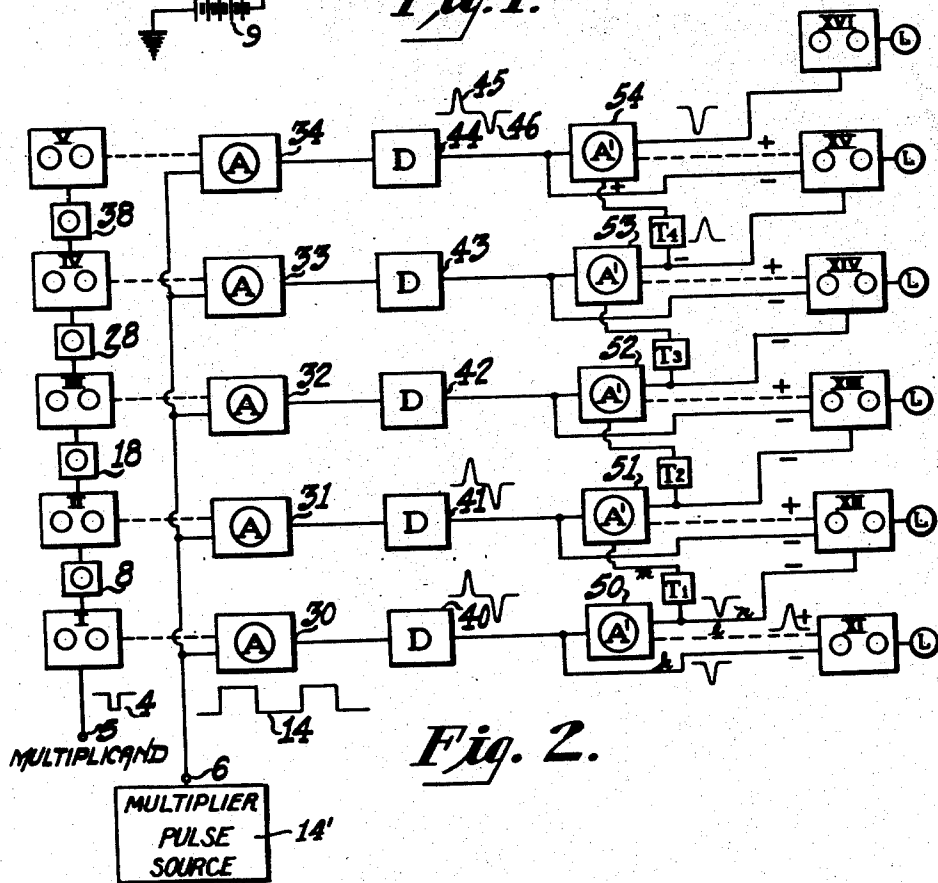
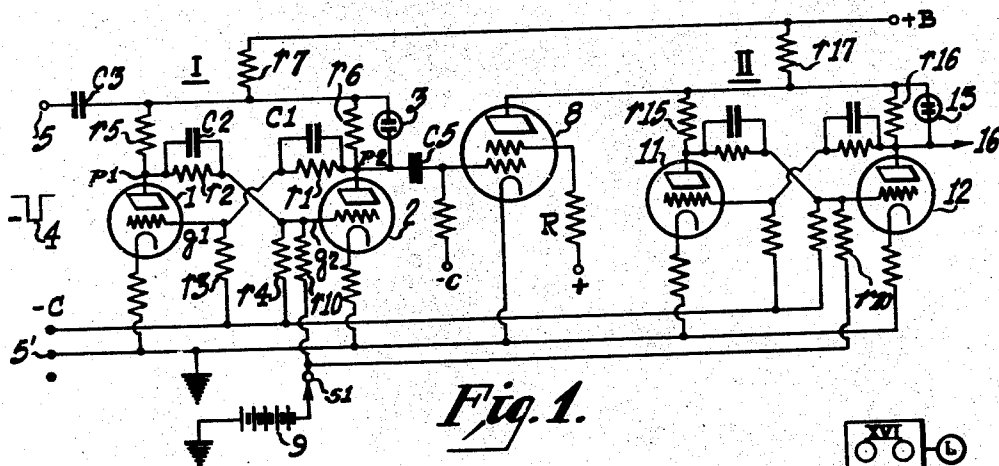
G. A. MORTON ET AL

2,409,689

ELECTRONIC COMPUTING DEVICE

Filed Nov. 2, 1942

2 Sheets-Sheet 1



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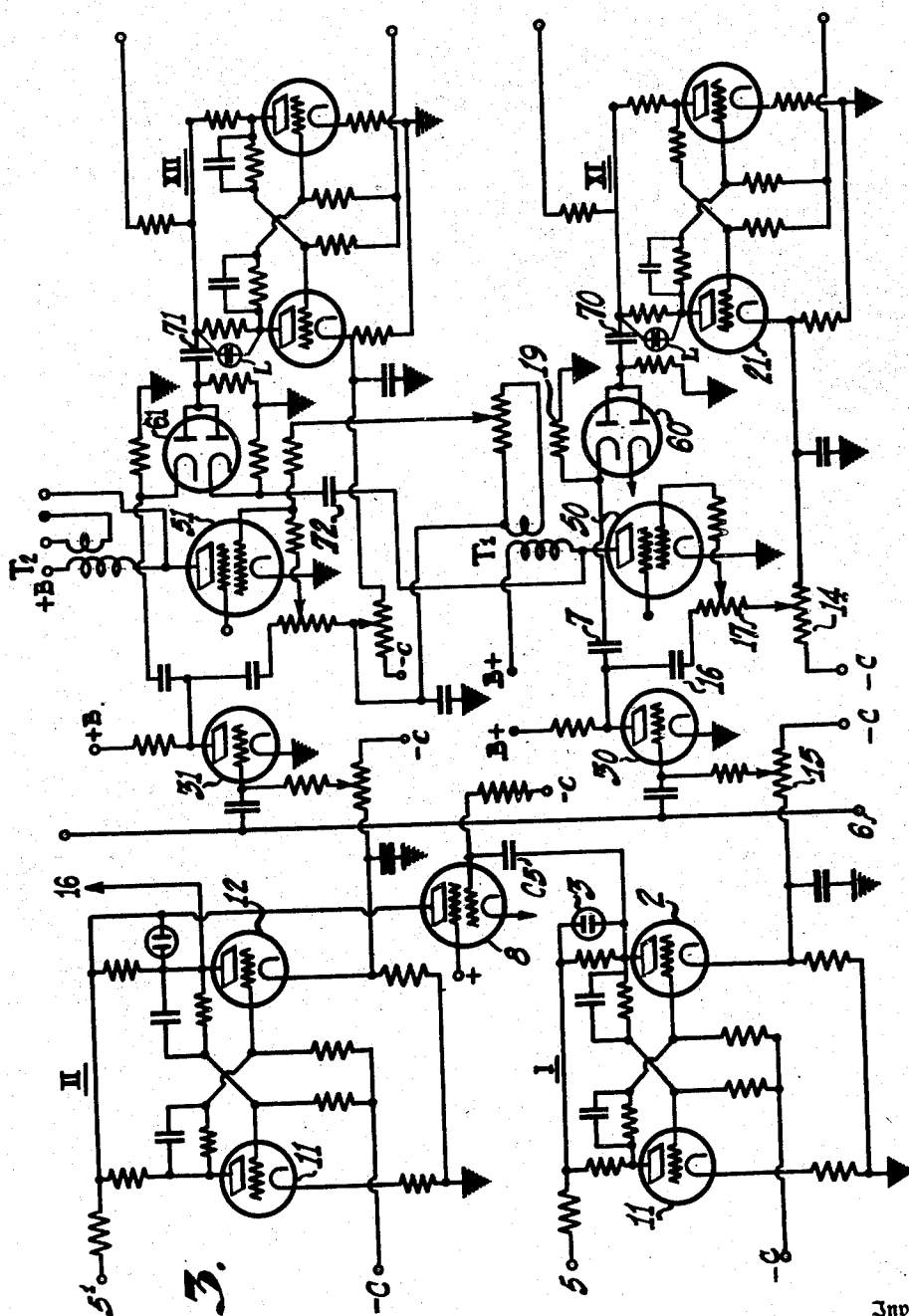
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UNITED STATES PATENT OFFICE

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ELECTRONIC COMPUTING DEVICE

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8 Claims. (Cl. 235—61)

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This invention relates generally to electronic computers and particularly to electronic apparatus for counting voltage pulses and for adding, subtracting, or multiplying quantities represented by groups of such pulses.

The basic circuit utilized in adapting the invention herein to the various circuits to be described in the well known "trigger" circuit of the general type described in "Theory and Application of Vacuum Tubes," by Herbert J. Reich. In one of its simplest forms, this trigger circuit includes two triodes in which the grid of the first triode is coupled to the anode of the second triode through a network comprising a parallel connected resistor and capacitor, and the grid of the second triode is similarly coupled to the anode of the first triode through a similar coupling network. The cathodes of both triodes are grounded, either directly, or through suitable cathode resistors. Grid and anode potentials are applied to the respective electrodes through separate resistors. If desired, a gaseous discharge tube may be connected across one of the anode resistors to indicate circuit operation.

In operation, if a negative voltage is applied to the grid of the first triode, the anode current of the triode will be reduced, and the anode potential will become more positive. Due to the connection through the coupling resistor, the grid potential of the second triode will become more positive, causing an increase in the anode current of the second triode, with a resultant decrease in the second triode anode potential. This decrease in anode potential will, in turn, cause the grid potential of the first triode to become more negative. This action will continue until the anode current of the first triode is cut off. The first triode will remain cut off, and the second triode will remain conducting, until a positive potential is applied to the grid of the first triode or until a negative potential is applied to the grid of the second triode. In either latter instance, the tube operating conditions will be reversed and the first triode will become conducting and the anode current of the second triode will be cut off.

One of the features of the instant invention is the utilization of such trigger circuits in cascade arrangement, whereby a predetermined change in the polarization or activation of one triode of the trigger circuit will generate a pulse to trigger or activate a succeeding trigger circuit in the cascade arrangement. As many trigger circuits as desired may be connected in cascade. The instant invention is an improvement

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of our copending U. S. application, Serial No. 464,293, filed November 2, 1942, which describes a cascade trigger circuit arrangement for counting voltage pulses to derive the binary sum, or difference, of successive series of pulses. The instant invention, however, is adapted to counting voltage pulses and indicating the product of two groups of pulses as a binary number.

The binary system of computation is particularly suited to electronic computers since a complete binary term of a binary number may be expressed in terms of the conducting or cut-off condition of the anode circuit of a conventional vacuum tube. A saving in the number of tubes required for a given number is also possible in a ratio of 3 to 1 over the scale of 10 system. More complete discussions of the binary and similar systems of computation may be found in "Elementary Number Theory" by Uspenski and Heaslet, "Mathematical Excursions" by H. A. Merrill, and "A Mathematician Explains" by M. I. Logston.

In order to operate a counter utilizing the binary system, it is necessary to adapt the conventional trigger circuit described heretofore to effect a reversal in polarization or activation by succeeding applied pulses of a similar nature. The circuits to be described hereinafter are adapted to this purpose by applying in a symmetrical manner negative operating pulses to the anode circuits of the trigger tubes.

Among the objects of the invention are to provide an improved means for counting voltage pulses. Another object of the invention is to provide improved means for utilizing conventional trigger circuits in a novel cascade arrangement for deriving the product of the numbers of pulses in successive series of voltage pulses. Still another object is to provide an improved means for connecting conventional trigger circuits in cascade arrangement to provide a continuous counter. A further object is to provide improved means for clearing the counter after each operation thereof, for conditioning the circuit for counting succeeding applied pulses. Another object is to provide an improved means for deriving the sum of two or more binary numbers which are successively applied to the circuit as groups of potentials. A further object is to provide an improved means for deriving the difference between two binary numbers. Another object is to provide an improved means for deriving the binary product of two series of pulses applied to a thermionic tube trigger circuit. Still another object is to provide an improved means for de-

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ripping the binary product of the number of pulses in succeeding series of voltage pulses applied to one or more groups of cascaded trigger circuits, wherein the multiplicand is applied as a binary number to an electronic counter and is added to itself a number of times which is equal to the multiplier.

The invention will be described by reference to the accompanying drawings of which Fig. 1 is a schematic circuit diagram of a binary counter, Fig. 2 is a block circuit diagram of the invention, and Fig. 3 is a schematic circuit diagram of a preferred embodiment of a typical portion of Fig. 2. Similar reference characters indicate similar elements in the drawings.

Referring to the drawings, Figure 1 comprises a trigger circuit of the type described heretofore. The grid $g1$ of a first triode 1 is connected to the anode $p2$ of a second triode 2 through a network comprising the parallel connected resistor $r1$ and capacitor $c1$. The anode $p1$ of the first triode 1 is connected to the grid $g2$ of the second triode 2 through a second network comprising the parallel connected resistor $r2$ and capacitor $c2$. The cathodes of the first and second triodes 1, 2 are grounded through suitable resistors. A source of negative bias potential is connected to the grid $g1$ of the first tube 1 through a grid resistor $r3$, and to the grid $g2$ of the second triode 2 through a second grid resistor $r4$. Anode potential is applied to the anode $p1$ of the first tube 1 through an anode coupling resistor $r5$, and to the anode $p2$ of the second tube 2 through a second anode coupling resistor $r6$. A gaseous indicator tube 3, which may be a conventional neon tube, is connected across the second anode resistor $r6$ to indicate when the current exceeds a predetermined value, which depends upon the anode current flowing in the second tube 2. A choking resistor $r7$ is connected in series with the positive anode power supply lead to the common terminals of the anode resistors $r5$ and $r6$. Negative input control pulses 4 are applied to the input terminals 5, 5', which are connected between ground and through an input coupling capacitor $c3$, to the common terminal of the anode resistors $r5$ and $r6$.

In operation, if it is assumed that the first tube 1 initially is drawing anode current, the second tube 2 will be biased off. A negative pulse 4, applied to the input terminals 5, will appear on the anode $p2$ of the tube 2 and on the grid $g1$ of the first tube 1 which will in turn reduce the anode current in the first tube 1. This, in turn, will make the potential on the anode $p1$ of the first tube 1 more positive, and degenerate simultaneously any of the original negative pulse applied at $p1$. A positive pulse will be applied to the grid $g2$ of the tube 2 causing the tube 2 to become conducting. This effect will increase and continue, because of the difference in the potential charges on the capacitors $c1$ and $c2$, until the first tube 1 is cut off, and the second tube 2 becomes completely conducting. A subsequent negative pulse applied to the input terminals 5 will cause the stable conditions of the trigger tubes 1, 2 to be reversed since the circuit is completely symmetrical.

The indicator tube 3 will be illuminated when the second tube 2 is conducting, since only under this condition is there an appreciable voltage drop across the anode coupling resistor $r6$. If it is assumed that the conducting condition of the first tube $p1$ represents zero, and the conducting condition of the second tube 2 represents 1, the

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result is a binary counter in which zero is indicated on the indicator tube 3 when the tube is extinguished, and 1 is indicated when the tube is illuminated. The second pulse applied to the input terminals 5 will cut off the second trigger tube 2 and cause the first tube 1 to again become conducting. In order to indicate that two pulses have occurred instead of none, it is essential that a carryover system, corresponding to the carryover in arithmetic, be employed which will provide a second indication representative of the second term of the binary total.

It will be seen that the circuit of Fig. 1 employs two identical trigger circuits I and II connected in a novel cascade arrangement whereby two terms of a binary number may be indicated. As illustrated, the circuit comprises two trigger circuits of the general type described heretofore, but it should be understood that as many such circuits as required for the multiplicand may be connected in cascade arrangement in a similar manner. The first and second trigger tubes 1 and 2, and the first indicator tube 3 correspond to the first term of the binary number. The third and fourth trigger tubes 11 and 12 and the second indicator tube 13 correspond to the second term of the binary number. The connection 16 from the anode $p12$ is provided for coupling to succeeding trigger circuits of similar types. The grid of a transfer tube 8 is connected to the anode $p2$ of the second trigger tube 2 through a second coupling capacitor $c5$. The anode of the transfer tube 8 is connected to the common terminal of the anode resistors $r15$, $r16$ and $r17$ of the second trigger circuit comprising the tubes 11 and 12. The grids of the second and fourth trigger tubes 2 and 12 are connected respectively through suitable choking resistors $r10$ and $r20$ to a fixed contact of a reset switch $s1$. The movable contact of the reset switch $s1$ is connected to a suitable negative terminal of a potential source 9 to provide cut-off grid bias for the tubes 2 and 12 when the switch is closed. The positive terminal of the bias potential source is grounded.

In operation, if the reset switch $s1$ is open, the first trigger tube 1 is assumed to be conducting and the second trigger tube 2 to be cut off, the first negative pulse applied to the input terminals 5 will reverse the stable conditions of the trigger tubes causing the second tube 2 to become conducting and illuminating the first indicator tube 3. The second pulse applied to the input terminals 5 will again reverse the stable conditions of the tubes 1 and 2 and the indicator tube 3 will be extinguished. When the second trigger tube 2 becomes non-conducting upon the application of the second input pulse to the input terminals 5, the potential upon the anode $p2$ thereof becomes more positive which, in turn, applies a positive pulse to the grid of the second transfer tube 8, which is biased normally to anode current cut off condition. Due to normal phase inversion in the transfer tube 8, a negative pulse will be derived from the anode thereof and applied to the second trigger circuit comprising the third and fourth tubes 11 and 12, causing the stable condition of the second trigger circuit II to be reversed. It will therefore be understood that the first pulse applied to the circuit will cause the first indicator tube 3 to be illuminated. The second pulse applied to the circuit will cause the first indicator tube 3 to be extinguished, and cause the second indicator tube 13 to be illuminated. A third pulse applied to the circuit will

cause the first indicator tube 3 to be illuminated in addition to the second indicator tube 13.

Figure 2 comprises a block diagram of an electronic multiplying system wherein a multiplicand is set up as a binary number on a series of cascaded trigger circuits I, II, III, IV, and V of the general type described heretofore. The binary multiplicand is then transferred to a second binary counter, including a second series of cascaded trigger circuits XI, XII, XIII, XIV, XV, and XVI, upon which the binary product is derived. The circuits to be described hereinafter accomplish both the direct transfer of the multiplicand to the product counter and the carryover operation required as each element product counter changes from one to zero in the binary system. Each of the trigger circuits I, II, III, IV, V of the multiplicand counter is connected to a corresponding transfer amplifier 30, 31, 32, 33, 34, respectively, in such a manner that when the counter trigger circuit is in the binary zero condition, the amplifier tube is inoperative, and when the counter is in the binary 1 condition, the corresponding amplifier is biased to the anode current cutoff condition. Negative pulses 4 are applied to the multiplicand binary counter to establish the multiplicand as a binary quantity.

Pulses 14, the number of which correspond to the value of the multiplier, are derived from a multiplier pulse source 14' and applied to the terminal 6, which is connected to the respective grid circuits of the transfer amplifiers 31, 32, 33 and 34. The pulses 14 may be derived in any known manner, such as a telephone dial or other sequential contactor which is connected to interrupt a source of potential. The multiplier pulses 14 will therefore be transmitted by only the transfer amplifiers which are connected to the corresponding multiplicand trigger circuits which are in the binary 1 condition. The pulses transmitted by the respective transfer amplifiers are next applied to separate differentiating circuits 40, 41, 42, 43 and 44, respectively, from which are derived a positive pulse 45 and a negative pulse 46, separated by the width of the multiplier pulses 14. These pulses are next applied directly to the product binary counter comprising the trigger circuits XI, XII, XIII, XIV, and XV, respectively. The positive pulse 45 is utilized to accomplish the carryover operation between successive product counter trigger circuits whenever it is applied to one of the trigger circuits which is in the binary 1 condition. The negative pulse 46 is utilized to trigger the corresponding product binary trigger circuit to the next binary number.

Both negative and positive pulses 46 and 45, respectively, are applied to the input of a second group of transfer amplifiers 50, 51, 52, 53, and 54, respectively, which are connected to the corresponding product trigger circuits. The second transfer amplifiers are so connected that they are inoperative when the corresponding product trigger circuit is in the binary zero condition, and are just cut off when the corresponding trigger circuit is in the binary 1 condition. The outputs of the second transfer amplifiers are connected by the leads *n* to trigger the next succeeding trigger circuits of the product counter. It will therefore be seen that if the first product trigger circuit XI is in the binary 1 condition, the transfer amplifier 50 will be just cut off. The positive pulse 45 applied to the input of the transfer amplifier will, therefore, provide a negative pulse in the lead *n* to the second product

trigger circuit XII. The negative pulse 46, which immediately follows the positive pulse 45, will then trigger the first product trigger circuit XI to the binary zero condition by means of the directly transmitted pulse over the connection *k*.

A condition may arise, for example, where successive carryover pulses are applied to successive circuits in which no positive or negative pulses 45, 46 exist due to the fact that the corresponding term in the multiplicand is binary zero, and the corresponding product trigger circuit is initially also in the binary zero condition. The first pulse on the line *n*, connecting, for example, the transfer amplifier 50 to the trigger circuit XII of the product counter will change the trigger circuit XII from the binary zero to the binary 1 condition, which will activate the corresponding transfer amplifier 51. A succeeding, or a coinciding, carryover pulse on the line *n* is applied to a transformer T1 to apply a second positive pulse to the transfer amplifier 51 over the line *m*. The coincidence of the positive pulse through the transformer T1 and the control voltage from the second trigger circuit XII will therefore make the second transfer amplifier 51 conducting, and provide a negative pulse in its anode circuit which will be applied to trigger the next succeeding product trigger circuit XIII. Likewise, the coincidence of a pulse on the line *n* with a pulse on the line from the corresponding differentiating circuit, will provide a carryover pulse to the next succeeding product trigger circuit, even though the transfer amplifier is initially inactive.

As many trigger circuits as desired may be utilized in the multiplicand counter. As explained heretofore in Figure 1, the successive trigger circuits are connected together by transfer amplifiers 8, 18, 28 and 38, respectively, for accomplishing the carryover operation incident to setting up the multiplicand. The number of trigger circuits required in the product counter will be one more than the sum of the number of binary terms in the multiplicand and multiplier, respectively. Indicator lamps L may be connected in the anode circuits of the individual trigger circuits of the product counter in the same manner as described heretofore in Figure 1 for the individual trigger circuits of the multiplicand counter. Likewise, the anode circuits of the product counter may be connected to apply the binary product directly to other utilization circuits. The product trigger circuits, with their associated carryover transfer amplifiers and coupling circuits, comprise a product accumulator.

Figure 3 indicates the apparatus required for two binary terms in the multiplicand. The multiplicand counter comprises the trigger circuits I and II and the carryover transfer tube 8. The multiplicand is applied to the counter through one or both of the input terminals 5, 5', depending upon the nature of the multiplicand source. For example, if the multiplicand is in the form of a plurality of pulses corresponding in number to the numerical value thereof, the pulses are all applied to the input terminal 5, and accumulated on the counter as a binary number. If the multiplicand is already in the form of a plurality of separate voltages corresponding in magnitude and arrangement with the binary value thereof, the separate voltages are applied to the separate corresponding input terminals 5, 5', etc. to transfer the binary multiplicand directly to the corresponding multiplicand counter elements. The product counter comprises the trigger circuits

XI, XII which have a different type of carryover transfer tube 50, the circuit of which will be described hereinafter. A second product carryover transfer tube 51 is shown for the application of carryover pulses to the next succeeding product trigger circuit, not shown.

The grid of the transfer tube 30 is connected to the input terminal 6 for the multiplier pulses and through a suitable resistor network which includes a voltage divider 15 to the cathode of the second tube 2 of the first multiplicand trigger circuit I. The anode of the transfer tube 30 is connected through a differentiating circuit comprising the capacitor 16 and the potentiometer 17 to the grid of the product carryover tube 50. The anode of the transfer tube 30 is similarly connected through a second differentiating circuit comprising the capacitor 7 and the resistor 18 to the cathode of a diode rectifier 60. The anode of the diode rectifier tube 60 is connected through a coupling capacitor 70 to the common terminal of the anode circuits of the tubes of the product trigger circuit XI. A control potential is derived from the cathode of the first trigger tube 21 of the product trigger circuit XI, and applied to the control electrode of the carryover transfer tube 50 through voltage dividers 17 and 14, whereby the normally high negative bias applied to the grid of the tube 50 is reduced to approximately cut-off when the product trigger circuit XI is in the binary 1 condition.

The second multiplicand trigger circuit II is similarly connected through a transfer tube 31 to a carryover transfer tube 51 and a diode 61, and then to the second product trigger circuit XII. In order to accomplish the carryover operation in the product counter, a connection is made, through the coupling capacitor 72, between the second cathode of the second diode rectifier 61, and the anode of the first carryover transfer tube 50. The primary winding of the transformer T1 is connected in series with the anode circuit of the first carryover transfer tube 50. The secondary winding of the transformer T1 is connected in any suitable manner to apply a positive pulse to the control electrode of the second carryover transfer tube 51 when coincidental carryover pulses occur. The functions of the diodes are to prevent reaction on preceding trigger circuits due to pulses in subsequent binary term trigger circuits.

All counters may be cleared after each multiplying operation is completed by applying a high negative bias simultaneously to all binary 1 tubes in the manner which is described in referring to Fig. 1.

The circuit may also be utilized for deriving directly the sum of two binary numbers. The first number is applied as a group of potentials representative of a binary number to the multiplicand counter. A single multiplying pulse is then applied to transfer the number to the product or final counter. The multiplicand counter is then cleared. The second number is then applied to the multiplicand counter, and a second multiplying pulse is applied to transfer it to the final counter. The two numbers are then added directly in the final counter. If the multiplicand counter is again cleared, the process may be repeated, and the sum of any desired number of binary numbers obtained. By modifying the carryover circuit in accordance with the disclosure in the copending application, referred to heretofore, the difference of two binary

numbers may also be obtained in a similar manner.

Thus the invention described comprises an electronic multiplying device in which the multiplicand is applied to a cascaded binary counter and transferred to a second or product binary counter, in which the first binary indications are multiplied a number of times corresponding to the value of the multiplier. Provision has been made in both counters to accomplish binary carryover operations where required, and to segregate the carryover operation from the direct application of the multiplicand to the product counter.

We claim as our invention:

1. A binary multiplying device including a plurality of cascaded trigger circuits, means for polarizing said trigger circuits to represent a binary multiplicand, a source of pulses the number of which is representative of a multiplier, a plurality of blocking amplifiers, means responsive to predetermined polarization of said trigger circuits for unblocking predetermined ones of said amplifiers, means for applying said pulses to all of said amplifiers, means for differentiating the pulses derived from said unblocked amplifiers, a plurality of cascaded second trigger circuits, a plurality of transfer blocking amplifiers, means responsive to the polarization of each of said second trigger circuits for unblocking selectively a different one of said transfer amplifiers, means for applying said differentiated pulses to vary the polarization of said second trigger circuits to transfer said multiplicand thereto for each of said multiplier pulses, and means for applying said differentiated pulses to trigger said second trigger circuits in response to said selective unblocking of said transfer amplifiers for providing carryover binary numbers.

2. A binary multiplying device for two quantities including a first binary counter circuit having a plurality of trigger circuits, means for applying one of said quantities to said counter as a multiplicand, a second binary counter circuit having a plurality of trigger circuits, a plurality of blocking amplifiers, means interposing one of said amplifiers between corresponding trigger circuits of said first and said second counters, means including said first counter for unblocking said amplifiers for transferring said multiplicand to said second counter, means for applying pulses to said transferring means for repeating said transfer a number of times corresponding to said other quantity as a multiplier, and means for deriving from said second counter voltages characteristic of the binary sum of said repeated multiplicands.

3. A binary multiplying device for two quantities including a first binary counter circuit having a plurality of trigger circuits, means for applying one of said quantities to said counter as a multiplicand, a second binary counter circuit having a plurality of trigger circuits, a plurality of blocking amplifiers, means interposing one of said amplifiers between corresponding trigger circuits of said first and said second counters, means including said first counter for unblocking said amplifiers for transferring said multiplicand to said second counter, means for applying pulses to said transferring means for repeating said transfer a number of times corresponding to said other quantity as a multiplier, a plurality of transfer amplifiers, means interposing one of said transfer amplifiers between successive trigger circuits of said second counter and between said second

counter and said blocking amplifiers, means including said transfer amplifiers responsive to predetermined polarization of each of said trigger circuits of said second counter for changing the polarization of succeeding trigger circuits of said second counter, and means for deriving from said second counter voltages characteristic of the binary sum of said repeated multiplicands.

4. An electronic computer including a group of electronic tubes connected in pairs to form trigger circuits, means for applying to said circuits different polarizing potentials corresponding to a number, a second group of electronic tubes connected in pairs to form trigger circuits, means connecting said first and said second groups for deriving output potentials in response to said applied potentials, and means for applying pulses to said connecting means for deriving additional output potentials a number of times corresponding to a second number to derive on said second group voltages characteristic of the product of said first and second numbers.

5. An electronic computer including a group of electronic tubes, means for applying to said tubes potentials corresponding to a number to vary the current conditions in said tubes, a second group of electronic tubes, means connecting said first and said second groups for deriving output currents in response to said applied potentials, a number of times corresponding to a second number to derive on said second group the product of said numbers in terms of the current conditions in said tubes of said second group.

6. The combination of first and second groups of electron discharge units, means for establishing in said first group potentials representative of one number, means for applying pulses representative of another number, means for trans-

mitting said potentials once for each of said pulses, means for differentiating said transmitted potentials to derive positive and negative half cycles from each of said potentials, and means for transmitting said negative half cycles to said second group.

7. The combination of first and second groups of electron discharge units, means for establishing in said first group potentials representative of one number, means for applying pulses representative of another number, means for transmitting said potentials once for each of said pulses, means for differentiating said transmitted potentials to derive positive and negative half cycles from each of said potentials, means for transmitting said negative half cycles to said second group, and means for transmitting potentials dependent on said positive half cycles to said second group when the units of said second group are in a predetermined condition.

8. The combination of first and second groups of electron discharge units, means for establishing in said first group potentials representative of one number, means for applying pulses representative of another number, means for transmitting said potentials once for each of said pulses, means for differentiating said transmitted potentials to derive positive and negative half cycles from each of said potentials, means for transmitting said negative half cycles to said second group, and amplifying means controlled by the units of said second group so as to transmit potentials dependent on said positive half cycles to the units of said second group when the units of said second group are in a predetermined condition.

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