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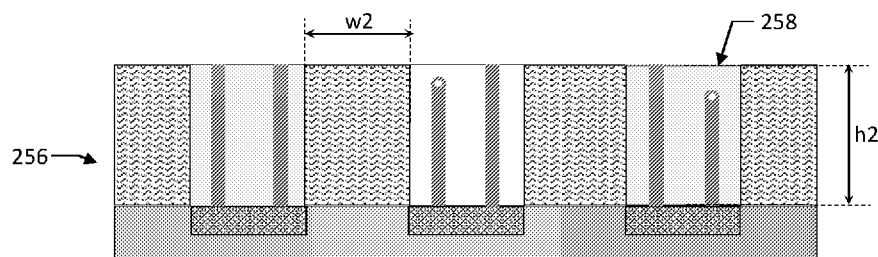


FIG. 18

(57) Abstract: Disclosed herein are methods for manufacturing devices using nanotubes, such as e.g. carbon nanotubes or boron nitride nanotubes, as a guide for selective deposition of materials. For example, in some embodiments, the methods include growing nanotubes on one or more areas on a surface of a substrate which are referred to herein as "nanotube growth areas," followed by depositing one or more materials over or around the nanotubes and then removing either one or more of the deposited material, or the nanotubes. Assemblies and devices manufactured using such methods are disclosed as well. Such assemblies and devices may advantageously be used in semiconductor ICs.



USING NANOTUBES AS A GUIDE FOR SELECTIVE DEPOSITION IN MANUFACTURING INTEGRATED CIRCUIT COMPONENTS

Background

[0001] For the past several decades, the scaling of features in integrated circuits (ICs) has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor IC chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. Since products that implement IC chips are used in a variety of devices including automobiles, computers, appliances, mobile phones and consumer electronics, increasing capacity of the chips is always desirable.

[0002] The drive for the ever-increasing capacity, however, is not without issue. The desire to make smaller IC chips continuously places demands on the methods and materials used to manufacture these devices.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements (e.g. the same, similar, or analogous elements) and, therefore, discussions of these elements provided with respect to one of the drawings are applicable to other drawings and, in the interests of brevity, are not repeated for each of the drawings separately. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGS. 1A-1C are flow diagrams of example methods for manufacturing a device using sparsely grown nanotubes as a guide for selective deposition, in accordance with various embodiments.

[0005] FIGS. 2-25 are cross-sections illustrating various example stages in the manufacture of a device using the methods of FIGS. 1A-1C, in accordance with various embodiments.

[0006] FIGS. 26A-26C are flow diagrams of example methods for manufacturing a device using densely grown nanotubes as a guide for selective deposition, in accordance with various embodiments.

[0007] FIGS. 27-36 are cross-sections illustrating various example stages in the manufacture of a device using the methods of FIGS. 26A-26C, in accordance with various embodiments.

[0008] FIGS. 37A-37B are flow diagrams of example methods for manufacturing a device using nanotubes grown inside one or more openings, in accordance with various embodiments.

[0009] FIGS. 38-44 are cross-sections illustrating various example stages in the manufacture of a device using the methods of FIGS. 37A-37B, in accordance with various embodiments.

[0010] FIGS. 45A and 45B are top views of a wafer and dies that include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein.

[0011] FIG. 46 is a cross-sectional side view of an integrated circuit (IC) device that may include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein.

[0012] FIG. 47 is a cross-sectional side view of an IC device assembly that may include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein.

[0013] FIG. 48 is a block diagram of an example computing device that may include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein.

Detailed Description

[0014] Disclosed herein are methods for manufacturing devices using nanotubes, such as e.g. carbon nanotubes or boron nitride nanotubes, as a guide for selective deposition of materials. For example, in some embodiments, the methods include growing nanotubes on one or more areas on a surface of a substrate which are referred to herein as “nanotube growth areas,” followed by depositing one or more materials over or around the nanotubes and then removing either one or more of the deposited material, or the nanotubes. Assemblies and devices manufactured using such methods are disclosed as well. Such assemblies and devices may advantageously be used in semiconductor ICs.

[0015] Performance of an IC may depend on the number of factors. For example, one factor is how accurately the manufactured features represent those theoretically designed. Challenges often arise in manufacturing features with relatively high aspect ratios (ARs). For example, integration of advanced backend interconnects of IC chips requires materials with unique compositions forming high aspect ratio structures. However, existing selective deposition techniques are limited by AR. As a result, multiple deposition steps are usually required, which introduces defects into the structures and causes the fabrication process to be less amenable to large-scale manufacturing. In addition, filling high AR openings with materials having unique etching properties without creating voids or other defects also continues to be a challenge.

[0016] The methods and devices disclosed herein may improve on one or more of these challenges by using nanotubes as a guide for selecting deposition of other materials. Inventors of the present

disclosure realized that, because nanotubes only grow on certain types of surfaces, namely, they can be used as a guide for where other materials are deposited, thus allowing selective deposition of materials with unique composition in a manner that provides advantages over existing selective deposition techniques. One advantage of the disclosed techniques is that relatively high AR structures may be formed, e.g. structures having an AR of at least 3, e.g. an AR of 10 or even greater, where, as used herein, the term “aspect ratio” refers to a ratio between a height of a structure a depth of an opening to a width of a structure or an opening. Another advantage is that the disclosed techniques may reduce edge placement errors (EPEs), where an EPE commonly refers to a measure of the difference between where the edge of a pattern ends up and where the edge of that pattern was supposed to be, and is closely related to an overlay error, which refers to an offset between the centerlines of two features overlaid over one another. Overall, the techniques disclosed herein may enable manufacturing devices having improved performance and using a wider array of materials, than realizable using conventional approaches.

[0017] The devices and assemblies described herein may be implemented in one or more components associated with an IC or/and between various such components. In various embodiments, components associated with an IC include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an IC may include those that are mounted on IC or those connected to an IC. The IC may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the IC. The IC may be employed as part of a chipset for executing one or more related functions in a computer.

[0018] The devices and assemblies described herein could be a part of a semiconductor device or an IC package, e.g. a part of an interconnect, e.g. a backend interconnect, used for providing electrical conductivity in a semiconductor device or an IC package. As used herein, the term “backend interconnect” is used to describe a region of an IC chip containing wiring between components associated with an IC, e.g. transistors, and other elements, while the term “frontend interconnect” is used to describe a region of an IC chip containing the rest of the wiring.

Nanostructures described herein may be used in any devices or assemblies where one electrically conductive element of the wiring needs to be separated from another electrically conductive element, which could be done both in backend and frontend interconnects. Such devices or assemblies would typically provide an electronic component, such as e.g. a transistor, a die, a sensor, a processing device, or a memory device, and an interconnect for providing electrical connectivity to the component. The interconnect includes a plurality of conductive regions, e.g. trenches and vias

filled with electrically conductive materials as known in the art. Another term commonly used in the art for a plurality of trenches and vias filled with electrically conductive materials is a "metallization stack." The devices and assemblies having portions made of dielectric materials as described herein could be used to electrically isolate at least some of the conductive regions from one another.

[0019] For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details or/and that the present disclosure may be practiced with only some of the described aspects. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0020] Further, references are made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0021] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0022] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges.

[0023] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. The terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. Unless otherwise specified, the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of

like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0024] In the following detailed description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. For example, as used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide (i.e. a material having a dielectric constant higher than 3.9). The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 20% of a target value based on the context of a particular value as described herein or as known in the art.

[0025] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0026] In various embodiments, the interconnects as described herein may be used to connect various components associated with an integrated circuit. Components include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an integrated circuit may include those that are mounted on an integrated circuit or those connected to an integrated circuit. The integrated circuit may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a computer.

[0027] In the embodiments where at least some of the components associated with an integrated circuit are transistors, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as

double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors.

[0028] Each MOS transistor includes a gate stack formed of at least two layers, a gate interconnect support layer and a gate electrode layer. The gate interconnect support layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate interconnect support layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate interconnect support layer to improve its quality when a high-k material is used.

[0029] The gate electrode layer is formed on the gate interconnect support layer and may include at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may include a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0030] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0031] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may include a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is

substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may include a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may include one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0032] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0033] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0034] One or more interlayer dielectrics (ILDs) may be deposited over the MOS transistors. In general, an interlayer dielectric (ILD) or inter metal dielectric (IMD) refers to an insulating material used between metal conductors and devices (such as transistors) in integrated circuit devices. ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide, carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and

organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0035] FIGS. 1A-1C are flow diagrams of example methods 100A-100C for manufacturing a device using sparsely grown nanotubes as a guide for selective deposition, in accordance with various embodiments. Although the operations of the methods 100A-100C are illustrated once each and in a particular order, the operations may be performed in any suitable order and repeated as desired, unless described otherwise. For example, one or more operations may be performed in parallel to manufacture multiple patterns of interconnects substantially simultaneously. In addition, manufacturing methods 100A-100C may include other operations, not specifically shown in FIGS. 1A-1C, such as e.g. various cleaning operations as known in the art.

[0036] Accompanying FIGS. 1A-1C are FIGS. 2-25, which illustrate various example stages in the manufacture of a device using the methods of FIGS. 1A-1C, in accordance with various embodiments. Each of FIGS. 2-25 illustrates a cross-sectional view of an assembly provided at, or resulting from, a certain operation of the methods shown in FIGS. 1A-1C. A legend provided within a dashed box at the bottom of each sheet of drawings with FIGS. 2-25 illustrates patterns used to indicate different elements shown in the drawings, so that the drawings are not cluttered by many reference numerals.

[0037] Referring to the method 100A shown in FIG. 1A, at 102, a substrate with one or more nanotube growth areas is provided. In general, any of the substrates as described herein may be used as a substrate provided at 102, as long as it further includes one or more nanotube growth areas, where, as used herein, the term “nanotube growth areas” refer to areas, on the surface of a substrate, which allow, or enable, growth of the nanotubes. As previously described herein, nanotubes only grow on certain types of surfaces. For example, nanotubes grow on some metal surfaces. At the same time, there are surfaces which reliably prevent growth of nanotubes, such as e.g. certain metal or metal nitride surfaces. This unique nature of nanotubes is exploited herein in having the nanotubes guide deposition of other materials.

[0038] In some embodiments, the upper surface of the substrate may already include areas of one or more metals which allow nanotube growth. Such metals include e.g. iron, cobalt, nickel, gold, silver, platinum and/or palladium. For example, the substrate may be a dielectric substrate that include one or more metal elements formed of such metals, e.g. for use as interconnects, which extend to the upper surface of the substrate. FIG. 2 illustrates an assembly 214 as an example of such a substrate with metal elements. As shown in FIG. 2, the assembly 214 includes a dielectric material 202 in which metal elements 204 are provided. The metal elements 204 may e.g. be provided as a grating (i.e. a collection of parallel lines), with a pitch (i.e. a center-to-center distance

between a pair of two adjacent lines) varying e.g. between 10 and 100 nanometers (nm), including all values and ranges therein. In other embodiments, any other patterns of metal elements 204 may be used as well. The dielectric material 202 may include any suitable dielectric material or a combination of materials, such as, but not limited to, one or more of the materials conventionally used in semiconductor manufacturing as an ILD described above, e.g. silicon dioxide, carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass.

[0039] It should be noted that FIG. 2 and some of the subsequent FIGS. illustrating cross-sectional views only show the upper portion of substrates. In various embodiments, the substrates shown in such FIGS. may include additional layers below the views shown in the FIGS., such as e.g. layers having other features (e.g. additional metallization layers) or a carrier substrate commonly used to provide mechanical support during manufacture (e.g., a metal sheet, a dielectric material, or a reinforced dielectric material).

[0040] In other embodiments, before beginning the nanotube growth, the substrate may undergo special processing in order to ensure that some areas on the surface of the substrate allow the growth, i.e. in order to create the one or more nanotube growth areas as described herein. In general, such special processing of the surface may include treating the surface of the substrate, either the metal portions 204 or the dielectric portions 202, with a catalyst in order to promote nanotube growth on certain areas, thus creating one or more nanotube growth areas. Various embodiments of such processing are described in greater details below, with reference to FIGS. 3-13.

[0041] FIGS. 3-13 illustrate stages of processing a substrate having metal portions and dielectric portions as illustrated with the assembly 214 shown in FIG. 2 because such an assembly is typical for semiconductor manufacturing where, e.g. high AR structures need to be provided over previous patterns, e.g. over previous patterns of the metal portions 204 (i.e. FIGS. 3-13 illustrate subsequent manufacturing stages of the substrate 214 of FIG. 2). Therefore, FIGS. 3-13 refer to elements shown in FIG. 2 and described above. However, in general, descriptions provided for these figures are applicable to any other scenarios where nanotube growth areas need to be created over a substrate, all of which being within the scope of the present disclosure.

[0042] In some embodiments, nanotube growth areas may be formed by depositing a metal catalyst, which may include one or more metal catalysts, on either the metal portions 204 or on the dielectric portions 202 of the substrate of FIG. 2.

[0043] FIG. 3 illustrates an assembly 216 showing the result of depositing a metal catalyst 206 on the metal portions 204 of the substrate of FIG. 2. As shown in FIG. 3, the dielectric portions 202 are not covered with the catalyst 206. In various embodiments, the metal catalyst 206 may be provided as a layer having a thickness substantially between 1 and 5 nanometers. When the nanotubes to be grown are carbon nanotubes (CNTs), the metal catalyst 206 may include one or more metals or metal alloys which can form carbides and supersaturate themselves with carbon when exposed to the carbon feedstock gas, such as, but not limited to, iron, nickel, manganese, or cobalt, and their alloys. When such metal catalyst is provided over the metal portions 204 as shown in FIG. 3, metal catalysts which do not interdiffuse with the metal portions 204 and become inactive should be selected, such as e.g. iron, nickel, or cobalt, and their alloys, described above. When the nanotubes to be grown are boron nitride nanotubes (BNNTs), the metal catalyst 206 may e.g. include iron, magnesium oxide, or nickel. Depositing such metal catalysts on the metal portions 204 may be particularly useful when the metal portions 204 include metals or metal nitrides which are not able to support nanotube growth. Some examples of metals which are not able to support nanotube growth include copper and ruthenium. The metal catalyst 206 may be deposited using electroless deposition, selective atomic layer deposition (ALD), or selective chemical vapor deposition (CVD), as known in the art.

[0044] Depositing the metal catalyst 206 on the metal portions 204 would result in nanotubes later growing on those portions (i.e. the metal portions 204 become the nanotube growth areas). On the other hand, growth of the nanotubes may be carried out on the dielectric portions 202 of FIG. 2 by depositing the metal catalyst 206 on those portions, as shown with an assembly 218 of FIG. 4, showing the result of depositing the metal catalyst 206 as described above on the dielectric portions 202 of the substrate of FIG. 2.

[0045] While FIGS. 3 and 4 illustrate selective deposition of the metal catalyst 206 on certain portions of the substrate while not depositing the catalyst on other portions, other embodiments may include depositing a continuing layer of the metal catalyst 206 as described above over the substrate of FIG. 2, as illustrated with an assembly 220 shown in FIG. 5. In such embodiments, a metal catalyst that would interdiffuse with the metal portions 204 and become inactive as a catalyst may be used, such as e.g. iron, magnesium oxide, or nickel. As illustrated with an assembly 222 shown in FIG. 6, such metal catalyst 206 will interdiffuse with the metal portions 204 and form a material 208 on the metal portions, which does not enable growth of nanotubes, but will remain on the dielectric portions 202, resulting in the subsequent growth of the nanotubes over the dielectric portions 202 (i.e. similar to the embodiment of FIG. 4, the dielectric portions 202 become the nanotube growth areas in the embodiment of FIG. 6). In various embodiments, a continuous layer of

the metal catalyst 206 may be deposited as shown in FIG. 5 using ALD, CVD, physical vapor deposition (PVD), or evaporation, as known in the art.

[0046] In further embodiments, nanotube growth areas may be formed by covering some parts of the substrate with a material that prevents growth of nanotubes (such material referred to herein as a “poisoning material” to indicate that it prevents, or poisons, growth of nanotubes), while covering other parts with a material that, in combination with a metal catalyst on top of it, would enable nanotube growth, and then providing a continuous layer of a catalyst over the substrate. Such an embodiment is illustrated in FIGS. 7-10.

[0047] FIG. 7 illustrates an assembly 224 that includes the metal portions 204 and the dielectric portions 202 as described above, except that now the dielectric portions 202 have been capped with the poisoning material 210 that prevents growth of nanotubes. The poisoning material 210 may e.g. be a metal nitride, e.g. titanium nitride. FIG. 8 illustrates an assembly 226 which results from the metal portions 204 of the assembly 224 of FIG. 7 being recessed as shown, where recess may be implemented as known in the art. In some embodiments, the metal portions 204 could be recessed to be substantially at the same level with an interface between the dielectric portions 202 and the poisoning material 210, as shown in FIG. 8. FIG. 9 illustrates an assembly 228 which results from a metal oxide 212, such as e.g. hafnium oxide, aluminum oxide, zinc oxide, titanium oxide, and/or zirconium oxide, being deposited into the recessed portions of the assembly 226, followed, if needed, by polishing, such as e.g. chemical mechanical polishing (CMP) to remove excess portions of the metal oxide 212 so that the poisoning material 210 is at the surface again, as shown in FIG. 9. Deposition of the metal oxide and polishing may be performed as known in the art. After that, a continuous layer of the metal catalyst 206 may be provided, resulting in an assembly 230 as shown in FIG. 10, where the nanotubes can only grow over the metal portions 204 (i.e. the areas on the surface of the assembly 230 which are above the metal portions 204 are the nanotube growth areas). Similar to the embodiment of FIG. 5, such a continuous layer of the metal catalyst 206 may be deposited using ALD, CVD, PVD, or evaporation, as known in the art.

[0048] FIG. 11 illustrates an assembly 232 that includes the metal portions 204 and the dielectric portions 202 as described above, except that now the metal portions 204 have been capped with the poisoning material 210 that prevents growth of nanotubes and the dielectric portions 202 have been recessed, i.e. a situation opposite/complementary to that shown in FIG. 8. Again, the poisoning material 210 may e.g. be a metal nitride, e.g. titanium nitride. FIG. 12 illustrates an assembly 234 which results from a metal oxide 212 as described above being deposited into the recessed portions of the assembly 232, followed by polishing, if needed. After that, a continuous layer of the metal catalyst 206 may be deposited as described above, resulting in an assembly 236 as shown in FIG. 13,

where the nanotubes can only grow over the dielectric portions 202 (i.e. the areas on the surface of the assembly 236 which are above the dielectric portions 202 are the nanotube growth areas).

[0049] Turning back to the method 100A shown in FIG. 1A, once the substrate with one or more nanotube growth areas is provided, at 104, nanotubes can be grown on the nanotube growth areas. FIG. 14 illustrates an assembly 238 that includes the metal portions 204 and the dielectric portions 202 as described above and that further schematically illustrates nanotubes 240 grown on the metal portions 204. Thus, example of FIG. 14 illustrates the scenario where the metal portions 204 were the nanotube growth areas, as described above and as shown e.g. in FIGS. 3 and 9. FIG. 14 and subsequent figures does not specifically show presence or use of the metal catalyst to form the nanotube growth areas, but such a catalyst could still be detectable in a typical real-life structure. Furthermore, FIG. 14 and subsequent figures showing nanotubes only provide a schematic illustration of the nanotubes and, in various embodiments, more nanotubes or less nanotubes than those shown in the figures could be used. Depicting only a few nanotubes in the assembly 238 illustrates an embodiment where the nanotubes 240 could be grown in a relatively sparse manner. For example, in some embodiments, nanotubes grown over substantially equal to or less than 50% of the total surface area of the nanotube growth areas could be qualified as “sparsely grown” nanotubes, while nanotubes grown over, e.g. more than 75% of the surface area of the nanotube growth areas could be qualified as “densely grown” nanotubes. Since density of the nanotubes will have an effect on the overall properties of the structures formed by such nanotubes, such as e.g. dielectric constant value, etch characteristics, etc., density of the nanotubes grown at 104 may be adjusted as needed for a particular implementation in order to optimize and achieve the desired properties.

[0050] In general, the nanotubes may be grown substantially vertically to the wafer surface, on the nanotube growth areas (e.g. where the catalyst was deposited). Nanotubes can grow to heights 10 nanometers to a millimeter, thus creating high AR structures which are impossible to create by conventional selective deposition techniques alone. Even if, due to a limited mechanical stiffness, the nanotubes only remain standing vertically until they are about 1 micrometer high before falling down, such a height would still translate to an AR of about 100. Practically, the height of the nanotubes 240 could be anywhere between 10 nanometers and hundreds of nanometers.

[0051] In some embodiments, the nanotubes grown at 104 could be CNTs. CNTs can be grown by chemical vapor deposition (CVD) at temperatures typically ranging anywhere from 450 to 1000 degrees Celsius, using a suitable metal or metal oxide catalyst as described herein (e.g. Ni, Co, Fe, or alloys thereof) and a carbon-containing gas such as methane, acetylene, carbon monoxide and a reducing gas such as hydrogen. The growth can be assisted by plasma. Growth typically takes place

in two steps: a thermal pretreatment step without the carbon feedstock intended to agglomerate the catalyst thin film into discrete nanoparticles of desired areal density and diameter, and the growth step where the catalyst nanoparticles are exposed to the carbon feedstock, supersaturate with carbon, and carbon nanotubes subsequently grow from the catalyst.

[0052] In other embodiments, the nanotubes grown at 104 could be BNNTs. In some embodiments, BNNTs can be grown by e.g. plasma-enhanced pulsed laser deposition techniques. When such techniques are used, a substrate with the nanotube growth areas is placed into a reaction chamber and a negative substrate bias voltage is induced by nitrogen radio frequency (RF) plasma, which accelerates the positive ions in the RF plasma and boron nitride (BN) vapors to bombard the substrate surface. BN vapors can be created by heating precursors such as borazine, or boron oxides (B_xO_y) in the presence of ammonia. When the kinetic energy of the ions is sufficient, BNNTs will begin to grow at the nanotube growth areas, e.g. at the sites of the metal catalyst as described above. Preferably, the rate of BN species diffusion into the catalyst is higher than the rate of re-sputter. Once the metal catalyst is supersaturated with BN vapor, the BN species will condense into ordered nanotube structures extending away from the surface of the substrate.

[0053] Once the nanotubes are grown, at 106 of the method 100A shown in FIG. 1A, a passivation material may be deposited over one or more areas on the surface of the substrate referred to herein as “passivation areas” to suppress (i.e. eliminate or reduce) deposition of another material on these areas. FIG. 15 illustrates an assembly 242 that includes the metal portions 204, the dielectric portions 202, and the nanotubes 240 grown on the metal portions 204 as was in the assembly 238, and further showing a passivation material 244. The passivation material could be any material, or a combination of materials, that can suppress, eliminate, or reduce subsequent deposition of another material on the areas designated as passivation areas. The example of FIG. 15 illustrates that passivation areas are areas over the dielectric portions 202, while the nanotubes are grown over the metal portions 204. However, if the nanotubes were grown over the dielectric portions 202, then the metal portions 204 could be considered the passivation areas, i.e. in some embodiments, passivation areas could be areas other than those where the nanotubes are grown.

[0054] In some embodiments, the passivation material 244 could be a self-assembled monolayer (SAM) material or a hydrophobic polymer. The selectivity of the passivation material (i.e. surfaces to which the material could attach or be deposited on and surfaces to which the material could not attach or be deposited on) can be defined by selecting appropriate reactive head groups of the SAM molecules. In the embodiments when the passivation material 244 is to be provided over, or attached to, dielectric surfaces, as is shown e.g. with the example of FIG. 15, such a SAM material could include alkyl chains and head groups having one or more of alkoxysilanes,

aminosilanes, and chlorosilanes, which selectively attach to dielectrics. In the embodiments when the passivation material 244 is to be provided over, or attached to, metal surfaces, as is not shown in FIGs, such a SAM material could include one or more of alkenes, alkynes, amines, phosphines, thiols, phosphonic acids, and carboxylic acids, which selectively attach to metals. Octadecylphosphonic acid or octadecylthiol are common examples of chemical compounds that can be used as the passivation material 244 that could selectively combine to metals. Still other passivation materials can attach to both metallic and dielectric surfaces. If such materials are used as the passivation material 244, an additional operation may be implemented to selectively remove the passivation layer from the areas where passivation is not desired, e.g. using thermal annealing, dry etch or wet etch. Examples of passivation materials which can attach to both metallic and dielectric surfaces can be determined based on the type of the metal and the dielectric materials used, as known in the art.

[0055] In some embodiments, the passivation material 244 may be assembled in a solution and then deposited onto the substrate with the nanotubes 240 using e.g. spin-coating or vapor phase deposition. Various methods of growing various SAM materials which could be used as the passivation material 244 are known in the art, all of which are within the scope of the present disclosure.

[0056] In the embodiments where the passivation material 244 is a hydrophobic polymer, such a polymer could include polystyrene based polymers or fluorinated polymer chains, linear or branched alkyl chain decorated polymers. The polymers might contain one or more functional groups such as alkoxysilanes, aminosilanes, and chlorosilanes that allow them to successfully graft to the dielectric surface.

[0057] In various embodiments, the passivation material 244 deposited at 106 could have a thickness between 1 and 20 nanometers, including all values and ranges therein. In general, any thicknesses of the passivation material 244 which allow adequately preventing or reducing deposition of a material in the subsequent operation are within the scope of the present disclosure.

[0058] Once the passivation material has been deposited, at 108 of the method 100A shown in FIG. 1A, a first material may be deposited over the substrate. Since the passivation material 244 is intended to prevent or reduce deposition of the first material, the first material will not be substantially deposited onto the passivation areas. FIG. 16 illustrates an assembly 246 that includes a first material 248 deposited over the metal portions 204, also over the nanotubes 240, but not over the dielectric portions 202 because the passivation material 244 was deposited over the dielectric portions in the example illustrated.

[0059] In some embodiments, the first material 248 may be deposited onto the nanotubes 240, i.e. along the length of the substantial vertical nanotubes. In such embodiments, a pre-treatment of the nanotubes 240 may be carried out prior to depositing the first material at 108, so that the first material can attach to the nanotubes. In some embodiments, such pre-treatment of the nanotubes may include any one of known treatments of using mineral acids, plasma treatments to introduce hydroxyl groups, and other chemical treatments to make the nanotubes more hydrophilic.

[0060] In some embodiments, especially in case the nanotubes 240 are sparsely grown, the first material 248 could be deposited onto the unpassivated surfaces of the substrate between the nanotubes 240, one example of which is indicated in FIG. 16 as an area 250. In other embodiments, the first material 248 is such that it can only be deposited onto the nanotubes but not in between the nanotubes.

[0061] The first material may be deposited at 108 using any suitable deposition process, such as e.g. ALD, for depositing a desired material. In some embodiments, the first material 248 may be a dielectric material such as any one or more of the dielectric materials described herein which could be used as an ILD. In other embodiments, the first material 248 may be a metallic material containing oxygen, e.g. a metal oxide such as but not limited to hafnium oxide, titanium oxide, titanium nitride, zirconium oxide, or aluminum oxide. In still other embodiments, the first material 248 may include any of the metals or their alloys as described herein.

[0062] Because the first material 248 is deposited onto the nanotubes 240 and the nanotubes 240 form structures with relatively high AR, the first material 248 is also deposited to form structures with having a relatively high AR, such as e.g. an AR of equal to or greater than 3, e.g. at least an AR of at least 10 or at least 100, not achievable with conventional selective deposition techniques. An example of height and width used for calculation of the AR for a structure formed by the first material 248 is indicated in FIG. 16 with a height h_1 and a width w_1 , showing that the maximum values for the height and the width are taken into consideration. However, in other embodiments, any other measurements of the height and width may be used for assessing the AR of such structures (as well as AR of other structures described herein), such as e.g. average values or minimum values of the height and the width.

[0063] Once the first material has been deposited, at 110 of the method 100A shown in FIG. 1A, a second material may be deposited over the substrate, as shown in FIG. 17 illustrating an assembly 252 which is a result of a second material 254 being deposited over the assembly 246 of FIG. 16. The second material may be deposited at 110 using any suitable deposition process for depositing a

desired second material over the assembly 246, such as e.g. spin-coating. In other embodiments, the second material 254 may be deposited using CVD, ALD, or PVD.

[0064] In some embodiments, the second material 254 may be a material having sufficient etch selectivity with respect to the first material 248, i.e. a material which would not be substantially etched when etchants which can etch the first material 248 are used, and vice versa.

[0065] In various embodiments, the second material 254 may be a dielectric material such as any one or more of the dielectric materials described herein which could be used as an ILD, or a metallic material containing oxygen, e.g. one or more metal oxides as described herein.

[0066] In some embodiments, prior to the deposition of the second material, the passivation material 244 may be removed, as is shown with the example of FIG. 17. In various embodiments, the passivation material may be removed by thermal treatment of the assembly 246 prior to the deposition of the second material 254, e.g. at temperatures higher than 400 degrees Celsius, or by applying various ash, dry or wet etch to the assembly 246 to remove the passivation material 244.

[0067] Optionally, at 112 of the method 100A shown in FIG. 1A, excess of the second material 254 may be removed so that the first material is exposed on the surface of the substrate, as shown in FIG. 18 illustrating an assembly 256 which is a result of removing the upper layer of the assembly 252 of FIG. 17 that includes some of the second material 254 and some of the first material 248 so that the first material 248 is exposed on the surface 258 of the assembly 256. In some embodiments, the upper portion of the second, and possibly the first, materials may be removed using polishing, e.g. CMP, as known in the art.

[0068] Because the second material 254 was deposited around the structures of the first material 248 which were formed around the nanotubes 240, the second material 254 may also form structures with having a relatively high AR, such as e.g. an AR of equal to or greater than 3, e.g. at least an AR of at least 10 or at least 100. An example of height and width used for calculation of the AR for a structure formed by the second material 254 is indicated in FIG. 18 with a height h_2 and a width w_2 , showing that the maximum values for the height and the width are taken into consideration. However, in other embodiments, any other measurements of the height and width may be used for assessing the AR of such structures. The AR of the structures formed by the second material 254 may be the same or different from that of the structures formed by the first material 248.

[0069] At this point, a structure that includes two materials with different etch selectivity is formed, i.e. the structure of the assembly 256 of FIG. 18 for example. At least the material deposited onto the nanotubes 240 (i.e. the first material 248), but possibly also the material deposited later around such a material (i.e. the second material 254) forms high-AR structures. When one of these two

materials is etched, relatively high AR openings may be advantageously created, or/and relatively high AR structures may be left remaining. Each of FIGS. 1B and 1C provides an example method of how the different etch selectivity of the first and second materials 248 and 254 may advantageously be exploited.

[0070] Referring to the method 100B shown in FIG. 1B, at 114, as a continuation from 112 of the method 100A of FIG. 1A, either the first material 248 or the second material 254 may be removed. Such a removal may be performed by etching, using a suitable etchant for removing the material, as known in the art.

[0071] FIG. 19 illustrates an assembly 260 for an example where the first material 248 is removed at 114 from the assembly 256 of FIG. 18, forming openings 262 in the second material 254. Because the structures of the first material 248 were relatively high AR structures, removing those advantageously allows forming openings with also relatively high AR.

[0072] On the other hand, FIG. 20 illustrates an assembly 264 for an example where the second material 254 was removed at 114, resulting in structures 266 of the first material 248 remaining. As discussed above, these structures of the first material 248 are advantageously relatively high AR structures, not achievable using conventional selection deposition techniques.

[0073] Continuing with the method 100B shown in FIG. 1B, at 116 a third material may be deposited in place of the material removed at 114, and, if necessary, excess of the third material may be removed and the structure may subsequently be planarized, at optional 118, using e.g. CMP. A resulting structure is shown in FIG. 21 illustrating an assembly 268 which is a result of depositing a third material 270 into the openings 262 formed in the assembly 260 of FIG. 19. Similarly, the third material 270 could be deposited into the openings formed by removing the second material as shown with the assembly 264 of FIG. 20 (not specifically shown in the FIGS.) The third material 270 could e.g. include any one or more of electrically conductive materials described herein, thus forming e.g. conductive interconnects, when surrounded by a dielectric material that was not removed at 114. In various embodiments, the third material 270 could be deposited using any suitable technique, such as e.g. CVD, ALD, PVD, electroless deposition, sputtering, etc.

[0074] Referring to the method 100C shown in FIG. 1C, at 120, as a continuation from 112 of the method 100A of FIG. 1A that is alternative to that shown with the method 100B of FIG. 1B, a layer of cover material may be deposited over the substrate with the first and second materials. A resulting structure is shown in FIG. 22 illustrating an assembly 272 which is a result of depositing a cover material 274 over the assembly 256 of FIG. 18. The cover material 274 may be any material prescribed by a particular design, e.g. any one of the dielectric materials or any one of the

electrically conductive materials as described herein, and may be deposited at 120 using any suitable deposition technique for the particular kind of material used.

[0075] Continuing with the method 100C of FIG. 1C, a portion of the cover material 274 may be removed at 122, forming one or more openings exposing one or more of the structures formed of the first material 248 and one or more of the structures formed of the second material 254. A resulting structure is shown in FIG. 23 illustrating an assembly 276 which is a result of removing a portion of the cover material 274 from the assembly 272 of FIG. 22 to form an opening 278 which, in the example illustrated, exposes both the first material 248 and the second material 254.

[0076] At 124 of the method 100C, either the first or the second material may be removed through the opening formed at 122. A resulting structure is shown in FIG. 24 illustrating an assembly 280 which is a result of removing the portion of the first material 248 exposed by the opening 278 of the assembly 276 of FIG. 23 to form an extended opening 282. FIG. 24 illustrates an example of the first material 248 being removed, but, in other embodiments, the second material 254 could be removed instead. Removal of the first or second material at 124 may be performed using etching with an appropriate etchant.

[0077] Advantageously, because the first and second materials 248 and 254 have different etch selectivity, using a particular etchant at 124 will remove one of those materials without substantially etching the other, as shown with the illustration of FIG. 24, which reduces EPE if e.g. the opening in the cover material was formed not exactly where it was supposed to be. This is illustrated in the example shown in FIGS. 22-24 where one could e.g. assume that the opening 278 was supposed to be formed only over the middle structures of the first material 248 shown in these FIGS., but instead it was formed with an offset $d1$, illustrated in FIG. 24, shown as a difference between the centerline of the resulting opening 278 and the centerline of the middle structures of the first material 248. The offset $d1$ is representative of EPE, i.e. a measure of the difference between where the edge of a pattern (in this case – the opening 278) ends up and where the edge of that pattern was supposed to be (in this case, the centerline of the opening 278 was supposed to be aligned with the centerline of the middle structures of the first material 248 shown in FIG. 24).

[0078] Continuing with the method 100C shown in FIG. 1C, at 126 a third material may be deposited in the extended opening formed at 124, and, if necessary, excess of the third material may be removed and the structure may subsequently be planarized, at optional 126, using e.g. CMP. A resulting structure is shown in FIG. 25 illustrating an assembly 284 which is a result of depositing a third material 286 into the extended openings 282 formed in the assembly 280 of FIG. 24. The third material 286 could e.g. include any one or more of electrically conductive materials described herein, thus forming e.g. conductive interconnects, when surrounded by a dielectric material that

was not removed at 124 (e.g. when the second material 254 is a dielectric material, for the embodiment illustrated in FIG. 25). In various embodiments, the third material 286 could be deposited using any suitable technique, such as e.g. CVD, ALD, PVD, electroless deposition, sputtering, etc.

[0079] Many modifications may be made to the examples of using sparsely grown nanotubes as a guide for selecting deposition of other materials. Some of the modifications are mentioned in the exemplary descriptions provided above, but further modifications are possible based on these descriptions, all of which modifications being within the scope of the present disclosure. For example, any one of the first, second, and third materials may be one or more electrically conductive or dielectric materials as described herein, in some embodiments, the one or more nanotube growth areas could be the one designated as the passivation areas described herein, etc.

[0080] As a result of implementing methods of using sparsely grown nanotubes as a guide for selective deposition of other materials as described herein, structures having relatively high ARs may be made of materials from which it was not previously possible to form such structures. For example, in some embodiments, structures of zirconium oxide, hafnium oxide, titanium oxide, zinc oxide, tantalum oxide and/or aluminum oxide having an AR of 3 or higher, or AR of 10 or higher, or AR of 100 or higher may be manufactured. In other embodiments, structures of silicon oxide, silicon nitride, or carbon doped oxide (CDO) having an AR of 3 or higher, or AR of 10 or higher, or AR of 100 or higher may be manufactured.

[0081] FIGS. 26A-26C are flow diagrams of example methods 300A-300C for manufacturing a device using densely grown nanotubes as a guide for selective deposition, in accordance with various embodiments. Although the operations of the methods 300A-300C are illustrated once each and in a particular order, the operations may be performed in any suitable order and repeated as desired, unless described otherwise. For example, one or more operations may be performed in parallel to manufacture multiple patterns of interconnects substantially simultaneously. In addition, manufacturing methods 300A-300C may include other operations, not specifically shown in FIGS. 26A-26C, such as e.g. various cleaning operations as known in the art.

[0082] Accompanying FIGS. 26A-26C are FIGS. 27-36, which illustrate various example stages in the manufacture of a device using the methods of FIGS. 26A-26C, in accordance with various embodiments. Each of FIGS. 27-36 illustrates a cross-sectional view of an assembly provided at, or resulting from, a certain operation of the methods shown in FIGS. 26A-26C. A legend provided within a dashed box at the bottom of each sheet of drawings with FIGS. 27-36 illustrates patterns used to indicate different elements shown in the drawings, so that the drawings are not cluttered by many reference numerals.

[0083] Referring to the method 300A shown in FIG. 26A, at 302, a substrate with one or more nanotube growth areas is provided. Discussions provided above regarding providing the substrate at 102 of FIG. 1A are applicable here, including the discussions of forming the one or more nanotube growth areas as described with reference to FIGS. 3-13, and, in the interests of brevity, are not repeated here.

[0084] Continuing with the method 300A shown in FIG. 26A, once the substrate with one or more nanotube growth areas is provided, at 304, nanotubes can be grown on the nanotube growth areas. FIG. 27 illustrates an assembly 402 that includes the metal portions 204 and the dielectric portions 202 as described above (i.e. the illustrations of FIG. 27 and subsequent figures illustrate a starting substrate of 302 as the assembly 214 shown in FIG. 2 and described above), the assembly 402 further schematically illustrating nanotubes 404 grown on the metal portions 204. Similar to FIG. 14 illustrating a similar manufacturing stage for sparsely grown nanotubes, example of FIG. 27 illustrates the scenario where the metal portions 204 were the nanotube growth areas, as described above and as shown e.g. in FIGS. 3 and 9. FIG. 27 and subsequent figures does not specifically show presence or use of the metal catalyst to form the nanotube growth areas, but such a catalyst could still be detectable in a typical real-life structure. Furthermore, FIG. 27 and subsequent figures showing nanotubes only provide a schematic illustration of the nanotubes and, in various embodiments, more nanotubes or less nanotubes than those shown in the figures could be used. Depicting significantly more nanotubes in the assembly 402 compared to only a few nanotubes depicted in the assembly 238 illustrates an embodiment where the nanotubes 404 could be grown in a relatively dense manner. For example, in some embodiments, the nanotubes 404 could be grown over substantially equal to or less than 75% of the surface area of the nanotube growth areas. Again, since density of the nanotubes will have an effect on the overall properties of the structures formed by such nanotubes, such as e.g. dielectric constant value, etch characteristics, etc., density of the nanotubes grown at 304 may be adjusted as needed for a particular implementation in order to optimize and achieve the desired properties.

[0085] Discussions provided above regarding growth of nanotubes at 104 are applicable to growth of nanotubes at 304 and, therefore, in the interests of brevity, are not repeated here. What defines the density of the nanotubes grown at 304, and thus, differentiates dense growth from sparse growth, is the choice of the catalyst material, the catalyst thickness, the growth surface, and the conditions (temperature, heat-up rate and growth atmosphere) during the initial pretreatment step aimed at forming nanoparticles from which the CNTs subsequently grow. For instance, a fast heat up rate will result in dense distribution of small catalyst nanoparticles and, hence, dense nanotube

growth, while a slower heat up rate will result in sparse distribution of catalyst nanoparticles and, hence, sparse nanotube growth.

[0086] Once the nanotubes are grown, at 306 of the method 300A shown in FIG. 26A, a first material may be deposited around, and possibly over, the nanotubes 404. FIG. 28 illustrates an assembly 406 that includes a first material 248 deposited over the metal portions 204 and over the nanotubes 404. In this implementation, because the nanotubes 404 are densely grown, there is not enough space in between the nanotubes to substantially deposit the first material 248 between the nanotubes 404. Furthermore, as grown, nanotubes are typically hydrophobic and inherently unreactive and, therefore, dense array of nanotubes 404 may restrict deposition of another material, in this case – the first material 248, to areas around the nanotubes 404, as shown in FIG. 28. The first material may be deposited at 306 using any suitable deposition process, such as e.g. spin-coating, CVD, ALD, or any other known deposition techniques for depositing a desired material.

[0087] In various embodiments, the first material 248 deposited around the nanotubes 404 at 306 may be a dielectric material such as any one or more of the dielectric materials described herein which could be used as an ILD, or a metallic material containing oxygen, e.g. one or more of metal oxides described herein. In still other embodiments, the first material 248 deposited around the nanotubes 404 at 306 may include any of the materials described herein which could provide sufficient etch selectivity with respect to the neighboring material, i.e. the nanotubes 404.

[0088] Because the first material 248 is deposited around the nanotubes 404 and the nanotubes 404 form structures with relatively high AR, the first material 248 deposited at 306 may also form structures with having a relatively high AR, such as e.g. an AR of equal to or greater than 3, e.g. at least an AR of at least 10 or at least 100, not achievable with conventional selective deposition techniques.

[0089] Once the first material has been deposited, at optional 308 of the method 300A shown in FIG. 3A, excess of the first material 248 may be removed so that the densely packed structures of the nanotubes 404 are exposed on the surface of the substrate, as shown in FIG. 29 illustrating an assembly 408 which is a result of removing the upper layer of the assembly 406 of FIG. 28 that includes some of the first material 248 and some of the nanotubes 404 so that the nanotubes 404 are exposed on the surface 410 of the assembly 408. In some embodiments, the upper portion of the assembly 406 of FIG. 28 may be removed using polishing, e.g. CMP, as known in the art.

[0090] At this point, a structure that includes two materials with different etch selectivity is formed, i.e. the structure of the assembly 408 of FIG. 29 for example. At least the nanotubes 404 grown on the nanotube growth areas, but possibly also the first material 248 deposited around the nanotubes 404, form high-AR structures. When one of these two materials is etched, relatively high AR

openings may be advantageously created, or/and relatively high AR structures may be left remaining. Each of FIGS. 3B and 3C provides an example method of how the different etch selectivity of the first material 248 and the densely grown nanotubes 404 may advantageously be exploited.

[0091] Referring to the method 300B shown in FIG. 26B, at 310, as a continuation from 308 of the method 300A of FIG. 3A, either the nanotubes 404 or the first material 248 may be removed. Such a removal may be performed by etching, using a suitable etchant for removing the material, as known in the art. FIG. 30 illustrates an assembly 412 for an example where the nanotubes 404 are removed at 310 from the assembly 408 of FIG. 29, forming openings 414 in the first material 248. Because the nanotubes 404 formed relatively high AR structures, removing those advantageously allows forming openings in the first material 248 with also relatively high AR.

[0092] Continuing with the method 300B shown in FIG. 26B, at 312 a second material may be deposited in place of the material removed at 310, and, if necessary, excess of the second material may be removed and the structure may subsequently be planarized, at optional 314, using e.g. CMP. Discussions provided above with reference to operations 116 and 118 of FIG. 1B regarding depositing the third material 270 into openings 262 are applicable to depositing a second material into openings 414 formed at 310 and, therefore, are not repeated here. As a result of carrying out the method 300B of FIG. 26B, structure similar to the assembly 268 shown in FIG. 21 may be formed.

[0093] Referring to the method 300C shown in FIG. 26C, at 316, as a continuation from 308 of the method 300A of FIG. 26A that is alternative to that shown with the method 300B of FIG. 26B, a layer of cover material may be deposited over the substrate with the first and second materials. A resulting structure is shown in FIG. 31 illustrating an assembly 416 which is a result of depositing the cover material 274 over the assembly 408 of FIG. 29. Discussions regarding deposition of the cover material 274 provided above with reference to operation 120 of FIG. 1C are applicable to the deposition of the operation 316 of FIG. 26C and, therefore, are not repeated here.

[0094] Continuing with the method 300C of FIG. 26C, a portion of the cover material 274 may be removed at 318, forming one or more openings exposing one or more of the structures formed of the first material 248 and one or more of the structures formed of the nanotubes 404. A resulting structure is shown in FIG. 32 illustrating an assembly 418 which is a result of removing a portion of the cover material 274 from the assembly 416 of FIG. 31 to form an opening 420 which, in the example illustrated, exposes both the first material 248 and the nanotubes 404. Discussions regarding removing of a portion of the cover material 274 provided above with reference to operation 122 of FIG. 1C are applicable to the operation 318 of FIG. 26C and, therefore, are not repeated here.

[0095] At 320 of the method 300C shown in FIG. 26C, either the first material 248 or the nanotubes 404 exposed by the opening formed at 318 may be removed through said opening. A resulting structure is shown in FIG. 33 illustrating an assembly 422 which is a result of removing the portion of the nanotubes 404 exposed by the opening 420 of the assembly 418 of FIG. 32 to form an extended opening 424. FIG. 33 illustrates an example of the nanotubes 404 being removed, but, in other embodiments, the first material 248 could be removed instead. Removal of the first material 248 or the nanotubes 404 at 320 may be performed using etching with an appropriate etchant.

[0096] Advantageously, because the first material 248 and the nanotubes 404 have different etch selectivity, using a particular etchant at 320 will remove one of those materials without substantially etching the other, as shown with the illustration of FIG. 33, which reduces EPE if e.g. the opening in the cover material was formed not exactly where it was supposed to be. Discussions provided regarding the offset of the opening 278 provided with reference to FIG. 24 are applicable to an analogous offset shown in FIG. 33 and, therefore, are not repeated here.

[0097] Continuing with the method 300C shown in FIG. 26C, at 322 a second material may be deposited in the extended opening formed at 320, and, if necessary, excess of the second material may be removed and the structure may subsequently be planarized, at optional operation 324, using e.g. CMP. A resulting structure is shown in FIG. 34 illustrating an assembly 426 which is a result of depositing a second material, e.g. material 254, into the extended opening 424 formed in the assembly 422 of FIG. 23. The second material 254 could e.g. include any one or more of electrically conductive materials described herein, thus forming e.g. conductive interconnects, when surrounded by a dielectric material that was not removed at 320 (e.g. when the first material 248 is a dielectric material, for the embodiment illustrated in FIG. 34). In various embodiments, the second material 254 could be deposited using any suitable technique, such as e.g. CVD, ALD, PVD, electroless deposition, sputtering, etc.

[0098] FIGS. 35 and 36 illustrate embodiments alternative to those shown in FIGS. 28 and 30 and described above. As shown in FIG. 35 with an assembly 430, the first material 248 deposited at 316 could be such that it is provided only around the nanotubes 404 but not over the nanotubes. In such a case, removal of the first material 248 to expose the nanotubes 404, as described above, is not necessary because the nanotubes 404 are already exposed. The exposed nanotubes 404 may then be removed, e.g. by etching, at operation 310, to form an assembly 432 as shown in FIG. 36, with openings 434, which is similar to FIG. 30 and the openings 414, as described above. The openings 434 may then be filled with a second material, as described in 312, and possibly planarized, as described in 314.

[0099] Alternatively, the assembly 430 of FIG. 35 may be planarized and then the method 300C of FIG. 26C may be applied.

[0100] It should be noted that the first and second materials 248 and 254 referred to in the description of FIGS. 26A-26C and FIGS. 27-36 are not necessarily the same materials as those described above with reference to the description of FIGS. 1A-1C and FIGS. 3-25.

[0101] Many modifications may be made to the examples of using densely grown nanotubes as a guide for selecting deposition of other materials. Some of the modifications are mentioned in the exemplary descriptions provided above, but further modifications are possible based on these descriptions, all of which modifications being within the scope of the present disclosure.

[0102] As a result of implementing methods of using densely grown nanotubes as a guide for selecting deposition of other materials as described herein, structures having relatively high ARs may be made of materials from which it was not previously possible to form such structures. For example, in some embodiments, structures of zirconium oxide, hafnium oxide, titanium oxide, zinc oxide, tantalum oxide and/or aluminum oxide having an AR of 3 or higher, or AR of 10 or higher, or AR of 100 or higher may be manufactured. In other embodiments, structures of silicon oxide, silicon nitride, or carbon doped oxide (CDO) having an AR of 3 or higher, or AR of 10 or higher, or AR of 100 or higher may be manufactured.

[0103] In various embodiments, the use of the methods of using either sparsely grown or densely grown nanotubes as a guide for selecting deposition of other materials as described herein may be detected by examining cross-sections of the final structures using e.g. Transmission Electron Microscopy (TEM) or Scanning Electron Microscopy (SEM) or by performing chemical analysis of the components present. For example, in some embodiments, the shape of the resulting structures of materials grown on or around nanotubes may be influenced, e.g. may conform to, the nanotube structures used for guiding their growth. In some embodiments, the upper portions of the resulting structures of materials may be less wide than the lower portions, as e.g. shown in FIGS. 16 or 17. In some embodiments where the materials with the nanotubes in them are not removed, a cross-section would reveal the presence of the nanotubes. In still other embodiments, presence of various remaining catalysts used to provide nanotube growth areas as described herein may be detected.

[0104] Embodiments described above refer to nanotubes grown, either as sparsely or as densely packed structures, over the upper surface of a substrate. In other embodiments, parts of the methods described above may be used to grow nanotubes inside openings in order to form structures having two or more materials having different etch selectivity. FIGS. 37A-37B are flow diagrams of example methods 500A-500B for manufacturing a device using nanotubes grown inside one or more openings, in accordance with various embodiments. Although the operations of the

methods 500A-500B are illustrated once each and in a particular order, the operations may be performed in any suitable order and repeated as desired, unless described otherwise. For example, one or more operations may be performed in parallel to manufacture multiple patterns of interconnects substantially simultaneously. In addition, manufacturing methods 500A-500B may include other operations, not specifically shown in FIGS. 37A-37B, such as e.g. various cleaning operations as known in the art.

[0105] Accompanying FIGS. 37A-37B are FIGS. 38-44, which illustrate various example stages in the manufacture of a device using the methods of FIGS. 37A-37B, in accordance with various embodiments. Each of FIGS. 38-44 illustrates a cross-sectional view of an assembly provided at, or resulting from, a certain operation of the methods shown in FIGS. 37A-37B. A legend provided within a dashed box at the bottom of each sheet of drawings with FIGS. 38-44 illustrates patterns used to indicate different elements shown in the drawings, so that the drawings are not cluttered by many reference numerals.

[0106] Referring to the method 500A shown in FIG. 37A, at 502, a substrate with one or more openings and nanotube growth areas provided within the openings is provided. Any of the substrates as discussed herein may be used as a starting substrate at 502. Discussions provided above regarding forming the one or more nanotube growth areas as described with reference to FIGS. 3-13 are applicable here except that now the nanotube growth areas are formed at the bottom of the openings.

[0107] Since nanotubes can be used particularly advantageously due to their etch selectivity with respect to other materials, in some implementations, the substrate may further include one or more openings filled with another material that has sufficient etch selectivity with respect to the nanotubes which will be grown in other openings. An example of such a substrate is shown in FIG. 38 illustrating an assembly 602 that includes a base 604 with the metal portions 204 and the dielectric portions 202 as described above as well as an overlayer 606, formed e.g. of any one of the dielectric materials described herein. In the overlayer 606, one or more openings 608 are formed for growing the nanotubes. The one or more openings 608 may be treated to ensure that the bottoms of these openings are suitable for growing the nanotubes, e.g. by applying various catalysts as described herein or/and by providing the openings 608 over the metal portions 204 which are able to support nanotube growth, as also described herein and as shown in the example of FIG. 38 and the subsequent FIGS. 39-44. As also shown in FIG. 38 and the subsequent FIGS., the overlayer 606 may further include one or more openings 610 filled with a material 612. The material 612 may be any of the materials described herein and is preferably selected so that it would have sufficient

etch selectivity with respect to the nanotubes later grown in the openings 608 so that etchants which would etch the nanotubes would not substantially etch the material 612, and vice versa.

[0108] Continuing with the method 500A shown in FIG. 37A, once the substrate with the openings having one or more nanotube growth areas is provided, at 504, nanotubes can be grown in the openings. FIG. 39 illustrates an assembly 614 that shows the assembly 602 of FIG. 38 after nanotubes 616 are grown in the openings 608. In various embodiments, the nanotubes 616 may be sparsely grown or densely grown nanotubes, as described herein. Again, since density of the nanotubes in the openings 608 will have an effect on the overall properties of the materials formed by such nanotubes, such as e.g. dielectric constant value, etch characteristics, etc., density of the nanotubes grown at 504 may be adjusted as needed for a particular implementation in order to optimize and achieve the desired properties. Discussions provided above regarding growth of nanotubes at 104 and at 304 are applicable to growth of nanotubes at 504 and, therefore, in the interests of brevity, are not repeated here.

[0109] As with the FIGS. described above, FIG. 38 and subsequent figures does not specifically show presence or use of the metal catalyst to form the nanotube growth areas, but such a catalyst could still be detectable in a typical real-life structure. Furthermore, FIG. 39 and subsequent figures showing nanotubes only provide a schematic illustration of the nanotubes and, in various embodiments, more nanotubes or less nanotubes than those shown in the figures could be used.

[0110] Once the nanotubes 616 have been grown, at optional process 506 of the method 500A shown in FIG. 37A, the nanotubes 616 may be planarized (i.e. the excess of the nanotubes may be removed), as shown in FIG. 40 illustrating an assembly 618 which is a result of performing such planarization. In some embodiments, the planarization of 506 may be performed by polishing, e.g. CMP, as known in the art.

[0111] In another optional process 508 of the method 500A shown in FIG. 37A, which could take place before, after, or instead of the process 506 described above, the nanotubes 616 may be cured. Curing of 508 may be performed e.g. by using heat, ultraviolet (UV) photons or light of different wavelength range, or/and electron beams. In some embodiments, curing may involve heating the assembly 618 between 200-450 degrees Celsius, including all values and ranges therein, while simultaneously exposing to optical radiation of 170-254 nm wavelengths (i.e., deep ultraviolet light), including all values and ranges therein. In other embodiments, curing may involve heating the assembly 618 between 200-450 degrees Celsius, including all values and ranges therein, and exposing the assembly 618 to electrons.

[0112] At this point, a structure that includes two materials with different etch selectivity is formed, i.e. the structure of the assembly 618 of FIG. 40 for example. At least the nanotubes 606 grown in

the openings 608, but possibly also the material 612 provided in the openings 610, form high-AR structures, i.e. at least the openings 608 but possibly also the openings 610 described herein are high-AR openings, e.g. with an AR of at least 3, e.g. with an AR of at least 10 or an AR of at least 100, including all values and ranges therein. In some embodiments, the nanotubes 606 may be left in the openings 608 because e.g. they serve as electrically conductive materials of interconnects as described herein. In some embodiments, some of the nanotubes 606 may later be removed from the nanotubes, as needed, e.g. either because the electrically conductive material that the nanotubes formed is not needed in certain locations on the substrate or/and because the nanotubes 606 in the openings 608 serve as a sacrificial material with sufficient etch selectivity to the material 612, i.e. some of the nanotubes 606 are to be etched later on. FIG. 37B provides an example method of how the different etch selectivity of the material 612 in the openings 610 and of the nanotubes 606 in the openings 608 may advantageously be exploited.

[0113] Referring to the method 500B shown in FIG. 37B, at 510, as a continuation from 504, 506, or 508 of the method 500A of FIG. 37A, a layer of cover material may be deposited over the substrate with the nanotubes in the openings. A resulting structure is shown in FIG. 41 illustrating an assembly 622 which is a result of depositing the cover material 274 over the assembly 618 of FIG. 40. Discussions regarding deposition of the cover material 274 provided above with reference to operation 120 of FIG. 1C are applicable to the deposition of the operation 510 of FIG. 37B and, therefore, are not repeated here.

[0114] Continuing with the method 500B of FIG. 37B, a portion of the cover material 274 may be removed at 512, forming one or more openings exposing one or more openings 608 filled with the nanotubes 606 and possibly also one or more openings 610 filled with the material 612. A resulting structure is shown in FIG. 42 illustrating an assembly 624 which is a result of removing a portion of the cover material 274 from the assembly 622 of FIG. 41 to form an opening 626 which, in the example illustrated, exposes both the first material 612 in one of the openings 610 and the nanotubes 606 in one of the openings 608. Discussions regarding removing of a portion of the cover material 274 provided above with reference to operation 122 of FIG. 1C are applicable to the operation 512 of FIG. 37B and, therefore, are not repeated here.

[0115] At 514 of the method 500B shown in FIG. 37B, either the material 612 or the nanotubes 606 exposed by the opening formed at 512 may be removed through said opening. A resulting structure is shown in FIG. 43 illustrating an assembly 628 which is a result of removing the portion of the nanotubes 606 exposed by the opening 626 of the assembly 624 of FIG. 42 to form an extended opening 630. FIG. 43 illustrates an example of the nanotubes 606 being removed, but, in other

embodiments, the material 612 could be removed instead. Removal of the material 612 or the nanotubes 606 at 514 may be performed using etching with an appropriate etchant.

[0116] Advantageously, because the material 612 and the nanotubes 606 have different etch selectivity, using a particular etchant at 514 will remove one of those materials without substantially etching the other, as shown with the illustration of FIG. 43, which reduces EPE if e.g. the opening in the cover material was formed not exactly where it was supposed to be. Discussions provided regarding the offset of the opening 278 provided with reference to FIG. 24 are applicable to an analogous offset shown in FIG. 43 and, therefore, are not repeated here.

[0117] Continuing with the method 500B shown in FIG. 37B, at 516 a filling material may be deposited in the extended opening formed at 514, and, if necessary, excess of the filling material may be removed and the structure may subsequently be planarized, using e.g. CMP. A resulting structure is shown in FIG. 44 illustrating an assembly 632 which is a result of depositing a filling material, e.g. the material 254 as described herein, into the extended opening 630 formed in the assembly 628 of FIG. 43. In various embodiments, the material 254 could be deposited using any suitable technique, such as e.g. CVD, ALD, PVD, electroless deposition, sputtering, etc.

[0118] In some embodiments, the material 254 deposited into the extended opening 630 may be any of the dielectric materials described herein. When used in combination with the nanotubes 606 forming electrically conductive interconnects at other locations in the substrate, removing the electrically conductive material of the nanotubes 606 from one of the openings 608 and, instead, filling the opening with a dielectric material may be used as a plug commonly employed in metallization stacks. The dielectric material 254 could then be either the same or different than the material 606 which could also be a dielectric.

[0119] It should be noted that the materials 254 and 274 referred to in the description of FIGS. 37A-37B and FIGS. 38-44 are not necessarily the same materials as those described above with reference to the description of FIGS. 1A-1C and FIGS. 3A-3C and their associated cross-sectional illustrations of assemblies.

[0120] Many modifications may be made to the examples of depositing nanotubes into openings. Some of the modifications are mentioned in the exemplary descriptions provided above, but further modifications are possible based on these descriptions, all of which modifications being within the scope of the present disclosure.

[0121] As a result of implementing methods of depositing nanotubes into openings as described herein, openings with relatively high ARs may be filled with materials which was not possible to get into such openings before. For example, in some embodiments, openings having an AR of 5 or higher, or AR of 10 or higher, or AR of 100 or higher may be filled with nanotubes.

[0122] In various embodiments, the use of the methods of depositing nanotubes into openings as described herein may be detected by examining cross-sections of the final structures using e.g. TEM or SEM or by performing chemical analysis of the components present. For example, in some embodiments where the nanotubes are not removed, a cross-section would reveal the presence of the nanotubes. In still other embodiments, presence of various remaining catalysts used to provide nanotube growth areas at the bottom of the openings as described herein may be detected.

[0123] Structures formed with an assistance of nanotubes as disclosed herein may be included in any suitable electronic device. FIGS. 45-48 illustrate various examples of apparatuses that may include one or more of the transistor source/drain stacks disclosed herein.

[0124] FIGS. 45A-B are top views of a wafer 1100 and dies 1102 that may include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein. The wafer 1100 may be composed of semiconductor material and may include one or more dies 1102 having IC structures formed on a surface of the wafer 1100. Each of the dies 1102 may be a repeating unit of a semiconductor product that includes any suitable IC (e.g., ICs including one or more structures formed with an assistance of nanotubes as described herein). After the fabrication of the semiconductor product is complete (e.g., after manufacture of the one or more structures formed with an assistance of nanotubes as described herein), the wafer 1100 may undergo a singulation process in which each of the dies 1102 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices that include one or more structures formed with an assistance of nanotubes as described herein as disclosed herein may take the form of the wafer 1100 (e.g., not singulated) or the form of the die 1102 (e.g., singulated). The die 1102 may include one or more transistors (e.g., one or more of the transistors 1240 of FIG. 46, discussed below) and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components. In some embodiments, the wafer 1100 or the die 1102 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1102. For example, a memory array formed by multiple memory devices may be formed on a same die 1102 as a processing device (e.g., the processing device 1402 of FIG. 48) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0125] FIG. 46 is a cross-sectional side view of an IC device 1200 that may include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein. The IC device 1200 may be formed on a substrate 1202 (e.g., the wafer 1100 of FIG. 45A) and may be included in a die (e.g., the die 1102 of FIG. 45B). The substrate 1202 may be a

semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. The substrate 1202 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 1202 may be formed using alternative materials, which may or may not be combined with silicon, that include, but are not limited to, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 1202. Although a few examples of materials from which the substrate 1202 may be formed are described here, any material that may serve as a foundation for an IC device 1200 may be used. The substrate 1202 may be part of a singulated die (e.g., the dies 1102 of FIG. 45B) or a wafer (e.g., the wafer 1100 of FIG. 45A).

[0126] The IC device 1200 may include one or more device layers 1204 disposed on the substrate 1202. The device layer 1204 may include features of one or more transistors 1240 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 1202. The device layer 1204 may include, for example, one or more source and/or drain (S/D) regions 1220, a gate 1222 to control current flow in the transistors 1240 between the S/D regions 1220, and one or more S/D contacts 1224 to route electrical signals to/from the S/D regions 1220. The transistors 1240 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 1240 are not limited to the type and configuration depicted in FIG. 46 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors. In particular, one or more of the transistors 1240 may include one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein.

[0127] Each transistor 1240 may include a gate 1222 formed of at least two layers, a gate dielectric layer and a gate electrode layer. Generally, the gate dielectric layer of a transistor 1240 may include one layer or a stack of layers, and the one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material.

[0128] In some embodiments, when viewed as a cross section of the transistor 1240 along the source-channel-drain direction, the gate electrode may include a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is

substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may include a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may include one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers. In some embodiments, the gate electrode may include a V-shaped structure (e.g., when the fin of the tri-gate transistor does not have a "flat" upper surface, but instead has a rounded peak).

[0129] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0130] The S/D regions 1220 may be formed within the substrate 1202 adjacent to the gate 1222 of each transistor 1240. In other embodiments, the S/D regions 1220 may be formed using any suitable processes known in the art. For example, the S/D regions 1220 may be formed using either an implantation/diffusion process or a deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate 1202 to form the S/D regions 1220. An annealing process that activates the dopants and causes them to diffuse farther into the substrate 1202 may follow the ion implantation process. In the latter process, an epitaxial deposition process may provide material that is used to fabricate the S/D regions 1220. In some implementations, the S/D regions 1220 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 1220 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 1220. In some embodiments, an etch process may be performed before the epitaxial deposition to create recesses in the substrate 1202 in which the material for the S/D regions 1220 is deposited.

[0131] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 1240 of the device layer 1204 through one or more interconnect layers disposed on the device layer 1204 (illustrated in FIG. 46 as interconnect layers 1206-1210). For example, electrically conductive features of the device layer 1204 (e.g., the gate 1222 and the S/D contacts

1224) may be electrically coupled with the interconnect structures 1228 of the interconnect layers 1206-1210. The one or more interconnect layers 1206-1210 may form an interlayer dielectric (ILD) stack 1219 of the IC device 1200.

[0132] The interconnect structures 1228 may be arranged within the interconnect layers 1206-1210 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 1228 depicted in FIG. 46). Although a particular number of interconnect layers 1206-1210 is depicted in FIG. 46, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0133] In some embodiments, the interconnect structures 1228 may include trench structures 1228a (sometimes referred to as "lines") and/or via structures 1228b (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The trench structures 1228a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 1202 upon which the device layer 1204 is formed. For example, the trench structures 1228a may route electrical signals in a direction in and out of the page from the perspective of FIG. 46. The via structures 1228b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 1202 upon which the device layer 1204 is formed. In some embodiments, the via structures 1228b may electrically couple trench structures 1228a of different interconnect layers 1206-1210 together.

[0134] The interconnect layers 1206-1210 may include a dielectric material 1226 disposed between the interconnect structures 1228, as shown in FIG. 46. In some embodiments, the dielectric material 1226 disposed between the interconnect structures 1228 in different ones of the interconnect layers 1206-1210 may have different compositions; in other embodiments, the composition of the dielectric material 1226 between different interconnect layers 1206-1210 may be the same.

[0135] A first interconnect layer 1206 (referred to as Metal 1 or "M1") may be formed directly on the device layer 1204. In some embodiments, the first interconnect layer 1206 may include trench structures 1228a and/or via structures 1228b, as shown. The trench structures 1228a of the first interconnect layer 1206 may be coupled with contacts (e.g., the S/D contacts 1224) of the device layer 1204.

[0136] A second interconnect layer 1208 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 1206. In some embodiments, the second interconnect layer 1208 may include via structures 1228b to couple the trench structures 1228a of the second interconnect layer 1208 with the trench structures 1228a of the first interconnect layer 1206. Although the trench structures 1228a and the via structures 1228b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 1208) for the sake of clarity, the trench

structures 1228a and the via structures 1228b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0137] A third interconnect layer 1210 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 1208 according to similar techniques and configurations described in connection with the second interconnect layer 1208 or the first interconnect layer 1206.

[0138] The IC device 1200 may include a solder resist material 1234 (e.g., polyimide or similar material) and one or more bond pads 1236 formed on the interconnect layers 1206-1210. The bond pads 1236 may be electrically coupled with the interconnect structures 1228 and configured to route the electrical signals of the transistor(s) 1240 to other external devices. For example, solder bonds may be formed on the one or more bond pads 1236 to mechanically and/or electrically couple a chip including the IC device 1200 with another component (e.g., a circuit board). The IC device 1200 may have other alternative configurations to route the electrical signals from the interconnect layers 1206-1210 than depicted in other embodiments. For example, the bond pads 1236 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0139] FIG. 47 is a cross-sectional side view of an IC device assembly 1300 that may include components having one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein. The IC device assembly 1300 includes a number of components disposed on a circuit board 1302 (which may be, e.g., a motherboard). The IC device assembly 1300 includes components disposed on a first face 1340 of the circuit board 1302 and an opposing second face 1342 of the circuit board 1302; generally, components may be disposed on one or both faces 1340 and 1342. In particular, any suitable ones of the components of the IC device assembly 1300 may include one or more structures formed with an assistance of nanotubes as described herein.

[0140] In some embodiments, the circuit board 1302 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1302. In other embodiments, the circuit board 1302 may be a non-PCB substrate.

[0141] The IC device assembly 1300 illustrated in FIG. 47 includes a package-on-interposer structure 1336 coupled to the first face 1340 of the circuit board 1302 by coupling components 1316. The coupling components 1316 may electrically and mechanically couple the package-on-interposer

structure 1336 to the circuit board 1302, and may include solder balls (as shown in FIG. 47), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0142] The package-on-interposer structure 1336 may include an IC package 1320 coupled to an interposer 1304 by coupling components 1318. The coupling components 1318 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1316. Although a single IC package 1320 is shown in FIG. 47, multiple IC packages may be coupled to the interposer 1304; indeed, additional interposers may be coupled to the interposer 1304. The interposer 1304 may provide an intervening substrate used to bridge the circuit board 1302 and the IC package 1320. The IC package 1320 may be or include, for example, a die (the die 1102 of FIG. 45B), an IC device (e.g., the IC device 1200 of FIG. 46), or any other suitable component. Generally, the interposer 1304 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1304 may couple the IC package 1320 (e.g., a die) to a ball grid array (BGA) of the coupling components 1316 for coupling to the circuit board 1302. In the embodiment illustrated in FIG. 47, the IC package 1320 and the circuit board 1302 are attached to opposing sides of the interposer 1304; in other embodiments, the IC package 1320 and the circuit board 1302 may be attached to a same side of the interposer 1304. In some embodiments, three or more components may be interconnected by way of the interposer 1304.

[0143] The interposer 1304 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 1304 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1304 may include metal interconnects 1308 and vias 1310, including but not limited to through-silicon vias (TSVs) 1306. The interposer 1304 may further include embedded devices 1314, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1304. The package-on-interposer structure 1336 may take the form of any of the package-on-interposer structures known in the art.

[0144] The IC device assembly 1300 may include an IC package 1324 coupled to the first face 1340 of the circuit board 1302 by coupling components 1322. The coupling components 1322 may take the form of any of the embodiments discussed above with reference to the coupling components

1316, and the IC package 1324 may take the form of any of the embodiments discussed above with reference to the IC package 1320.

[0145] The IC device assembly 1300 illustrated in FIG. 47 includes a package-on-package structure 1334 coupled to the second face 1342 of the circuit board 1302 by coupling components 1328. The package-on-package structure 1334 may include an IC package 1326 and an IC package 1332 coupled together by coupling components 1330 such that the IC package 1326 is disposed between the circuit board 1302 and the IC package 1332. The coupling components 1328 and 1330 may take the form of any of the embodiments of the coupling components 1316 discussed above, and the IC packages 1326 and 1332 may take the form of any of the embodiments of the IC package 1320 discussed above. The package-on-package structure 1334 may be configured in accordance with any of the package-on-package structures known in the art.

[0146] FIG. 48 is a block diagram of an example computing device 1400 that may include one or more components including one or more structures formed with an assistance of nanotubes in accordance with any of the embodiments disclosed herein. For example, any suitable ones of the components of the computing device 1400 may include a die (e.g., the die 1102 (FIG. 45B)) having one or more structures formed with an assistance of nanotubes as described herein. Any one or more of the components of the computing device 1400 may include, or be included in, an IC device 1200 (FIG. 46). Any one or more of the components of the computing device 1400 may include, or be included in, an IC device assembly 1300 (FIG. 47).

[0147] A number of components are illustrated in FIG. 48 as included in the computing device 1400, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 1400 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0148] Additionally, in various embodiments, the computing device 1400 may not include one or more of the components illustrated in FIG. 48, but the computing device 1400 may include interface circuitry for coupling to the one or more components. For example, the computing device 1400 may not include a display device 1406, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 1406 may be coupled. In another set of examples, the computing device 1400 may not include an audio input device 1424 or an audio output device 1408, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 1424 or audio output device 1408 may be coupled.

[0149] The computing device 1400 may include a processing device 1402 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 1402 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 1400 may include a memory 1404, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 1404 may include memory that shares a die with the processing device 1402. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0150] In some embodiments, the computing device 1400 may include a communication chip 1412 (e.g., one or more communication chips). For example, the communication chip 1412 may be configured for managing wireless communications for the transfer of data to and from the computing device 1400. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0151] The communication chip 1412 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 1412 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 1412 may operate in accordance

with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 1412 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 1412 may operate in accordance with other wireless protocols in other embodiments. The computing device 1400 may include an antenna 1422 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0152] In some embodiments, the communication chip 1412 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 1412 may include multiple communication chips. For instance, a first communication chip 1412 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1412 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 1412 may be dedicated to wireless communications, and a second communication chip 1412 may be dedicated to wired communications.

[0153] The computing device 1400 may include battery/power circuitry 1414. The battery/power circuitry 1414 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 1400 to an energy source separate from the computing device 1400 (e.g., AC line power).

[0154] The computing device 1400 may include a display device 1406 (or corresponding interface circuitry, as discussed above). The display device 1406 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0155] The computing device 1400 may include an audio output device 1408 (or corresponding interface circuitry, as discussed above). The audio output device 1408 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0156] The computing device 1400 may include an audio input device 1424 (or corresponding interface circuitry, as discussed above). The audio input device 1424 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0157] The computing device 1400 may include a global positioning system (GPS) device 1418 (or corresponding interface circuitry, as discussed above). The GPS device 1418 may be in communication with a satellite-based system and may receive a location of the computing device 1400, as known in the art.

[0158] The computing device 1400 may include another output device 1410 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1410 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0159] The computing device 1400 may include another input device 1420 (or corresponding interface circuitry, as discussed above). Examples of the other input device 1420 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0160] The computing device 1400 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 1400 may be any other electronic device that processes data.

[0161] The following paragraphs provide various examples of the embodiments disclosed herein.

[0162] Example 1 provides a method for manufacturing a device using sparsely grown nanotubes as a guide for selective deposition. The method includes growing nanotubes on one or more nanotube growth areas on a surface of a substrate, the one or more nanotube growth areas including areas which allow growth of the nanotubes, where, before the growth, the substrate could be processed to ensure that some areas of the surface of the substrate allow the growth; after growing the nanotubes, depositing a passivation material over one or more areas referred to herein as passivation areas on the surface of the substrate to suppress (i.e. eliminate or reduce) deposition of a first material on the one or more passivation areas; and, after depositing the passivation material, depositing the first material over the substrate.

[0163] Example 2 provides the method according to Example 1, where the one or more passivation areas comprise areas different from the one or more nanotube growth areas and where depositing the first material over the substrate may include depositing the first material over the one or more

nanotube growth areas while suppressing deposition of the first material over the one or more passivation areas.

[0164] Example 3 provides the method according to Example 2, where the first material is deposited over or on the nanotubes grown on the one or more nanotube growth areas and over surfaces of the one or more nanotube growth areas lacking nanotubes. Thus, in some embodiments, the first material may be deposited on the nanotubes themselves, as well as on the unpassivated surfaces of the nanotube growth areas between the nanotubes. In other embodiments, the first material may be such that it is deposited only, or substantially, on the nanotubes, but not on the unpassivated surfaces of the nanotube growth areas between the nanotubes.

[0165] Example 4 provides the method according to Examples 2 or 3, further including applying chemical treatment to the nanotubes prior to depositing the first material to enable deposition of the first material over the nanotubes. In various embodiments, such chemical treatment may include e.g. treatment with mineral acids, plasma treatments to introduce hydroxyl groups, or other chemical treatments to make the nanotubes more hydrophilic.

[0166] Example 5 provides the method according to Example 1, where the one or more nanotube growth areas are the one or more passivation areas and where depositing the first material over the substrate may include depositing the first material over areas of the substrate besides the one or more nanotube growth areas while suppressing deposition of the first material over the one or more nanotube growth areas.

[0167] Example 6 provides the method according to any one of the preceding Examples, where the first material is not deposited over the one or more passivation areas.

[0168] Example 7 provides the method according to any one of the preceding Examples, where the first material forms first structures having an aspect ratio (i.e. a ratio of a vertical dimension of a structure to a horizontal dimension of a structure) of at least 3, e.g. at least 10 or at least 100.

[0169] Example 8 provides the method according to any one of the preceding Examples, where depositing the first material may include performing atomic layer deposition (ALD) to deposit the first material.

[0170] Example 9 provides the method according to any one of the preceding Examples, where the first material may include a dielectric material, e.g. a dielectric as may be used to form an interlayer dielectric (ILD), such as e.g. SiO₂, SiN, CDO, SiNCO, or a metal oxide such as but not limited to hafnium oxide, titanium oxide, titanium nitride, zirconium oxide, or aluminum oxide.

[0171] Example 10 provides the method according to any one of the preceding Examples, further including depositing a second material over the substrate after depositing the first material.

[0172] Example 11 provides the method according to Example 10, where the second material is deposited by spin-coating.

[0173] Example 12 provides the method according to Example 10, where the second material is deposited by chemical vapor deposition (CVD), atomic layer deposition (ALD), or physical vapor deposition (PVD).

[0174] Example 13 provides the method according to any one of Examples 10-12, further including removing the passivation material prior to depositing the second material. In various embodiments, the passivation material may be removed by thermal treatment e.g. at temperatures higher than 400 degrees Celsius, or by various ash, dry or wet etch conditions.

[0175] Example 14 provides the method according to any one of Examples 10-13, where the second material forms second structures having an aspect ratio of at least 3, e.g. at least 10 or at least 100.

[0176] Example 15 provides the method according to any one of Examples 10-14, where the second material is a material having different etch properties from the first material (i.e. the first and second materials are etch selective materials; in other words, etchants that can be used to etch the first material do not substantially etch the second material, and vice versa).

[0177] Example 16 provides the method according to any one of Examples 10-15, further including partially removing the second material so that at least some of upper surfaces of the first material are not covered with the second material.

[0178] Example 17 provides the method according to Example 16, where partially removing the second material may include performing polishing of the substrate (e.g. chemical-mechanical polishing) after depositing the second material to expose the upper surfaces of the first material.

[0179] Example 18 provides the method according to any one of Examples 10-17, further including removing either the first material or the second material to form one or more openings over the substrate.

[0180] Example 19 provides the method according to Example 18, where the removal of either the first material or the second material may include etching either the first material or the second material.

[0181] Example 20 provides the method according to Examples 18 or 19, where each of the one or more openings has an aspect ratio (i.e. a ratio of a vertical dimension of an opening to a horizontal dimension of an opening) of at least 3, e.g. at least 10 or at least 100.

[0182] Example 21 provides the method according to any one of Examples 18-20, further including depositing a third material in at least one of the one or more openings.

[0183] Example 22 provides the method according to Example 21, where the third material may include an electrically conductive material.

[0184] Example 23 provides the method according to Examples 16 or 17, further including providing a layer of a cover material, e.g. a layer of an interlayer dielectric (ILD) material, over the substrate with the first material and the second material deposited thereon; forming a via opening in the layer of the cover material, the via opening exposing at least one of the first material and the second material; forming an extended via opening by removing either the first material or the second material exposed by the via opening; and filling the extended via opening with a third material.

[0185] Example 24 provides the method according to Example 23, where the via opening exposes both the first material and the second material.

[0186] Example 25 provides the method according to Examples 23 or 24, where the third material may include an electrically conductive material.

[0187] Example 26 provides the method according to any one of Examples 1-25, where the one or more nanotube growth areas comprise a metal or a metal oxide that allows nanotube growth. The metal may e.g. be a result of previous patterning steps. In such embodiments, nothing further needs to be done to the metal surfaces of these areas. In various embodiments, metals and metal oxides that allow growing nanotubes on their surfaces include metals capable of supersaturating with carbon, their alloys or oxides. Such metals include e.g. cobalt, nickel, iron, manganese, etc. Catalyst materials can also be supported on inert metal oxide layer such as AlOx or HfOx, which will also serve as suitable barrier to prevent intermixing of catalyst with underlying metal.

[0188] Example 27 provides the method according to any one of Examples 1-25, where the one or more nanotube growth areas initially comprise a material that does not allow nanotube growth, and where the method further may include selectively depositing a catalyst material that allows growth of the nanotubes over the material of the one or more nanotube growth areas prior to growing the nanotubes.

[0189] Example 28 provides the method according to Example 27, where the material that does not allow nanotube growth may include a metal that does not allow nanotube growth, such as e.g. copper or ruthenium, or a metal nitride, such as e.g. titanium nitride.

[0190] Example 29 provides the method according to any one of Examples 1-25, where the one or more nanotube growth areas comprise a dielectric material that does not allow nanotube growth and the one or more nanotube growth areas are surrounded by a metal that does not allow nanotube growth, and where the method further may include, prior to growing the nanotubes, depositing over the substrate a layer of a catalyst material that allows growth of the nanotubes, and allowing the catalyst material to interdiffuse with the metal surrounding the one or more nanotube growth areas to become inactive, thus leaving the catalyst material that is active and can support nanotube growth only on the one or more nanotube growth areas.

[0191] Example 30 provides the method according to any one of Examples 1-25, where the method further may include, prior to growing the nanotubes providing a metal oxide over the one or more nanotube growth areas; providing a material that prevents nanotube growth over areas of the substrate except for the one or more nanotube growth areas; and depositing a layer of a catalyst material over the metal oxide and the material that prevents nanotube growth. In such an embodiment, nanotubes can only grow over the catalyst material that is provided over the metal oxide, i.e. the nanotubes will only grow in the nanotube growth area, because the material that prevents nanotube growth will prevent growth of nanotubes even if the catalyst material is provided on top of it.

[0192] Example 31 provides the method according to Example 30, where the material that prevents nanotube growth may include a metal nitride, such as e.g. titanium nitride.

[0193] Example 32 provides the method according to any one of Examples 27-31, where the catalyst material may include one or more of iron, nickel, and cobalt, or an alloy including one or more of iron, nickel, and cobalt.

[0194] Example 33 provides the method according to any one of the preceding Examples, where the nanotubes comprise carbon nanotubes or boron nitride nanotubes.

[0195] Example 34 provides the method according to any one of Examples 1-33, where the passivation material may include a self-assembled monolayer (SAM) material or a hydrophobic polymer.

[0196] Example 35 provides the method according to any one of Examples 1-33, where the passivation material may include a self-assembled monolayer (SAM) material that includes alkyl chains and head groups including one or more of alkoxysilanes, aminosilanes, and chlorosilanes. Such a passivation material may advantageously be used in embodiments where the passivation material needs to be provided over, or attached to, dielectric surfaces.

[0197] Example 36 provides the method according to any one of Examples 1-33, where the passivation material may include a self-assembled monolayer (SAM) material that includes one or more of alkenes, alkynes, amines, phosphines, thiols, phosphonic acids, and carboxylic acids. Such a passivation material may advantageously be used in embodiments where the passivation material needs to be provided over, or attached to, metal surfaces.

[0198] Example 37 provides the method according to any one of the preceding Examples, where the nanotubes occupy 50% or less of a surface area of the one or more nanotube growth areas.

[0199] Example 38 provides a method for manufacturing a device using densely grown nanotubes as a guide for selective deposition. The method includes growing nanotubes over at least 75% of a surface area of one or more nanotube growth areas on a surface of a substrate (i.e. growing a

relatively dense array of nanotubes), the one or more nanotube growth areas including areas which allow growth of the nanotubes, where, before the growth, the substrate could be processed to ensure that some areas of the surface of the substrate allow the growth; and after growing the nanotubes, depositing a first material around the one or more nanotube growth areas.

[0200] Example 39 provides the method according to Example 38, where the first material is deposited by spin-coating, chemical vapor deposition (CVD), atomic layer deposition (ALD), or physical vapor deposition (PVD).

[0201] Example 40 provides the method according to Examples 38 or 39, where the first material forms first structures having an aspect ratio (i.e. a ratio of a vertical dimension of a structure to a horizontal dimension of a structure) of at least 3, e.g. at least 10 or at least 100.

[0202] Example 41 provides the method according to any one of Examples 38-40, where the nanotubes form nanotube structures having an aspect ratio (i.e. a ratio of a vertical dimension of a structure to a horizontal dimension of a structure) of at least 3, e.g. at least 10 or at least 100.

[0203] Example 42 provides the method according to any one of Examples 38-41, where the nanotubes comprise carbon nanotubes or boron nitride nanotubes.

[0204] Example 43 provides the method according to any one of Examples 38-42, where the first material is a material having different etch properties from the nanotubes (i.e. the first material and the nanotubes are etch selective materials; in other words, etchants that can be used to etch the first material do not substantially etch the nanotubes, and vice versa).

[0205] Example 44 provides the method according to any one of Examples 38-43, further including ensuring that, after depositing the first material, at least some of upper surfaces of the nanotubes are not covered with the first material.

[0206] Example 45 provides the method according to Example 43, where ensuring that at least some of upper surfaces of the nanotubes are not covered with the first material may include performing polishing of the substrate (e.g. chemical-mechanical polishing) to expose the upper surfaces of the nanotubes.

[0207] Example 46 provides the method according to Examples 44 or 45, further including removing the nanotubes to form one or more openings over the substrate.

[0208] Example 47 provides the method according to Example 46, where the removal of the nanotubes may include etching the nanotubes.

[0209] Example 48 provides the method according to Examples 46 or 47, where each of the one or more openings has an aspect ratio (i.e. a ratio of a vertical dimension of an opening to a horizontal dimension of an opening) of at least 3, e.g. at least 10 or at least 100.

[0210] Example 49 provides the method according to any one of Examples 46-48, further including depositing a third material in at least one of the one or more openings.

[0211] Example 50 provides the method according to Example 49, where the third material may include an electrically conductive material.

[0212] Example 51 provides the method according to any one of Examples 38-50, where the nanotubes grown over each of the one or more nanotube growth areas form an electrically conductive material.

[0213] Example 52 provides the method according to Examples 44 or 45, further including providing a layer of a cover material, e.g. a layer of an interlayer dielectric (ILD) material, over the substrate with the first material and the nanotubes; forming a via opening in the layer of the cover material, the via opening exposing at least one of the first material and the nanotubes; forming an extended via opening by removing either the first material or the nanotubes exposed by the via opening; and filling the extended via opening with a second material.

[0214] Example 53 provides the method according to Example 52, where the via opening exposes both the first material and the nanotubes.

[0215] Example 54 provides the method according to Examples 52 or 53, where the third material may include an electrically conductive material.

[0216] Example 55 provides the method according to any one of Examples 38-54, where the one or more nanotube growth areas comprise a metal or a metal oxide that allows nanotube growth. The metal may e.g. be a result of previous patterning steps. In such embodiments, nothing further needs to be done to the metal surfaces of these areas. In various embodiments, metals and metal oxides that allow growing nanotubes on their surfaces include metals capable of supersaturating with carbon, their alloys or oxides. Such metals include e.g. cobalt, nickel, iron, manganese, etc. Catalyst materials can also be supported on inert metal oxide layer such as AlO_x or HfO_x, which will also serve as suitable barrier to prevent intermixing of catalyst with underlying metal.

[0217] Example 56 provides the method according to any one of Examples 38-54, where the one or more nanotube growth areas initially comprise a material that does not allow nanotube growth, and where the method further may include selectively depositing a catalyst material that allows growth of the nanotubes over the material of the one or more nanotube growth areas prior to growing the nanotubes.

[0218] Example 57 provides the method according to Example 56, where the material that does not allow nanotube growth may include a metal that does not allow nanotube growth, such as e.g. copper or ruthenium, or a metal nitride, such as e.g. titanium nitride.

[0219] Example 58 provides the method according to any one of Examples 38-54, where the one or more nanotube growth areas comprise a dielectric material that does not allow nanotube growth and the one or more nanotube growth areas are surrounded by a metal that does not allow nanotube growth, and where the method further may include, prior to growing the nanotubes depositing over the substrate a layer of a catalyst material that allows growth of the nanotubes, and allowing the catalyst material to interdiffuse with the metal surrounding the one or more nanotube growth areas to become inactive, thus leaving the catalyst material that is active and can support nanotube growth only on the one or more nanotube growth areas.

[0220] Example 59 provides the method according to any one of Examples 38-54, where the method further may include, prior to growing the nanotubes providing a metal oxide over the one or more nanotube growth areas; providing a material that prevents nanotube growth over areas of the substrate except for the one or more nanotube growth areas; and depositing a layer of a catalyst material over the metal oxide and the material that prevents nanotube growth. In such an embodiment, nanotubes can only grow over the catalyst material that is provided over the metal oxide, i.e. the nanotubes will only grow in the nanotube growth area, because the material that prevents nanotube growth will prevent growth of nanotubes even if the catalyst material is provided on top of it.

[0221] Example 60 provides the method according to Example 59, where the material that prevents nanotube growth may include a metal nitride, such as e.g. titanium nitride.

[0222] Example 61 provides the method according to any one of Examples 56-60, where the catalyst material may include one or more of iron, nickel, and cobalt, or an alloy including one or more of iron, nickel, and cobalt.

[0223] Example 62 provides a device including a substrate and a plurality of structures disposed over the substrate, where each structure includes zirconium oxide, hafnium oxide, titanium oxide, zinc oxide, tantalum oxide, aluminum oxide, silicon oxide, silicon nitride, or carbon doped oxide and having an aspect ratio (AR) between 3 and 100, where the AR is a ratio of a height of the each structure to a width of the each structure.

[0224] Example 63 provides the device according to Example 62, where the each structure may include one or more nanotubes enclosed therein.

[0225] Example 64 provides the device according to Example 63, further including a filling material disposed between the plurality of structures.

[0226] Example 65 provides the device according to Example 64, where the filling material is etch selective with respect to the plurality of structures.

[0227] Example 66 provides the device according to Example 64, where the filling material is an electrically conductive material.

[0228] Example 67 provides the device according to Example 62, where the each structure is adjacent to one or more structures including nanotubes.

[0229] Example 68 provides the device according to Example 67, where the one or more structures including nanotubes are electrically conductive.

[0230] Example 69 provides the device according to any one of Examples 63-68, where the nanotubes comprise carbon nanotubes.

[0231] Example 70 provides the device according to any one of Examples 63-68, where the nanotubes comprise boron nitride nanotubes.

[0232] Example 71 provides the device according to any one of Examples 63-70, where the nanotubes are provided on one or more nanotube growth areas and occupy less than 50% of a surface area of the one or more nanotube growth areas.

[0233] Example 72 provides the device according to any one of Examples 63-70, where the nanotubes are provided on one or more nanotube growth areas and occupy more than 75% of a surface area of the one or more nanotube growth areas.

[0234] Example 73 provides the device according to Example 62, where the each structure further includes a layer of iron, nickel, manganese, or cobalt, or an alloy thereof, in a portion of the structure closest to the substrate.

[0235] Example 74 provides the device according to Example 73, where the each structure further includes a layer of oxygen containing iron, nickel, manganese, or cobalt in a portion of the structure closest to the substrate.

[0236] Example 75 provides the device according to Examples 73 or 74, where the layer has a thickness between 1 and 5 nanometers.

[0237] Example 76 provides a method for manufacturing a device using nanotubes to reduce or eliminate edge placement error (EPE). The method includes depositing a first material in one or more first openings provided in a substrate and growing nanotubes in one or more second openings provided in the substrate, where the first material is a material having different etch properties from the nanotubes (i.e. the first material and the nanotubes are etch selective materials; in other words, etchants that can be used to etch the first material do not substantially etch the nanotubes, and vice versa).

[0238] Example 77 provides the method according to Example 76, further including performing polishing of the substrate (e.g. chemical-mechanical polishing), following deposition of the first material and of the nanotubes.

[0239] Example 78 provides the method according to Examples 76 or 77, further including curing the nanotubes to form a conductive material in the one or more second openings.

[0240] Example 79 provides the method according to any one of Examples 76-78, further including providing a layer of an interlayer dielectric (ILD) material over the substrate with the first material and the nanotubes; forming a via opening in the layer of the ILD material, the via opening exposing at least a portion of one opening of the one or more first openings filled with the first material and at least a portion of one opening of the one or more second openings filled with the nanotubes; forming an extended via opening by removing either the first material from the one opening of the one or more first openings or the nanotubes from the one opening of the one or more second openings; and filling the extended via opening with a second material.

[0241] Example 80 provides the method according to Example 79, where the second material may include an electrically conductive material.

[0242] Example 81 provides the method according to any one of Examples 76-80, where the one or more first openings and the one or more second openings are provided in the substrate in an alternating manner.

[0243] Example 82 provides the method according to any one of Examples 76-81, where the one or more first openings and the one or more second openings comprise trenches provided in the substrate.

[0244] Example 83 provides the method according to any one of Examples 76-82, where the nanotubes grown in the one or more second openings occupy at least 75% of a volume of the one or more second openings.

[0245] Example 84 provides the method according to any one of Examples 76-83, where the nanotubes comprise carbon nanotubes or boron nitride nanotubes.

[0246] Example 85 provides the method according to any one of Examples 76-84, where, prior to growing the nanotubes, bottoms of the one or more second openings comprise one or more nanotube growth areas.

[0247] Example 86 provides the method according to Example 85, where the one or more nanotube growth areas comprise a metal or a metal oxide that allows nanotube growth. The metal may e.g. be a result of previous patterning steps. In such embodiments, nothing further needs to be done to the metal surfaces of these areas. In various embodiments, metals and metal oxides that allow growing nanotubes on their surfaces include metals capable of supersaturating with carbon, their alloys or oxides. Such metals include e.g. cobalt, nickel, iron, manganese, etc. Catalyst materials can also be supported on inert metal oxide layer such as AlO_x or HfO_x, which will also serve as suitable barrier to prevent intermixing of catalyst with underlying metal.

[0248] Example 87 provides the method according to Example 85, where the one or more nanotube growth areas initially comprise a material that does not allow nanotube growth, and where the method further may include selectively depositing a catalyst material that allows growth of the nanotubes over the material of the one or more nanotube growth areas prior to growing the nanotubes.

[0249] Example 88 provides the method according to Example 87, where the material that does not allow nanotube growth may include a metal that does not allow nanotube growth, such as e.g. copper or ruthenium, or a metal nitride, such as e.g. titanium nitride.

[0250] Example 89 provides the method according to any one of Examples 87 or 88, where the catalyst material may include one or more of iron, nickel, and cobalt, or an alloy including one or more of iron, nickel, and cobalt.

[0251] Example 90 provides a device including a substrate including a first plurality of openings and a second plurality of openings, where the first plurality of openings are filled with a first material, and the second plurality of openings are filled with nanotubes.

[0252] Example 91 provides the device according to Example 1 where the nanotubes form an electrically conductive material within the second plurality of openings.

[0253] Example 92 provides the device according to Examples 90 or 91, where an aspect ratio (AR) of each opening of the second plurality of openings is between 3 and 100, where the AR is a ratio of a depth of the each opening to a width of the each opening.

[0254] Example 93 provides the device according to any one of Examples 90-92, where the first material may include zirconium oxide, hafnium oxide, titanium oxide, zinc oxide, tantalum oxide, aluminum oxide, silicon oxide, silicon nitride, or carbon doped oxide.

[0255] Example 94 provides the device according to any one of Examples 90-93, where the first material is etch selective with respect to the nanotubes.

[0256] Example 95 provides the device according to any one of Examples 90-94, where the nanotubes comprise carbon nanotubes.

[0257] Example 96 provides the device according to any one of Examples 90-94, where the nanotubes comprise boron nitride nanotubes.

[0258] Example 97 provides the device according to any one of Examples 90-96, where the nanotubes occupy more than 75% of a surface area of a bottom of each of the second plurality of openings.

[0259] Example 98 provides the device according to any one of Examples 90-97, where the nanotubes are disposed over a layer of iron, nickel, manganese, or cobalt, or an alloy thereof.

[0260] Example 99 provides the device according to any one of Examples 90-97, where the nanotubes are disposed over a layer of oxygen containing iron, nickel, manganese, or cobalt.

[0261] Example 100 provides the device according to Examples 98 or 99, where the layer has a thickness between 1 and 5 nanometers.

[0262] Example 101 provides an integrated circuit package, including a component and a device according to any one of Examples 62-75 or any one of Examples 90-100.

[0263] Example 102 provides the integrated circuit package according to Example 101, where the component may include a transistor, a die, a sensor, a processing device, or a memory device.

[0264] Example 103 provides a computing device that includes a substrate and an integrated circuit (IC) die coupled to the substrate, where the IC die includes a semiconductor device having a component and a device according to any one of Examples 62-75 or any one of Examples 90-100.

[0265] Example 104 provides the computing device according to Example 103, where the computing device is a wearable or handheld computing device.

[0266] Example 105 provides the computing device according to Examples 103 or 104, where the computing device further includes one or more communication chips and an antenna.

[0267] Example 106 provides the computing device according to any of Examples 103-105, where the substrate is a motherboard.

[0268] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0269] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. A method for manufacturing a device using nanotubes as a guide for selective deposition, the method comprising:
 - growing nanotubes on one or more nanotube growth areas on a surface of a substrate;
 - after growing the nanotubes, depositing a passivation material over one or more passivation areas on the surface of the substrate to suppress deposition of a first material on the one or more passivation areas; and
 - after depositing the passivation material, depositing the first material over the substrate.
2. The method according to claim 1, wherein the first material forms first structures having an aspect ratio of at least 3.
3. The method according to claim 1, further comprising depositing a second material over the substrate after depositing the first material, wherein the second material is deposited by spin-coating.
4. The method according to claim 3, wherein the second material forms second structures having an aspect ratio of at least 3.
5. The method according to claim 3 or 4, further comprising removing either the first material or the second material to form one or more openings over the substrate.
6. The method according to claim 5, wherein each of the one or more openings has an aspect ratio of at least 3.
7. The method according to any one of claims 1-4, wherein the passivation material comprises a self-assembled monolayer (SAM) material or a hydrophobic polymer.
8. A method for manufacturing a device using densely grown nanotubes as a guide for selective deposition, the method comprising:
 - growing nanotubes over at least 75% of a surface area of one or more nanotube growth areas on a surface of a substrate; and
 - after growing the nanotubes, depositing a first material around the one or more nanotube growth areas.
9. The method according to claim 8, wherein the nanotubes form nanotube structures having an aspect ratio of at least 3.
10. The method according to claims 8 or 9, further comprising removing the nanotubes to form one or more openings over the substrate.
11. The method according to claims 8 or 9, wherein the nanotubes grown over each of the one or more nanotube growth areas form an electrically conductive material.

12. A device comprising:
 - a substrate; and
 - a plurality of structures disposed over the substrate, each structure comprising zirconium oxide, hafnium oxide, titanium oxide, zinc oxide, tantalum oxide, aluminum oxide, silicon oxide, silicon nitride, or carbon doped oxide and having an aspect ratio (AR) between 3 and 100, wherein the AR is a ratio of a height of the each structure to a width of the each structure.
13. The device according to claim 12, wherein the each structure comprises one or more nanotubes enclosed therein.
14. The device according to claim 13, further comprising a filling material disposed between the plurality of structures.
15. The device according to claim 12, wherein the each structure is adjacent to one or more structures comprising nanotubes.
16. The device according to claim 15, wherein the one or more structures comprising nanotubes are electrically conductive.
17. The device according to any one of claims 13-16, wherein the nanotubes are provided on one or more nanotube growth areas and occupy less than 50% of a surface area of the one or more nanotube growth areas.
18. The device according to any one of claims 13-16, wherein the nanotubes are provided on one or more nanotube growth areas and occupy more than 75% of a surface area of the one or more nanotube growth areas.
19. The device according to claim 12, wherein the each structure further includes a layer of iron, nickel, manganese, or cobalt, or an alloy thereof, in a portion of the structure closest to the substrate.
20. The device according to claim 19, wherein the each structure further includes a layer of oxygen containing iron, nickel, manganese, or cobalt in a portion of the structure closest to the substrate.
21. The device according to claims 19 or 20, wherein the layer has a thickness between 1 and 5 nanometers.
22. A method for manufacturing a device using nanotubes, the method comprising:
 - depositing a first material in one or more first openings provided in a substrate; and
 - growing nanotubes in one or more second openings provided in the substrate, wherein the first material is a material having different etch properties from the nanotubes.
23. The method according to claim 22, further comprising:

providing a layer of an interlayer dielectric (ILD) material over the substrate with the first material and the nanotubes;

forming a via opening in the layer of the ILD material, the via opening exposing at least a portion of one opening of the one or more first openings filled with the first material and at least a portion of one opening of the one or more second openings filled with the nanotubes;

forming an extended via opening by removing either the first material from the one opening of the one or more first openings or the nanotubes from the one opening of the one or more second openings; and

filling the extended via opening with a second material.

24. The method according to claims 22 or 23, wherein the one or more first openings and the one or more second openings are provided in the substrate in an alternating manner.

25. The method according to claims 22 or 23, wherein the nanotubes grown in the one or more second openings occupy at least 75% of a volume of the one or more second openings.

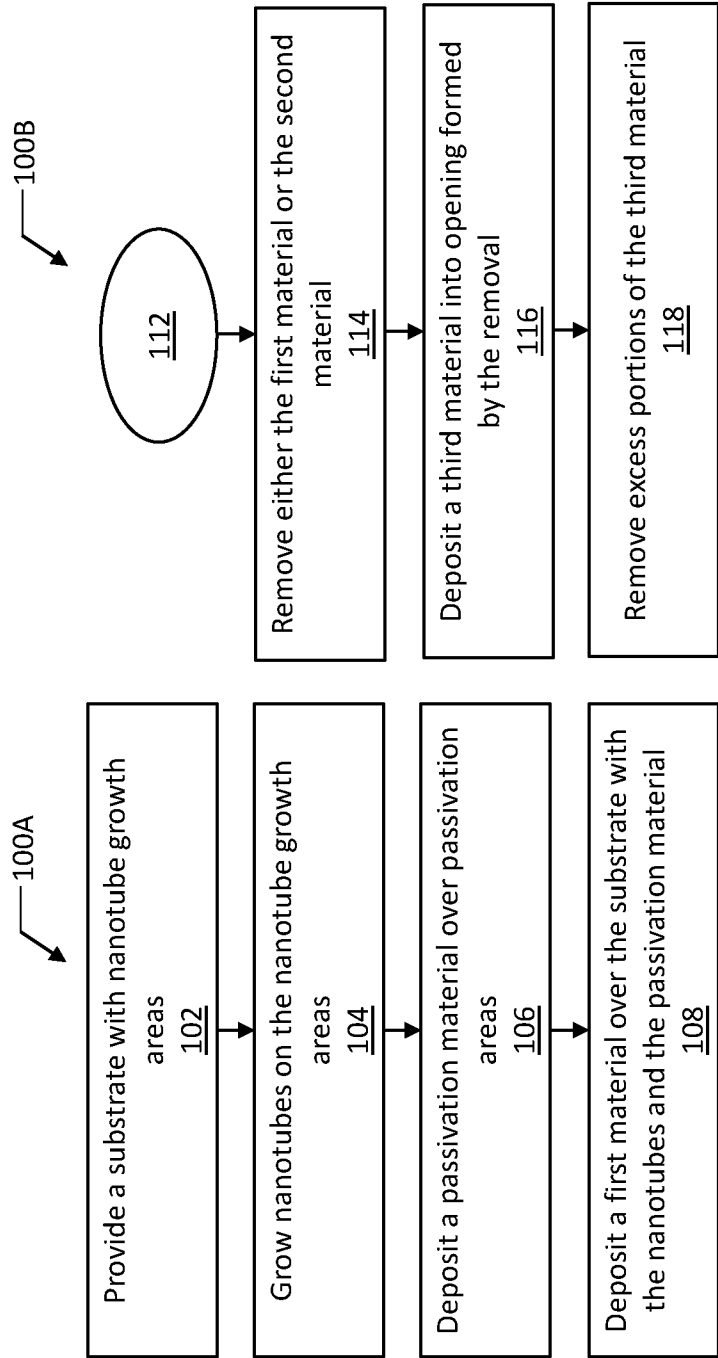


FIG. 1B

FIG. 1A

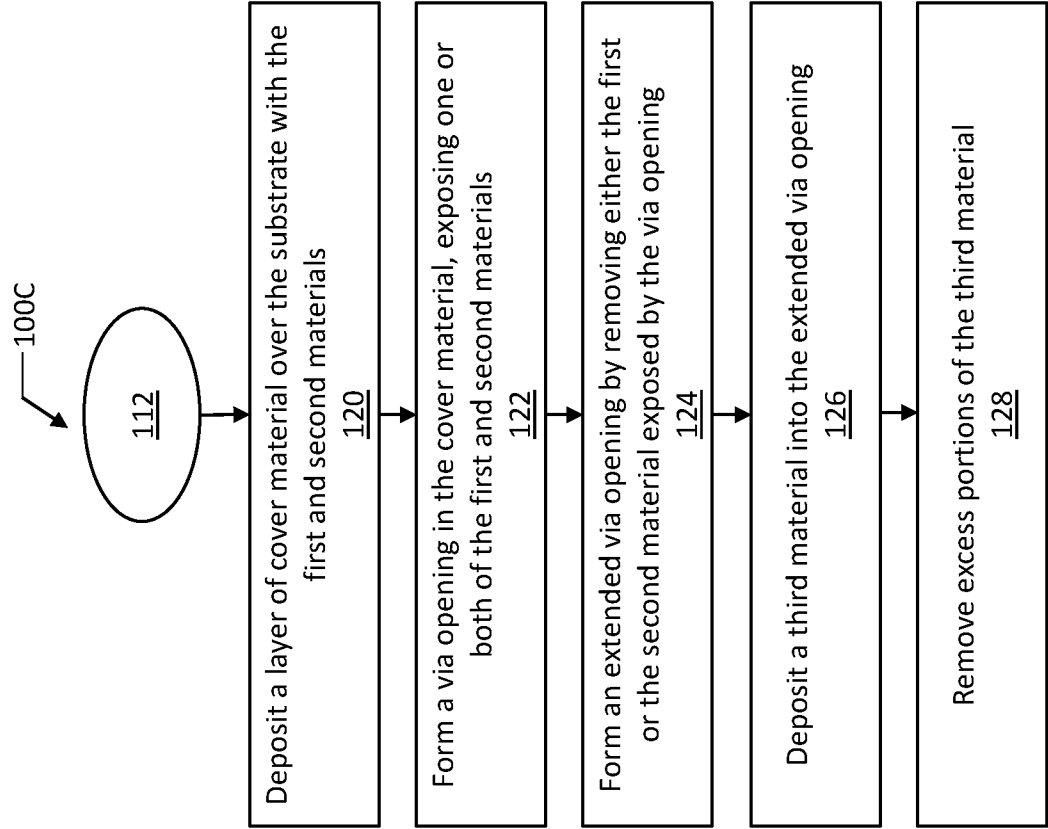


FIG. 1C



FIG. 2

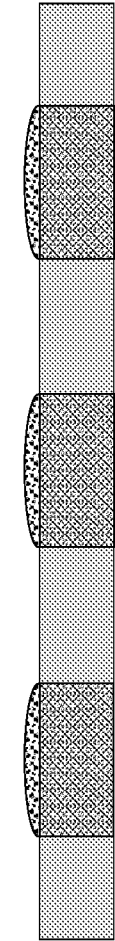


FIG. 3

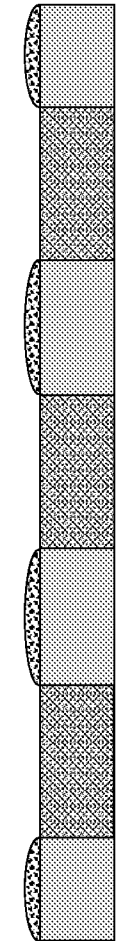


FIG. 4

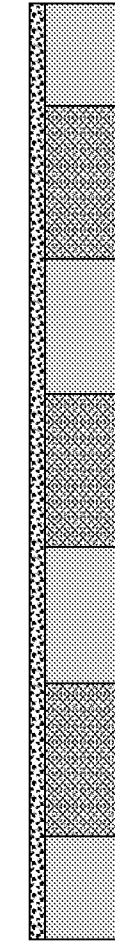


FIG. 5



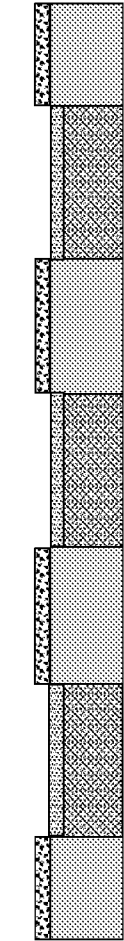


FIG. 6

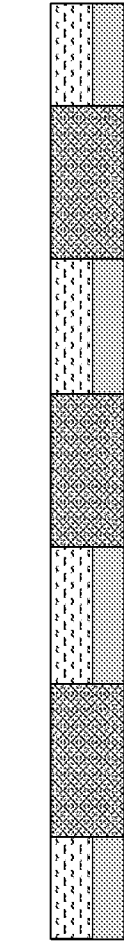


FIG. 7

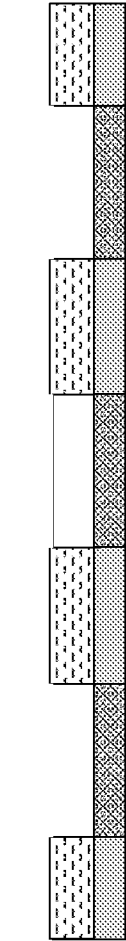


FIG. 8

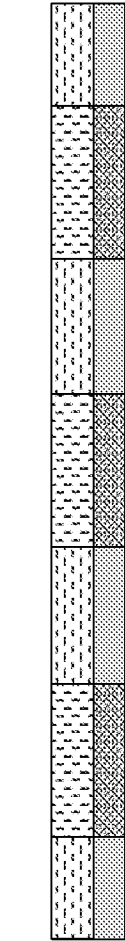
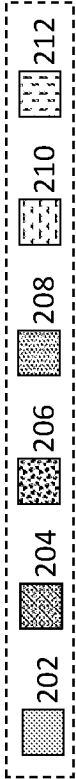


FIG. 9



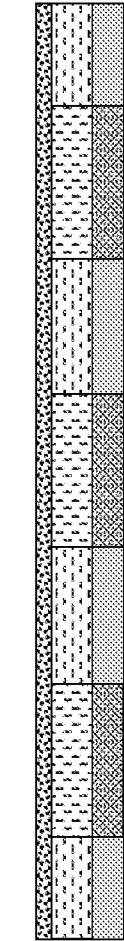


FIG. 10

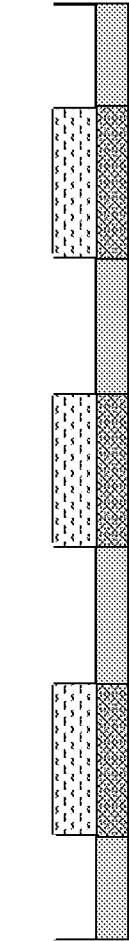


FIG. 11

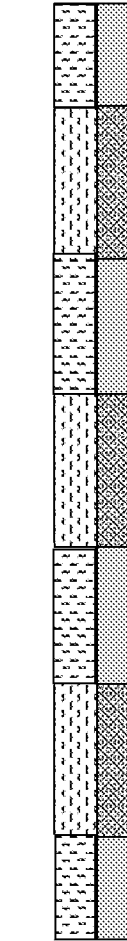


FIG. 12

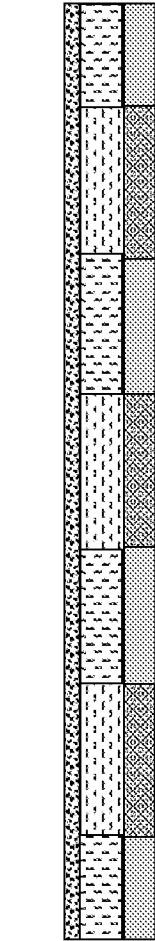
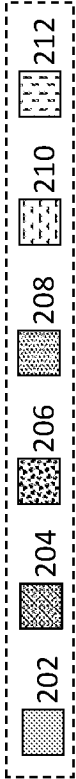


FIG. 13



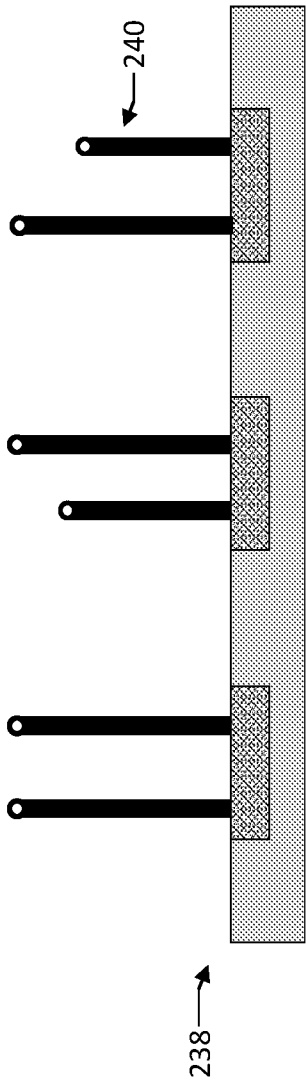


FIG. 14

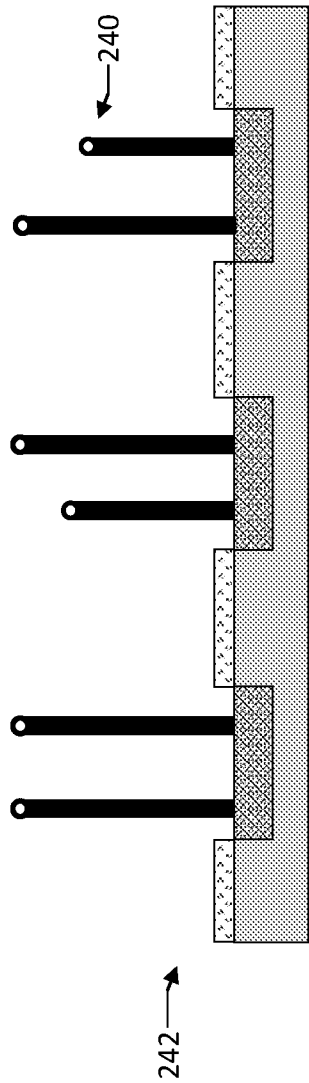
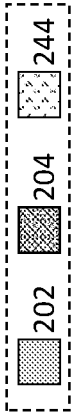


FIG. 15



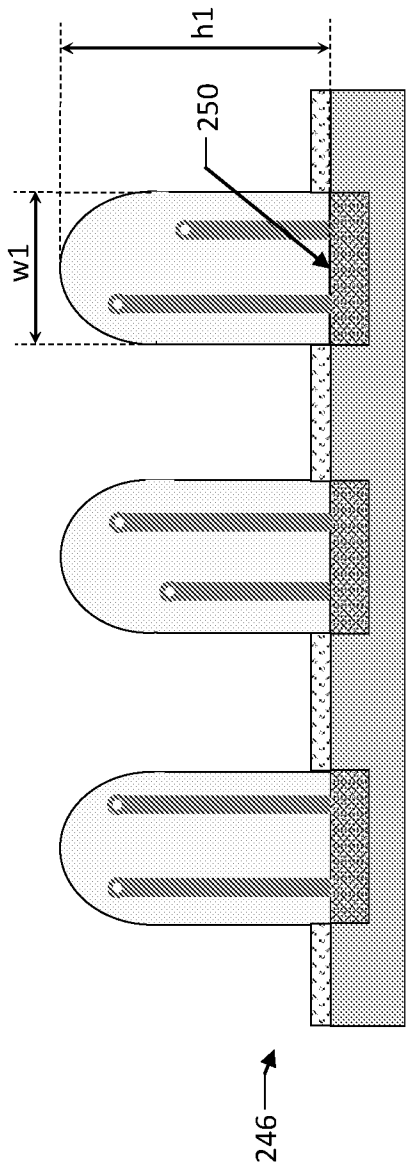


FIG. 16

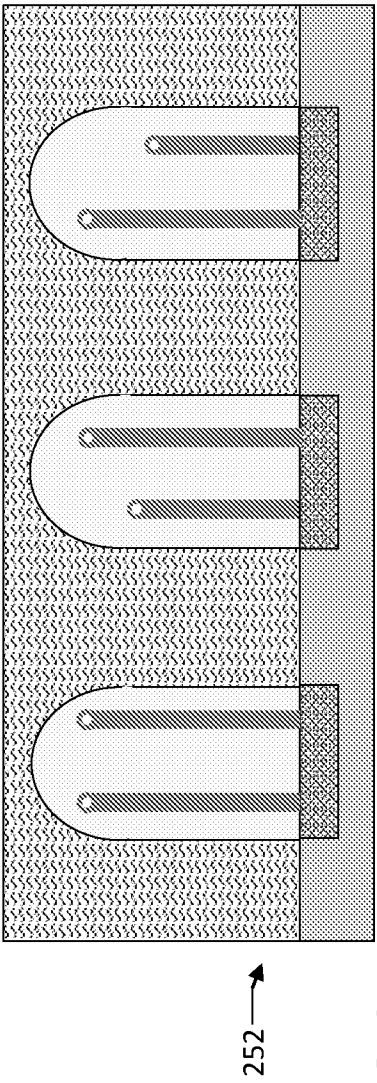
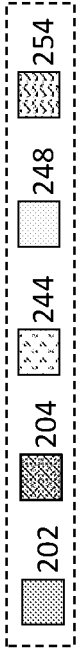


FIG. 17



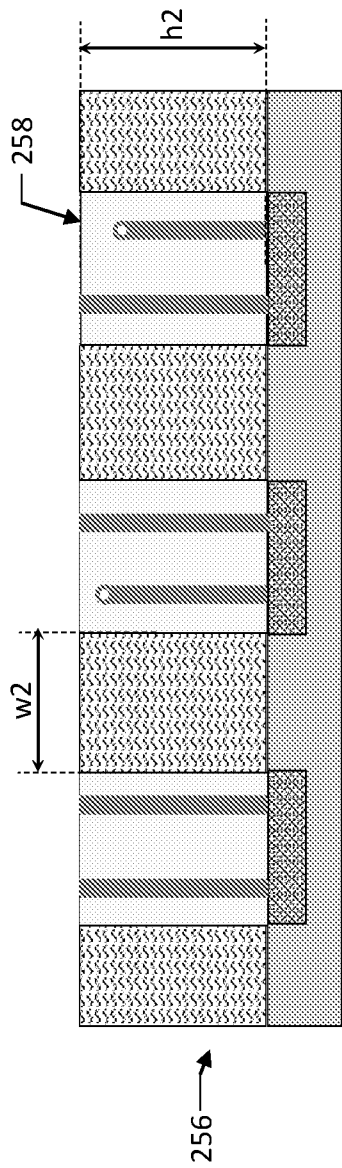


FIG. 18

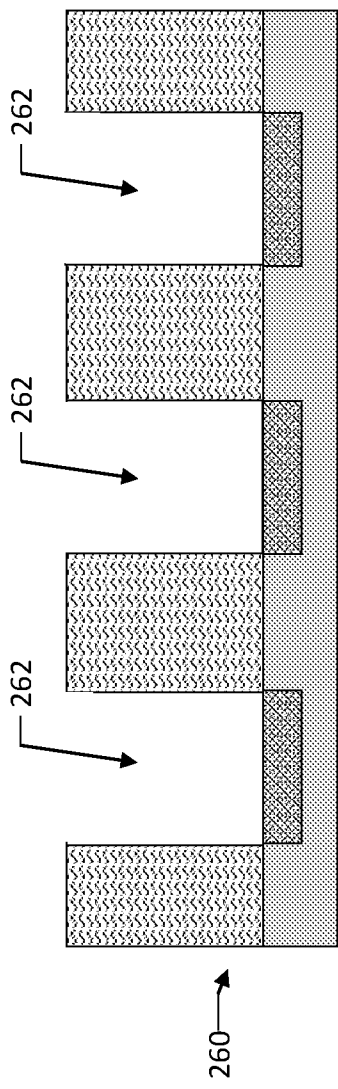
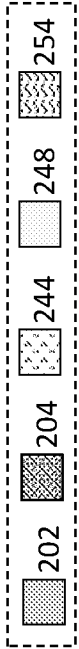


FIG. 19



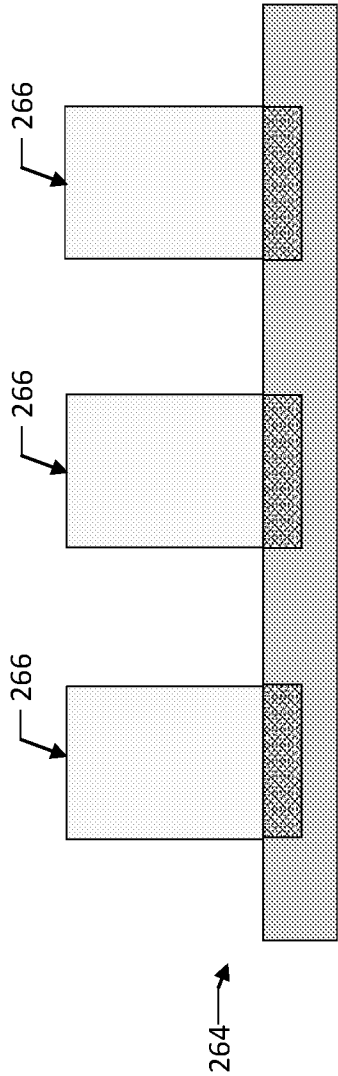


FIG. 20

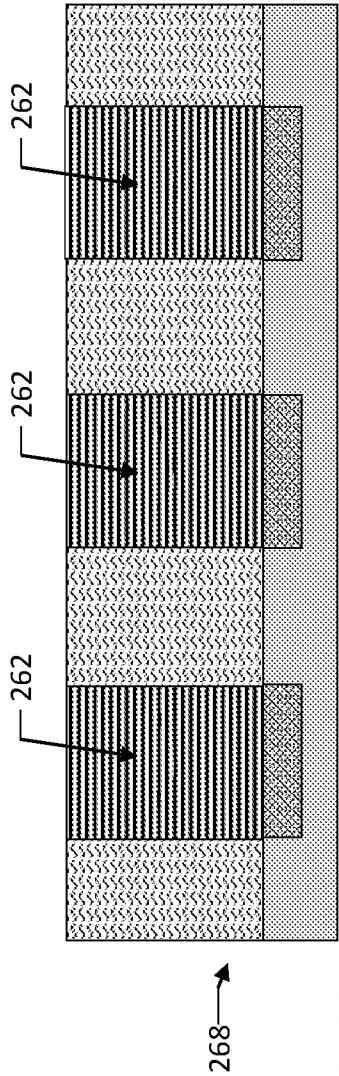
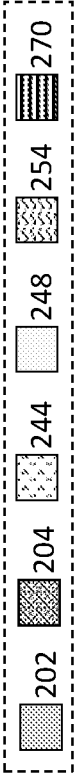
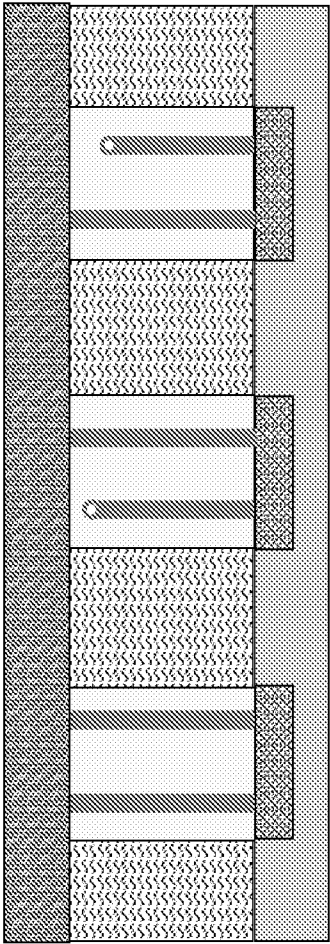


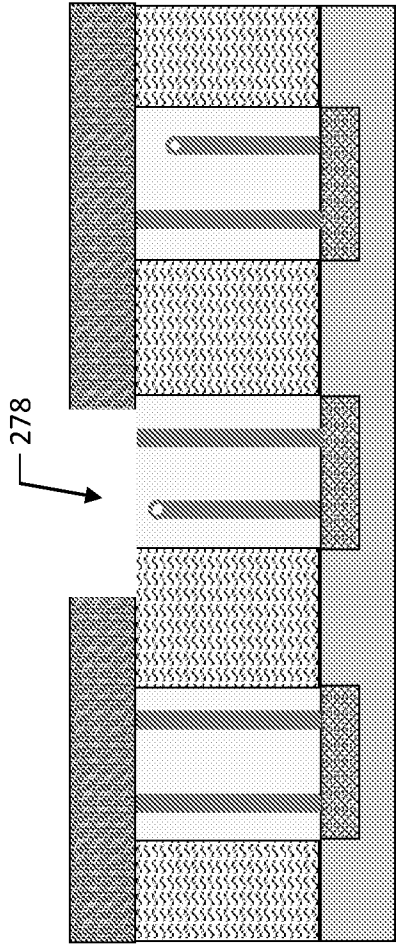
FIG. 21





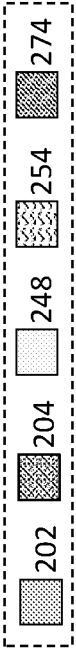
272

FIG. 22



276

FIG. 23



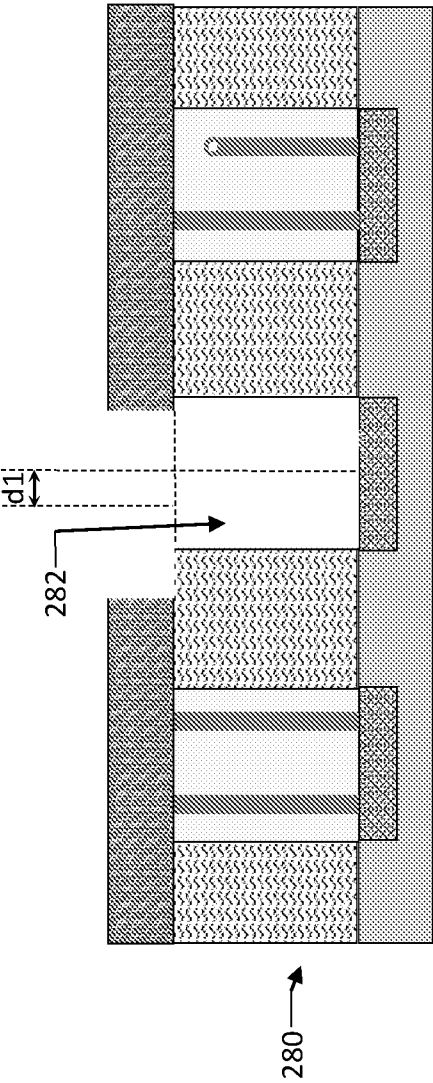


FIG. 24

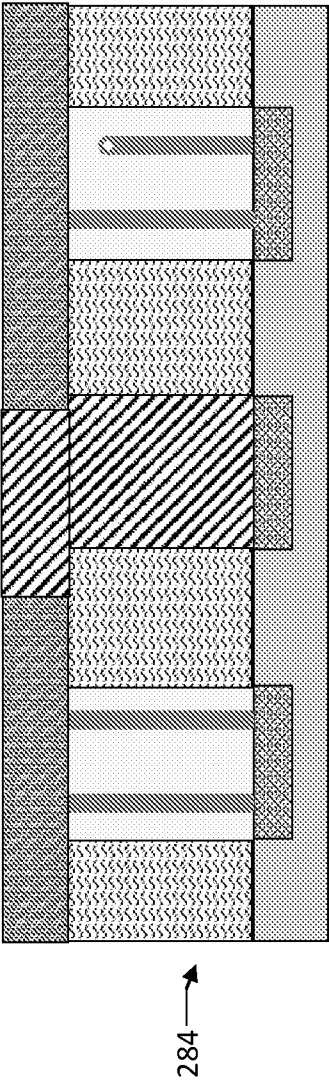
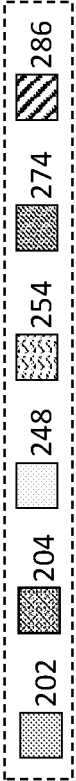


FIG. 25



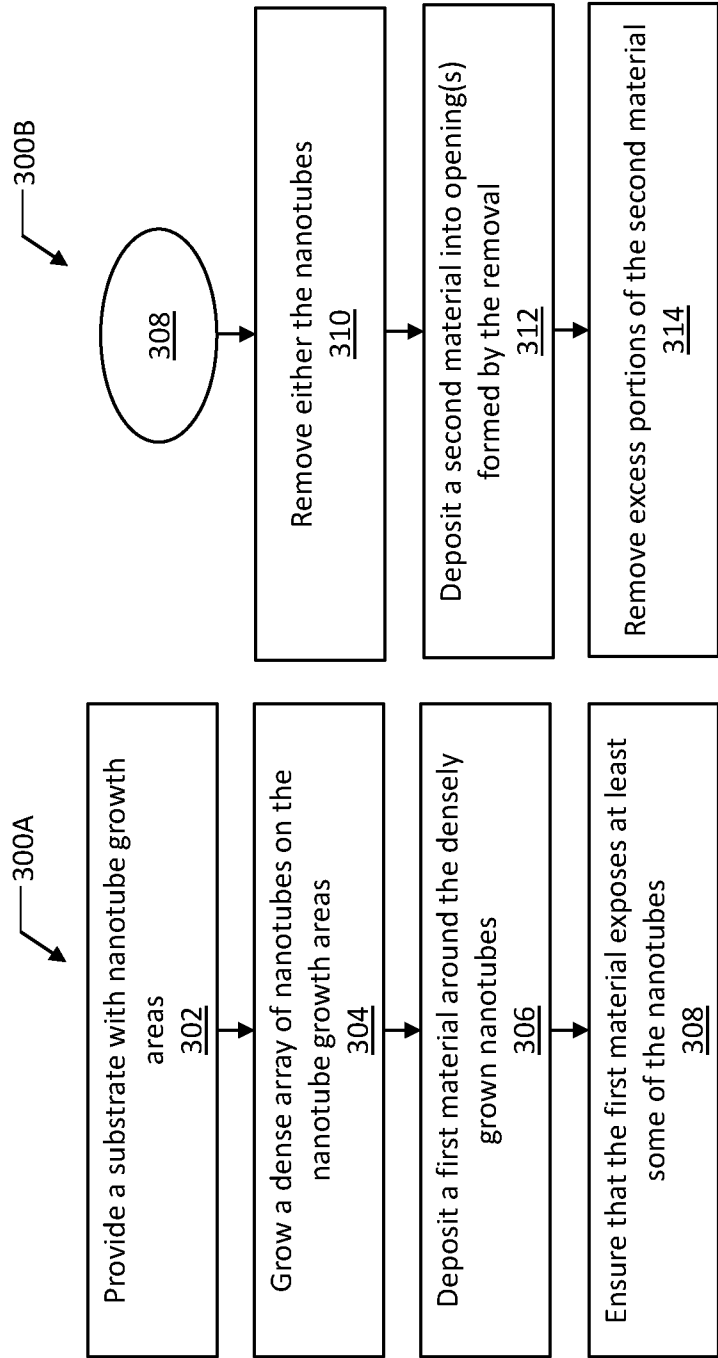


FIG. 26B

FIG. 26A

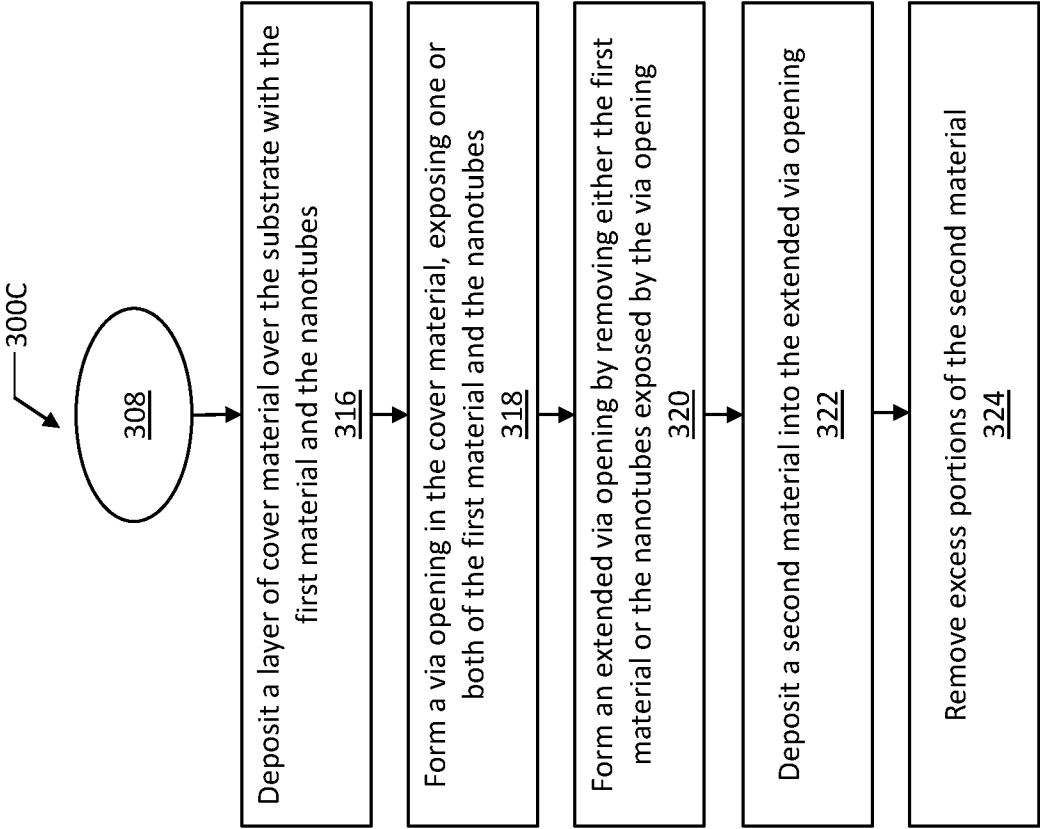
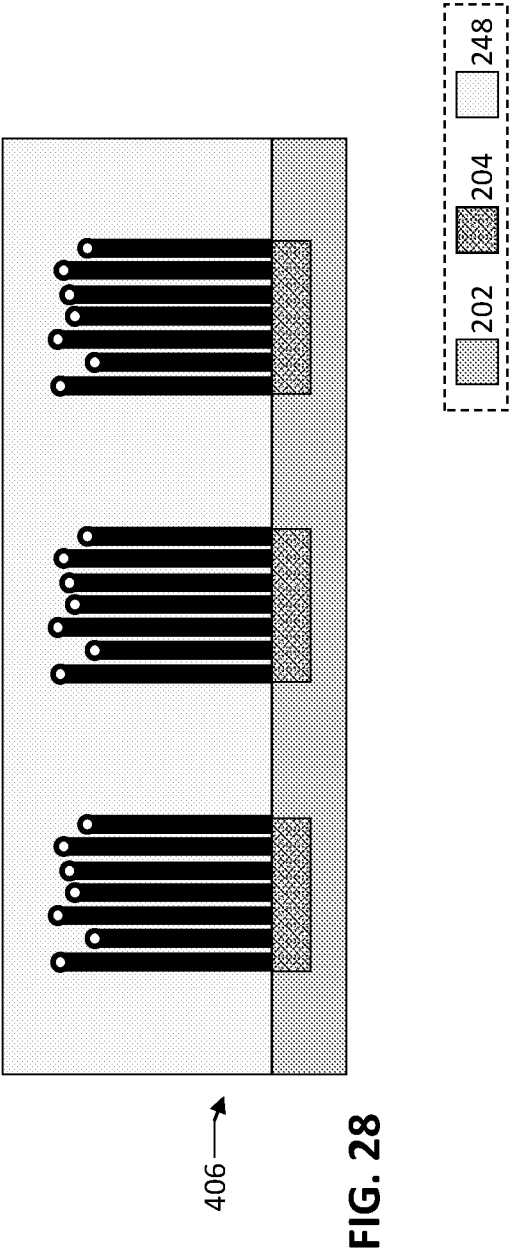
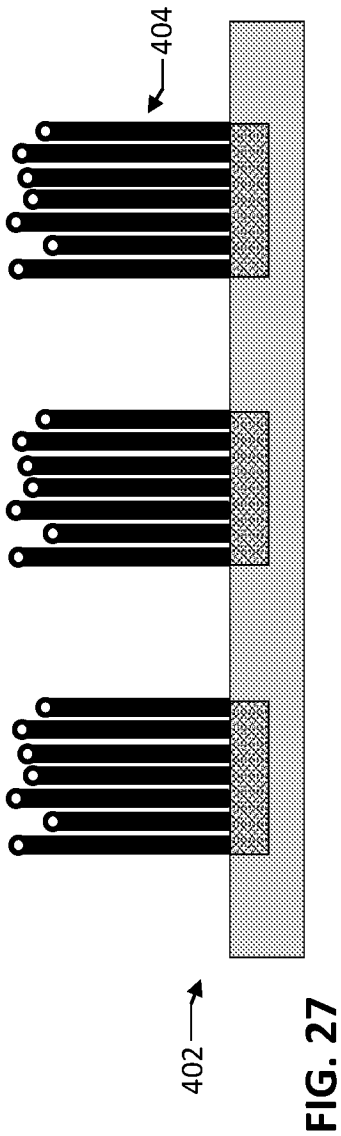


FIG. 26C



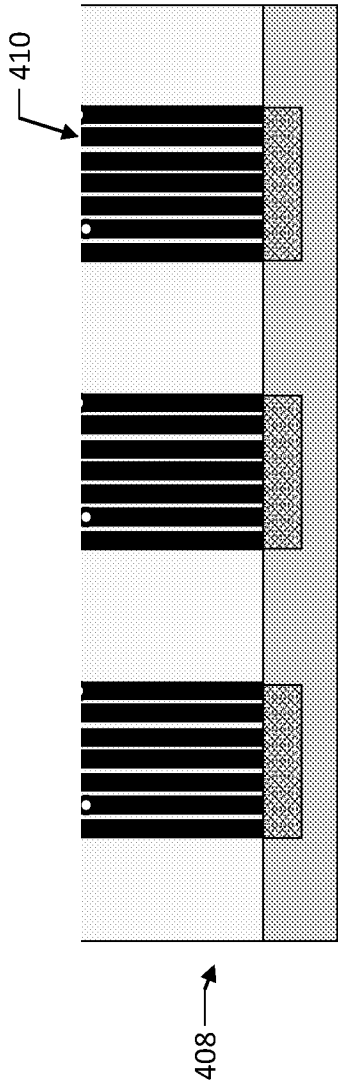


FIG. 29

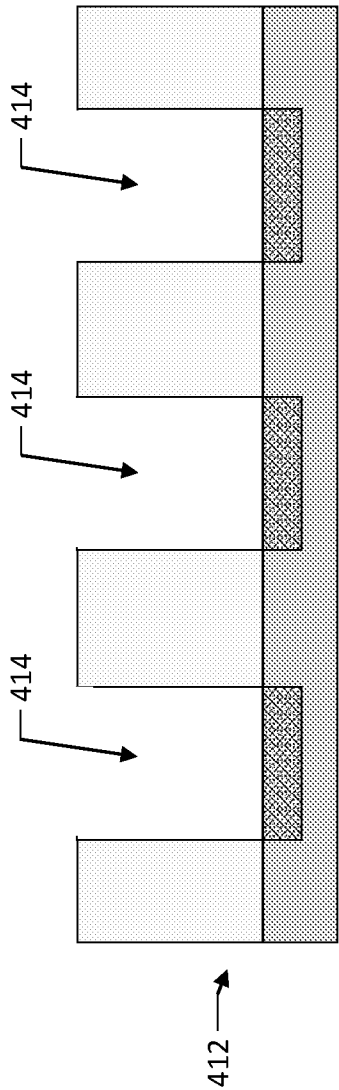
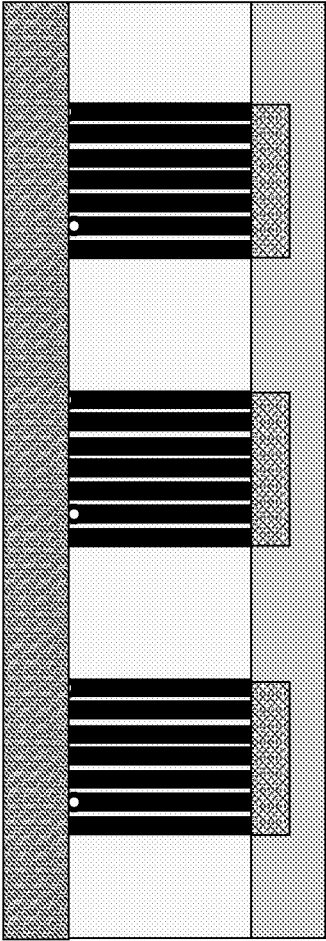


FIG. 30



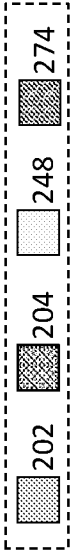
416 →

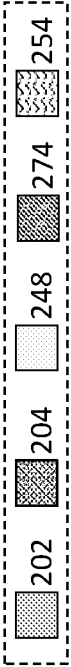
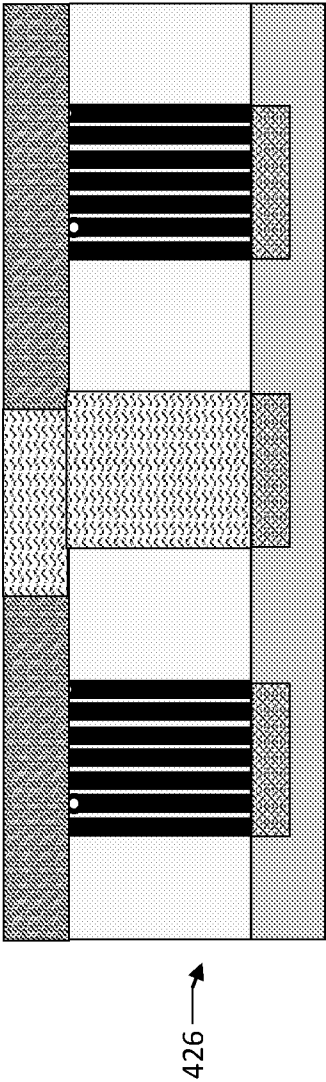
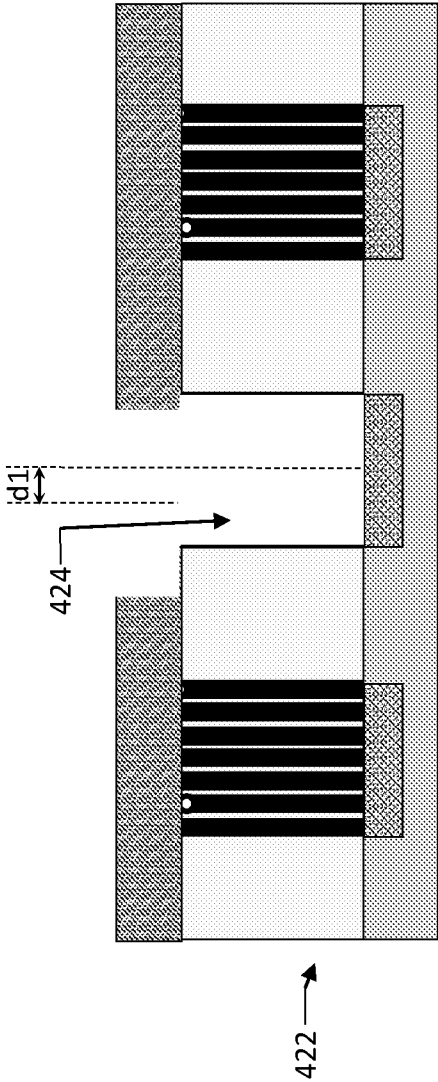
FIG. 31



418 →

FIG. 32





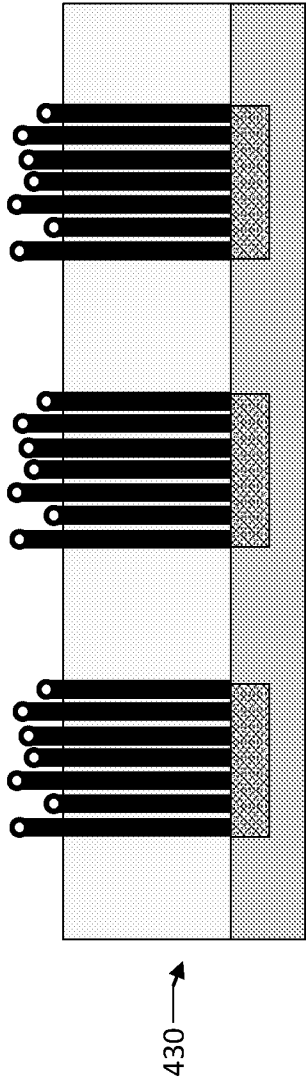


FIG. 35

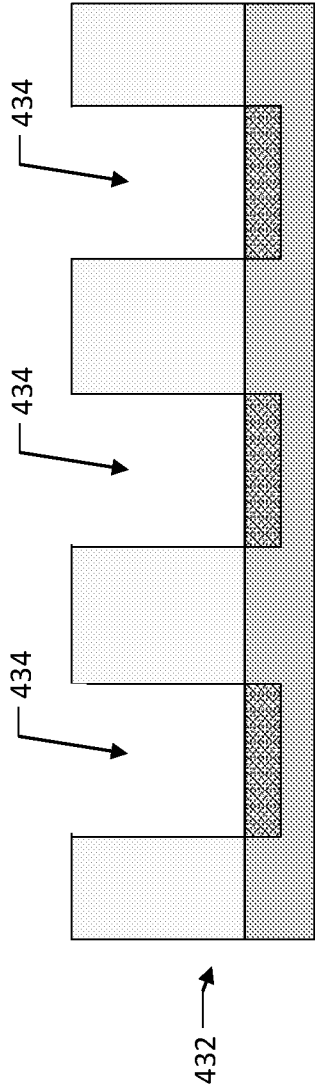


FIG. 36



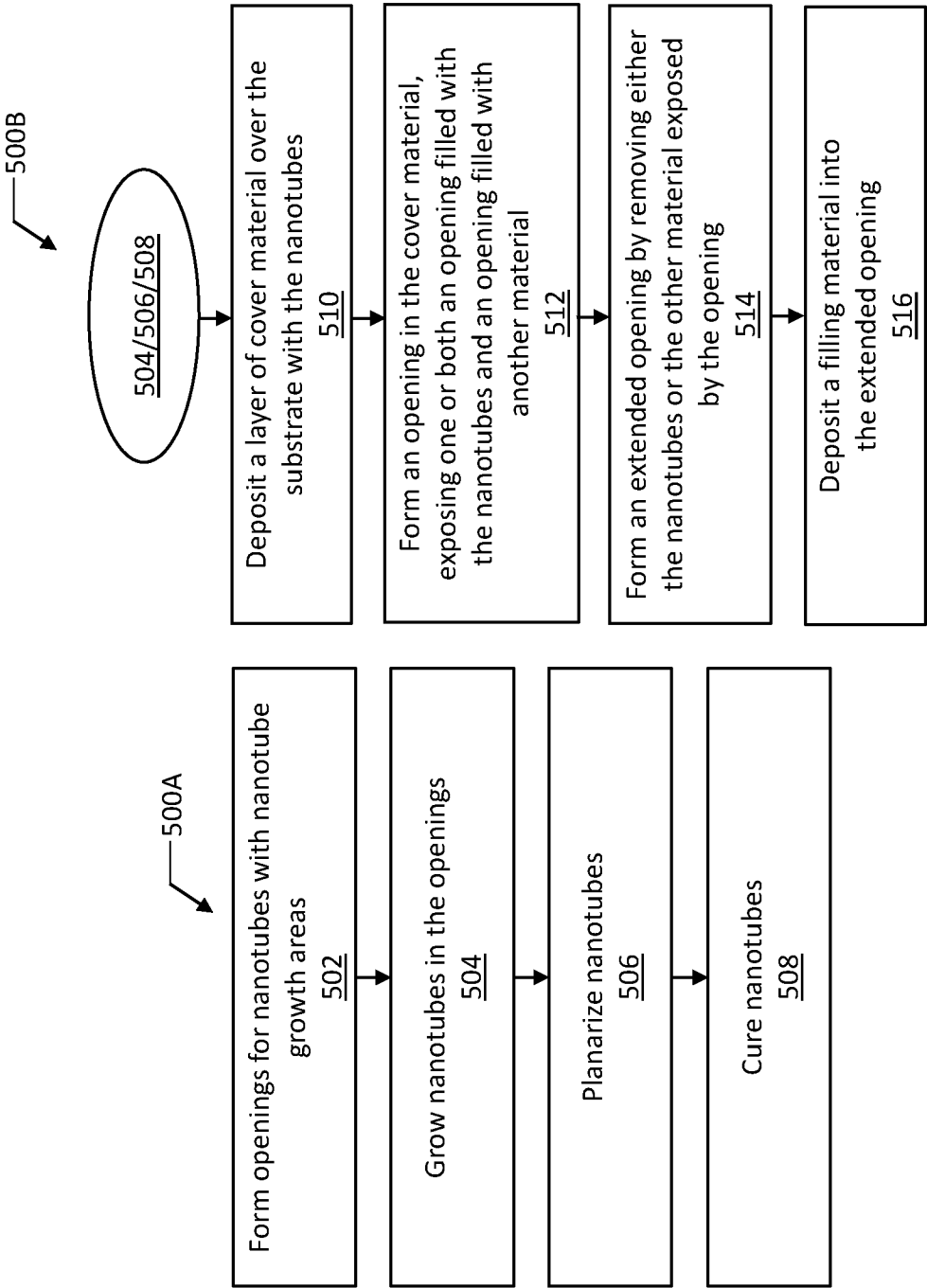


FIG. 37A

FIG. 37B

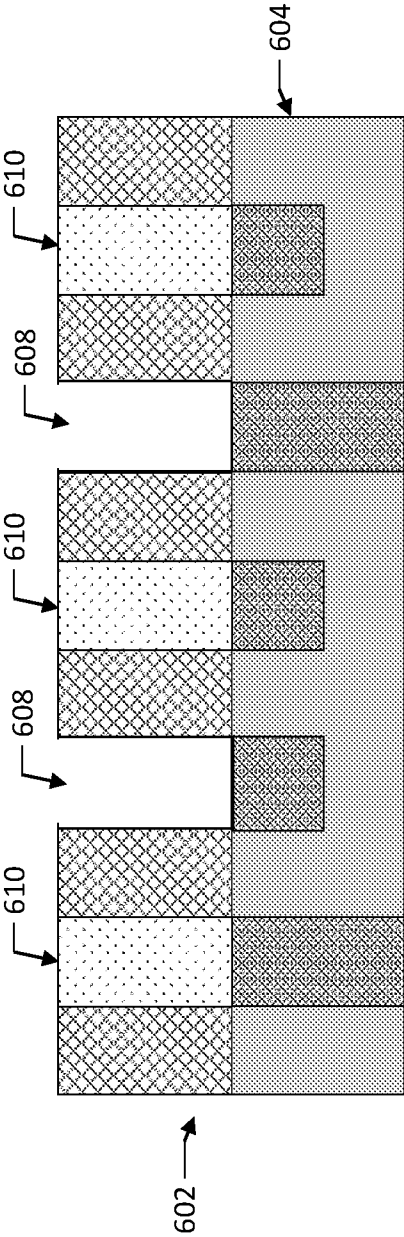


FIG. 38

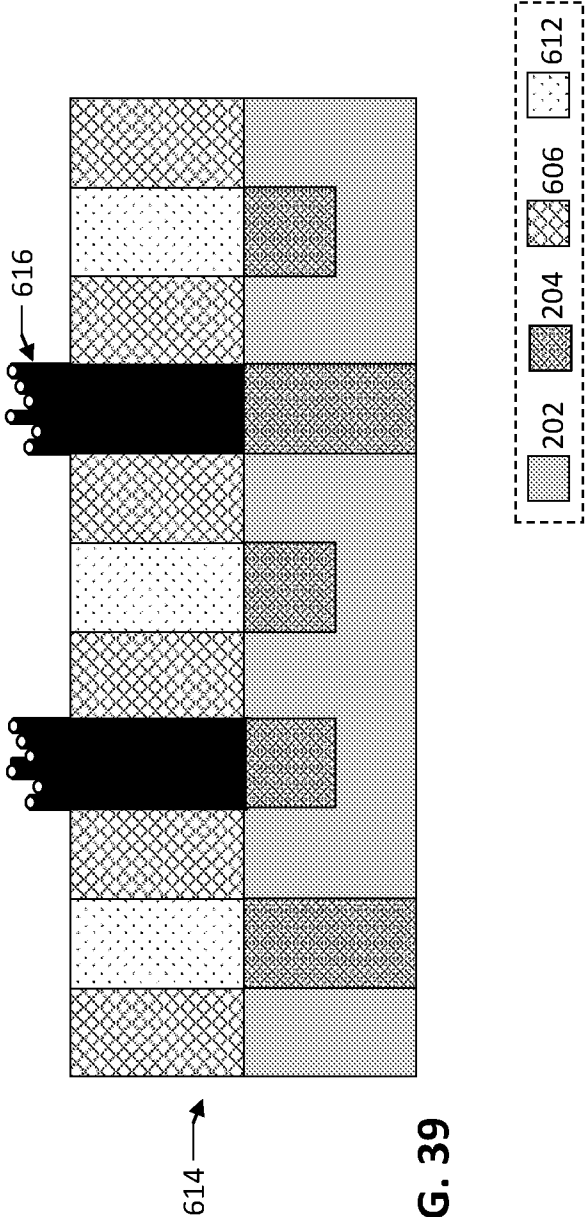


FIG. 39

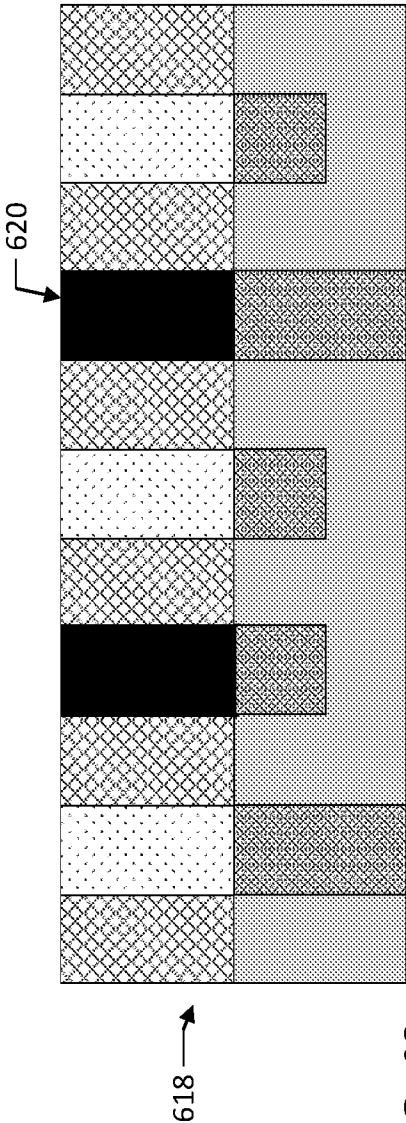


FIG. 40

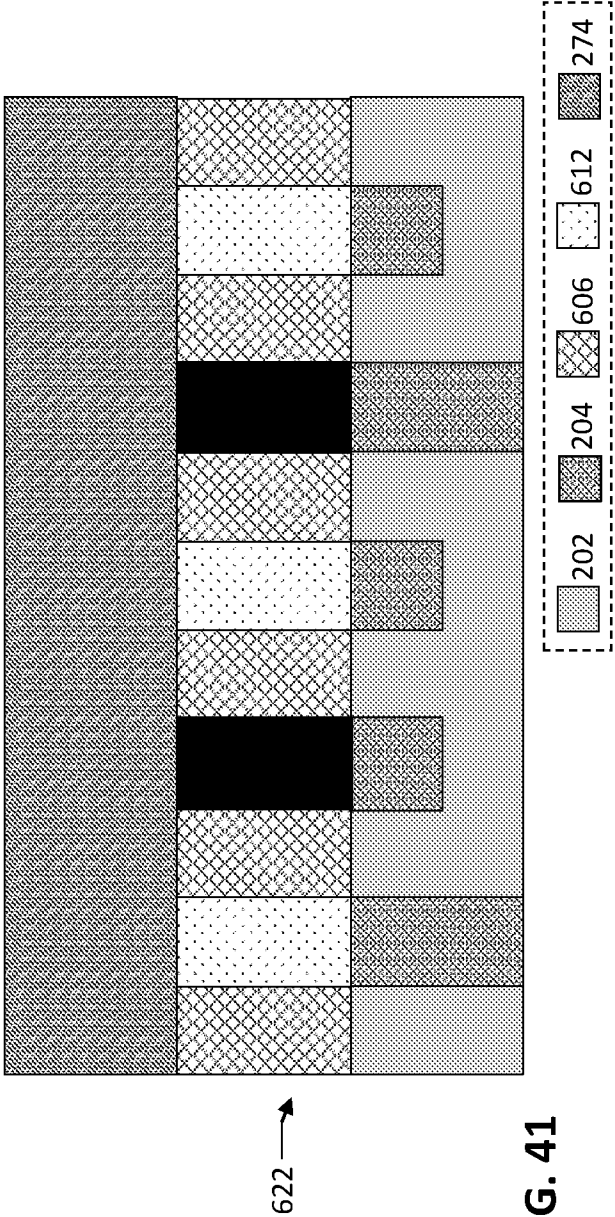
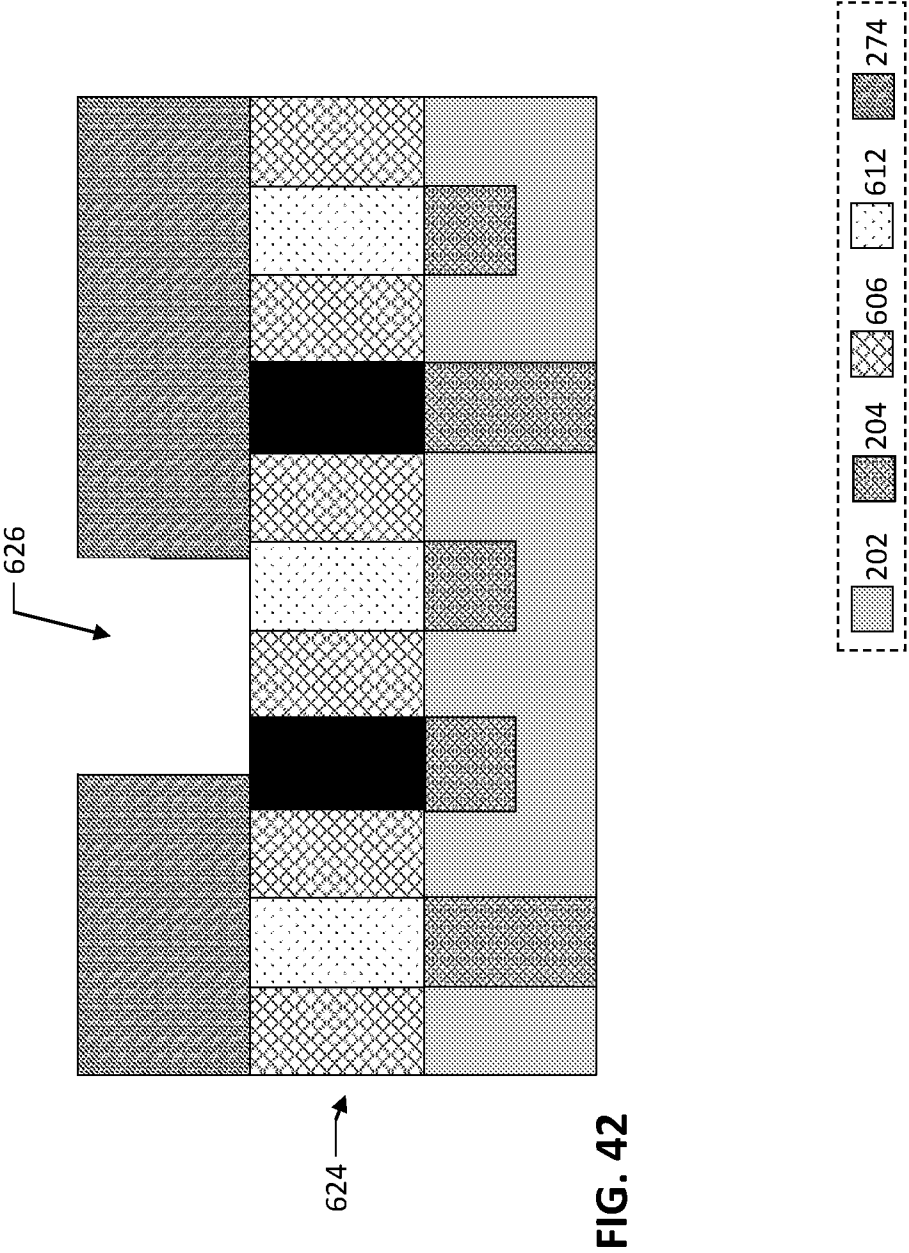
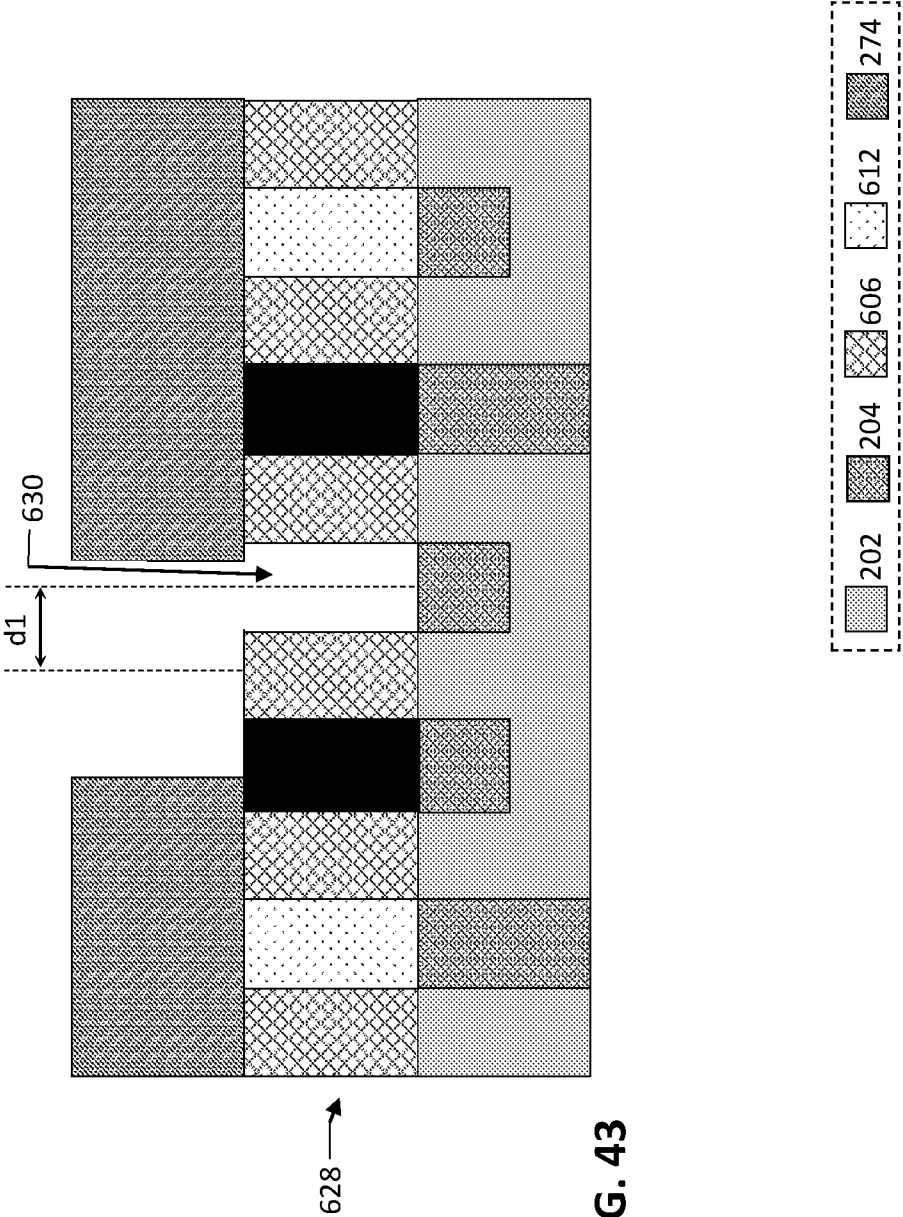
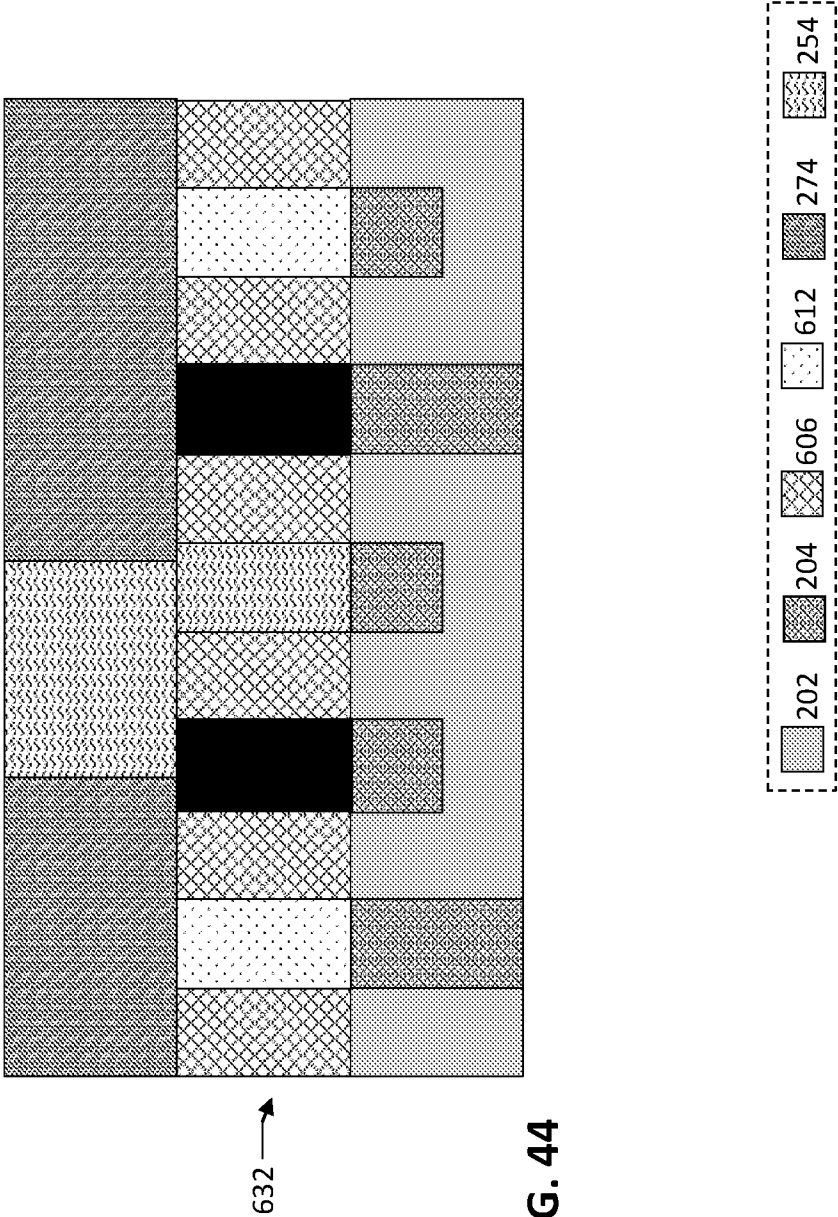


FIG. 41







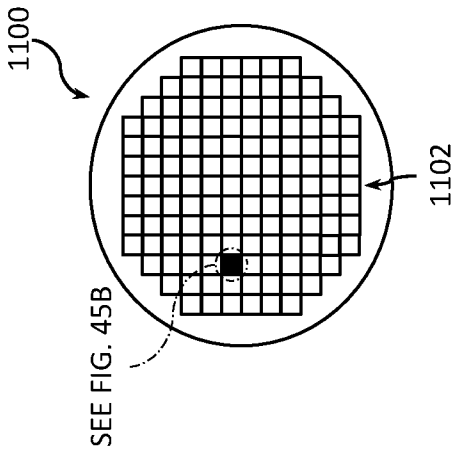


FIG. 45A

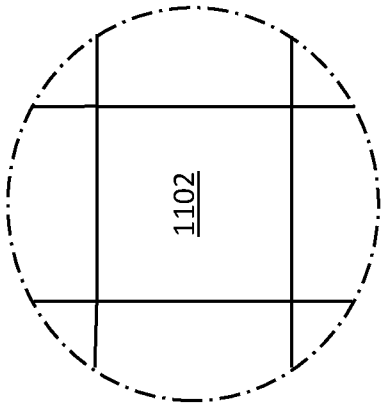


FIG. 45B

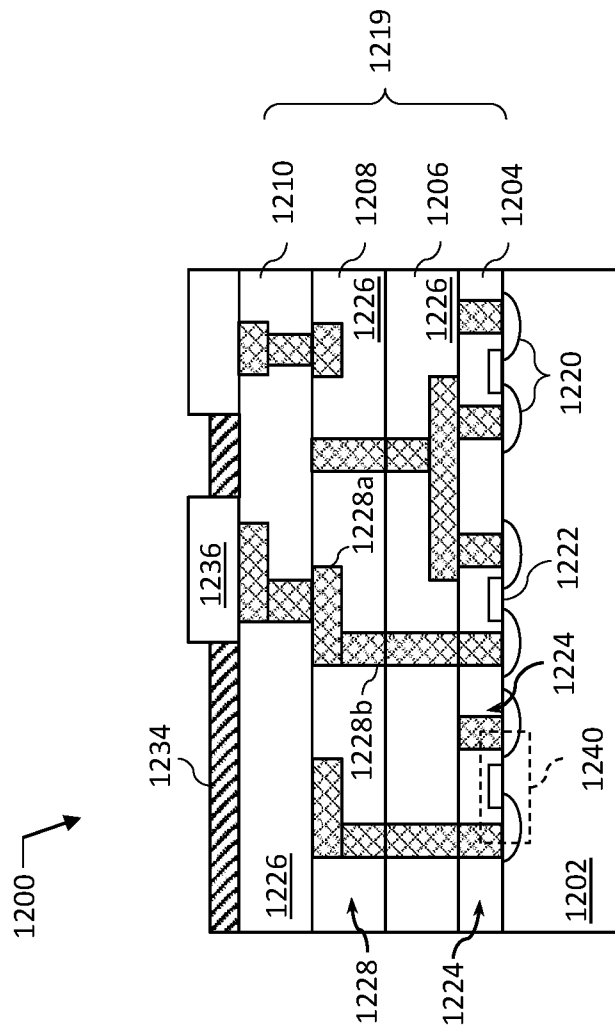


FIG. 46

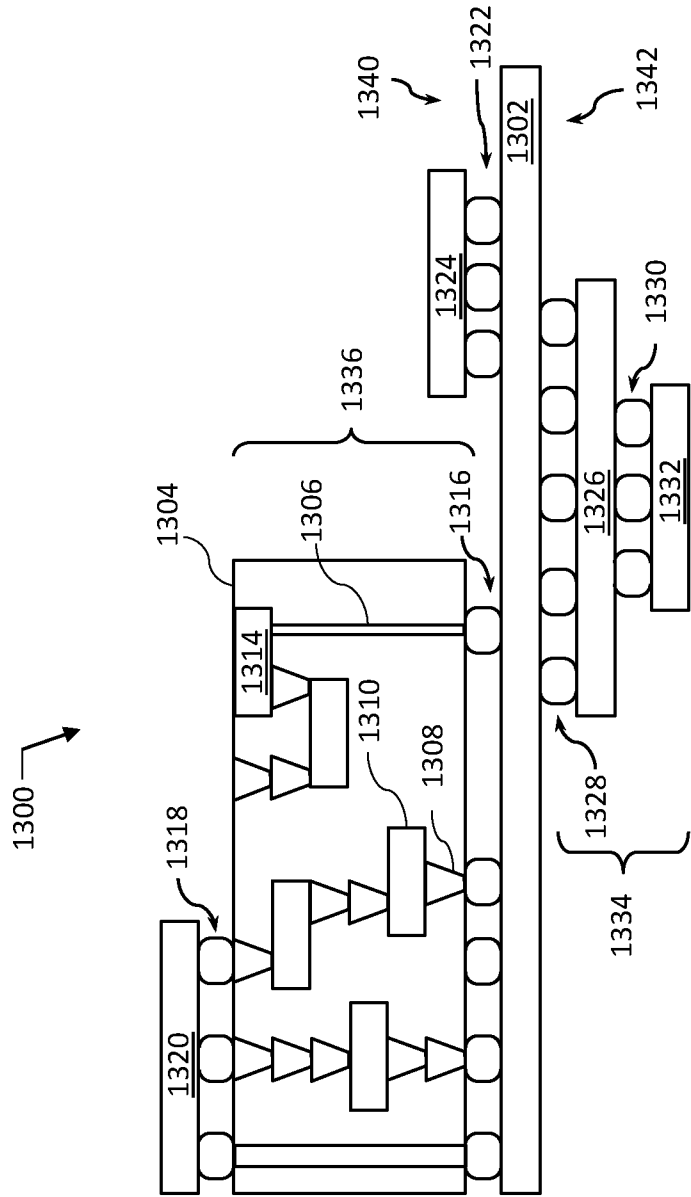


FIG. 47

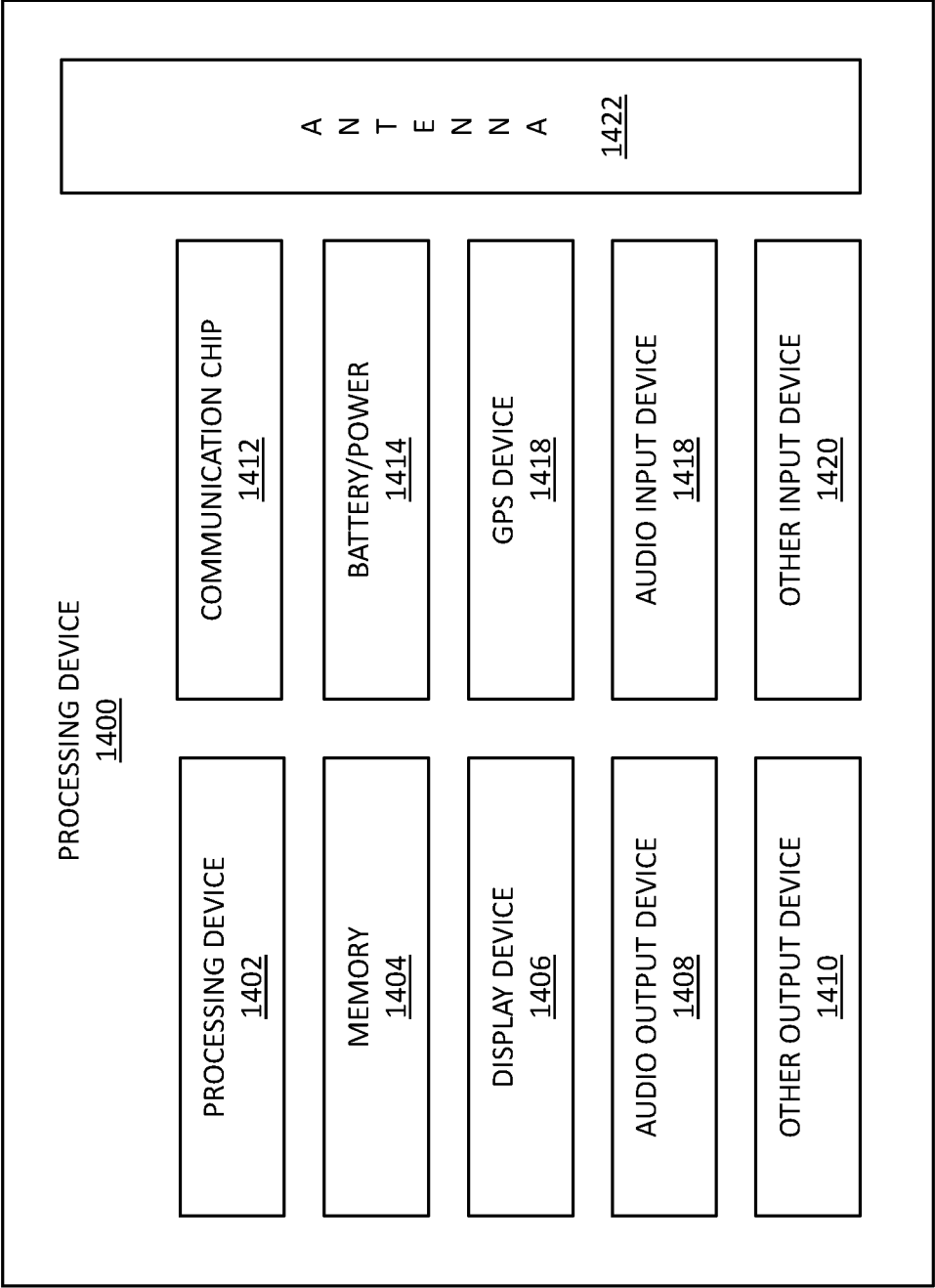


FIG. 48

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/02(2006.01)i, H01L 29/06(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/02; H01L 23/528; H01L 21/28; H01L 51/40; H01L 29/06; H01L 27/04; H01L 21/00; H01J 1/304

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: nanotube, patterning, passivation, aspect ratio, opening, deposition

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0214144 A1 (INFINEON TECHNOLOGIES AG) 30 July 2015 See paragraphs [0011]–[0031] and figures 1A–4.	8–21
A		1–7, 22–25
A	US 8492293 B1 (ALI AFZALI–ARDAKANI et al.) 23 July 2013 See the whole document.	1–25
A	US 2005-0167655 A1 (TOSHIHARU FURUKAWA et al.) 04 August 2005 See paragraphs [0023]–[0033] and figures 1–6.	1–25
A	KR 10-0663076 B1 (KOREA ADVANCED INSTITUTE OF SCIENCE AND TECHNOLOGY) 02 January 2007 See the whole document.	1–25
A	US 9058954 B2 (GEORGIA TECH RESEARCH CORPORATION) 16 June 2015 See column 5, line 1 - column 11, line 67 and figures 1–9.	1–25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 September 2017 (22.09.2017)

Date of mailing of the international search report

22 September 2017 (22.09.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/069069

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015-0214144 A1	30/07/2015	CN 104821291 A US 2015-0311157 A1 US 2015-0371942 A1 US 9159669 B2 US 9704800 B2	05/08/2015 29/10/2015 24/12/2015 13/10/2015 11/07/2017
US 8492293 B1	23/07/2013	US 8394727 B1	12/03/2013
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