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(54) IMPROVEMENTS IN OR RELATING TO MOS MULTI-STAGE LOGIC CIRCUITS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, German Federal Republic, do hereby declare the inention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The inention relates to MOS multi-stage logic circuits of itnegrated circuit form, with gates provided for the production and transmission of carry signals between stages.

One known design of logic-linking circuits for binary signal transmission using integrated circuits made by the use of MOS techniques consists in the use of static gates, in which one MOS transistor is connected as load resistor in series with at least one MOS switching transistor. The point of connection of a load transistor and the or each switching transistor represents the output of a stage. The control electrodes of the switching transistors represent the inputs of that stage. Whenever a current path formed by a switching transistor is switched to its conductive state, d.c. current flows through the entire stage, i.e. a stage of this kind can consume power in the rest state. In the case of multi-stage, logic circuit arrangements which execute logic or arithmetic operations with carry signals which are thereby formed (for example in the addition of multi-bit words), then if gate stages of this kind are employed for feeding on the carry signals, the power loss becomes considerable.

Furthermore, in order to be able to safeguard against any mulfunction due to interference, a specific minimum change in signal levels must be available at the output of such gate stages. This signal level change is determined by the conductivity ratio of the one or more switching transistors to the associated load transistor, which conductivity ratio is itself governed by the characteristic transistor values, namely the channel length and the channel width. Therefore gates of this kind are also referred to as ratio gates. In order that the availabie signal change is great, this ratio of channel width to channel length must be selected to be high for the MOS transistor that is connected as a load resistor. Consequently, there is a limited freedom of dimensioning for static ratio gates. This is a particularly disadvantageous aspect, in respect of the switching times of such gates. If the output resistance is high as a result of the above mentioned dimensioning limitation regarding the signal change, the time constants determined by the output impedance of a preceding stage and the capacitive input impedance of the following stage are also high, as a result of which the switching times are of a corresponding length.

In order to avoid the above mentioned disadvantage in ratio gates, ratio-less, dynamic gates have been proposed, but with such ratio-less, dynamic gates, the advantage of a low d.c. power loss is only acquired at the cost of greater circuit complexity, on account of the requisite control pulse trains.

It is known that MOS transistors possess a symmetrical switching behaviour, i.e. they can have their controlled path between source and drain connected directly into a signal-conducting arm, where a signal transfer is possible in both directions as a function of control signals connected to the control electrode, i.e. the gate electrode.

One object of the present invention is to provide a substantially d.c.-free transmission of carry signals in logic circuit arrangements, in which static switching behaviour is adopted to avoid the use of dynamic, ratio-less gates.

According to this invention there is provided a MOS multi-stage logic circuit in the form of an integrated circuit with gates for the production and transmission of carry signals between its stages, the logic circuit being in the form of a synchronous binary counter each counting stage of which has a bistable trigger stage, a carry signal input for a carry signal from the counting stage for the relevant lower valued counting position if any, and a carry signal output which is coupled to the

carry signal of the counting stage for the relevant high-valued counting position if any, wherein each counting stage is provided with a respective transfer gate having two branches, first and second transfer transistors being connected in series with the carry signal input in each said branch, the control electrode of each said first transistor being connected to the control electrode of the second transistor in the other branch, the control electrodes of the transfer transistors whose conductive path is directly connected to the associated carry signal input being coupled respectively to the complementary outputs of that stage's bistable trigger stage, the connection point of the controlled paths of the first and second transfer transistors in each branch being coupled to a respective timing signal input of the bistable trigger stage and the connection point of the controlled paths of the first and second transfer transistors in one of said branches providing an output carry signal of that stage.

Embodiments of this invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a circuit diagram of an embodiment of a synchronous binary counter constructed in accordance with the invention;

Figure 2 is a circuit diagram of an embodiment of a forwards-backwards synchronous binary counter constructed in accordance with the invention; and

Figure 3 is a circuit diagram of an embodiment of a decadic counter constructed in accordance with this invention.

Figure 1 illustrates an exemplary embodiment of a stage of a multi-stage, logic circuit constructed in accordance with the invention, for use as a synchronous binary counter. A synchronous binary counter of this kind firstly contains, in known manner, one bistable trigger stage 22 or 23 etc., for each counting stage. In respect of each trigger stage there are provided two cross-coupled gates 30 and 31, which combine an AND- and NOR-function. These gates are fed via a common input 32, with pulses which are to be counted, and also via an inverter 33 connected thereto, so that all the trigger stages of the counter are fed with the pulses which are to be counted both directly or via the inverter 33. In any stage, the outputs of the gates 30 and 31 simultaneously constitutes the relevant outputs $\overline{Q_n}$ and Q_n of that stage, and of outputs $\overline{Q_{n+1}}$, etc. of the subsequent counter stages. At inputs T_{n-1}, T_n, T_{n+1}, etc., a carry signal is fed in from the relevant preceding stage. For the transfer of these carry signals, a transfer gate is provided which possesses two branches, in each of which two transfer transistors T_{20} and T_{23}, or T_{22} and T_{21} are respectively connected in series to the associated carry signal input (for example T_{n-1}). The control electrodes of these transfer transistors are mutually cross-coupled, and the control electrodes of those transfer transistors T_{20} and T_{22} which are directly connected to the associated carry signal input are connected to an output of the associated bistable trigger stage (for example $\overline{Q_n}$ and Q_n of the trigger stage 22). The intermediate connection points of the controlled paths series-connected transfer transistors T_{20} and T_{23} or T_{21} and T_{22} are each connected with a controlled path of a respective further transfer transistor T_{24} or T_{25}, to the respective input of the AND-function of the associated gates 30 and 31, the gate control electrodes of the transfer transistors T_{24} and T_{25} being fed by the inverted pulses which are to be counted, from the input 32. Respective capacitances C_1 and C_2 which are connected to earth from these inputs, serve in known manner as pre-storage capacitances for the output switching states to be assumed by the bistable trigger stages 22, 23 etc.

The mode of operation of a synchronous binary counter of this kind will now be explained on the basis of a starting counting state in which a logic "0" is present at all the outputs Q_n, Q_{n+1} etc., and a logic "1" is present at all the outputs $\overline{Q_n}$, $\overline{Q_{n+1}}$, etc. Each trigger stage in the chainn is only to switch over, in accordance with the set aim, when all its preceding, lower valued trigger stages have previously switched over, to produce a logic "1" at the corresponding carry signal input e.g. at T_{n-1}.

It will first be assumed that the trigger stage 22 occupies a switching state in which a logic "0" is present at its output Q_n, and a logic "1" is present at its output $\overline{Q_n}$, i.e. that this stage has not yet switched over. It will further be assumed that all the preceding stages for the lower valued counting stages have already switched over. Therefore a logic "1" is assumed to be present at the carry signal input T_{n-1}. As the transfer transistor T_{22} is held blocked as a result of a logic "0" at its control input, the carry signal at the input T_{n-1} cannot yet be transferred to the following higher-value counting stage.

Only when the trigger stage 22 switches over, on receiving the subsequent input pulse which is to be counted, at the input control electrode of transistor 24 does a logic "1" appear at the output $\overline{Q_n}$ and a logic "0" appear at its output Q_n, so that when all the lower valued trigger stage outputs Q_1 to Q_{n-1} have assumed the logic "1" switching state, the transistor T_{22} may transfer a carry signal to the next stage, which has outputs Q_{n+1} and $\overline{Q_{n+1}}$.

It can also be seen from the circuit illustrated in Figure 1 that at the respective inputs of the gates 30 and 31, via the associated transfer transistors T_{24} and T_{25}, the set of transfer transistors T_{20} to T_{23} produce the

required logic signals for the switch-over function of the trigger stages which operate the latter.

The arrangement shown in Figure 2 is generally similar to that shown in Figure 1, and those components serving an identical function to those in Figure 1 have been identified by the reference already used in Figure 1. The Figure 2 embodiment is a multi-stage, logic circuit arrangement constructed in accordance with the invention to serve as a forwards-backwards, synchronous binary counter.

As a supplementation to the basic synchronous binary counter arrangement illustrated in Figure 1, in the embodiment shown in Figure 2 there is a further arm provided, consisting of two series-connected transfer transistors T_{40} and T_{41} whose controlled paths between source and drain are connected in series between the connection point of the series-connected, controlled paths between the transfer transistors T_{20} and T_{23} and the connection point of the series-connected controlled paths between the transfer transistors T_{22} and T_{21}. The carry signal output of each counter stage is formed by the connection point of the controlled paths of the respective transfer transistors T_{40} and T_{41} and as in the embodiment shown in Figure 1, lead to the upper transfer transistors T_{20} and T_{22} of the next higher stage. At an input 40, a control signal is fed in which passes via one conductor path directly into the counter stages to control the transfer transistors T_{41}, and is also inverted via an inverter 41 and fed to control the transfer transistors T_{40}, facilitating forwards or backwards counting, as required.

In the backwards-counting mode, in contrast to the forwards-counting mode, the counting stage with the output Q_n is to switch over whenever all the lower-value counting stages previously assume the logic "0" state at their outputs Q_1 to Q_{n-1}. In this case all the transistors T_{20} of the lower-value stages with the outputs Q_1 to Q_{n-1} are switched through, and all the transistors T_{40} of the entire counting chain are switched through via the inverted control input 40. For the carry input T_{n-1} of the stages with a Q_n output, there then occurs a logic "1", which in accordance with the set aim, causes the trigger stage with the output Q_n to switch over when a further counting pulse is supplied at the input 32. In the same manner, via the transistor T_{23} of the counting stage having the output Q_n, a logic "0" is applied to the carry input T_n of the stage having the output Q_{n+1}, which remains blocked from switching over until all the stages with the outputs Q_1 to Q_n have assumed the logic "0" stage at these outputs.

In order to attain the forwards-counting mode, the signal fed in from the input 40 via the inverter 41 to the transistors T_{41} causes those to be switched on, and at the same time the transistors T_{40} are switched off. As can be readily seen, the counting process in the circuit represented in Figure 2 then proceeds in the same way as already explained in respect of the circuit illustrated in Figure 1.

The stages of the embodiment shown in Figure 3 also have components with functions identical to those of Figures 1 and 2 and these have been identified by use of references used in Figure 1 and Figure 2. The Figure 3 embodiment is a multi-stage, logic circuit arrangement constructed in accordance with the invention to serve as a forwards synchronous counting decade. A binary coded counting decade of this type contains four trigger stages 22 to 25 arranged in known manner to count upwards in a 1, 2, 4, 8, BCD code as counting pulses fed in at the input 32. The binary weighting of outputs Q_0 to Q_3 of the trigger stages 22 to 25 corresponds to the indices selected for the outputs, i.e. the counts are passed through in accordance with the following code table:

STAGE AND OUTPUT				Count
22 Q_0	23 Q_1	24 Q_2	25 Q_3	
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	0	0	0	0

For the execution of the requisite, logic operations, the arrangement shown for the synchronous binary counter illustrated in Fig. 1 is extended by the following additional circuitry to form the forwards synchronous counting decade shown in Fig. 3.

The series arrangement of the controlled paths of the transfer transistors T_{21} and T_{22} at the output of the transfer gate formed by transistors T_{20} to T_{23} of the last trigger stage 25 of the n-th decade is coupled via a signal

link T3b to the connection point of the controlled paths of the transfer transistors T_{21} and T_{22} at the output of the corresponding transfer gate of the first trigger stage 22, and to the series arrangement of the controlled paths of the transfer transistors T_{21} and T_{22} at the output of the corresponding transfer gate of the second trigger stage 23.

Furthermore the signal link T3b is connected to a reference potential point via a series arrangement of the controlled paths of two transfer transistors T_{50} and T_{51} in the stage 25.

The control input of the transfer transistor T_{50}, whose controlled path is directly connected to the signal link T3b is coupled to the output $\overline{Q_3}$ of the last trigger stage 25 of the decade whereas the control input of the transfer transistor T_{51}, whose controlled path is connected to the signal link T3b via the controlled path of the transfer transistor T_{50}, is coupled to the other output Q_3 of the last trigger stage 25.

The connection point of the controlled paths of the transfer transistors T_{50} and T_{51} is connected to the series arrangement of the controlled paths of the transfer transistors T_{20} and T_{23} at the input end of the transfer gate of the second trigger stage 23.

The series arrangement of the controlled paths of the transfer transistors T_{20} and T_{23} at the input end of the transfer gate of the last trigger stage 25 of the decade is connected to the connection point of the controlled paths of the transfer transistors T_{21} and T_{22} at the output end of the corresponding transfer gate of the last but one trigger stage 24 in the decade.

Finally, the connection point of the controlled paths of the transfer transistors T_{21} and T_{22} at the output end of the transfer gate of the last stage 25 serves as a carry signal output C_{n-1} for the decade.

In order to facilitate a series connection of an arbitrary number of counting decades of identical construction, whose trigger stages will all be assumed to be operated by a common counting signal at each respective input 32, the carry output C_{n+1} of the general counting decade n illustrated in Fig. 3 must, during the count "9", emit a signal which will be effective, when the counting decade n is stepped on to repeat the count "0", to cause the next general counting decade $n+1$ to be advanced.

As can be seen from the code table, the switching states of the output Q_0 and Q_2 of the trigger stages 22 and 24 correspond to the switching states in a four-stage binary counter. The transistors T_{20} to T_{23} of the trigger stages 22 and 24 in Fig. 3 are therefore connected into the signal flow in the same manner as that illustrated in the case of the corresponding transistors T_{20} to T_{23} in the stages of the exemplary embodiment of a synchronous binary counter shown in Fig. 1. However, in contrast to the binary counter, in the case of the decadic counter shown in Fig. 3, the output Q_1 of the trigger stage 23 must be prevented from switching over to a logic "1" in the count 0, and it must be ensured that in the count 0 the output Q_3 of the trigger stage 25 switches over to a logic "0".

In the circuit illustrated in Fig. 3 this is achieved by arranging that the upper terminals of the transistors T_{20} and T_{22} of the transfer gates assigned to the trigger stages 23 and 25 are operated with different signals for the setting and resetting of these trigger stages.

In the exemplary embodiment illustrated in Fig. 3, these signals for the setting and resetting of the trigger stage 23 are referenced T1a and T3b, whereas the signals for the setting and resetting of the trigger stage 25 are referenced T3a and T3b. The signals T3a and T3b represent the carry outputs of the transfer-gates which, in accordance with Fig. 1, are assigned to the trigger stages 24 and 22 and consist of the transistors T_{21} and T_{22}. In the exemplary embodiment shown in Fig. 3 a further transfer-gate consisting of the transistors T_{50} and T_{51} has been introduced, with their controlled paths connected in series between the signal line T3b and an earth terminal, and whose respective gate terminals are driven respectively from the outputs $\overline{Q_3}$ and Q_3 of the trigger stage 25. A setting signal T_1 which serves to set the trigger stage 23 is withdrawn at the connection point between the controlled paths of the transistors T_{50} and T_{51}. As regards the mode of operation of the exemplary embodiment shown in Fig. 3, it will readily be seen that from the count 0 to the count 7, the switching sequence of the trigger stages 22 to 24 corresponds to the binary code shown in the preceding code table. At the count 7 the setting signal T3a becomes a logic "1", so that at the next counting pulse the trigger stage 25 switches over, and the desired count of 8 is set up. Consequently the transistor T_{50} is switched off and the transistor T_{51} is switched on, so that the setting signal T1 assumes the logic "0" level, and the trigger stage 23 is initially blocked from further switch-over.

A further counting pulse causes the trigger stage 22 to switch over, and thus brings about a transition into the count 9. Here it will readily be seen that the trigger stages 22 to 25 are switched over with counting pulses arriving at the input 32 only when a logic "1" is present at the input C_n, signalling a carry from the preceding counting decade. Therefore a carry to the next counting decade via the output C_{n+1} occurs only when the carry C_n from the preceding counting decade and the trigger stage outputs Q_0 and Q_3 of the decade in question have assumed the logic "1" state. Due to the fact that the signal

T3b has assumed the logic "1" state and at the same time a logic "1" is present at the output Q_3 of the trigger stage 25, a counting pulse arriving at the input 32 in the count 9 causes the trigger stage 25 of the counting decade in question to switch over and causes the trigger stage 22 of the following counting decade to switch over, as a result of which the count 0 re-occurs in the counting decade in question, and a count increased by 1 occurs in the following counting decade.

WHAT WE CLAIM IS:—

1. A MOS multi-stage logic circuit in the form of an integrated circuit with gates for the production and transmission of carry signals between its stages, the logic circuit being in the form of a synchronous binary counter each counting stage of which has a bistable trigger stage, a carry signal input for a carry signal from the counting stage for the relevant lower valued counting position if any, and a carry signal output which is coupled to the carry signal input of the counting stage for the relevant higher-valued counting position if any, wherein each counting stage is provided with a respective transfer gate having two branches, first and second transfer transistors being connected in series with the carry signal input in each said branch, the control electrode of each said first transistor being connected to the control electrode of the second transistor in the other branch, the control eiectrodes of the transfer transistors whose conductive path is directly connected to the associated carry signal input being coupled respectively to the complementary outputs of that stage's bistable trigger stage, the connection point of the controlled paths of the first and second transfer transistors in each branch being coupled to a respective timing signal input of the bistable trigger stage and the connection point of the controlled paths of the first and second transfer transistors in one of said branches providing an output carry signal of that stage.

2. A logic circuit as claimed in claim 1, for operation as a forwards-backwards synchronous binary counter, in each counting stage of which the connection points of the controlled paths of the first and second transfer transistors are connected to respective ends of a series arrangement of two further transfer transistors whose control electrodes are respectively connected to separate input lines, one for forwards counting and the other for backwards counting control signals, the connection point of the controlled paths of the further transfer transistors serving as the carry signal output.

3. A logic circuit as claimed in claim 1, for use as a forwards synchronous counting decade with four bistable trigger stages, the series arrangement of the controlled paths of the transfer transistors at the carry signal output of the transfer gate of the last trigger stage of the decade being coupled via a signal link to the connection point of the controlled paths of the transfer transistors at the carry signal output of the transfer gate of the first trigger stage and to the series arrangement of the controlled paths of the transfer transistors at the carry signal output of the transfer gate of the second trigger stage, said signal link being connected via series arrangement of the controlled paths of two additional transfer transistors to a reference potential point, the control electrode of that additional transfer transistor whose controlled path is directly connected to said signal link being connected to one of the complementary outputs of the last trigger stage of the decade, whereas the control electrode of the other additional transfer transistor is connected to the other of the complementary outputs of the last trigger stage of the decade; the connection point of the controlled paths of said additional transfer transistors being connected to the series arrangement of the controlled paths of the transfer transistors at the carry signal input of the transfer gate of the second trigger stage of the decade; the series arrangement of the controlled paths of the transfer transistors at the carry signal input of the transfer gate of the last trigger stage of the decade being connected to the connection point of the controlled paths of the transfer transistors at the carry signal output of the transfer gate of the last but one trigger stage of the decade; and the connection point of the controlled paths of the transfer transistors at the carry signal output of the transfer gate of the last stage serving as a carry signal output for said decade.

4. A logic circuit arrangement comprising a plurality of decades as claimed in claim 3, said decades being connected in sequence by their respective carry signal outputs, and supplied by a common counting signal.

5. A MOS multi-stage logic circuit in the form of an integrated circuit substantially as described with reference to any one of Figures 1 to 3 of the accompanying drawings.

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Sheet 1

Fig.1

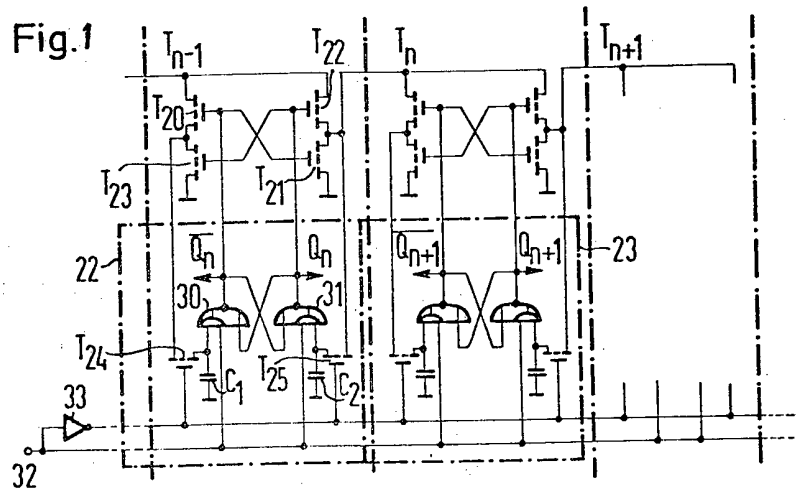
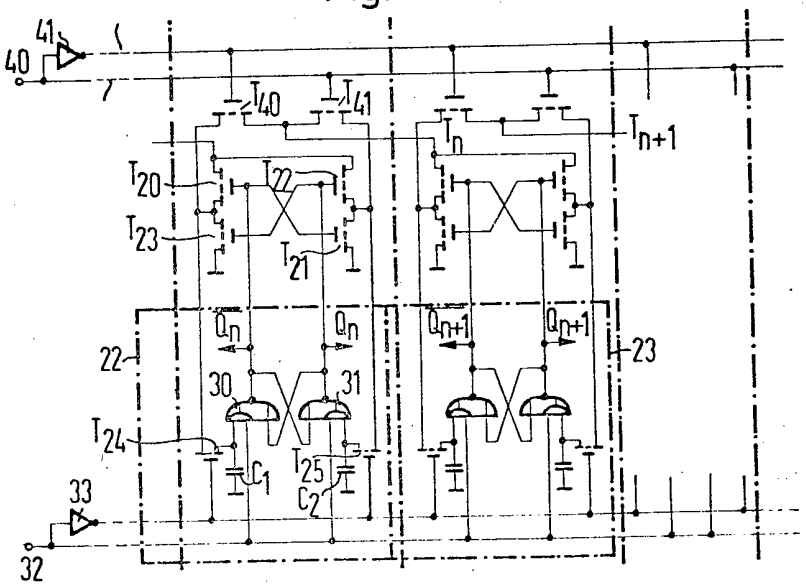


Fig.2



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Sheet 2

Fig.3