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(54) Title: AREA SELECTIVE DEPOSITION FOR CAP LAYER FORMATION IN ADVANCED CONTACTS

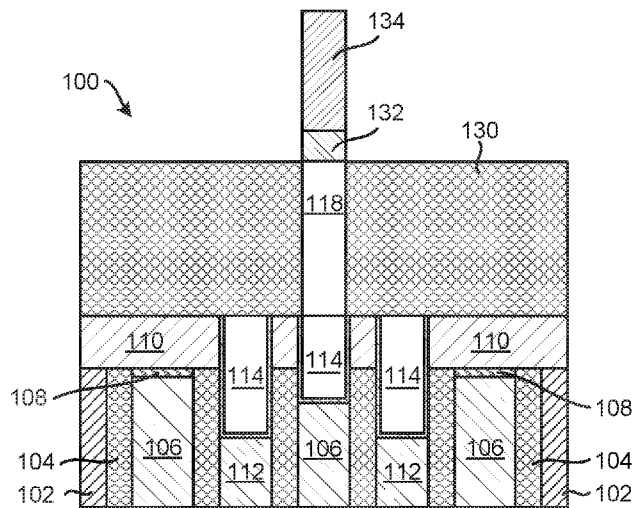


FIG. 1C

(57) Abstract: A method of area selective deposition for cap layer formation in advanced semiconductor contacts. The method includes providing a planarized substrate including a first dielectric layer and a first metal layer, oxidizing a surface of the first metal layer to form an oxidized metal layer, and selectively depositing a second dielectric layer on the oxidized metal layer. The selectively depositing the second dielectric layer can include moving the planarized substrate below a gas inlet dispensing a deposition gas during a spatial vapor phase deposition process, where the deposition gas is preferentially exposed to the oxidized metal layer extending above a surface of the first dielectric layer.



EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
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AREA SELECTIVE DEPOSITION FOR CAP LAYER FORMATION IN ADVANCED CONTACTS

CROSS-REFERENCE TO RELATED APPLICATIONS

5 [0001] This application is related to and claims priority to United States Provisional Patent Application serial no. 62/663,916 filed on April 27, 2018, the entire contents of which are herein incorporated by reference.

FIELD OF THE INVENTION

10 [0002] This invention relates to methods for processing a substrate, and more particularly to area selective deposition for cap layer formation in advanced contacts.

BACKGROUND OF THE INVENTION

15 [0003] As smaller transistors are manufactured, the critical dimension (CD) or resolution of patterned features is becoming more challenging to produce. Self-aligned patterning needs to replace overlay-driven patterning so that cost-effective scaling can continue even after EUV introduction. Patterning options that enable reduced variability, extend scaling and enhanced CD and process control are needed. Selective deposition of thin films are key steps in patterning in highly scaled technology nodes.

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SUMMARY OF THE INVENTION

[0004] An area selective deposition method for cap layer formation in advanced semiconductor contacts is described. The area selective deposition enables a simplified metallization scheme that requires reduced lithography-based patterning.

25 [0005] According to one embodiment, the method includes a cap layer formation in advanced semiconductor contacts. The method includes providing a planarized substrate including a first dielectric layer and a first metal layer, oxidizing a surface of the first metal layer to form an oxidized metal layer, and selectively depositing a second dielectric layer on the oxidized surface of the first metal layer. The selectively depositing the second dielectric layer can include
30 moving the planarized substrate below a gas inlet dispensing a deposition gas during a spatial vapor phase deposition process, where the deposition gas is preferentially exposed to the oxidized metal layer extending above a surface of the first dielectric layer.

[0006] According to another embodiment, the method includes providing a planarized substrate including a first dielectric layer and a first metal layer, selectively depositing a second dielectric layer on the first dielectric layer, where the selectively depositing forms a recessed feature above the first metal layer, filling the recessed feature with a second metal layer, removing the second dielectric layer from the substrate, and selectively depositing a third dielectric layer on the second metal layer.

[0007] According to another embodiment, the method includes providing a planarized substrate including a first dielectric layer and a first metal layer, recessing the first dielectric layer below an upper surface of the first metal layer, and selectively depositing a second dielectric layer on the first metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with a general description of the invention given above, and the detailed description given below, serve to explain the invention.

[0009] FIGS. 1A-1C schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention;

[0010] FIGS. 2A-2E schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention; and

[0011] FIGS. 3A-3C schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention.

DETAILED DESCRIPTION OF SEVERAL EMBODIMENTS

[0012] FIGS. 1A-1C schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention. The exemplary substrate 100 shown in FIG. 1A contains various material layers commonly found in semiconductor devices, however, embodiments of the invention may be applied to simpler or more advanced semiconductor devices. The substrate 100 contains an oxide layer 102 (e.g., SiO₂), a nitride layer 104 (e.g., SiN), a gate contact layer 106, a cap layer 108 (e.g., SiN or SiCN), a source/drain layer 112 (e.g., Si or SiC), a dielectric layer 110 (e.g., SiO₂), and a metal-containing layer 114 (e.g., a

trench silicide layer: CoSi_2 , NiSi , or MoSi_2). In the exemplary substrate 100, the metal-containing layer 114 and the source/drain layer 112 may be part of a contact region. The substrate 100 further includes a first dielectric layer 130 and a first metal layer 118. The first dielectric layer 130 can, for example, include SiO_2 or a low-k material. The first metal layer 118
5 may, for example, be selected from the group consisting of tungsten (W) metal, ruthenium (Ru) metal, cobalt (Co) metal, molybdenum (Mo), and a combination of thereof. The substrate 100 may be planarized using a chemical mechanical polishing (CMP) process.

[0013] FIG. 1B shows the substrate 100 following an oxidation process that oxidizes the exposed first metal layer 118 to form an oxidized metal layer 132 on the first metal layer 118.

10 The oxidation process can include exposing the substrate 100 to plasma-excited O_2 gas. In one example, a W metal layer is oxidized to form an oxidized W metal layer. The oxidation process is accompanied by an increase in volume since oxidized W (e.g., WO_3) occupies a larger volume than W metal. This results in the oxidized W metal layer extending a few nanometers (nm) above the horizontal plane of the W metal layer and the first dielectric layer 130.

15 **[0014]** FIG. 1C shows the substrate 100 following selective deposition of a second dielectric layer 134 on the oxidized metal layer 132. In one example, the second dielectric layer 134 can include a metal oxide layer or a metal nitride layer. In another example, the second dielectric layer 134 may be selected from the group consisting of TiO_2 , HfO_2 , ZrO_2 , Al_2O_3 , SiO_2 , SiN , and a combination thereof. The selective deposition of the second dielectric layer 134 is, at least in
20 part, enabled by the oxidized metal layer 132 extending above the horizontal plane of the first metal layer 118 and the first dielectric layer 130. According to one embodiment, the second dielectric layer 134 may be deposited by spatial deposition by moving the substrate 100 below a gas inlet dispensing a deposition gas during spatial vapor phase deposition process, for example a spatial atomic layer deposition (ALD) process or a spatial chemical vapor deposition (CVD).

25 A rotation speed of the substrate support and the gas exposure parameters may be selected such that the deposition gas is preferentially exposed to a top surface of the raised oxidized metal layer 132 but not to a surface of the first dielectric layer 130 that is below the top surface of the raised oxidized metal layer 132. According to other embodiment, the second dielectric layer 134 may be deposited carefully controlling the precursor exposure, including gas flow, exposure
30 time) in order to preferentially expose the top surface of the raised oxidized metal layer 132.

[0015] The second dielectric layer 134, also known as a cap layer, may be used as a hard mask for a subsequent etching process to form a fully self-aligned via, a self-aligned contact, a

supervia, or a self-aligned gate contact in the first dielectric layer 130 adjacent the first metal layer 118. The second dielectric layer 134 protects the first metal layer 118 during the etching process by preventing or reducing etching of the first metal layer 118.

[0016] FIGS. 2A-2E schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention. The substrate 100 shown in FIG. 1A has been reproduced as substrate 200 in FIG. 2A. FIG. 2B shows the substrate 200 following selective deposition of a second dielectric layer 140 on the first dielectric layer 130. The selective deposition of the second dielectric layer 140 forms a recessed feature 133 above the first metal layer 118. In some examples, the second dielectric layer 140 may be selected from the group consisting of TiO₂, HfO₂, ZrO₂, Al₂O₃, SiO₂, SiN, and a combination thereof.

[0017] In one example, the second dielectric layer 140 can contain SiO₂, and the selective deposition may be achieved by alternating exposures of a metal-containing precursor and a silanol gas. The metal-containing precursor selectively adsorbs on the first dielectric layer 130 and subsequently catalyzes reaction of the silanol gas to deposit SiO₂ material. The silanol gas may be selected from the group consisting of tris(tert-pentoxy) silanol (TPSOL), tris(tert-butoxy) silanol, and bis(tert-butoxy)(isopropoxy) silanol. The exposures to the silanol gas may be performed in the absence of any oxidizing and hydrolyzing agent, and the substrate may be exposed, at a substrate temperature of approximately 150°C or less, to a process gas containing a silanol gas to deposit a SiO₂ film. The thickness of the SiO₂ film is controlled by self-limiting adsorption of the silanol gas on the metal-containing precursor layer. This catalytic effect has been observed until the SiO₂ films were about 3nm thick, thereafter the SiO₂ deposition stopped. In another embodiment, the substrate temperature may be approximately 120°C or less. In yet another embodiment, the substrate temperature may be approximately 100°C or less.

[0018] Examples of metal-containing precursor include aluminum (Al), titanium (Ti), or both aluminum and titanium. Examples of aluminum-containing precursors include: AlMe₃, AlEt₃, AlMe₂H, [Al(O^tBu)₃]₄, Al(CH₃COCHCOCH₃)₃, AlCl₃, AlBr₃, AlI₃, Al(OⁱPr)₃, [Al(NMe₂)₃]₂, Al(ⁱBu)₂Cl, Al(ⁱBu)₃, Al(ⁱBu)₂H, AlEt₂Cl, Et₃Al₂(O^tBu)₃, and Al(THD)₃.

Examples of titanium-containing precursors that have “Ti-N” intra-molecular bonds include Ti(NEt₂)₄ (TDEAT), Ti(NMeEt)₄ (TEMAT), Ti(NMe₂)₄ (TDMAT). Other examples include titanium-containing precursors containing “Ti-C” intra-molecular bonds include Ti(COCH₃)(η⁵-C₅H₅)₂Cl, Ti(η⁵-C₅H₅)Cl₂, Ti(η⁵-C₅H₅)Cl₃, Ti(η⁵-C₅H₅)₂Cl₂, Ti(η⁵-C₅(CH₃)₅)Cl₃, Ti(CH₃)(η⁵-C₅H₅)₂Cl, Ti(η⁵-C₉H₇)₂Cl₂, Ti((η⁵-C₅(CH₃)₅)₂Cl, Ti((η⁵-C₅(CH₃)₅)₂Cl₂, Ti(η⁵-C₅H₅)₂(μ-Cl)₂,

Ti(η^5 -C₅H₅)₂(CO)₂, Ti(CH₃)₃(η^5 -C₅H₅), Ti(CH₃)₂(η^5 -C₅H₅)₂, Ti(CH₃)₄, Ti(η^5 -C₅H₅)(η^7 -C₇H₇), Ti(η^5 -C₅H₅)(η^8 -C₈H₈), Ti(C₅H₅)₂(η^5 -C₅H₅)₂, Ti((C₅H₅)₂)₂(η -H)₂, Ti(η^5 -C₅(CH₃)₅)₂, Ti(η^5 -C₅(CH₃)₅)₂(H)₂, and Ti(CH₃)₂(η^5 -C₅(CH₃)₅)₂. TiCl₄ is an example of a titanium halide precursor containing a “Ti-halogen” bond.

5 [0019] In another example, the second dielectric layer 140 can contain TiO₂, and the selective deposition may be achieved by alternating exposures of a Ti-containing precursor and an oxygen-containing gas.

[0020] FIG. 2C shows the substrate 200 following selective deposition of a second metal layer 136 on the first metal layer 118 in the recessed feature 133. The first metal layer 118 may fully
10 fill the recessed feature 133. The second metal layer 136 can be selected from the group consisting of tungsten (W) metal, ruthenium (Ru) metal, cobalt (Co) metal, molybdenum (Mo), and a combination of thereof.

[0021] In one example, the selective deposition of the second metal layer 136 may be performed in a bottom-up fashion by blocking metal deposition on the first dielectric layer 130. The metal
15 deposition may be blocked by exposing the substrate 200 to a reactant gas containing a hydrophilic functional group that adsorbs on the first dielectric layer 130 but not on the first metal layer 118. The reactant gas can contain a silicon-containing gas, including an alkyl silane, an alkoxy silane, an alkyl alkoxy silane, an alkyl siloxane, an alkoxy siloxane, an alkyl alkoxy siloxane, an aryl silane, an acyl silane, an aryl siloxane, an acyl siloxane, a silazane, or
20 any combination thereof. In some examples, the reactant gas may be selected from dimethylsilane dimethylamine (DMSDMA), trimethylsilane dimethylamine (TMSDMA), bis(dimethylamino) dimethylsilane (BDMADMS), and other alkyl amine silanes.

[0022] FIG. 2D shows the substrate 200 following removal of the first dielectric layer 130. The removal can include a dry etching process or a wet etching process.

25 [0023] FIG. 2E shows the substrate 200 following selective deposition of a third dielectric layer 138 on the second metal layer 136. Optionally, a surface of the second metal layer 136 may be oxidized using an oxidation process to form an oxidized metal layer and, thereafter, the third dielectric layer 138 selectively deposited on the oxidized metal layer. In one example, the third dielectric layer 138 can include a metal oxide layer or a metal nitride layer. In another example,
30 the third dielectric layer 138 may be selected from the group consisting of TiO₂, HfO₂, ZrO₂, Al₂O₃, SiO₂, SiN, and a combination thereof. The selective deposition of the third dielectric

layer 138 is, at least in part, enabled by the second metal layer 136 extending above the horizontal plane of the first metal layer 118 and the first dielectric layer 130.

[0024] According to one embodiment, the third dielectric layer 138 may be deposited by spatial deposition by moving the substrate 100 below a gas inlet dispensing a deposition gas during a spatial vapor phase deposition process, for example a spatial atomic layer deposition (ALD) process or a spatial chemical vapor deposition (CVD). A rotation speed of the substrate support and the gas exposure parameters may be selected such that the deposition gas is preferentially exposed to a top surface of the raised second metal layer 136 but not to a surface of the first dielectric layer 130 that is below the top surface of the raised second metal layer 136.

According to other embodiment, the third dielectric layer 138 may be deposited carefully controlling the precursor exposure, including gas flow, exposure time) in order to preferentially expose the top surface of the raised second metal layer 136.

[0025] FIGS. 3A-3C schematically show through cross-sectional views a method of processing a substrate according to an embodiment of the invention. The substrate 100 shown in FIG. 1A has been reproduced as substrate 300 in FIG. 3A. FIG. 3B shows the substrate 300 following an etching process that recesses the first dielectric layer below an upper surface of the first metal layer 118. Thereafter, the substrate 300 may be processed as described in FIG. 2E, including selectively depositing a second dielectric layer 140 deposited on the first metal layer 118.

Optionally, a surface of the first metal layer 118 may be oxidized using an oxidation process to form an oxidized metal layer and, thereafter, the second dielectric layer 140 selectively deposited on the oxidized metal layer. In one example, the second dielectric layer 140 can include a metal oxide layer or a metal nitride layer. In another example, the second dielectric layer 140 may be selected from the group consisting of TiO_2 , HfO_2 , ZrO_2 , Al_2O_3 , SiO_2 , SiN , and a combination thereof. The selective deposition of the second dielectric layer 140 is, at least in part, enabled by the first metal layer 118 extending above the horizontal plane of the first dielectric layer 130.

[0026] A plurality of embodiments for an area selective deposition for cap layer formation in advanced semiconductor contacts has been described. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description.

It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms that are used for descriptive purposes only and are not to be construed as limiting. Persons skilled in the relevant art can appreciate that

many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

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WHAT IS CLAIMED IS:

1. A substrate processing method, comprising:
 - providing a planarized substrate including a first dielectric layer and a first metal layer;
 - oxidizing a surface of the first metal layer to form an oxidized metal layer; and
 - selectively depositing a second dielectric layer on the oxidized metal layer.
2. The method of claim 1, wherein the selectively depositing the second dielectric layer includes moving the planarized substrate below a gas inlet dispensing a deposition gas during a spatial vapor phase deposition process, and wherein the deposition gas is preferentially exposed to the oxidized metal layer extending above a surface of the first dielectric layer.
3. The method of claim 1, wherein the first metal layer is selected from the group consisting of tungsten (W) metal, ruthenium (Ru) metal, cobalt (Co) metal, molybdenum (Mo), and a combination of thereof.
4. The method of claim 3, wherein the first metal layer includes W metal and the oxidizing forms an oxidized W metal layer that is accompanied by an increase in volume such that the oxidized W metal layer extends above a horizontal plane of the first metal layer and the first dielectric layer.
5. The method of claim 1, wherein the second dielectric layer is selected from the group consisting of TiO₂, HfO₂, ZrO₂, Al₂O₃, SiO₂, SiN, and a combination thereof.
6. The method of claim 1, wherein the second dielectric layer is selected from the group consisting of a metal oxide or a metal nitride.
7. The method of claim 1, further comprising:
 - using the second dielectric layer as a hard mask for a subsequent etching process to form a fully self-aligned via, a self-aligned contact, a supervia, or a self-aligned gate contact in the first dielectric layer.

8. A substrate processing method, comprising:
 - providing a planarized substrate including a first dielectric layer and a first metal layer;
 - selectively depositing a second dielectric layer on the first dielectric layer, wherein the selectively depositing forms a recessed feature above the first metal layer;
 - filling the recessed feature with a second metal layer;
 - removing the second dielectric layer from the substrate; and
 - selectively depositing a third dielectric layer on the first metal layer.
9. The method of claim 8, wherein the selectively depositing the third dielectric layer includes moving the planarized substrate below a gas inlet dispensing a deposition gas during a spatial vapor phase deposition process, and wherein the deposition gas is preferentially exposed to the second metal layer extending above a surface of the first dielectric layer.
10. The method of claim 8, wherein the first metal layer is selected from the group consisting of tungsten (W) metal, ruthenium (Ru) metal, cobalt (Co) metal, molybdenum (Mo), and a combination of thereof.
11. The method of claim 8, wherein the second metal layer is selected from the group consisting of tungsten (W) metal, ruthenium (Ru) metal, cobalt (Co) metal, molybdenum and a combination of thereof.
12. The method of claim 8, wherein the second dielectric layer is selected from the group consisting of TiO₂, HfO₂, ZrO₂, Al₂O₃, SiO₂, SiN, and a combination thereof.
13. The method of claim 8, wherein the third dielectric layer is selected from the group consisting of TiO₂, HfO₂, ZrO₂, Al₂O₃, SiO₂, SiN, and a combination thereof.

14. The method of claim 8, further comprising:
using the third dielectric layer as a hard mask for a subsequent etching process to form a fully self-aligned via, a self-aligned contact, a supervia, or a self-aligned gate contact in the first dielectric layer.
15. A substrate processing method, comprising:
providing a planarized substrate including a first dielectric layer and a first metal layer;
recessing the first dielectric layer below an upper surface of the first metal layer;
and
selectively depositing a second dielectric layer on the first metal layer.
16. The method of claim 15, wherein the selectively depositing the second dielectric layer includes moving the planarized substrate below a gas inlet dispensing a deposition gas during a spatial vapor phase deposition process, and wherein the deposition gas is preferentially exposed to the first metal layer extending above a surface of the first dielectric layer.
17. The method of claim 15, further comprising:
prior to selectively depositing the second dielectric layer, oxidizing a surface of the first metal layer to form an oxidized metal layer.
18. The method of claim 15, wherein the first metal layer is selected from the group consisting of tungsten (W) metal, ruthenium (Ru) metal, cobalt (Co) metal, molybdenum and a combination of thereof.
19. The method of claim 15, wherein the second dielectric layer is selected from the group consisting TiO₂, HfO₂, ZrO₂, Al₂O₃, SiO₂, SiN, and a combination thereof.
20. The method of claim 15, further comprising
using the second dielectric layer as a hard mask for a subsequent etching process to form a fully self-aligned via, a self-aligned contact, a supervia, or a self-aligned gate contact in the first dielectric layer.

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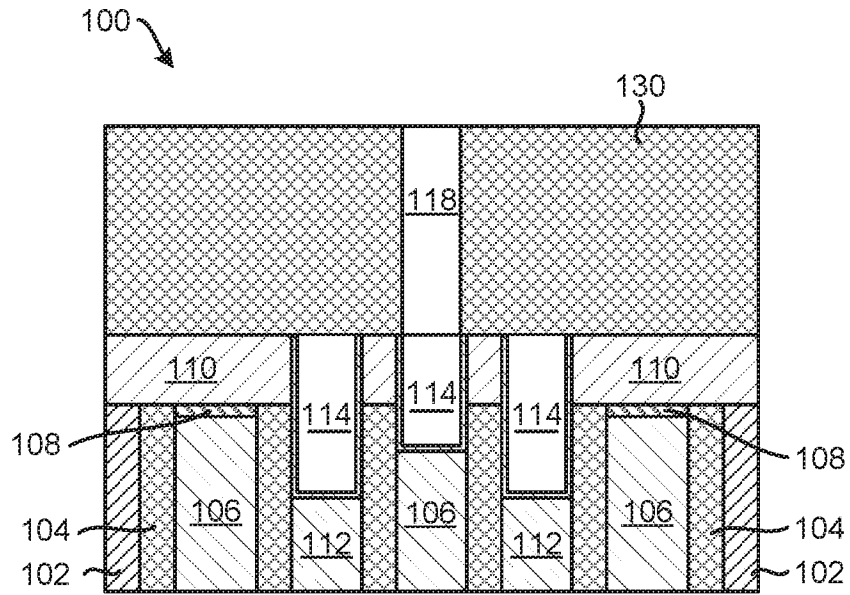


FIG. 1A

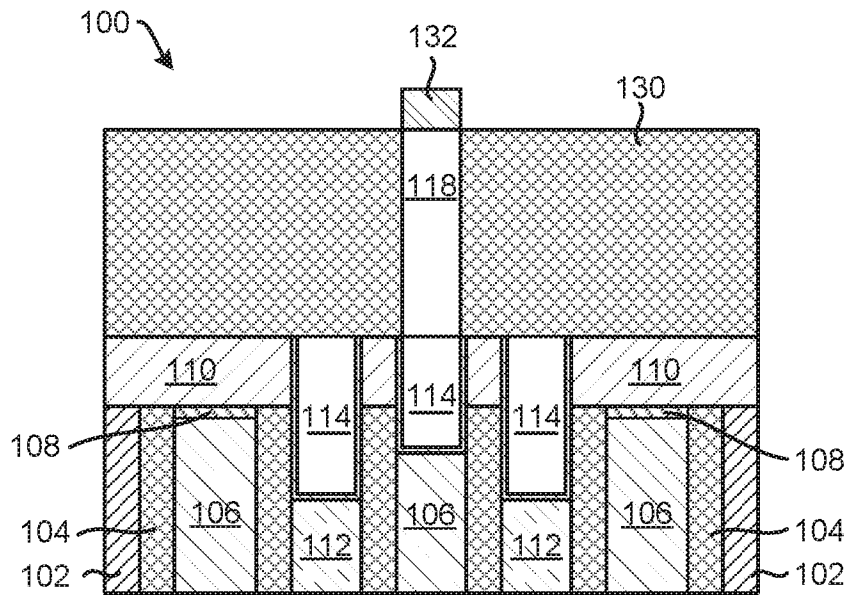


FIG. 1B

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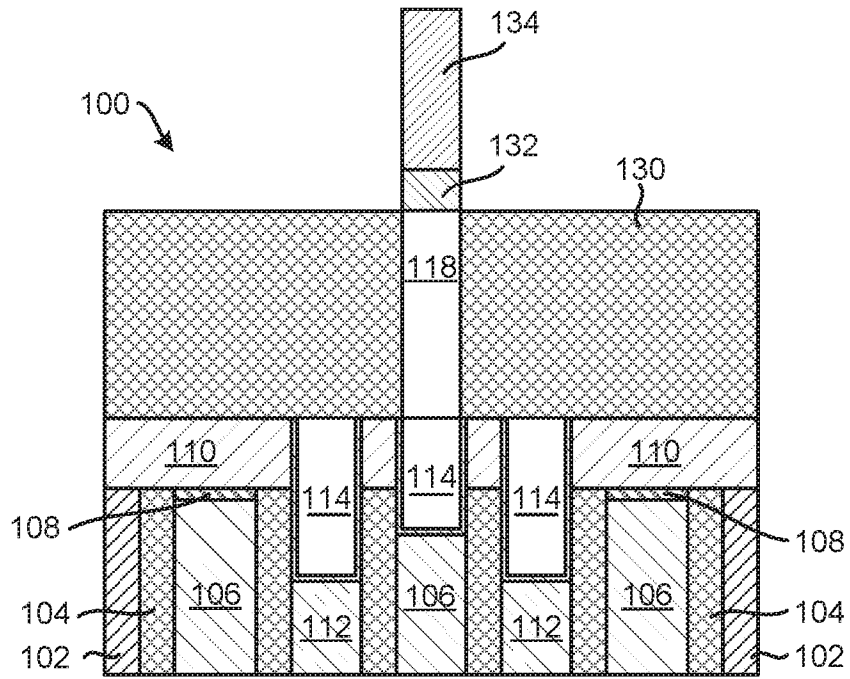


FIG. 1C

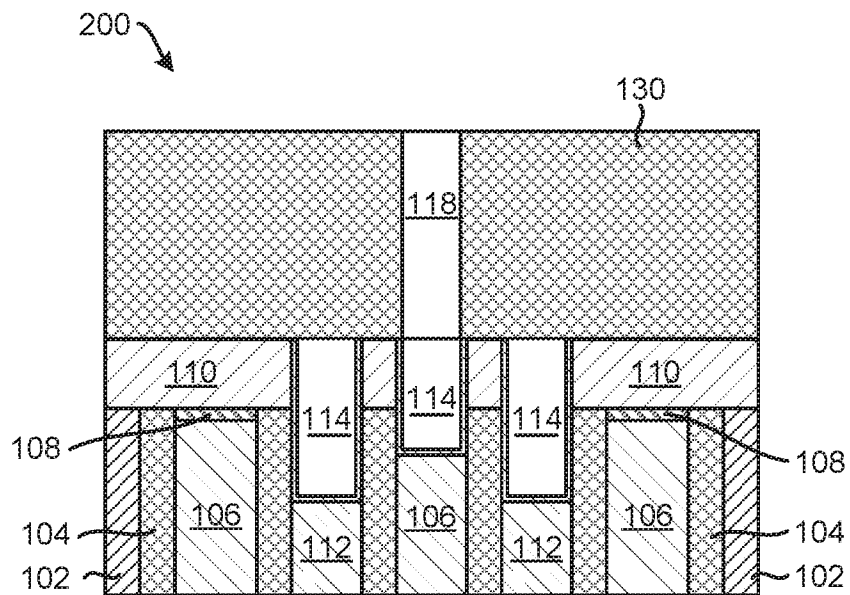


FIG. 2A

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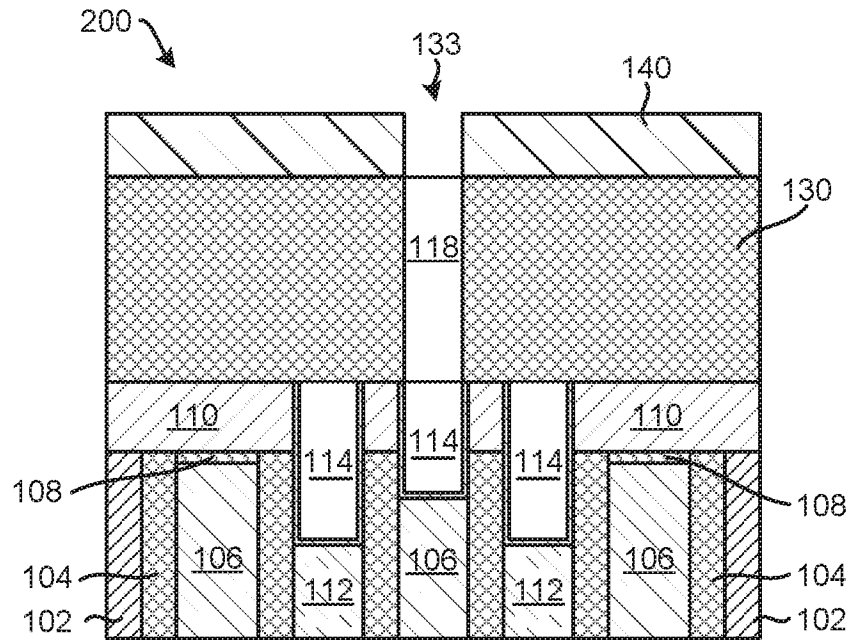


FIG. 2B

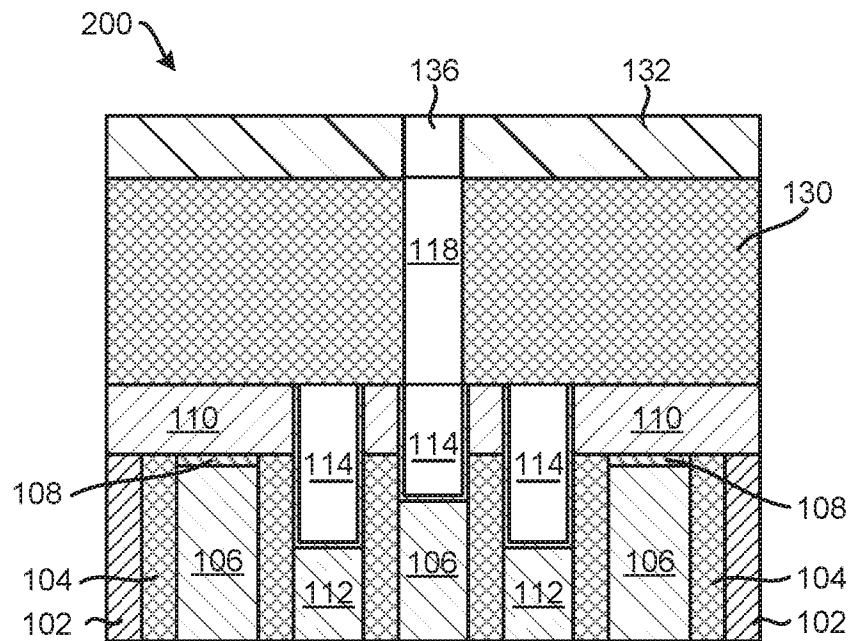


FIG. 2C

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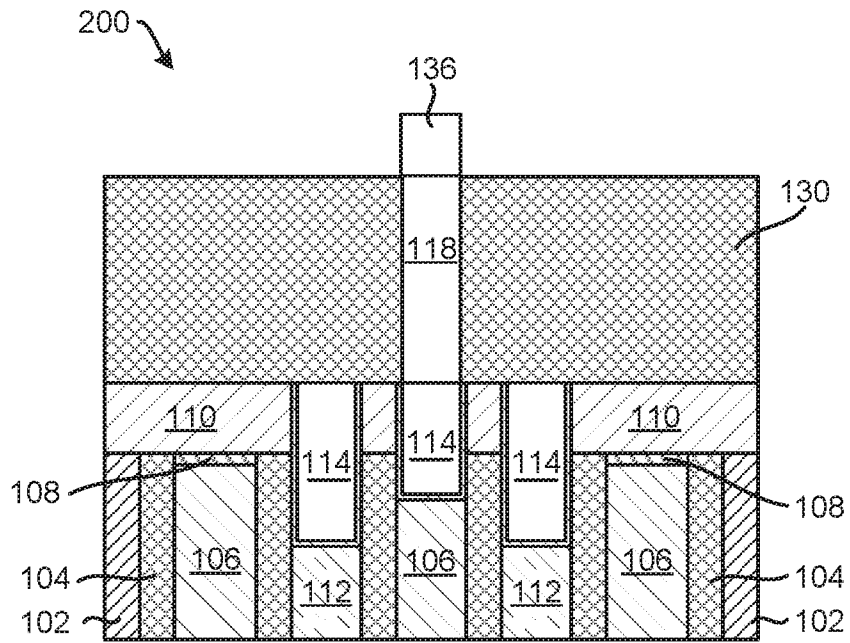


FIG. 2D

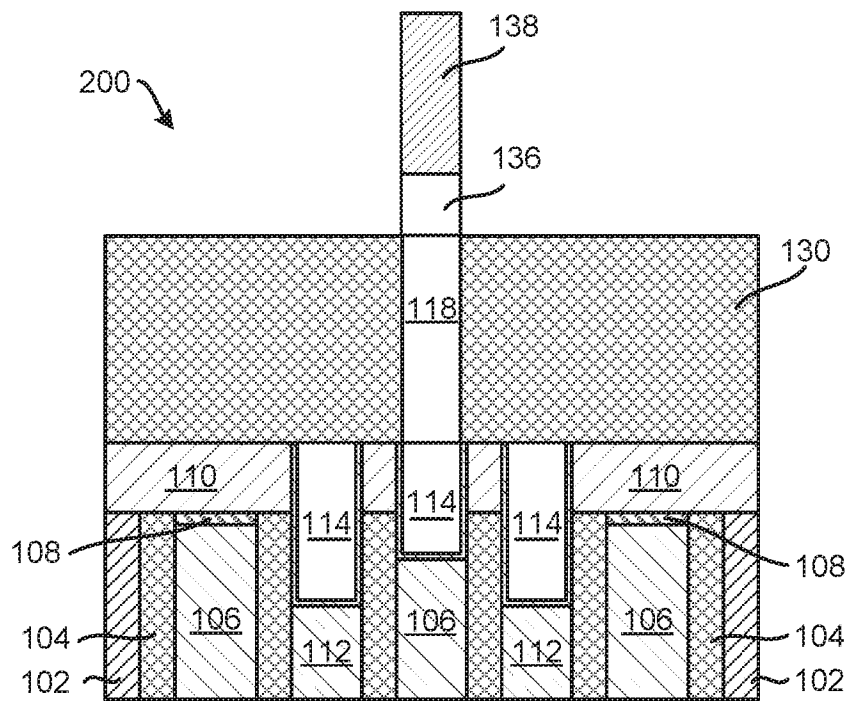


FIG. 2E

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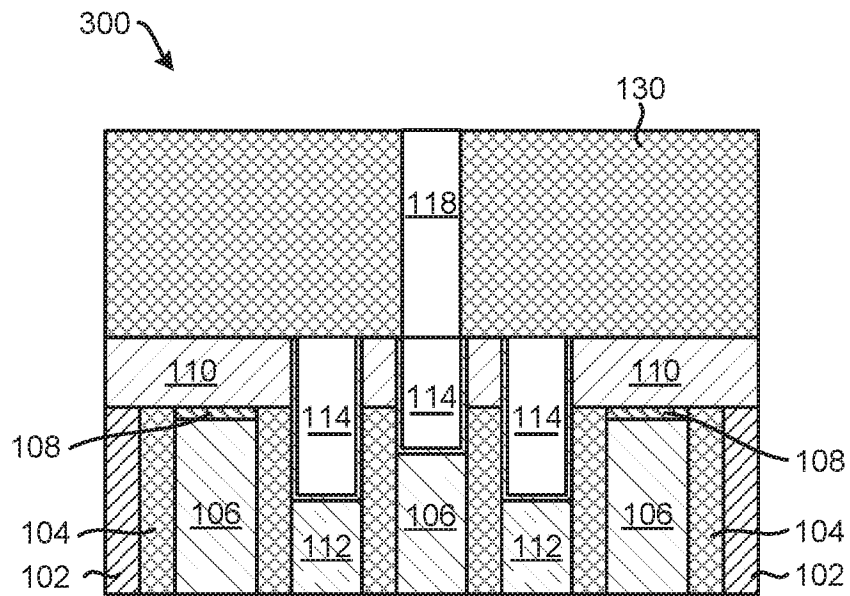


FIG. 3A

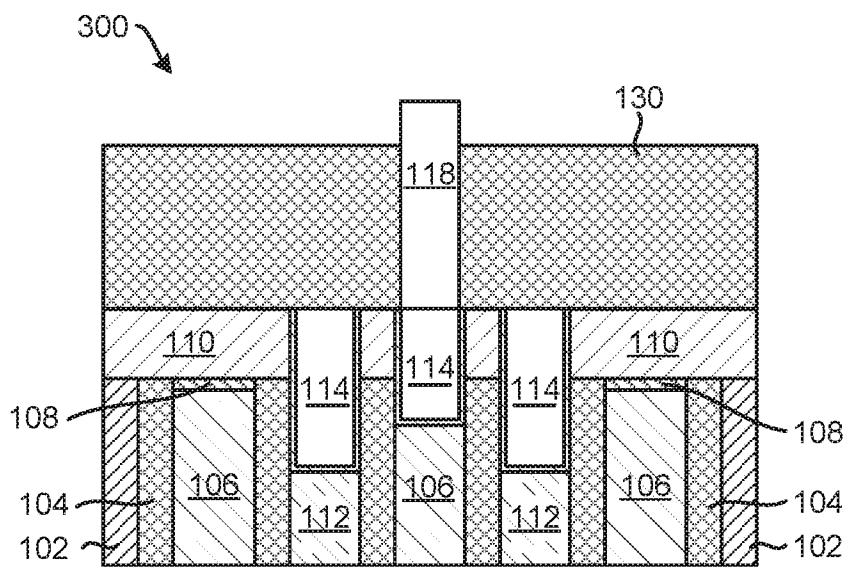


FIG. 3B

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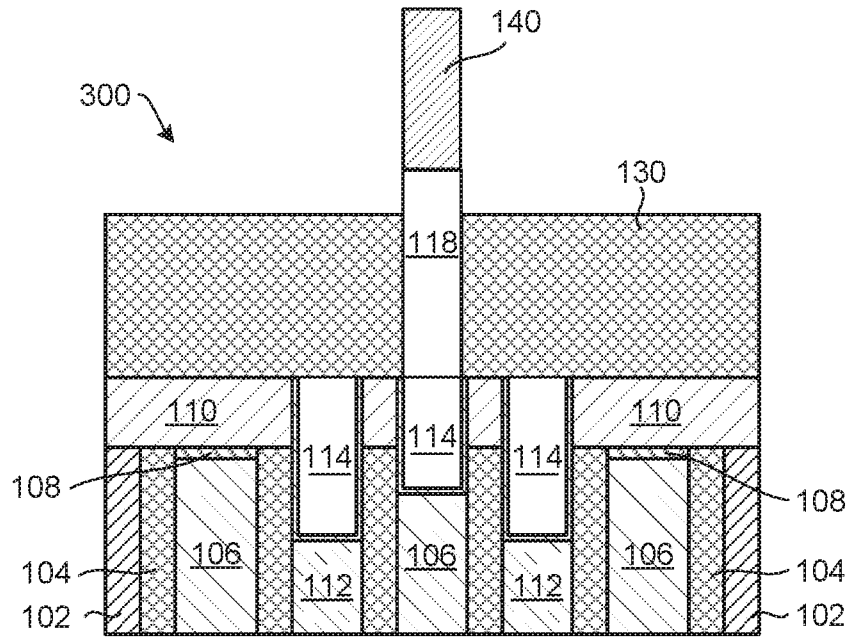


FIG. 3C

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/768(2006.01)i, H01L 21/285(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; C23C 16/04; C23C 16/06; H01L 21/00; H01L 21/28; H01L 21/4763; H01L 21/762; H01L 23/532; H01L 29/06; H01L 47/00; H01L 21/285

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: oxidizing, metal, dielectric, deposition, etching, hard mask

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|---|-----------------------|
| X | US 2015-0299848 A1 (ASM IP HOLDING B.V.) 22 October 2015 See paragraphs [0029]-[0357] and figures 1A-2. | 1-7 |
| Y | | 8-20 |
| Y | US 2008-0185567 A1 (NITIN KUMAR et al.) 07 August 2008 See paragraphs [0086]-[0091] and figures 10-12. | 8-20 |
| A | US 2012-0223407 A1 (THILO SCHEIPER et al.) 06 September 2012 See paragraphs [0037]-[0053] and figures 2a-2j. | 1-20 |
| A | US 2012-0252210 A1 (KAZUHITO TOHNOE) 04 October 2012 See paragraphs [0018]-[0033] and figures 1A-2. | 1-20 |
| A | US 2010-0176514 A1 (CHIH-CHAO YANG et al.) 15 July 2010 See paragraphs [0014]-[0020] and figures 2A-2H. | 1-20 |

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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