SOLID STATE TIMEPIECE


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ABSTRACT
Disclosed is a wristwatch comprising a crystal oscillator, a frequency divider formed of complementary MOS transistors, a display actuator, and a time display. The watch may be all solid state with integrated circuit construction and include a digital time display of light-emitting diodes. It includes display interrogation on demand and display scanning or strobing as well as time setting.

15 Claims, 22 Drawing Figures
FIG. 15

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ATTORNEYS.
SOLID STATE TIMEPIECE

This application is a continuation-in-part of copending application Ser. No. 70,787, filed Sept. 9, 1970, now U.S. Pat. No. 3,644,118, which application is in turn a continuation-in-part of the then copending application Ser. No. 768,076, filed Oct. 16, 1968, now U.S. Pat. No. 3,560,998. This application is also a continuation-in-part of copending application Ser. No. 818,228, filed Apr. 22, 1969, now U.S. Pat. No. 3,576,099.

The present invention relates to electronic timekeeping devices and more particularly to an electronically regulated timekeeping device employing a master frequency standard of relatively high frequency and an electronic frequency converter to provide lower frequency drive signals at the desired timekeeping rate through suitable actuating means to a timekeeping display. The concepts disclosed herein are particularly adapted for use in electronic wristwatches or the like where compact construction and low power dissipation are essential.

Battery-powered wristwatches and other small timekeeping devices of various types are well known and are commercially available. One such device which has proven to be quite successful commercially is shown and described in assignee's United States Reissue Patent No. RE 26,187, reissued Apr. 4, 1967, to John A. Van Horn et al., for ELECTRIC WATCH. Electric watches of this type employ a balance wheel and a hairspring driven by the interaction of a current-carrying coil and a magnetic field produced by small permanent magnets. Other types of mechanically-regulated, battery-operated wristwatches are also known.

Considerable effort has also been directed toward the development of high accuracy wristwatches which do not employ electromechanical oscillators as the master speed reference. One approach which has been considered and has been subjected to substantial investigation is the use of completely electronic circuits to generate a master drive signal for the time display. For example, it has been proposed to provide a low frequency oscillator or pulse generator operating at the desired timekeeping rate for a direct drive of the time display through an electromechanical energy converter. However, difficulties have been encountered in implementing this, including the difficulty of providing a suitable stable low frequency oscillator of realistic size and power consumption for use in a wristwatch.

Alternatively, there has been considered the use of a high frequency oscillator as a frequency standard in conjunction with frequency conversion circuitry to provide a drive signal at the timekeeping rate. Unfortunately, there has not heretofore been available an oscillator/frequency converter combination having not only the required frequency stability, but also sufficiently low power consumption and small size to be practical for use in a battery-powered wristwatch.

The present invention overcomes the aforementioned difficulties in providing a battery-operated wristwatch employing a purely electronic frequency standard. The construction employed includes a relatively high frequency oscillator and a low power integrated circuit frequency divider coupled with a time display and suitable time display actuator. The circuitry includes an ultra low power integrated circuit, free-running multivibrator, and frequency divider constructed of a series of stages of integrated transistor circuitry so arranged that current flow through the circuit takes place only during circuit state transitions and not during the stable periods between transitions. The required circuitry can be constructed of relatively inexpensively components, thereby making the new electronically controlled wristwatch commercially competitive with conventional spring-driven and electric watches.

The circuit is characterized, as previously mentioned, by small size and ultra low power consumption. The primary frequency source is of a sufficiently high frequency to avoid the problems heretofore encountered with low frequency, direct drive of the timekeeping display, yet not so high as to require an excessive number of frequency divider stages. Utilization of even a large number of divider stages without excessive power consumption is achieved by a circuit arrangement in which circuit state transitions in response to operation of the primary frequency source are responsive to signal voltage transitions rather than current or power level changes.

The foregoing is achieved in the present invention by provision of a frequency divider constructed of a series of stages of transistor integrated circuitry, including transistors of opposite conductivity types, arranged in a complementary configuration, with a transistor of one conductivity type serving as a load circuit for a transistor of another conductivity type. Preferably, the free-running multivibration primary frequency source is also constructed in this manner.

A preferred embodiment is comprised of a plurality of metal oxide semiconductor (MOS) transistor integrated circuit stages arrayed in a complementary P- and N-channel configuration, both for the primary frequency source and the divider. A suitable number of divider stages is employed to convert the primary frequency to a 1 Hz drive signal for the time display.

In accordance with the present invention, utilization of electronic circuitry as described above, together with an integrated electro-optic display, are incorporated in a timekeeping system capable of providing an effectively visible display under daylight conditions without excessive power consumption.

Briefly, the improved electronic timekeeping device of the present invention comprises an integrated light-emitting diode display, an integrated circuit for generating a timekeeping signal, a display drive unit adapted to be manually interrogated, and a suitable time setting mechanism. The electro-optic display may be provided in one of several forms with the preferred arrangement being a 7-bar segment array for each of the time digits used. Alternatively, a 13-element array for each of the time digits to be presented may be substituted.

The display drive unit includes suitable counting and other digital logic and memory circuitry which operates in response to the low frequency output of the frequency divider to actuate the time display indicators in the proper manner to present an accurate time display.

In order to assure minimum power consumption, the display drive unit includes an interrogation and scanning mechanism to eliminate power consumption when the time display is not actually being consulted. When the user wishes to determine the time, the actuator is manually operated and power is provided to the
display indicators. For additional power conservation, the display is periodically interrupted, but at a sufficiently rapid rate to exceed the time of persistence of human vision, thereby providing the view with an illusion of a continuous display.

The time setting function is accomplished by selectively adjusting the memory states of the display drive unit to produce gross variations in the indicated time. Accordingly, it is an object of this invention to provide an improved electronically regulated timekeeping device.

It is another object of this invention to provide an improved electronically regulated timekeeping device characterized by high accuracy, small size, and low power dissipation.

It is a further object of this invention to provide an electronically regulated timepiece as described above constructed of relatively inexpensive components, yet retaining the required accuracy and compactness to provide a commercially satisfactory product.

It is also an object of this invention to provide an electronically regulated timepiece including an electronic primary frequency source of relatively high frequency and a frequency divider, the circuitry of the frequency source and the frequency divider being so arranged that current flow through the circuit takes place only during circuit state transitions and not during the stable periods between transitions.

It is a further object of this invention to provide such an electronically regulated timepiece in which the circuit state transitions in the frequency divider circuit stages are initiated in response to a change in voltage level rather than power or current level.

Another object of the present invention is to provide an improved electronic oscillator.

Another object of the present invention is to provide a simplified integrated circuit oscillator comprised of a complementary MOS inverter controlled by a crystal or other frequency regulation device.

It is another object of this invention to provide an electronically regulated timekeeping device comprised of a series of stages of transistor integrated circuitry including transistors of opposite conductivity types arranged in complementary configuration with a transistor of one conductivity type serving as a load circuit for a transistor of another conductivity type.

It is an additional object of this invention to provide an electronically regulated timekeeping device including an integrated circuit high frequency oscillator and frequency divider formed of a plurality of metal oxide semiconductor transistor stages to produce timekeeping pulses, a time display, and actuating means responsive to the timekeeping pulses for operating the time display.

It is also an object of this invention to provide an electronically regulated timekeeping device employing an oscillator/frequency converter combination including a plurality of integrated circuit metal oxide semiconductor transistor stages, each stage being constructed of an array of metal oxide semiconductor transistors in complementary N- and P-channel configuration.

It is an additional object of this invention to provide an electronic timekeeping device employing an electronic frequency divider characterized by extremely low power dissipation.

It is yet a further object of this invention to provide an electronic timekeeping device having an integrated circuit frequency divider as described above including a plurality of metal oxide semiconductor transistor stages, each stage including a plurality of transistors arranged so that the load circuit for a given transistor includes another transistor of opposite conductivity type.

Another object of the present invention is to provide a fully electronic timekeeping device suitable for wristwatch use.

A further object of this invention is to provide an electronic wristwatch having a completely non-mechanical time display.

It is yet a further object of this invention to provide a wristwatch with an electro-optical time display and with solid state integrated circuitry to provide timekeeping signals and display actuation.

It is yet a further object of this invention to provide a completely non-mechanical wristwatch with an illuminated digital time display in the form of a plurality of integrated arrays of light-emitting diode elements selectively actuated to present an illuminated time display.

It is also an object of this invention to provide a wristwatch having an electro-optical time display including a plurality of selectively illuminated elements and circuitry for periodically interrupting the illumination of the display at a rate sufficiently rapid to present an illusion of a continuous display.

It is another object of the invention to provide a timekeeping device having such an interrupted electro-optical timekeeping display which is normally inactivated to reduce the power consumption of the display.

It is a further object of this invention to provide an electronic timekeeping device providing a non-mechanical digital timekeeping display in the form of a plurality of integrated arrays of solid state light-emitting diode elements selectively activated by an electronic translating circuit responsive to periodic timekeeping pulses and having means for periodically interrupting the illuminated display at a rate sufficiently rapid to provide the illusion of a continuous display, together with means for maintaining the display in normally inactive condition and subject to interrogation on demand to provide the time display readout and having semi-automatic means for resetting the time display to maintain accurate timekeeping.

These and further objects and advantages of the invention will be more apparent upon reference to the following specification, claims, and appended drawings, wherein:

FIG. 1 is an overall block diagram of the electronically controlled timekeeping device in accordance with this invention;

FIG. 2 is a circuit diagram of a suitable embodiment of the frequency standard shown in FIG. 1;

FIG. 3 is a waveform diagram pertinent to the operation of the circuits described herein;

FIG. 4 is a block diagram showing the construction of the frequency converter shown in FIG. 1;

FIG. 5 is a circuit diagram of a practical embodiment of a frequency divider circuit suitable for use in the frequency converter of FIGS. 1 and 4;

FIG. 6 is a circuit diagram of a preferred oscillator construction usable as the frequency standard of FIG. 1;
FIG. 7 is a perspective view of an electronic timekeeping device having a digital time display and constructed in accordance with the present invention; FIG. 8 is an enlarged view of a portion of the display face illustrating the 13 element digital display devices; FIGS. 9A-9F are enlarged fragmentary cross-sectional views showing the construction of the integrated light-emitting diode dot matrix of FIG. 8 taken generally along lines 9-A in FIG. 8; FIG. 10 is a block diagram showing the construction and operation of the timing signal generating unit, the display interrogation and scanning unit, the display drive unit, and the time setting mechanism; FIG. 11 is a representation of a combined setting control and display interrogating mechanism; FIG. 12 is an enlarged view showing a preferred digital display indicator in the form of a 7-bar segment array; FIG. 13 is a block diagram of a strobing arrangement for the display of the present invention; FIG. 14 shows the circuit connections for a 7-bar segment numeral of the type illustrated in FIG. 12; FIG. 15 is a more detailed block diagram of the strobing system of FIG. 13; FIG. 16 is a circuit diagram showing the connections for all the bar segment numerals of the display; and FIG. 17 shows a modified construction showing an arrangement for displaying the seconds using the same numerals as are used for the minutes.

Referring now to FIG. 1, there is shown a block diagram of an electronically regulated timekeeping device in accordance with this invention. The device, generally indicated at 10, includes a frequency standard 12, frequency converter 14, a time display 16, and a display actuating means 18 coupling time display 16 to frequency converter 14. Frequency standard 12 and frequency converter 14 are constructed of a plurality of stages of transistor integrated circuitry to achieve compactness and a low order of power consumption. To achieve ultra low power consumption, however, it has been found necessary to construct the circuitry in such a manner that current flows only during circuit state transitions and not during the stable periods between transitions.

This is best accomplished by employment of a circuit stage configuration including transistors of complementary conductivity types, with a transistor of one conductivity type serving in the load circuit for a transistor of opposite conductivity type. The circuits should employ transistors which switch in response to changes in voltage rather than current or power levels, and are preferably formed of metal oxide semiconductor (MOS) transistor integrated circuits such as described more fully hereinafter.

Time display 16 may take several suitable forms, such as the conventional watch face and cooperating second, minute, and hour hands shown. In that case, display actuating means 18 is preferably a suitable miniaturized electromechanical energy converter responsive to the periodic drive signal provided by frequency converter 14.

Frequency standard 12 provides a primary or master signal at a frequency substantially in excess of that employed in the actual operation of time display 16 and actuating means 18. Accordingly, frequency converter 14 is provided to reduce the frequency of the master signal. This produces the drive signal which operates the display actuating means 18. In a practical embodiment, a standard frequency of at least about 5 kHz and a drive signal rate of 1 Hz for direct drive of the second hand are preferred, together with a conventional gear train mechanism to operate the minute and hour hands.

The construction of a suitable frequency standard oscillator 12 is illustrated in FIG. 2. The circuit embodies the concepts described above, viz., complementary construction with transistors of opposite conductivity type serving mutually in load circuits for each other, and current flow only during circuit state transitions and not during the steady state periods between transitions.

In the preferred embodiment having elements responsive to changes in voltage rather than current or power levels, the circuit comprises two pairs of metal oxide semiconductor (MOS) transistors denoted 20 and 22. Transistor pair 20 includes a P-channel transistor 23 and an N-channel transistor 24. A source terminal 28 of P-channel transistor 23 is coupled to a positive power supply at 30 while source terminal 32 of N-channel transistor 24 is connected to ground 34. Drain terminals 36 and 38 of P-channel transistor 23 and N-channel transistor 24, respectively, are coupled together at 40. Also, gate terminals 42 and 44 of P-channel transistor 23 and N-channel transistor 24, respectively, are coupled together at 46.

Transistor pair 22 is similarly constructed and includes a P-channel transistor 48 and an N-channel transistor 50. A source terminal 52 of P-channel transistor 48 is coupled to positive power supply at 30 while a source terminal 58 of N-channel transistor 50 is connected to ground 34. Drain terminals 54 and 56 of P-channel transistor 48 and N-channel transistor 50, respectively, are coupled together at 60. Also, gate terminals 62 and 64 of P-channel transistor 48 and N-channel transistor 50, respectively, are coupled together at 66.

As is known, MOS transistors are ordinarily provided with substrate terminals. While these have been omitted here, in the interest of clarity, it should be understood that for P-channel transistors 23 and 48, substrate connections are made to the positive power supply at 30 while for N-channel transistors 24 and 50, substrate connections are made to ground.

Common drain terminal 40 of transistor pair 20 is directly coupled to common gate terminal 66 of transistor pair 22. Also, common drain terminal 60 of transistor pair 22 is coupled through a feedback capacitor 68 to common gate terminal 46 of transistor pair 20. A further feedback path is provided by a resistor which is connected from the common junction points 40 and 66 to common gate terminal 46.

As may be appreciated, free-running multivibrator operation is achieved by the feedback paths and direct coupling described, with the frequency of oscillation being determined by the values selected for capacitor 68 and resistor 70.

Two frequency standard outputs, hereinafter denoted as F and F, are provided. Output F is taken from common drain terminal 60 of transistor pair 22, while output F is taken at common drain terminal 40 of transistor pair 20.
In operation, frequency standard oscillator 12 provides squarewave outputs F and F' at a frequency determined by capacitors 68 and resistor 70. The output F' is at approximately the power supply voltage when output F is at ground. Conversely, the output F is at approximately the power supply voltage when output F' is at ground.

The operation may best be understood by first considering transistor pairs 20 and 22 separately. For transistor pair 20, if the voltage at common gate terminal 46 is sufficiently above a certain minimum threshold voltage, P-channel transistor 23 will be in its nonconductive (OFF) state and N-channel transistor 24 will be in its highly conducting (ON) state. Under those conditions, common drain terminal 40 will essentially be shorted to ground through ON transistor 24 and the signal output F will be a low voltage. This will be referred to hereinafter as the ZERO state. On the other hand, if the voltage appearing at common gate terminal 46 is sufficiently below the threshold, the conductive states are reversed with N-channel transistor 24 being OFF and P-channel transistor 23 being ON. Under these conditions, common drain terminal 40 is shorted to the power supply terminal 30 through ON transistor 23 and the output F is at a high voltage. This will be denoted as the ONE state. Operation of transistor pair 22 is identical to that of transistor pair 20.

As previously explained, transistor pairs 20 and 22 are interconnected. Thus, the input at common gate terminal 66 is the same as the output at common drain terminal 40. If the output F is ONE, the input to common gate terminal 66 is high and N-channel transistor 50 is ON. Common drain 60 is then shorted to ground and output F is ZERO. Conversely, if the voltage at common drain terminal 40 is low, P-channel transistor 48 is ON and output F will be ONE.

To understand the mechanism of transition between ONE and ZERO states, assume that the common drain terminal 40 is at a high voltage, i.e., F is ONE. Common drain terminal 60 is then at a low voltage, i.e., F is ZERO. Under these conditions, a charging path for capacitor 68 exists from power supply terminal 32 through transistors 23, resistor 70, capacitor 68, and transistor 50 to ground whereby a positive voltage across the capacitor in the direction shown is established.

Since the positive side of capacitor 60 is coupled to common gate terminal 46 of transistor pair 20, the voltage there rises with the voltage across the capacitor, ultimately reaching a level exceeding the threshold voltage for N-channel transistor 24. This causes an inversion of the conductivity states of transistors 23 and 24, and output F switches from ONE to ZERO. Since common drain terminal 40 (output F') is directly coupled to common gate terminal 66 in transistor pair 20, the voltage there falls below the threshold voltage of N-channel transistor 50. This causes an inversion of conductivity states of transistors 48 and 50, and output F switches from ZERO to ONE.

Since the voltage across capacitor 68 cannot change instantaneously, the rapid voltage rise of output F is transmitted back to common gate terminal 46 of transistor pair 20. The latter, previously at or slightly above the threshold voltage, is now driven to a large positive value. This insures that the common drain output 40 (F) will remain at ZERO.

With conductivity states of the circuit reversed, capacitor 68 discharges to ground through resistor 70 and N-channel transistor 24. After capacitor 68 has been discharged, it begins to charge again but in the sense opposite to that indicated in FIG. 2, through P-channel transistor 48, capacitor 68, resistor 70, and N-channel transistor 24 to ground.

The charging process continues until the voltage at common gate terminal 46 falls to the threshold voltage for N-channel transistor 24, whereupon the conductivity states of transistors 23 and 24 again switch. Common drain terminal 40 of transistor pair 20 and common gate terminal 66 of transistor pair 22 both rise toward the power supply voltage as transistor 23 begins to conduct. This changes output F from ZERO to ONE. Also, this causes the conductivity states of transistors 48 and 50 to reverse, which changes output F from ZERO to ONE.

Since the voltage across capacitor 68 cannot change instantaneously, the output F at common drain terminal 60 is coupled directly to common gate terminal 46 maintaining transistor 23 OFF and transistor 24 ON. At this time, the same charging path for capacitor 68 as existed originally now exists again and the previously described process is continuously repeated. The resulting squarewave outputs F and F' are shown in FIGS. 3a and 3b.

The above-described circuit possesses several distinct advantages for use in the electronic watch of this invention. However, it should be appreciated that other oscillator circuits, capable of providing highly stable operation, low power consumption, small size, etc., may be substituted.

The required frequency conversion between the frequency standard signals and the low frequency drive signal may best be accomplished by utilization of a multistate binary frequency divider illustrated schematically in FIG. 4. Frequency converter 14 includes a plurality of series connected stages, four of which are shown. Each stage is provided with a pair of input terminals and a pair of output terminals. The inputs to first stage 71 are provided by the F and F' outputs of frequency standard oscillator 12. Correspondingly, the input to second stage 72 is provided by the outputs of first stage 71, denoted F1 and F1'. This is continued for all remaining stages whereby the output of the nth stage 74 provides inputs Fm and Fm' to the nth stage 76. Stage 76 provides an output Fw which constitutes the drive signal for display actuating means 18.

Each of the stages in frequency converter 14 serves to divide the input to that particular stage by 2. Thus, a succession of n stages provides division by 2^n. If the frequency of output signal Fw is to be 1 Hz, frequency f of the standard signal must be a power of 2 and the number of stages n must be chosen in accordance with the relationship: n = log2 f. For example, frequency standard oscillator 12 must operate at 4096 Hz with a frequency converter 14 having 12 stages (n = 12) to achieve a drive frequency of 1 Hz.

To achieve suitably low power dissipation levels to render such a multistage counter arrangement practical for use in a battery-powered wristwatch, it has been found preferable to employ integrated circuits of a par-
ticular type as now described in detail. The particular circuitry which has been employed here is of the type described in connection with FIG. 2 above employing pairs of complementary voltage-level sensitive transistors so arranged that transistors of opposite conductivity type serve mutually in load circuits for each other. Again, the circuit construction is preferably such that current flow occurs only during state transitions. To achieve compactness and low power consumption, integrated circuit construction should be employed here as in FIG. 2.

The construction and operation of a suitable embodiment employing complementary MOS circuitry will now be described in connection with FIGS. 3 and 5.

As illustrated in FIG. 5, the circuit is constructed of a series of MOS transistor pairs, some of which serve signal transmission or gating functions and others of which serve frequency conversion or logic functions. These will be denoted as transmission pairs and logic pairs, respectively.

Specifically, the circuit comprises a first transmission pair 78 including a P-channel transistor 80 and N-channel transistor 82 connected source-to-source at 84 and drain-to-drain at 86. Gate 88 of P-channel transistor 80 is connected to the F input while gate 90 of N-channel transistor 82 is connected to the F input. As will be understood, the F and F inputs constitute the high frequency inputs which are divided by a factor of 2 in each stage of frequency converter 14 shown in FIG. 4.

A second transmission pair 92 includes a P-channel transistor 94 and an N-channel transistor 96 coupled source-to-source at 98 and drain-to-drain at 100. Gate 102 of N-channel transistor 96 is connected to the F input while gate 104 of P-channel transistor 94 is connected to the F input. Common source terminal 98 of transmission pair 92 is connected to common drain terminal 86 of transmission pair 78.

A first logic pair 106 is formed of a P-channel transistor 108 and an N-channel transistor 110, connected at a common gate terminal 112 and at common drain terminal 114. Common gate terminal 112 is connected to output 86 of transmission pair 78. A source terminal 116 of P-channel transistor 108 is connected to the power supply at 118 while a source terminal 120 of N-channel transistor 110 is connected to ground at 122.

A second logic pair 124 is formed of a P-channel transistor 126 and an N-channel transistor 128 connected at a common gate terminal 130 to common drain terminal 114 of logic pair 106 and also by a feedback path 132 at common drain terminal 134 to input terminal 100 of transmission pair 92. A source terminal 136 of P-channel transistor 126 is connected to power supply 118 while a source terminal 138 of N-channel transistor 128 is connected to ground at 122.

The circuit of FIG. 5 also includes a second identical grouping of two transmission pairs 140 and 142 and logic pairs 144 and 146. Transmission pair 140 includes a P-channel transistor 148 and an N-channel transistor 150 connected source-to-source at 152 and drain-to-drain at 154. Gate terminal 156 of P-channel transistor 148 is connected to input F while gate terminal 158 of N-channel transistor 150 is connected to input F.

Transmission pair 142 includes a P-channel transistor 160 and an N-channel transistor 162 connected source-to-source at 164 and drain-to-drain at 166. Gate 168 of P-channel transistor 160 is connected to input F while gate 170 of N-channel transistor 162 is connected to input F.

Logic pair 144 includes a P-channel transistor 172 and N-channel transistor 174 having a common gate connection 176 and a common drain connection 178. Logic pair 146 includes a P-channel transistor 180 and an N-channel transistor 182 having a common gate terminal 184 and a common drain terminal 186. Terminals 188 and 190 of P-channel transistors 172 and 180 are connected to power supply at 118 while source terminals 192 and 194 of N-channel transistors 174 and 182 are connected to ground at 122. A circuit output F1 is provided at common drain terminal 178 of logic pair 144 while a second circuit output F1 is provided at common drain terminal 186 of logic pair 146.

Common drain terminal 186 also provides a feedback connection 196 to terminal 164 of transmission pair 142 and a second feedback connection 198 coupled to terminal 84 of transmission gate 78. As in the case of primary frequency source 12 described above, the substrate terminals for the various MOS transistors are not shown in the interest of clarity, but it should be understood that in all cases the substrates of P-channel transistors are coupled to the power supply and the substrates of N-channel transistors are coupled to ground.

To understand the operation of the above-described circuit, it should be recalled that for P-channel enhancement mode operation, a source to drain conductive path exists for low gate voltages. Increasing gate voltage reduces the conductivity, ultimately turning the transistor off when sufficient gate voltage is attained. Conversely, for N-channel enhancement operation, a conductive path does not exist for small gate voltages but rather is established when the gate voltage exceeds a minimum positive gating threshold.

By way of example only, for transmission pair 78, a ONE input state at F and a ZERO input state at F (high and low voltages, respectively) will maintain both transistors 80 and 82 in a nonconducting (OFF) state. Conversely, in transmission pair 140, both transistors 148 and 150 will be in the conductive (ON) state.

As to logic pair 106, a positive voltage at common gate terminal 112 exceeding the gating threshold will turn N-channel transistor 110 ON and P-channel transistor 108 OFF. This establishes common drain output terminal 114 at ground potential through conducting transistor 110. Conversely, a low voltage at common gate terminal 112 will turn P-channel transistor 108 ON and turn N-channel transistor 110 OFF, which establishes common drain terminal 114 at essentially the power supply potential through conducting transistor 108.

Description of the actual operation of the circuit illustrated in FIG. 5 is most conveniently given in terms of the operating states of the transmission pairs and logic pairs rather than in terms of the voltages associated with the individual transistors themselves. Thus, a transmission pair will be referred to as ON when both component transistors are conducting and OFF when both of the component transistors are nonconductive. Likewise, the output of a logic pair will be denoted as ONE when its common drain terminal volt-
age is high, i.e., when the input at the common gate terminal fails to exceed the gating threshold, thereby rendering the P-channel transistor conductive and the N-channel transistor nonconductive. Conversely, the output of a logic pair will be denoted as ZERO when the voltage at the common drain terminal is low, i.e., when the input at the common gate terminal exceeds the gating threshold, thereby rendering the P-channel transistor nonconductive and the N-channel transistor conductive.

With the foregoing in mind, and with reference to FIGS. 3a-3d and 5, assume that input states F and F' switch from ZERO to ONE, respectively, at time \( t_o \). Transmission pairs 78 and 142 go ON and transmission pairs 92 and 140 go OFF. Assume also that the output of logic pair 144 is high, thus making output state \( F_i = \text{ONE} \). (The alternative assumption of the output of logic pair 144 being low is also valid; this simply results in a one-half cycle shift in circuit operation as will be apparent from the description.) As a result, the input to logic pair 146 is ONE, and output state \( F_i = \text{ZERO} \), as illustrated in FIGS. 3c and 3d.

Common gate terminal 112 of logic pair 106 is directly connected to ground at 122 through the N-channel transistor 182 in logic pair 146, feedback path 198, and ON transmission pair 78. Consequently, P-channel transistor 108 is ON, and logic pair 106 is in the ONE state. The resulting high voltage at common gate terminal 130 of logic pair 124 maintain the N-channel transistor 128 ON, and the common output 134 is low.

At time \( t_1 \), the input states F and F' change to ONE and ZERO, respectively. Transmission pair 78 goes OFF and transmission pair 92 goes ON. The output of logic pair 106 is maintained in the ONE state since common gate terminal 112 is now coupled to ground through transmission pair 92, feedback path 132, and conducting N-channel transistor 128 in logic pair 124. (The latter is maintained conducting by the continued high output at common drain 114 of logic pair 106.)

The input transition at time \( t_1 \) also turns transmission pair 140 ON. This transfers the ONE state output of logic pair 106 to common gate terminal 176 of logic pair 144. Output 178 then switches to the ZERO state and circuit output state \( F_i \) goes to ZERO as shown in FIG. 3c. This in turn switches logic pair 146 to the ONE state, and circuit output state \( F_i \) goes to ONE as illustrated in FIG. 3d.

At time \( t_2 \), the input states F and F' again change to ZERO and ONE, respectively. This turns transmission pair 78 ON, and couples the ONE output of logic pair 146 to the input of logic pair 106 through feedback path 198. This establishes output 114 in the ZERO state which in turn establishes output 134 of logic pair 124 in the ONE state.

The input transition at time \( t_2 \) also causes transmission pair 140 to be turned OFF and transmission pair 142 to be turned ON, thereby connecting common gate terminal 176 of logic pair 144 through feedback path 196 to the output of logic pair 146. Since the latter is in the ONE state, this maintains the output of logic pair 144 in the ZERO state. This in turn maintains the circuit output \( F_i \) at ZERO, as shown in FIG. 3c.

Correspondingly, the low level at drain terminal 178 is connected to common gate 184 of logic pair 146.

This maintains P-channel transistor 180 conductive with common drain 187 still connected to the power supply. This keeps circuit output state \( F_i \) at ONE, as shown in FIG. 3d.

During the next input transition at time \( t_3 \), F and F' switch to ONE and ZERO, respectively, as shown in FIGS. 3a and 3b. This turns transmission pair 78 OFF and transmission pair 92 ON so that common gate terminal 112 of logic pair 106 is connected through feedback path 132 to output 134 of logic pair 124. The latter is already in the ONE state, since common drain terminal 114 was low during time \( t_2 - t_3 \) due to the connection of gate terminal 112 through transmission pair 78 and feedback path 198 to drain terminal 186. Accordingly, there is no change in the output states of either logic pair 106 or 124.

The input transition at time \( t_3 \) also causes transmission pair 140 to be turned ON and transmission pair 142 to be turned OFF. This causes common gate terminal 176 of logic pair 144 to be connected to the output of logic pair 106. The low signal level at gate 176 causes logic pair 144 to switch stages since the output 178 of logic pair 144 was low during time \( t_2 - t_3 \) due to connection of gate 176 through ON transmission pair 142 and feedback path 198 to drain terminal 186 of logic pair 146. As a result, circuit output \( F_i \) switches from ZERO to ONE, as shown in FIG. 3c. Likewise, logic pair 106 switches state and circuit output \( F_i \) goes from ONE to ZERO, as shown in FIG. 3d.

During the next input transition at time \( t_4 \), F and F' return to ZERO and ONE, respectively, as shown in FIGS. 3a and 3b. The circuit has returned to the initially described conditions and the sequence of operations described above is repeated. Comparing FIGS. 3a and 3c, and FIGS. 3b and 3d, it may be seen that outputs \( F_i \) and \( F_i \) provide complementary signal transitions in response to transitions in the inputs F and F' at a frequency exactly one-half the input frequency.

To achieve the desired degree of frequency division, it is merely necessary to combine a series of stages as described in FIG. 5 into a chain as shown in FIG. 4. Even a moderately large number of stages will be small enough for use in a wristwatch and will consume a realistically small amount of power.

FIG. 5 shows a modified oscillator construction in accordance with the present invention. The oscillator, generally indicated at 200 in FIG. 6, is a crystal controlled oscillator and may form the frequency standard 12 of FIG. 1. It comprises a complementary pair of integrated circuit enhancement transistors comprising P-channel transistor 201 and N-channel transistor 202 connected between positive supply terminal 203 and the other or grounded side of the power supply as indicated at 199. The F and F' outputs of the divider, such as divider 14 of FIG. 1, are developed on output leads 204 and 205 in FIG. 6. Transistors 201 and 202 form an MOS integrated circuit inverter and have connected across them a bias resistor 206, a quartz crystal 207, and a variable tuning capacitor 208. Connected between the positive power supply terminal 203 and the transistor gates is a protective diode 209.

The active element of the oscillator 200 of FIG. 6 is the complementary MOS inverter with the protective diode 209 between the gate and source of the P-channel transistor 201. This inverter can be either a
separate device or a part of the integrated circuit divider chain. The bias resistor 206 is used to bias the inverter into the linear region by making the input voltage equal to the output voltage under static conditions. Once the oscillator is under the control of the crystal, the bias resistor 206 is no longer a significant part of the circuit. A typical value for the bias resistor is about 22 megohms. Quartz crystal 207 is of the type normally used in oscillators where the Q is high and the series resistance is low. The shunt capacitance of the crystal should be less than 10 picofarads. Tuning capacitor 208 is used to adjust the oscillator over a narrow range of frequencies. The value of this capacitor is normally between 0.5 and 5.0 picofarads. Oscillator 200 provides the two-phase output required by the first stage of the divider chain. If another oscillator were used with a single phase output, it would be necessary to add an inverter either as a part of the oscillator or a part of the divider chain to shift the phase 180° and provide the two-phase input required by the divider.

The gate protective diode 209 is desirable because in MOS transistors it is easy to permanently damage a transistor by applying a voltage to the gate which is higher than the source or substrate voltage. A high potential on the gate will cause arcing across the gate dielectric which will create pin holes in the dielectric and alter the transistor characteristics. By adding the diode 209 between the gate and source of transistor 201, a current path is provided when the gate voltage is higher than the source of potential.

In the foregoing there has been described an electronically regulated timekeeping device characterized by sufficiently small size and low power dissipation to be practical for use in a device of wristwatch size. While the preferred embodiment and certain especially significant operating conditions have been set forth in detail, it should be understood that various modifications will be apparent to those skilled in the art in light of the foregoing description. These include, for example, the substitution of other circuit designs for the frequency standard oscillator described in FIGS. 2 and 6, as well as substitution of alternative time display means for the watch face and hands illustrated in FIG. 1. One such modification contemplated is an optical display providing an illuminated time indication. In this case, display actuating means 18 is a simple integrated circuit switching means providing selective actuation of the display elements in response to the drive signal output of frequency converter 14. A variation of transistor types for the latter circuit, consistent with the requirements set forth herein, are also possible.

The display has been described in only general terms, it being understood that it can assume any one of several forms. The most conventional form for accumulating the output of the last stage of the divider and further subdividing it for eventual display of time is to use as low frequency (0.5 to 64 Hz approximately) output to control the speed of motor (transducer) which drives a conventional watch-type gear train with hands attached to the shafts of appropriate gears. The motor can take several forms, such as reciprocating, continuous rotation, or stepper switch, and the like. An example of one form a mechanical actuator and display may take is that shown and described in my copending application Ser. No. 726,090, filed May 2, 1968, now U.S. Pat. No. 3,538,703, the disclosure of which is incorporated herein by reference.

Another form which the display can take is to replace the gear train (mechanical computer) with electronic circuits to perform the same function of subdividing and storing the low frequency output of a last stage of the divider. This stored information is then decoded in such a way as to selectively activate light-emitting or light-reflecting areas which create a digital display of the time stored in the electronic circuits. In order to conserve power, these electronic circuits can also be made using complementary MOS transistors with or without protective diodes in the inputs. In the case of a completely solid state watch, the numeral can be formed using such well known devices as miniature incandescent bulbs, light-emitting diodes, or liquid crystals, as well as lesser known devices, such as ferroelectric crystals or electro-luminescent displays, and others. FIG. 7 shows a watch constructed in accordance with the present invention incorporating an electro-optical actuator and display.

With reference now to FIG. 7, there is illustrated a wristwatch, generally indicated at 210, having a watchband 212, and a time display face, generally indicated at 214. Wristwatch 210 includes a casing 216 for housing the time display unit and an electronic system including a time signal generating unit circuitry for translating the time signal into mechanical form for the electro-optical display, a setting mechanism, and display interrogation and scanning means described in more detail hereinafter. A slide actuator 218 is mounted in a slot 220 in the side of casing 216 to actuate the setting mechanism and to operate the display interrogation and scanning mechanism also as hereinafter described.

In the embodiment of FIG. 7, four digital display indicators 222, 224, 226, and 228 are provided for presenting the time display in digital form. Face 214 inclines upwardly at an angle from housing 216 to be readily viewable by the wearer of the watch when the wearer's arm is naturally raised to bring the watch into view.

Digital display indicators 222 through 228 are preferably formed of a plurality of display elements selectively activatable to provide a readily visible time display. In one arrangement, the indicators each comprise an array of thirteen properly arranged semiconductor light-emitting diodes. As illustrated, the four display indicators are arranged across face 214, to present a four digit display of hours and minutes, but it should be understood that a six unit display including two seconds digits may be provided.

The nature and construction of the light-emitting diode arrays will be described more fully hereinafter in connection with FIGS. 9a–9f. However, as illustrated in FIG. 8, each array is formed of three columns of diodes 230, 232, and 234. Left and right columns 230 and 234 each comprise five diodes, while center column 232 comprises three diodes.

Each diode is provided with a separate path for electrical actuation. The thirteen individual leads 236 are connected respectively to one of the diode elements, e.g., on the reverse side as indicated in FIG. 8. A common return path 238 connects all the diodes and terminates as shown in a single return path 240. By selec-
tively actuating various combinations of diodes over leads 236 and 240, all of the digits between 0 and 9 may be readily synthesized. Thus, to represent the numeral 0, all of the diodes would be illuminated except that at the center, i.e., the middle element of column 232. Likewise, to display the numeral 1, all of the elements in either of columns 230 or 234 would be illuminated. Other numerals would be represented in a similar fashion.

It should be pointed out that light-emitting solid state diodes, and even thirteen element display indicators as described above, are known for alphanumeric display purposes and it should therefore be understood that the use per se of such an arrangement does not constitute part of this invention. However, employment of an integrated solid state matrix of light-emitting diodes having certain carefully selected properties as hereinafter detailed, in conjunction with the electronic system disclosed herein, has been found to be quite important to successful practice of the invention.

As mentioned above, display indicator 222 comprises a thirteen element array coupled to suitable logic and memory circuits to display minutes in units from 0 to 9. The adjacent indicator 224 is arranged to display tens of minutes from 0 to 5. By selective actuation of indicators 222 and 224, the full range of minutes from 0 to 59 may be displayed.

Correspondingly, display indicator 226 is arranged to display hours in selected units from 0 to 9, while indicator 228 is arranged to display selected tens of hours in units from 0 through 2, whereby the hours from 1 through 24 may be displayed.

It should be appreciated, however, that it may be preferable to provide only a 12 hour time cycle. In that event, indicator 228 need not comprise an entire thirteen element array. Rather, it may be formed of a column of five diode elements, such as column 230 or 234 (in FIG. 8). In that case, all of the elements are illuminated to display the hours 10, 11, and 12, but are otherwise not illuminated. Accordingly, for the hours 1 through 9, only a three digit display is necessary.

FIGS. 9a–9f show the construction of one of the thirteen element display indicators such as indicator 222. As previously mentioned, each of the indicators comprise an integrated array of thirteen light-emitting semiconductor diodes. As illustrated in FIG. 9a, individual diode elements, denoted at 242a, 242b, and 242c, are supported in a matrix 244 of transparent insulating material, such as glass or plastic, having suitable dielectric properties. Each of the diodes 242a–242c is formed of a substrate layer 246 of semiconductor material having substantially intrinsic properties, and the two layers 248 and 250 of P- and N-type semiconductor material respectively which actually form the diode. Electrical connections from leads 236 and 238 to each diode are made to substrate layers 246 and P-type layers 250 at 251a and 251b, respectively. The actual conductors are omitted from FIG. 9a in the interest of clarity, but it should be appreciated that the required connections may be made in any suitable fashion. For example, thin conductive leads are evaporated onto the P-type layer 250 to provide the desired common return path 238. Similarly, individual conductors 238 are evaporated on the reverse side of the indicator in an appropriate pattern to lie on the dielectric matrix 244 with contact only to one of the substrate areas 246 of each lead.

As will be appreciated by those skilled in the art, several techniques are available for manufacturing the above described integrated display indicators. The manufacturing technique per se does not constitute a part of this invention, and therefore only a brief description is presented in the interest of brevity. With reference to FIG. 9b, the manufacturing process begins with a composite diode element in the form of a monolithic substrate 246a having epitaxially deposited N and P type layers 248a and 250a. The composite structure constitutes a single diode approximately equal in size to the ultimately manufactured thirteen element array.

Individualizing the diode elements is accomplished as shown in FIG. 9c by transforming the epitaxially deposited N and P type layers into an array of 13 mesas or lands in the required configuration, e.g., by use of a commercially available ultrasonic cutting tool. As illustrated in FIG. 9c, substrate 246a is partially cut away leaving upwardly extending substrate bodies 246 of approximately the same thickness as the N- and P-type layers 248 and 250.

After cutting, a thin layer 252 of silicon dioxide is applied to the array as a passivation layer, and the transparent supporting matrix 244 is provided. (See FIG. 9d) This may be done in several ways. For example, a glass blank may be heated, and the partially processed display indicator pressed into the glass so that the latter fully occupies the interelement spacing resulting from the cutting operation. Alternatively, suitable transparent polymer material having appropriate dielectric properties may be used to encapsulate the partially processed structure.

At this point, the partially finished array is ready for the final processing steps and attachment of electrical contacts. As shown in FIG. 9e, a series of small openings 254 are formed in the surface of supporting matrix 244 directly above each of the diode elements. Then, the remaining portion of the monolithic substrate 246a is removed, e.g., by lapping to the lower surface of the matrix 244. This provides a flat surface with substrate bodies 246 only in the areas of the thirteen diode elements. Then, the electrical connectors are attached, as previously noted. The openings 254 may then be filled if desired to produce the integrated display indicator array shown in FIG. 9e.

An alternative finishing technique is illustrated in FIG. 9f. Here, instead of providing openings 254 in matrix 244, the latter is lapped down to expose the tops of P-type layers 250, and the thin conductive path 238 applied as before. Then, a unitary lens array 255 of epoxy or the like is formed, e.g., by molding on the upper surface of matrix 244. Lens array 255 includes thirteen raised lens elements 256 axially aligned with the diode elements to concentrate the light output for more efficient operation.

The lower surface of the array may be finished as before. Alternatively, it may be coated with a phosphorescent layer 258 as illustrated in FIG. 9f to permit a shorter duty cycle during scanning as later explained.

While the foregoing represents suitable techniques for manufacturing the diode indicator arrays, it should
be understood that other techniques may also be employed. In addition, it might be noted that the above description pertains to manufacture of a single indicator. However, an integrated structure of the four or six required indicators constituting the entire time display for the watch could also be provided.

As pointed out above, light-emitting diodes are well known. However, it has been found that most such diodes are totally unsuitable for use in a display indicator for an electronic wristwatch. It is also found that the nature of the semiconductor materials employed, the doping, etc., are the primary factors in determining suitability.

More specifically, satisfactory operation requires utilization of semiconductor materials and constructions yielding a satisfactory brightness level at an appropriate wavelength and with reasonable power consumption. Thus, it has been found that the semiconductor material employed should be such that the emission spectrum of the diode is centered at a wavelength between about 4500 Angstroms and about 6500 Angstroms and preferably centered between 5000 Angstroms and about 6300 Angstroms. Such materials would exhibit band gap energies varying between 1.9 and 2.75 electron volts, and preferably varying between 2.0 and about 2.5 electron volts.

Satisfactory operation under varying lighting conditions requires not only attention to the primary emitted wavelength, but also to the brightness level at a realistic level of current excitation. As will be appreciated, a brightness level sufficient for satisfactory perception under relatively dark conditions may be insufficient for visibility in full daylight. Accordingly, it has been found that the diode elements should produce a brightness level on the order of at least about 30 foot Lambers for a current flow of between 1 ma and 5 ma at about 1.5 volts to about 2.5 volts. Diode elements exhibiting a lower brightness may be employed depending upon the primary wavelength of emission as long as satisfactory visual stimulation is achieved.

To meet the foregoing requirements, it has been found that several different semiconductor materials may be utilized. These include gallium phosphide which produces a green emission in the vicinity of 5500 Angstroms. Silicon carbide, which is capable of producing emissions varying in wavelength between about 4100 and about 5600 Angstroms may also be employed. Further, certain semiconductor alloys, particularly gallium phosphide-aluminum arsenide or gallium arsenide-phosphide can be employed. This latter, for example, may be employed to produce light-emitting diodes having a peak emission at about 6300 Angstroms with good radiation efficiency. The required P-N junction can be formed by depositing the semiconductor alloy on an appropriate substrate such as gallium arsenide. The junction is formed by diffusion of a suitable acceptor material, such as zinc. The thirteen element display indicator as described herein may be formed in the manner described in connection with FIGS. 9a through 9f above.

With reference now to FIGS. 10 and 11, there is shown an electronic timekeeping system employing the thirteen element integrated display indicator previously described.

As illustrated in FIG. 10, the timekeeping system includes a time signal unit 260 including a primary timing signal generator 262 and a frequency divider 264. A display drive unit, generally noted 266, includes six separate drive channels 266a through 266f, each including a digital counter 270a through 270f and a decoding or translating unit 272a through 272f functioning in the manner hereinafter described. Each of display drive channels 266a through 266f is coupled to an individual time display indicator 274a through 274f, preferably of the type described in connection with FIGS. 8 and 9a through 9f above.

Associated with display drive unit 266 is a time setting-display interrogation switch 276 and a scanner control unit 278. Switch 276 is a three-stage five-position switch described in detail hereinafter. A first stage 280 provides an interconnection between frequency divider 264 and counters 270c and 270d to reset the time display. A second stage 282 provides an interconnection between frequency divider 264 and counter 270a and serves as the input for the timekeeping display signal. Switch stage 284 provides an interconnection between frequency divider 264 and the scanner control unit 278 to periodically interrupt the display during interrogation whereby substantial saving in power consumption may be effected.

Time signal unit 260 serves to generate the display drive signal, the time setting signal, and the interruption control signal for scanner control unit 278. To permit display of time of the nearest second, a timekeeping signal at a frequency of 1 Hz is needed. This is provided by frequency divider 264 over lead 286. For time display setting, it is found that a faster drive rate may be employed, e.g., 2 Hz. This is provided by frequency divider 264 over lead 314.

As noted, the display is scanned or interrupted at a rapid rate during viewing, to conserve power. However, if the interruptions are frequent enough and the duty cycle or "on time" is sufficient, an illusion of continuous display can be produced. For this purpose, an interruption rate of at least 30 Hz is preferred in a binary counting chain like frequency divider 264, a signal at 32 Hz (2⁶) is available, and is provided on lead 316. The signals on leads 286, 314, and 316 are provided through switch 276 for the various purposes as herein described.

Because several frequencies are needed, it will be appreciated that the two-stage arrangement shown including primary timing signal generator 262 and frequency divider 264 should be employed. In addition, it is found that the frequency of generator 262 should be substantially in excess of the frequencies needed for operating the display. This is because it has been found that production of a low frequency timing signal generator having a sufficient level of accuracy and meeting the necessary size and power consumption requirements, is quite difficult. In contrast, employment of a high frequency ultrastable multivibrator, for example, as described above or in pending United States patent application Ser. No. 802,571, filed Feb. 26, 1969, in the name of C. H. Rehe, II, now U.S. Pat. No. 3,568,091 and commonly assigned herewith, produces excellent results.

Frequency divider 264 may be of any suitable and desired circuit configuration, but preferably employs
circuitry of the type disclosed in FIGS. 4 and 5. In one embodiment, primary timing signal generator 262 is a free-running multivibrator pulse generator operating at a frequency of 524,288 (2²⁹) Hz, while frequency divider 264 comprises 19 stages of complementary MOS integrated circuit frequency dividers. This provides the output signal on lead 262 at the required 1 Hz frequency.

When connected to frequency divider 264 through switch stage 282, display drive channels 268a through 268f respond to the 1 Hz timing signal to produce an accurate seconds, minutes and hours display on time indicator units 274a through 274f. From comparison of FIGS. 7 and 10, it will be noted that the timekeeping device of FIG. 10 makes provisions for a seconds display while that of FIG. 7 does not. However, it will be appreciated that the seconds time display provided by indicators 274a and 274b may be added to the wristwatch of FIG. 7 (or removed from that of FIG. 10) without any significant departure from the techniques described herein.

Referring still to FIG. 10, the 1 Hz drive signal is connected through stage 282 of switch 276 and through lead 288 to the input of counter stage 270a which operates as a scale of 10 divider (i.e., mod 10). The output of counter stage 270a is connected to the input of counter stage 270b which operates mod 6. Accordingly, counters 270a and 270b together operate mod 60, whereby the 1 Hz input signal on lead 288 is divided down to produce an output signal from stage 270b on lead 290 at a frequency of 1 pulse per minute.

The latter signal is connected through a third counter stage 270c operating mod 10, and a fourth stage 270d operating mod 6 to produce a second mod 60 divider having an output signal on lead 292 at the rate of 1 pulse per hour. This signal in turn is connected to a fifth counter stage 270e operating mod 10, and sixth stage 270f operating mod 2 to control the hour portion of the time display.

Appropriate output connections are made from the internal stages of counters 270a through 270f to produce a unique binary code output assembly for each second of the 12 or 24 hour timing period. For example, the output code may be in the form of binary coded decimal in a 8-4-2-1 code, or in any other appropriate code. These signals in turn are transformed by decoders 272a through 272f including appropriate logic circuitry into a multilevel output code for actuation of the display indicators 274a through 274f. In the case of the thirteen element display indicators described in connection with FIGS. 8 and 9a through 9f, decoder units 272a through 272f each provide a thirteen element output code to the respective display indicators.

In FIG. 11, there is shown a specific representation of the time setting-display interrogation switch 276 shown in FIG. 10. Switch 276 comprises an elongated composite slide member formed of three electrically conducting portions 294, 296, and 298 with insulating spacers 300 and 302 separating conductive portions 294 and 296 and 296 and 298, respectively. Contact portions 304, 306, and 308 extend from conductive portions 294, 296, and 298, respectively, to engage with various ones of a plurality of fixed contact members generally denoted 309. A nonconductive actuator portion 218 extends from the end of conductive portion 294 out through the housing 216 as illustrated in FIG. 7. A compression spring 310 is secured in electrical isolation to conductive portion 298 to maintain slide switch 276 normally in the position shown. This corresponds to the normal operating position as hereinafter explained. Also, spring 310 allows switch 276 to be moved to the right as illustrated in FIG. 11 against the compressive spring force, and to return to the normal position when the switch is released. This corresponds to the interrogate position for the time display. In contrast, a detent mechanism 312 cooperates with actuator 218 when switch 276 is moved to the left making such motion relatively difficult in comparison to movement to the right. These positions are used for the time setting functions or to stop the watch completely.

As illustrated, the electrical input for switch stage 282 is provided by lead 286 from the 1 Hz output of frequency divider 264 through switch conductive portion 296. A suitable sliding contact mechanism provides the electrical connection. Switch stages 280 and 284 are energized by signals over leads 314 and 316, respectively, from outputs of frequency dividers 264 at frequencies of 2 Hz and 32 Hz. Again, suitable sliding contact mechanisms provide the electrical interconnection.

The first five fixed contact members 309 (from the left) are associated with switch stage 280, the second five fixed contacts are associated with switch stage 282, and the last five fixed contacts are associated with switch stage 284. As illustrated, for stage 280, the rightmost position, the normal position, and the leftmost position are electrically unconnected while the second position from the left, and the center position are connected by leads 318 and 320 to the input of divider stages 270c and 270d, respectively. For switch stage 282, the two left-hand positions are electrically unconnected, while the three right-hand positions are connected in common by lead 288 to the input of divider stage 270a. In switch stage 284, the leftmost position and the normal position are unconnected, while the remaining positions are connected to leads 319 through 323.

Referring back to FIG. 10, scanner control unit 278 is an electronic logic circuit whose purpose is to actuate decoders 272a through 272f in synchronism with the input drive signal on lead 322. The circuitry itself may be of any suitable form, for example, it may be a six input "inhibit" circuit which completes the power supply path for decoders 272a through 272f over signal leads 324a through 324f, respectively. When switch stage 284 is in the rightmost, center and second from left positions, as shown in FIG. 11, the 32 Hz output of frequency divider 264 is connected over lead 322 to periodically actuate scanner control unit 278. This periodically actuates decoders 272a through 272f which in turn periodically actuate time display indicators 274a through 274f with a changing pattern of drive signals to effect the desired time display. In other words, the input code provided by dividers 270a through 270f periodically is converted into the desired actuating code for the display indicators to produce the
required time display, but only when switch 276 is actuated to the interrogate position or during setting as later explained.

As will be appreciated, the persistence of human vision may be utilized to substantial advantage here since a relatively slow scanning rate may be employed with good perception while effecting a drastic reduction in power consumption. For example, an interrogation rate of 25 times per day for a period of about 5 seconds each may be assumed. In that case, with the thirteenth element display drawing about 1 ma per diode for a brightness of 38 foot Lamberts, a scanning rate of 32 times per second with an "on time" of approximately 4 milliseconds may be employed. This would produce an approximate power consumption of 25 ma hours per year. In contrast, a continuously operating display using the same elements but without interrogation and scanning would result in a power consumption on the order of 50 amperes per hour. Since marketability and consumer acceptance of battery-operated timepieces appear to require a battery replacement rate not exceeding approximately 1 per year, it should be appreciated that the power consumption reduction affected by the interrogation and scanning is a substantial factor in achieving success in accordance with this invention.

The operation of time interrogation and setting switch 276 may be described as follows. As illustrated in FIGS. 10 and 11, the normal operating position for switch 276 is with the moving contact projections 304, 306, and 308 on the second fixed contacts, i.e., the second position from the right as illustrated in FIG. 11. In this position, counters 270a through 270f continue to operate responsive to the 1 Hz signals from frequency divider 264 on lead 288. In this way, accurate time continues to be kept even when the display is inactive.

Interrogation is achieved by moving switch actuator 218 to the right to engage the contact projections 304 through 308 on slide members 294 through 298, respectively, with the rightmost fixed contacts 309. Movement to the right is resisted by compression spring 310 which normally biases the switch in the position illustrated. When switch 276 has been moved to the rightmost position, it may be seen that an electrical connection exists between lead 316 from the 32 Hz output of frequency divider 264 through lead 322 to scanner control unit 278. This actuates decoders 268a through 268f as previously described, thereby allowing the time display to be operated. In order to determine the time, the wearer simply moves the actuator lever 218 to the right. This causes time to be displayed on display indicators 274a through 274f for the duration of the time that the actuator is maintained depressed. The display is interrupted as previously explained, but the illusion of a constant display is produced by the persistence of human vision. When actuator 218 is released, spring 310 causes switch 276 to return to its normal position, whereby the timekeeping function produced by divider 270a through 270f continues but the display is disabled.

Various time setting functions are achieved by moving actuator lever 218 to the three positions to the left of normal in FIG. 11. Detent 212 serves to make movement of actuator lever 218 to the left somewhat difficult, thereby avoiding inadvertent operation of the setting mechanism, e.g., when time interrogation is intended. The first position to the left of normal for switch 276 provides a coarse time adjustment. Here, an electrical connection exists through switch stage 284 from the 32 Hz output of frequency divider 264 to scanner control unit 278, from the 1 Hz output of frequency divider 264 to divider 270a, and from the 2 Hz output of frequency divider 264 to the input of divider 270d. Hence, the watch continues to run (via stage 282), the display is actuated (via stage 284), and the time is represented by divider 270d, viz., the tens portions of the minutes display, is changed at the rate of two counts per second. In this way, the minutes display may be advanced 20 minutes per second and, correspondingly, the hour display may be advanced 1 hour in 3 seconds. This effects a coarse time correction as mentioned, or may be used to advance the watch rapidly during time zone changes.

Movement of slide switch 276 to the second position left of normal provides a fine adjustment of the time display by advancing the unit digit of the minutes display. In this position, an electrical circuit exists through switch stage 280 from the 2 Hz output of frequency divider 264 over lead 314, and lead 318 to divider stage 270c. Also, an electrical path exists between the 32 Hz output of divider stage 264 through switch stage 284 over lead 316, and lead 322 to scanner control unit 278. This is necessary so the user can observe the time change being effected. However, the watch preferably does not run at this time to facilitate accurate setting. Therefore, no electrical connection exists through switch stage 282 from the 1 Hz output of frequency divider 264 to divider stage 270a in this mode of operation.

Under these circumstances, the count of frequency divider stage 270c is changed at the rate of two counts per second whereby the time display may be changed a total of 9 minutes in 4-½ seconds and a total of 1 hour in 30 seconds. This alone, or in combination with the coarse adjustment provided in the previously described operating mode, allows rapid and convenient time setting.

Finally, the leftmost position of switch 276 provides no electrical connections between frequency divider 264 and display drive unit 266. Under these conditions, the wristwatch is effectively stopped. This allows the timepiece to be preset and then held in readiness prior to actuation at a precise instant, or permits the watch to be maintained completely inactive if desired for power conservation. (In the latter case, it may also be desirable to provide an additional switch contact or other means for disabling primary timing signal generators 262 and frequency divider 264 whereby a complete shutdown of the timepiece is achieved.)

From the foregoing, it will be appreciated that there has been provided a totally electronic wristwatch having no mechanical parts except the interrogation and setting actuator switch. At the same time, various problems encountered in past efforts to design such a wristwatch are overcome by the employment of an electro-optical display of small size and good visibility without excessive power consumption. However, several alternatives to the above described construction are also possible.
Thus, in addition to variations in the design of the logic circuit elements, as previously suggested, in the primary timing signal frequency, and in the corresponding number of stages of frequency divider 264, other display indicator configurations may also be employed. A preferred configuration is illustrated in FIG. 12 in the form of a seven bar segment indicator comprised of seven relatively elongated light-emitting diode elements formed as an integrated unit in the manner described in connection with FIGS. 8 and 9a through 9f. In such an arrangement, the diode elements themselves are substantially larger than in the thirteen element display indicator, with a correspondingly greater total illumination. On the other hand, an increase in power consumption by a factor of approximately 5 is encountered whereby it will be appreciated that a trade off between low power consumption and increased visibility may be necessary.

A further alternative would be to provide a suitable phosphorous screen in association with the light-emitting diode display indicators. This would be applicable either to the configuration of FIG. 8, as noted above, or the configuration of FIG. 12. This could permit a somewhat shorter "on time" for the interrogated display without substantial reduction in the level of visual perception.

As a further alternative, electro-optical display elements of the type disclosed in copending application Ser. No. 794,551, filed Jan. 28, 1969, in the name of John M. Bergey, and commonly assigned herewith, or miniature incandescent lamps arranged in seven or thirteen element arrays may be substituted for the light-emitting diodes herein disclosed. Other modifications within the scope of this invention will likewise occur to those skilled in the art in light of the foregoing description.

FIG. 13 shows a further modified wristwatch construction and illustrates the driving circuits for an electro-optical digital time display and particularly one incorporating light-emitting diodes of the type illustrated in FIGS. 9a through 9f. The wristwatch, illustrated generally at 330 in FIG. 13, comprises an oscillator 332 and divider 334 which oscillator preferably takes the form illustrated in FIG. 6 and with the divider preferably taking the form illustrated in FIGS. 4 and 5. In any event, oscillator 332 and divider 334 are preferably formed from integrated circuits comprising complementary connected MOS transistors. The output from divider 334 passes over lead 336 to a counting register 338. The output from the counting register 338 passes through selection gates 340, through input gates 342 to the decoder-driver 344 and, finally, to the light-emitting diode displays 346. Selection gates 340 also are connected to a strobe circuit 348 which controls the displays 346 by way of leads 350.

A manually operated demand switch 352 connects the positive terminal 354 of a suitable power supply, such as a 3 volt watch battery, to a timer 356. Timer 356 is connected by leads 358 and 360 between an intermediate stage of divider 334 and the strobe circuit 348. Lead 362 connects the strobe circuit to a later stage of divider 334. Finally, counting register 338 is adapted to be set by a signal from a setting circuit 364.

FIG. 14 shows a light-emitting diode display numeral, generally indicated at 366. The numeral is of the seven bar segment type illustrated in FIG. 12 and comprises light-emitting diode segments 368, 370, 372, 374, 376, 378, and 380. Electrical connections to the anodes of the light-emitting diodes are illustrated by leads 382, 384, 386, 388, 390, 392, and 394, labeled a through g, respectively. The common connection to the cathodes of all the segments of display numeral 366 is made through the common cathode connection lead 396.

FIG. 15 is a more detailed block diagram of the watch 330 and like parts bear like reference numerals to those appearing in FIG. 13. Oscillator 332 produces an output F on lead 398 and a complementary output F on lead 400 having a frequency of 32768 Hz. This timing signal passes through divider 334 to the counting registers comprising a divide by 10 register 402, a divide by 6 register 404, a second divide by 10 register 406, a second divide by 6 register 408, a third divide by 10 register 410, and a divide by 2 register 412. The outputs from these registers pass through selection gates 340 and input gates 342 to the decoder-driver 334. The outputs from the decoder-driver 334 are supplied to the display numeral leads a through h and an output from divider 334 at a frequency of 8 Hz is supplied by lead 414 to a divide by 10 counter 416 for a purpose more fully described below. Another output from divider 334 having a frequency of 256 Hz is supplied by lead 418 to a divider by 4 counter 420. A plurality of gates 422, 424, 426, 428, 430, and 432 are connected to the outputs of these latter two counters.

The drive system illustrated for the watch embodiment of FIGS. 13–15, provides an improved strobing action to activate the displays and conserve watch battery power. It also illustrates how the same set of numerals can be used to display minutes and seconds. The strobing is an extension of the pulsing technique previously described where the light-emitting diodes are periodically energized at a frequency sufficiently high to give the appearance of constant illumination.

As is apparent from FIG. 15, a common decoder 334 is used for all numerals to be displayed. The high frequency output of oscillator 332 is lowered in frequency by a series of binary divider stages in the divider 334. This divider produces several output frequencies, including a 1 Hz output which is fed into the counting registers 402 through 412 where it is further divided by 10, 6, 10, 6, 10, and 2 corresponding to the digits needed to display seconds, minutes and hours. The setting circuit 364 in FIG. 13 is associated with these registers and makes it possible to set the correct time into the registers. The binary coded decimal outputs of all the dividers in the counting registers are fed into six sets of selection gates 340. These gates are controlled by the strobe circuit 348 of FIG. 13 and the number passing through the input gates 342 into the decoder-driver 334 is determined by this strobe circuit.

In the operation of the system of FIGS. 13–15, the timer 416 controls the strobing circuit. When the demand switch is depressed, the minutes and hours are displayed for 1 and ½ seconds, and if the demand switch remains depressed, the display automatically switches to seconds. Therefore, it is necessary for the strobe circuit to strobe only four numerals at any one time, although it controls all six numerals. Later it will be shown how this circuit can be used to display the
seconds using the same numerals used to display the minutes.

After the strobing circuit 348 of FIG. 13 selects the register to be read, the time stored in that register (in binary coded decimal form) passes through the set of selection gates opened by the strobe circuit and through the input gates 342 which act as an interface to the decoder 334. This decoder changes the bcd information into the output necessary to form intelligible numerals.

The strobing circuit 348 not only chooses which counting register will be read, but also completes the anode circuit for the corresponding numeral. Therefore, only one numeral can be on at any one time, but because the strobing action takes place so rapidly, it appears that as many as four numerals are lighted simultaneously.

Referring to FIG. 15, the oscillator 332 is crystal controlled by crystal 207 and fine tuned by variable capacitor 208. In the preferred embodiment, the frequency of this oscillator is 32768 Hz. The divider 334 lowers the frequency in binary steps to at least 256 Hz, 8 Hz, and 1 Hz, although other designs may require other frequencies. The 1 Hz signal is fed into the first divide by 10 register 402 to accumulate and store the units of seconds. This carry output is fed into the divide by 6 register 404, which accumulates and stores the tens of seconds. This same process is repeated for the minutes and the hours. Each register has a set of bcd outputs. These outputs go into two-input NOR gates 340 which act as selection gates. A logic ONE on the other input of these gates will keep the bcd information from passing through. In this way it is possible for the strobe circuit to control which information from which register will pass to the decoder 334. This bcd information must pass through the input gates 342 and these gates are provided to prevent interference between the several outputs from the selection gates 340 as they enter the decoder 334. The tens of the hour does not require decoding and this output on lead 434 passes through an inverter 436 and then to the decoder-driver where it is used to energize the single segment of one or more of the input gates when it is in the ON state or in an OFF state to display the tens digit of time. The output of the decoder-driver 334 provides power to those segments which are to be activated to display the number corresponding to the bcd input number. In this case there are seven outputs plus the special output h for the tens of hours.

FIG. 16 shows all the numerals as they appear on the display and it is noted that with the exception of the hours display at 438 where the commonly connected segments 440 and 442 form the digit for the hour, all the other segments of all the numerals are connected in parallel. Thus, if all the anodes of all the numerals are connected to ground, all numerals in FIG. 16 would show the same number. This does not happen because the output of the strobe circuit 348 controls which anode is connected to ground through the transistors 444, 446, 448, 450, 452, and 454 for the particular numeral. As can be seen, separate transistors are provided for all six numerals to be displayed.

As was previously stated, a maximum of four numerals are activated at any one time. This is because hours, minutes, and seconds are never shown simultaneously. When the minutes and hours are displayed, seconds are blank and when seconds are displayed, hours and minutes are blank. This is controlled by the timer 356 and the strobe circuit 348. The divide by 4 circuit 420 in FIG. 15 takes the 256 Hz input signal from the divider and generates pulses which appear consecutively on the output lines 456 at a rate of 64 Hz. These strobing pulses are fed into NAND gates 422, 424, 426, 428, 430, and 432. These NAND gates have a logic ONE output unless all the inputs are logic ONE. For instance, NAND gate 432 must have a ONE input from the divider by 4 circuit 420 and the timer 356, in order to have a ZERO at ONE’ and a ONE at ONE. A ZERO at ONE’ passes the tens of hours signal to the decoder 334 and the ONE at ONE turns on the transistor 444 to complete the anode circuit for the tens of hours numeral. In order to have a ONE output from the timer 356, the pushbutton switch 352 must be manually depressed. This resets the counter 416 which counts the 8 Hz signal on lead 414 (FIG. 15) for one and one quarter seconds. The ONE from the timer goes to NAND gates 422, 424, 426, and 430 but due to inverter 458, a ZERO appears at the input of gates 428 and 432. Gates 428 and 432 control the seconds. Therefore, inverter 458 will not allow the hours and minutes and seconds to appear simultaneously. The seconds are activated after the one and one quarter seconds that the timer 416 is activated and the demand button switch 352 remains closed. At this time, the output of the timer 416 goes to ZERO, which causes the output of the inverter 458 to go to ONE. At the same time, the ONE from the demand switch 352 appears at the inputs of NAND gates 428 and 432. This means that when the signal from divider 420 appears at gate 428 or 432, the outputs will be activated and the seconds displayed. The input from the demand switch 352 is necessary on gates 428 and 432 to keep the seconds from displaying when the button of switch 352 is not depressed and the timer 416 is not counting, which is most of the time.

It can be seen from the above that it is a relatively simple matter to display the seconds using the same numerals that are used for the minutes. FIG. 17 shows such an arrangement in which the numerals 460 and 462 are used for both minutes and seconds. Each numeral is provided with a pair of transistors 464 and 466, 468 and 470, connecting the light-emitting diodes to ground. Transistors 464 and 466 are placed in parallel so that conduction of either one causes that numeral to display either the tens of minutes or the tens of seconds. The same thing applies to transistors 468 and 470 for the units minutes or seconds. The actual number is controlled by the decoder-driver 334.

While the drive system has been described in conjunction with the use of light-emitting diode segments of the type illustrated in FIG. 9, it is apparent that other electro-optical display devices may be used, such as liquid crystal segments. Furthermore, while described in conjunction with time display, it is apparent that the drive system may be used to display other information, such as the date, i.e., a calendar display, or temperature, without using additional display elements.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are
therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by United States Letters Patent is:

1. A timekeeping device of sufficiently small size and power consumption for use as a wrist watch comprising an oscillator including at least one pair of complementary MOS transistors and having a frequency of at least 5 kilohertz, a frequency divider coupled to said oscillator for reducing the frequency of the electrical signals from said oscillator, an electro-optical time display, a display actuator coupling said divider to said time display, said divider comprising a plurality of stages of transistor integrated circuitry, each stage comprising at least one pair of complementary MOS transistors, and an interrogator switch coupled to said display actuator whereby said display is energized by said actuator only upon operation of said switch.

2. A timekeeping device according to claim 1 wherein said oscillator transistors are formed of integrated circuitry.

3. A timekeeping device according to claim 1 wherein said display comprises a plurality of light-emitting diodes.

4. A timekeeping device according to claim 3 wherein said diodes give off light in the visible red region.

5. A timekeeping device of sufficiently small size and power consumption for use as a wrist watch comprising an oscillator including at least one pair of complementary integrated circuit MOS transistors, and electro-optical time display, a display actuator for actuating said time display in response to signals from said oscillator, frequency conversion means coupling said oscillator to said actuator for substantially reducing the frequency of the oscillator signals, said frequency conversion means comprising a plurality of stages of transistor integrated circuitry, each stage including a plurality of logic means and a plurality of signal transmission means coupling said logic means together, said logic means and said signal transmission means having control inputs and signal paths, with the conductivity states of said signal paths being switchable in response to changes in the signal at said control inputs, substantial current flow in said signal paths occurring only during transition between conductivity states, the logic means and signal transmission means in each of said stages of transistor integrated circuitry being comprised of first transistors of a predetermined conductivity type, and second transistors of opposite conductivity type, coupled together with transistors from one conductivity type serving as a load circuit for transistors of the opposite conductivity type, and an interrogator switch coupled to said display actuator whereby said display is energized by said actuator only upon operation of said switch.

6. A timekeeping device according to claim 1 wherein said display comprises a plurality of light-emitting diodes arranged to form digital numbers to the 10 base, each number being formed by a 7 bar segment array of diodes.

7. A timekeeping device according to claim 6 wherein a first electrode of said diodes are all connected in common, and a separate bipolar transistor coupled to a second electrode of the diodes for each number.

8. A timekeeping device according to claim 7 wherein the same numbers are connected to display both minutes and seconds.

9. A solid state wristwatch comprising an oscillator including at least one pair of complementary MOS transistors and forming a high frequency timing source, a frequency divider coupled to said oscillator for reducing the frequency of the electrical signals from said oscillator, said divider comprising a plurality of stages of transistor integrated circuitry, each stage comprising at least one pair of complementary MOS transistors, code generator means coupled to said divider and responsive to the output of said divider for establishing a multielement code having a unique code word for each unit time interval in a period, and a digital time display coupled to said code generator, said digital time display comprising a plurality of light-emitting diodes.

10. A wristwatch according to claim 9 wherein said divider comprises a binary counting chain of complementary MOS transistors.

11. A solid state wrist watch comprising a source of high frequency timing signals, a frequency divider coupled to said source for producing a low frequency timing signal, second, minute and hour dividers coupled in series to said low frequency timing signal, said second, minute and hour dividers each producing a binary code representing a one clock cycle period, a digital time display comprising a plurality of light-emitting diodes, decoders coupling said 8-4-2-1 code output signals to said light-emitting diodes, and timing means coupled to said display for periodically interrupting said display at a rate in excess of the timing signal applied to said second divider.

12. A solid state wristwatch according to claim 11 wherein said timing means is coupled to at least one intermediate stage of said frequency divider.

13. A solid state wristwatch according to claim 12 wherein said timing means comprises a strobe circuit coupled to said light-emitting diodes.

14. A solid state wristwatch according to claim 13 including a plurality of selection gates coupled between said second, minute and hour dividers and said light-emitting diodes, and means coupling said strobe circuit to said selection gates.

15. A solid state wristwatch according to claim 14 including a manually actuated demand switch coupled to said timing means.

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