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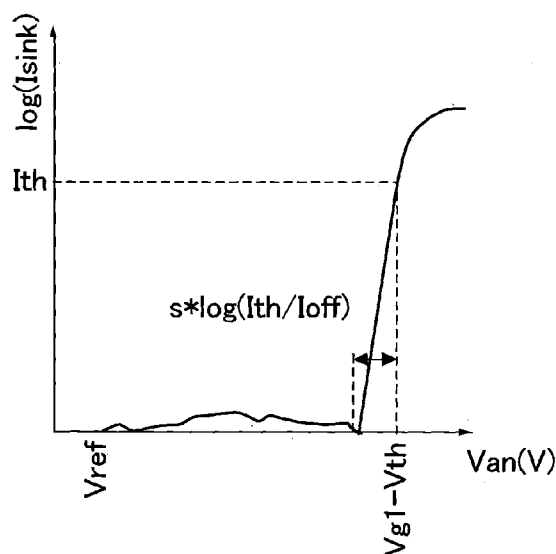
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(54) **Title:** PHOTOELECTRIC CONVERTER, PHOTOELECTRIC CONVERTER ARRAY AND IMAGING DEVICE

**FIG.3**



(57) **Abstract:** A photoelectric converter includes a first pn junction comprised of at least two semiconductor regions of different conductivity types, and a first field-effect transistor including a first source connected with one of the semiconductor regions, a first drain, a first insulated gate and a same conductivity type channel as that of the one of the semiconductor regions. The first drain is supplied with a second potential at which the first pn junction becomes zero-biased or reverse-biased relative to a potential of the other of the semiconductor regions. When the first source turns to a first potential and the one of the semiconductor regions becomes zero-biased or reverse-biased relative to the other semiconductor regions, the first pn junction is controlled not to be biased by a deep forward voltage by supplying a first gate potential to the first insulated gate, even when either of the semiconductor regions is exposed to light.



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## Description

PHOTOELECTRIC CONVERTER, PHOTOELECTRIC CONVERTER ARRAY  
AND IMAGING DEVICE

## CROSS REFERENCE TO RELATED APPLICATION

The present application is based on and claims priority from Japanese Patent Application No. 2011-222020, filed on October 6, 2011, the disclosure of which is hereby incorporated by reference in its entirety.

## Technical Field

[0001]

The present invention relates to improved photoelectric converters to convert optical information as optical intensity and wavelength and so on and an optical image into current, charge, voltage, or electric information including digital data, as well as to photoelectric conversion cells, photoelectric converter arrays comprised of the photoelectric conversion cells as the photoelectric converters and imaging devices incorporating such an array.

## Background Art

[0002]

A photocurrent flows through one end of a first pn junction with a photoelectric conversion function in an electrically floating state and is accumulated as charge for a certain period of time or accumulated charges are discharged by the photocurrent as will be described later. To detect a result of this as an electric signal, generally, the electric capacitance connected with said one end of the first pn junction is excessively charged or discharged if optical

intensity is large relative to accumulation time or integral time. This makes the photocurrent flow forward in the first pn junction. As a result, the first pn junction is biased by a deep forward voltage and excess minority carriers are accumulated in the two semiconductor regions of opposite conductivity types of the first pn junction. This causes a problem that response speed is degraded because of a delay due to so-called saturation time taken for switching the first pn junction to a reverse bias associated with the lifetime of minority carriers. This phenomenon is called a saturation effect.

[0003]

Japanese Patent Publication No. S47-18561 discloses a technique in which the pn junction is connected in parallel with Schottky junction, in order to prevent the pn junction from being biased by a deep forward voltage. The pn junction can be prevented from being deeply biased because a forward voltage is smaller at the Schottky junction than at the pn junction so that most currents flow into the Schottky junction. However, reverse currents at the Schottky junction are several orders of magnitude larger than at the pn junction, which increases the total amount of dark currents. Because of this, this technique cannot be adopted for a high-sensitive photoelectric converter.

[0004]

Herein, the first pn junction biased by a deep forward voltage refers to the forward voltage at the first pn junction when all the photocurrents flow therein as a forward current. If the amount of the photocurrents flowing as the forward current is reduced to one-tenth or less to decrease the saturation time to about one-tenth, the saturation problem is considered to be solved. In this case the forward voltage at the first pn junction is smaller than that in the deeply biased state by  $2.3kT/q$  (about 60mV at room temperature). Herein, under the

ambient condition in which the pn junction becomes biased by the deep forward voltage if left uncontrolled, the control over the pn junction to be maintained in zero bias or reverse bias state and to have the forward voltage smaller than this deep forward voltage by  $2.3kT/q$  is referred to as saturation control, where  $k$  is Boltzman constant,  $T$  is absolute temperature of the photoelectric converter, and  $q$  is elementary charge of electron.

[0005]

If the first pn junction is formed of a first semiconductor region of a first conductivity type and a second semiconductor region of a second conductivity type opposite to the first conductivity type adjacent thereto, accumulated excess minority carriers are spread from the first pn junction within the diffusion length of minority carriers in both of the first and second semiconductor regions. The diffusion lengths differ depending on the type of carriers, electron or hole, or the electric characteristics of the semiconductor regions and the diffusion lengths between the first and second semiconductor regions are different.

[0006]

Further, with a second pn junction having a photoelectric conversion function additionally provided in the diffusion length, currents flow in the second pn junction even if the second pn junction is not exposed to light, causing the photoelectric converter to malfunction. This leads to image blurs and equivalently degraded resolution in an imaging device comprising a photoelectric converter array in which photoelectric conversion elements as the pn junctions are arranged in the first semiconductor region.

[0007]

Now, referring to FIG. 1, using a photodiode as an example of a photoelectric conversion element, how to convert optical information as optical intensity and wavelength components into electric information for output is described. FIG. 1 shows a photodiode 1000a as the first pn junction having an anode 1002a and a field effect transistor 3000a operating as a switch, in which the anode 1002a is connected with the source or drain of the field effect transistor 3000a. The field-effect transistor 3000a switches off the anode 1002a of the photodiode 1000a to place it in a floating state during accumulation time in order to temporarily accumulate photocurrents in the electric capacitance associated with the photoelectric conversion element (in this case, anode-cathode electric capacitance) and switches it on to output accumulated charges as current or charge.

[0008]

First, the field effect transistor 3000a is switched on so that one end (anode 1002 in the drawing) of the photodiode 1000a is at a  $V_{ref}$  potential and the anode-cathode electric capacitance of the photodiode 1000a is charged with a  $V_{dd}-V_{ref}$  voltage.  $V_{dd}$  is a power supply voltage and  $V_{ref}$  is a read reference voltage.

[0009]

Next, the field effect transistor 3000a is switched off and the photoelectric conversion element is illuminated with light. Then, a photocurrent separately generated at the pn junction flows into the anode-cathode electric capacitance  $C_{anc}$  from the anode 1002a of the photodiode 1000a and the capacitance charged with  $V_{dd}-V_{ref}$  alone is discharged. Thereby, a cathode potential rises towards the power supply voltage  $V_{dd}$ . Thus, the anode-cathode electric capacitance is discharged by the

photocurrent in reality. However, it may be expressed herein that a photocurrent is stored as a charge for convenience.

[0010]

With a long switch-off time or a large photocurrent, the anode 1002a of the photodiode 1000a exceeds  $V_{dd}$  and reaches a forward potential. The forward potential continues to rise and reaches the maximum value when all the photocurrents flow through between the anode and cathode of the photodiode 1000a. This is referred to as "biased by a deep forward voltage". In this state excess minority carriers are stored in the semiconductor regions of the photodiode 1000a, causing a delay in switching the photodiode 1000a to a reverse bias direction.

#### Disclosure of the Invention

[0011]

An object of the present invention is to provide a photoelectric converter which prevents a first pn junction with a photoelectric conversion function from being placed in the saturated state in which the first pn junction is biased by the deep forward voltage while controlling a reverse current at the first pn junction not to be as large as that at the Schottky junction. Another object is to provide a photoelectric converter which can prevent image blurs and improve equivalent degradation in resolution.

[0012]

To solve the above objects, following solutions are provided in the present invention.

[0013]

(solution 1)

A photoelectric converter comprises a first pn junction having a photoelectric conversion function and comprised of at least two semiconductor regions of different conductivity types, and a first field-effect transistor including a first source, a first drain, a first insulated gate, the first source connected with one of the semiconductor regions, in which when either of the semiconductor regions is exposed to light, a photocurrent flows in the first pn junction, wherein the first field-effect transistor includes a same conductivity type channel as that of the one of the semiconductor regions, the first drain of the first field-effect transistor is supplied with a second potential at which the first pn junction is zero-biased or reverse-biased relative to a potential of the other of the semiconductor regions, and by supplying, to a first insulated gate, a first-gate potential which makes the first field-effect transistor conductive when the first source reaches a first potential at which the one of the semiconductor regions becomes zero-biased or reverse-biased relative to the other of the semiconductor regions, the photoelectric converter is configured to control saturation of the first pn junction not to be biased by the deep forward voltage, even when either of the two semiconductor regions is exposed to light.

[0014]

To control the two semiconductor regions of different conductivity types not to be biased by the deep forward voltage by flowing most (90% or more, for example) of the photocurrents to the drain through the source of the first field-effect transistor, the first gate potential needs to be preset under a certain condition.

[0015]

(solution 2)

A photoelectric converter according to solution 1, wherein



an absolute value of a difference between the first gate potential and the potential of the other of the semiconductor regions is equal to or larger than an absolute value of a gate threshold voltage of the first field-effect transistor.

[0016]

In case that a photoelectric element for the photoelectric converter of the present invention is a photo-transistor, a following architecture is applied.

[0017]

(solution 3)

A photoelectric converter according to solution 1, wherein

the first pn junction is a base-collector junction of a first bipolar transistor; and

the base of the first bipolar transistor is connected with the source of the first field-effect transistor.

[0018]

Architectures incorporating a second field-effect transistor for selecting the photoelectric converter or reading the stored photoelectric charge or the electric information from it are provided as solutions 4, 5 and 6.

[0019]

(solution 4)

A photoelectric converter according to solution 1, further comprising

a second field-effect transistor including a second source, a second drain, and a second gate, wherein

one of the second source and second drain is connected with an anode of the pn junction, and electric information (electric charge or current) is obtained from the other of the second source and second drain, on supplying a conductive signal at the second gate to make the second field-effect transistor conductive.

[0020]

(solution 5)

A photoelectric converter according to solution 3, further comprising  
a second field-effect transistor including a second source, a second drain, and a second gate, wherein

one of the second source and second drain is connected with an emitter of the first bipolar transistor, and electric information (as electric charge or current) is obtained from the other of the second source and second drain, on supplying a conductive signal at the second gate to make the second field-effect transistor conductive.

[0021]

(solution 6)

A photoelectric converter according to solution 3, further comprising  
a second field-effect transistor including a second source, a second drain, and a second gate; and

a single or plural second bipolar transistors, wherein

an emitter of the first bipolar transistor is connected with a base of the single or plural bipolar transistors;

a base and an emitter of the plural bipolar transistors are connected with each other;

an emitter not connected with the base is connected with one of the second source and second drain, and electric information (as electric charge or current) is obtained from the other of the second source and second drain, on supplying a conductive signal at the second gate to make the second field-effect transistor conductive.

[0022]

An example of a structure for the photoelectric convertor of the solution 1 is shown as follows.

[0023]

(solution 7)

A photoelectric converter comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type opposite to the first conductivity type, in contact with the first semiconductor region;

a third semiconductor region of the second conductivity type, provided in contact with the first semiconductor region and spaced apart from the second semiconductor region;

a first insulator film provided on a surface of the first semiconductor region between the second and third semiconductor region; and

a first gate provided on the first insulator film to bridge the second and third semiconductor region, in which when the second semiconductor region or a part of the first semiconductor region close to the second semiconductor region is exposed to light, a photocurrent flows between the first and second semiconductor regions, wherein

the third semiconductor region is supplied with a second potential at which the second semiconductor region is zero-biased or reverse-biased relative to the first semiconductor region, and when the second semiconductor region turns to a first potential, at which the second semiconductor region becomes zero-biased or reverse-biased relative to the first semiconductor region, the photoelectric converter is configured to control saturation of the second semiconductor region not to be biased by the deep forward voltage by supplying, to the first gate, a first gate potential to induce a channel or a current path on a

surface of the first semiconductor region under the first gate, even when the second semiconductor region or a portion of the first semiconductor region close to the second semiconductor region is exposed to light.

[0024]

To reduce dark current at the junction between the first semiconductor region and the second semiconductor region, the following architecture is provided.

[0025]

(solution 8)

A photoelectric converter according to solution 7, further comprising a fourth semiconductor region of the first conductivity type provided to cover an upper part of the second semiconductor region and be self-aligned with the first gate.

[0026]

In the photoelectric converter of the present invention, an example of the structures for photoelectric conversion elements having an amplification function is provided.

[0027]

(solution 9)

A photoelectric converter according to solution 7, further comprising a fifth semiconductor region of the first conductivity type in contact with the second semiconductor region, so that a current having flowed through the second semiconductor region is amplified through the first or fifth semiconductor region.

[0028]

Examples of array structures for the present photoelectric converter and imaging devices by the present photoelectric converter are provided as follows.

[0029]

(solution 10)

A photoelectric converter array comprising:

a plurality of the photoelectric converters according to solution 4, arranged in first and second directions intersecting with each other;

a plurality of first interconnections extending in the first direction;

a plurality of second interconnections extending in the second direction;

a third interconnection to supply the first gate potential; and

a fourth interconnection to supply the second potential, wherein:

the first to fourth interconnections are insulated with one another; and

the second gate of the second field-effect transistor is connected with one of the first interconnections extending in the first direction; and

the other of the second source and second drain of the second field-effect transistor is connected with one of the second interconnections extending in the second direction.

[0030]

(solution 11)

A photoelectric converter array according to solution 10, wherein

the second drain is arranged to have a common portion in neighboring photoelectric converters.

[0031]

(solution12)

An imaging device comprising:

the photoelectric converter array according to solution 10;

a drive circuit to scan the first interconnections;

a current or charge sense circuit connected with the second interconnections;

a third field-effect transistor for potential setting connected with the second interconnections at one of a source and a drain;

a reference potential supplier connected with the other of the source and drain of the third field-effect transistor;

a first gate potential supplier connected with the third interconnection;  
and

a second potential supplier connected with the fourth interconnection,  
wherein

the current or charge sense circuit is of a differential type, having a first input terminal connected with the second interconnections and a second input terminal, and supplied with a reference potential at the second input terminal.

[0032]

(solution 13)

An imaging device according to solution 12, wherein

the third field-effect transistor is configured to supply a reference potential to the second interconnections after the sense circuit completes sensing and before the second field-effect transistor is turned off.

### Brief Description of the Drawings

[0033]

Features, embodiments, and advantages of the present invention will become apparent from the following detailed description with reference to the accompanying drawings:

FIG. 1 shows a related art photodiode with a switch;

FIG. 2 is an exemplary circuit diagram comprising a photodiode with a first field-effect transistor according to one embodiment of the present invention;

FIG. 3 is a graph to describe the operation of the first field-effect transistor for saturation control;

FIG. 4 is a cross section view of the circuit in FIG. 2 excluding a second field-effect transistor by way of example;

FIG. 5A is a planar view of the circuit in FIG. 4 including a fourth semiconductor region according to one embodiment of the present invention and FIG. 5B is a cross section view of the same;

FIG. 6 is an equivalent circuit diagram in which the photoelectric converter according to the present invention is applied to a photo transistor;

FIG. 7 is a cross section view of the circuit in FIG. 6 excluding a second field-effect transistor;

FIG. 8 shows an example of cell structure in which the photoelectric converters according to one embodiment of the present invention are arranged in array;

FIG. 9 is an equivalent circuit diagram of the cell in FIG. 8; and

FIG. 10 shows an example of an imaging device to which the photoelectric converter array according to one embodiment of the present invention is applied.

### Description of the Embodiments

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. Wherever possible, the

same reference numbers will be used throughout the drawings to refer to the same or like parts.

#### First Embodiment

[0034]

FIG. 2 is a circuit diagram including first and second field effect transistors 3010, 3000 and a photodiode 1000 as a first pn junction according to a first embodiment. In FIG. 2 the photodiode 1000 is connected at an anode 1002 with one of the drain and source of the second field effect transistor 3000 as well as with a first source 3012 of the first field-effect transistor 3010. The first field-effect transistor 3010 is a saturation controlling transistor and the second field-effect transistor 3000 is a switching transistor. The first field-effect transistor 3010 is a p-channel type and comprises the first source 3012, a first drain 3011, and a first gate 3013 in the present embodiment.

[0035]

In the drawing a cathode potential  $V_{dd}$  is more positive than a read reference potential  $V_{ref}$ . The first gate 3013 of the first field-effect transistor is applied with a first gate potential  $V_{g1}$ , the first drain 3011 thereof is supplied with a potential  $V_{sink}$  which is equal to the cathode potential  $V_{dd}$  or closer to  $V_{ref}$  than  $V_{dd}$ . That is,  $V_{sink}$  is a second potential which reversely biases or zero-biases the first pn junction. A first gate potential  $V_{g1}$  is equal to  $V_{dd} + V_{th}$  or more negative than that. Thus, when the anode of the first pn junction reaches a first potential at which the first pn junction becomes reversely biased or zero-biased, the first field-effect transistor becomes conductive. In the present embodiment the first potential is  $V_{g1} - V_{th}$ , and  $V_{th}$  is a negative value when the first field-effect transistor is an enhancement type. On the other hand, the cathode 1001 of the photodiode 1000 is also connected with one of the



source and drain of the second field-effect transistor, when the cathode 1001 is connected with the first field-effect transistor. The anode potential  $V_{an}$  is more negative than  $V_{ref}$  and  $V_{th}$  is a positive value when the first field-effect transistor is an n channel type and enhancement type.

[0036]

First, the second field effect transistor 3000 is turned on so that the cathode 1002 of the photodiode 1000 turns to the read reference potential  $V_{ref}$ , and it is turned off. In this state the electric capacitance (mainly, junction capacitance)  $C_{anc}$  is charged with  $V_{dd} - V_{ref}$ . The capacitance  $C_{anst}$  between the anode of the photodiode and ground is charged with the reference potential  $V_{ref}$ .

[0037]

Next, the capacitance  $C_{anc}$  is discharged and the capacitance  $C_{anst}$  is further charged by a photocurrent  $i_{ph}$  from the photodiode 1000 exposed to light, and the anode potential  $V_{an}$  increases from  $V_{ref}$  to  $V_{dd}$ . After storage time  $t_{str}$ , the second field-effect transistor 3000 is turned on again to be able to output a charge  $(C_{anc} + C_{anst}) * (V_{an} - V_{ref})$  from the other of the source and drain not connected with the photodiode 1000. During switch time  $t_{on}$ , an average current,  $i_{out} = (C_{anc} + C_{anst}) * (V_{an} - V_{ref}) / t_{on}$  is output on average. The electric charge  $(C_{anc} + C_{anst}) * (V_{an} - V_{ref})$  is referred to as stored optical charge to distinguish it from the stored charge of excess minority carriers.

[0038]

In a long storage time  $t_{str}$  or with a large photocurrent  $i_{ph}$ , the anode potential  $V_{an}$  exceeds the cathode potential  $V_{dd}$  so that the anode is biased forward relative to the cathode and the photocurrents  $i_{ph}$  partially start flowing into the photodiode. When all the photocurrents  $i_{ph}$  flow in the photodiode,

the voltage of the photodiode stops varying. This voltage is called as “deep forward voltage”. It is called as open circuit voltage in solar battery.

[0039]

Excess minority carriers are stored in the semiconductor regions of the photodiode and the amount of carriers is approximately proportional to the forward current flowing into the photodiode. To pull out the excess minority carriers, the second field-effect transistor is turned on. However, a time delay occurs from the turning-on of the second field-effect transistor to the photodiode's reversely biased or the anode potential  $V_{an}$  reaching the cathode potential  $V_{dd}$  or less. Although it is preferable to reduce the excess minority carriers to zero, it is sufficiently effective to reduce the forward current to the photodiode to about one-tenth of the photocurrent  $i_{ph}$  or less. That is, in the forward biased photodiode the forward voltage has to be controlled to be smaller than the deep forward voltage by about 60mV or more. It is most preferable to control the anode-cathode voltage of the photodiode from zero to a reverse bias voltage.

[0040]

Next, the first field-effect transistor 3010 for the saturation control is described. The first gate potential  $V_{g1}$  is set to cathode potential  $V_{dd}$  + gate threshold voltage  $V_{th}$  for simplicity. A gate threshold voltage  $V_{th}$  is typically negative and closer to  $V_{ref}$  by  $|V_{th}|$  from  $V_{dd}$ . The anode 1002 of the photodiode 1000 is discharged by the photocurrent so that the potential  $V_{an}$  varies from  $V_{ref}$  to  $V_{dd}$ . This turns on the first field-effect transistor 3010 due to the connection of the anode 1002 and first source 3012 to start bypassing the photocurrent from the source 3012 to the drain 3011. Because of this, the anode potential  $V_{an}$  is prevented from exceeding the positive cathode potential

Vdd. In other words the anode-cathode voltage of the photodiode 1000 calculated from  $V_{an}$  minus  $V_{dd}$  will be never deeply biased by the deep forward voltage.

[0041]

The gate threshold voltage  $V_{th}$  of the first field-effect transistor is defined to be a gate-source voltage which flows a saturation current of  $1\mu A$  between the source and the drain. In the photodiode with light receiving area of  $50\mu m$  square or less, the anode-cathode voltage is clamped to about 0V under daytime ambient light. As shown in FIG. 3, a current  $I_{sink}$  bypassed by the first field-effect transistor increases exponentially when the anode potential  $V_{an}$  approaches  $V_{g1} - V_{th}$  from  $V_{ref}$  and it reaches  $I_{th}$  of  $1\mu A$ , for example, at the anode potential  $V_{an}$  being  $V_{g1} - V_{th}$ . Since the off-current value  $I_{off}$  of the first field-effect transistor can be designed to be in pA level, the amount of current added to an equivalent dark current of the photodiode is smaller than that when the photodiode is connected in parallel with the Schottky diode. While the anode potential  $V_{an}$  changes from  $V_{g1} - V_{th} - (0.4 \text{ to } 0.5V)$  to  $V_{g1} - V_{th}$ , the current  $I_{sink}$  increases from  $I_{off}$  to  $I_{th}$ . The change range of  $V_{an}$ , 0.4 to 0.5 V is given by  $s * \log(I_{th}/I_{off})$  where  $s$  is a device parameter as so-called sub-threshold slope.

[0042]

To keep the anode-cathode voltage in a reverse bias range, the first gate potential  $V_{g1}$  has to be set to be closer to  $V_{ref}$  than  $V_{dd} + V_{th}$ . Further, to control the saturation of the photocurrent  $i_{ph}$  of the photodiode 1000 having the light receiving area of larger than  $50\mu m$  square under direct sunlight in mid summer, the channel width of the first field-effect transistor 3010 is set to a width  $W$  enough to pass the photocurrent in addition to the first gate potential

Vg1 set as above. That is, at the photocurrent  $i_{ph}$  being larger than  $I_{th}$ , the width  $W$  is determined by the following expression:

$$W = (i_{ph} - I_{th}) * 2L / (\mu C_{ox} (V_{g1} - V_{dd} - V_{th})^2)$$

where  $V_{g1} < V_{dd} + V_{th}$ ,  $L$  is channel length,  $C_{ox}$  is electric capacitance per unit area of gate insulator film.

[0043]

FIG. 4 shows a cross section of a simplest example of the photodiode 1000 and the first field-effect transistor 3010 of the photoelectric converter in FIG. 2. The photoelectric converter includes a first semiconductor region 101 of a first conductivity type, a second semiconductor region 102 of a second conductivity type opposite to the first conductivity type. The first pn junction is formed of the junction plane of the first and second semiconductor regions 101, 102. The photodiode 1000 is formed of the second semiconductor region 102 and a portion of the first semiconductor region 101 adjacent to the second semiconductor region within the diffusion length of minor carriers.

[0044]

It also includes a third semiconductor region 311 of the second conductivity type provided as a first drain of the first field-effect transistor 3010 spaced apart from the second semiconductor region 102. A first gate insulator film 314 of the first field-effect transistor is provided to contact a part of the second and third semiconductor regions 102, 103 and the surface of the semiconductor region 101 therebetween. A first gate 313 thereof is formed to contact the first gate insulator film so that it bridges the second and third semiconductor regions. In the present embodiment the first source of the first field-effect transistor shares the second semiconductor region 102 with the photodiode 1000. The channel thereof is induced or disappears by the electric

field of the first gate in the surface of the first semiconductor region between the second and third semiconductor region.

[0045]

The first semiconductor region can be a semiconductor substrate or an electrically separated region on a semiconductor substrate or an insulated substrate.

[0046]

To apply the same bias as that in FIG. 2, the first semiconductor region 101 is supplied with the potential  $V_{dd}$ , the third semiconductor region 103 is supplied with the potential  $V_{sink}$  as  $V_{dd} + V_{th}$  or less (reference voltage  $V_{ref}$  or 0V, for example), and the first gate 313 is supplied with  $V_{g1}$ .

[0047]

FIGs. 5A, 5B are a planar view and a cross section view of a fourth semiconductor region 104 of the first conductivity type in contact with the second semiconductor region and the second field-effect transistor 3000 additionally disposed in the structure in FIG. 4, respectively. FIG. 5B is a cross section seen from 1 to 1' line in FIG. 5A. A fifth semiconductor region 301 of the second conductivity type is provided in contact with the surface of the first semiconductor region and as spaced apart from the second semiconductor region and is a second drain of the second field effect transistor 3000. A second gate insulator film 304 of the second field-effect transistor 3000 is provided to contact a part of the second and fifth semiconductor regions and the surface of the first semiconductor region therebetween. A second gate 303 of the second field-effect transistor is provided to contact the second gate insulator film 304 and bridge the second and fifth semiconductor areas. The source thereof shares the second semiconductor region with the photodiode 1000

in the present embodiment. The channel thereof is induced or disappears by the electric field of the second gate 303 on the surface of the first semiconductor region between the second and fifth semiconductor regions.

[0048]

In FIGs. 5A, 5B the fourth semiconductor region 104 can extend to the first semiconductor region from the second semiconductor region. It can be self-aligned with the first and second gates 313, 303 at both ends of the second semiconductor region via the insulator films. The fourth semiconductor region can reduce a dark current and stabilize it. Further, it can increase the anode-cathode capacitance  $C_{anc}$  of the photodiode 1000 and increase the upper limit of stored optical charges.

[0049]

Further, the fifth semiconductor region as the second drain of the second field-effect transistor 3000 is supplied with the reference potential  $V_{ref}$  and the second gate 303 (potential  $V_{g0}$ ) is supplied with  $V_{dd}$  to turn off the second field effect transistor 3000 and with a potential more negative than  $V_{ref} + V_{th}$  to turn it on (if the transistor 3000 is a p-channel). Stored optical charges can be read as charge or current from the second drain 301 of the second field effect transistor 3000 and the cathode 101 of the photodiode 1000 during the switch time.

[0050]

A single field effect transistor can be used for the first and second field effect transistors 3010, 3000. The cross section view of the circuit in FIG. 2 excluding the second field effect transistor 3000 is exact the same as that in FIG. 4. To charge the anode-cathode electric capacitance  $C_{anc}$  of the photodiode 1000 with  $V_{dd} - V_{ref}$  first, the potential  $V_{ref}$  is supplied to the first drain 311,

and a potential more negative than  $V_{ref} + V_{th}$  is supplied to the first gate 313 of the first field-effect transistor. Next, during the optical charge storage phase, the potential of the first gate 311 does not need to be changed, and a potential  $V_{g1}$  ( $\leq V_{dd} + V_{th}$ ) is supplied to the first gate. To read the stored optical charges or read them as a current, the potential more negative than  $V_{ref} + V_{th}$  is supplied to the first gate 313 again. Charge or current can be read from the first drain 311 or the cathode 101 of the photodiode 1000 by connecting a sense amplifier with a field-effect transistor to connect or activate it in synchronization with the change in the potential to the first gate 313. The connection or activation to the sense amplifier by the field effect transistor is not necessary for reading the charge or current from the cathode 101 of the photodiode. Note that activation refers to turning off a connector of the sense amplifier to a  $V_{ref}$  potential in a read phase, otherwise the input thereof is connected with a  $V_{ref}$  potential.

## Second Embodiment

[0051]

FIG. 6 shows an example of the first pn junction which is applied as a base-collector junction of a photo transistor 1010. A source 3012 of the first field-effect transistor is connected to a base 1012 of the photo transistor 1010 to control the saturation of the base-collector junction. The first gate is supplied with the potential  $V_{g1}$  while the first drain 3011 is supplied with the second potential  $V_{sink}$  which is  $V_{dd} + V_{th}$  or less such as  $V_{ref}$  or 0V. The collector 1011 of the photo transistor is supplied with  $V_{dd}$ . Here, the first potential is  $V_{g1} - V_{th}$  and  $V_{g1}$  is set to be equal to or more negative (when npn transistor is used, equal to or more positive when pnp transistor is used) than the collector potential ( $V_{dd}$ ). An emitter 1013 is connected to the source or drain of the

second field effect transistor 3000 and  $V_{ref}$  is supplied to the other of the source and drain.

[0052]

First, the second field effect transistor 3000 is turned on to set the emitter 1013 of the photo transistor 1010 to have a read reference potential  $V_{ref}$ , and it is turned off. Now, an electric capacitance  $C_{bc}$  (mainly, junction capacitance) between the base and collector of the photo transistor 1010 is charged with  $V_{dd} - V_{ref} - V_{be}$ . An electric capacitance  $C_{be}$  between the base and emitter of the photo transistor 1010 is charged with  $V_{be}$ , and a capacitance  $C_{bst}$  between the base and ground is charged with  $V_{ref} + V_{be}$ .  $V_{be}$  is a forward voltage between the base and emitter when a photocurrent flows from the base to the emitter. The photocurrent  $i_{ph}$  is generated when the collector or base is exposed to light, and amplified and output from the emitter and collector of the photo transistor 1010.

[0053]

Then, the electric capacitance  $C_{bc}$  is discharged and the capacitance  $C_{bst}$  is further charged by the photocurrent  $i_{ph}$  from the base 1012 of the photo transistor 1010 exposed to light, increasing the base potential  $V_b$  from  $V_{ref} + V_{be}$  to  $V_{dd}$ . After the storage time  $t_{str}$ , the second field effect transistor 3000 is switched on again to be able to read an amplified charge  $= (h_{FE} + 1) (C_{bc} + C_{bst}) * (V_b - V_{ref} - V_{be})$  from the other of drain and source thereof, where  $h_{FE}$  is amplification factor of the photo transistor 1010. During switch time  $t_{on}$ , mean amplified current  $i_{out} = (h_{FE} + 1) (C_{bc} + C_{bst}) * (V_b - V_{ref} - V_{be}) / t_{on}$  is read.  $(C_{bc} + C_{bst}) * (V_b - V_{ref} - V_{be})$  is referred to as stored optical charges and distinguished from the stored charges of excess minority carriers. Note that the electric capacitance  $C_{be}$  between the base and emitter of the photo



transistor 1010 remains at the voltage  $V_{be}$  so that it is not considered for the readout.

[0054]

The saturation of the pn junction can be controlled by supplying the first gate the potential  $V_{g1}$  to the first gate 3013 and the second potential  $V_{sink}$  to the first drain, as in the case of the photodiode.

[0055]

Next, FIG. 7 is a cross section view of the photo transistor 1010 and the first field-effect transistor 3010 of the photoelectric converter in FIG. 6. A part of the first semiconductor region 101 of the first conductivity type functions as the collector of the photo transistor 1010. The second semiconductor region 102 of the second conductivity type is provided in contact with the first semiconductor region 101 and functions as the base of the photo transistor 1010. A third semiconductor region 103 of the first conductivity type is provided in contact with the second semiconductor region and functions as the emitter of the photo transistor 1010. The first pn junction is formed of the junction plane between the first and second semiconductor regions 101, 102. A photocurrent  $i_{ph}$  is generated when the second semiconductor region 102 and a portion of the first semiconductor region close thereto (within diffusion length of minority carriers) are exposed to light, and acquired from the second semiconductor region 102 as the base.

[0056]

The fourth semiconductor region 104 of the first conductivity type is self-aligned with the first gate on the surface of the second semiconductor region 102. It extends to the first semiconductor region 101 on the surface where the second semiconductor region 102 contacts the first semiconductor

region 101. The fourth semiconductor region 104 is separated from the sixth semiconductor region 103. In order to prevent a leak current path and maintain a constant current amplification factor between the fourth and sixth semiconductor regions 104, 103, a seventh semiconductor region 107 of the second conductivity type can be provided in contact with the surface of the second semiconductor region therebetween. The seventh semiconductor region 107 possesses higher impurity concentration than the second semiconductor region.

[0057]

A third semiconductor region 311 of the second conductivity type is provided spaced apart from the second semiconductor region 102 and is the first drain of the first field-effect transistor 3010. A first gate insulator film 314 thereof is provided to contact a part of the second and third semiconductor region and the surface of the first semiconductor region therebetween. A first gate 313 thereof is provided to contact the first gate insulator film to bridge the second and third semiconductor regions. The first source shares the second semiconductor region 102 with the photo transistor in the present embodiment. The channel thereof is induced or disappears by the electric field of the first gate in the surface of the first semiconductor region between the second and third semiconductor regions. The first semiconductor region can be a semiconductor substrate or an electrically isolated region on a semiconductor substrate or an insulated substrate.

[0058]

The technique according to the present embodiment is applicable to a photo-transistor not including the second field-effect transistor 3000. The cross section view of the circuit in FIG. 6 excluding the second field effect

transistor 3000 is exact the same as that in FIG. 7. To charge the base-collector electric capacitance  $C_{bc}$  of the photodiode 1010 with  $V_{dd} - V_{ref} - V_{be}$  and the capacitance  $C_{bst}$  with  $V_{ref}$  first, the potential  $V_{dd}$  is supplied to the collector 1011, and  $V_{ref}$  is supplied to the emitter 1013. Next, to accumulate optical charges in the capacitances  $C_{bc}$ ,  $C_{bst}$ , the emitter 1013 is switched to a potential of  $V_{dd}$  or more. The base-emitter junction is reversely biased and the base is placed in a floating state so that the capacitance  $C_{bc}$  is discharged and the capacitance  $C_{bst}$  is charged by the photocurrent flowing from the base. The saturation can be thus controlled by supplying the potential  $V_{sink}$  to the first drain 311 of the first field-effect transistor and the potential  $V_{g1} (\leq V_{dd} + V_{th})$  to the first gate.

[0059]

To read the stored optical charges again, the potential of the emitter 1013 is returned to  $V_{ref}$ . Charge or converted current can be read from the emitter 1013 or the collector 1011. The switch connection or activation of the sense amplifier is not necessary for reading the charge or current from the collector 1011.

[0060]

In the above, the magnitude relation of potentials and polarity for the field-effective transistor as p-channel are described. For an n-channel field-effect transistor, they will be reverse.

[0061]

FIG. 8 shows an example of the photoelectric converter array in which four unit cells C1, C2, C3, C4 as a group are vertically and horizontally arranged. The area-efficient array can be structured by sharing an interconnection M2311 of the first drain 311 and an interconnection M1313 of

the first gate 313 of the saturation-controlling first field-effect transistor 3010 with neighboring cells. Although the interconnection M2311 and M1313 intersect with each other in the drawing, the array is in a double-layer interconnection structure and the two interconnections are insulated each other by an insulator film so that they will be never electrically short-circuited.

[0062]

The array in FIG.8 includes a second bipolar transistor 2010 for amplification in addition to the photo-transistor in each cell. The fifth semiconductor region 103 as the emitter of the photo-transistor 1010 is connected to a semiconductor region 212 of the second conductivity type as the base of the second bipolar transistor 2010 via a semiconductor region 217 of the second conductivity type. A semiconductor region 213 of the first conductivity type as the emitter of the second bipolar transistor 2010 is connected to one 302 of the source and drain of the second field-effect transistor. An equivalent circuit diagram of a single cell in FIG. 8 is shown in FIG. 9.

### Third Embodiment

[0063]

FIG. 10 shows an example of the structure of an imaging device incorporating the photoelectric converter array according to one embodiment of the present invention. The imaging device comprises the photoelectric converter array as above, first interconnections M1303-1, M1303-2, ..., M1303-n to connect the second gate 303 of the second field-effect transistor horizontally or in X direction, a Y drive circuit 9010 to scan the first interconnections, second interconnections as output lines M2303-1, M2303-2, ..., M2303-m to connect the other 301 of the source and drain of the second field-effect transistor vertically or in Y direction, current or charge sense

circuits 9020 with first input terminals connected to the second interconnections, and third field-effect transistors 3090-1, 3090-2, ..., 3090m for setting reference potential. The current or charge sense circuits 9020 are of a differential input type including second input terminals 922 for the reference potential. With use of a single current or charge sense circuit, scanning field-effect transistors are connected to the output lines sequentially switch one of the output lines to the single current or charge sense circuit.

[0064]

The second input terminals 922 of the sense circuit 9020 are supplied with the reference potential  $V_{ref}$  from a reference potential supplier 6001. One of the source and drain of each of the third field-effect transistors 3090-1, 3090-2, ..., 3090-m is connected to the second interconnections and the other thereof is supplied with the reference potential  $V_{ref}$  from the reference potential supplier 6001. The output of the sense circuits are converted to a serial signal by a serial-parallel converter circuit 9030.

[0065]

The output lines are charged with the reference potential  $V_{ref}$  by the third field-effect transistors 3090 after sensing when needed while all the second field-effect transistors are off. A third interconnection M2313 of the gate of the first field-effect transistor 3010 for saturation control is supplied with the first gate potential  $V_{g1}$  equal to or more negative than  $V_{dd} + V_{th}$  by a potential generator circuit in or from outside a chip. A fourth interconnections M 2311 of the drain 311 of the first field-effect transistor for saturation control 3010 is supplied with the second potential  $V_{sink}$ .

[0066]

The photoelectric converter according to the above embodiments can reduce the storage of excess minority carriers in the photoelectric conversion elements to be able to decrease a switching delay and improve the read speed. Further, in the photoelectric converter array a leakage of photocurrent from neighboring cells can be prevented. This results in preventing image blurs and equivalent degradation in resolution of the imaging device incorporating the photoelectric converter array.

[0067]

The present invention can broaden the field of application of a sensor, office machine, and scientific instrument using photoelectric conversion, and abate a switching delay or image blurs of a high-sensitive photoelectric converter or an imaging device used partially in an ambient condition of a large optical intensity and luminance.

[0068]

Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. It should be appreciated that variations or modifications may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims.

## Claims

1. A photoelectric converter comprising:

a first pn junction having a photoelectric conversion function and comprised of at least two semiconductor regions of different conductivity types; and

a first field-effect transistor including a first source, a first drain, and a first insulated gate, the first source connected with one of the semiconductor regions, in which when either of the semiconductor region is exposed to light, a photocurrent flows in the first pn junction, wherein:

the first field-effect transistor includes a same conductivity type channel as that of the one of the semiconductor regions;

the first drain of the first field-effect transistor is supplied with a second potential at which the first pn junction is zero-biased or reverse-biased relative to a potential of the other of the semiconductor regions; and

by supplying, to a first insulated gate, a first gate potential which makes the first field-effect transistor conductive when the first source reaches a first potential at which the one of the semiconductor regions becomes zero-biased or reverse-biased relative to the other of the semiconductor regions, the photoelectric converter is configured to control saturation of the first pn junction not to be biased by a deep forward voltage, even when either of the two semiconductor regions is exposed to light.

2. A photoelectric converter according to claim 1, wherein

an absolute value of a difference between the first gate potential and the potential of the other of the semiconductor regions is equal to or larger than an absolute value of a gate threshold voltage of the first field-effect transistor.

3. A photoelectric converter according to claim 1, wherein

the first pn junction is a base-collector junction of a first bipolar transistor; and

the base of the first bipolar transistor is connected with the source of the first field-effect transistor.

4. A photoelectric converter according to claim 1, further comprising

a second field-effect transistor including a second source, a second drain, and a second gate, wherein

one of the second source and second drain is connected with an anode of the pn junction, and electric information is obtained from the other of the second source and second drain, on supplying a conductive signal at the second gate to make the second field-effect transistor conductive.

5. A photoelectric converter according to claim 3, further comprising

a second field-effect transistor including a second source, a second drain, and a second gate, wherein

one of the second source and second drain is connected with an emitter of the first bipolar transistor, and electric information is obtained from the other of the second source and second drain, on supplying a conductive signal at the second gate to make the second field-effect transistor conductive.



6. A photoelectric converter according to claim 3, further comprising  
a second field-effect transistor including a second source, a second drain, and a second gate; and  
a single or plural second bipolar transistors, wherein  
an emitter of the first bipolar transistor is connected with a base of the single or plural bipolar transistors;  
a base and an emitter of the plural bipolar transistors are connected with each other;  
an emitter not connected with the base is connected with one of the second source and second drain, and electric information is obtained from the other of the second source and second drain, on supplying a conductive signal at the second gate to make the second field-effect transistor conductive.
7. A photoelectric converter comprising:  
a first semiconductor region of a first conductivity type;  
a second semiconductor region of a second conductivity type opposite to the first conductivity type, in contact with the first semiconductor region;  
a third semiconductor region of the second conductivity type, provided in contact with the first semiconductor region and spaced apart from the second semiconductor region;  
a first insulator film provided on a surface of the first semiconductor region between the second and third semiconductor region; and  
a first gate provided on the first insulator film to bridge the second and third semiconductor region, in which when the second semiconductor region or a part of the first semiconductor region close to the second semiconductor region

is exposed to light, a photocurrent flows between the first and second semiconductor regions, wherein

the third semiconductor region is supplied with a second potential at which the second semiconductor region becomes zero-biased or reverse-biased relative to the first semiconductor region, and when the second semiconductor region turns to a first potential, at which the second semiconductor region becomes zero-biased or reverse-biased relative to the first semiconductor region, the photoelectric converter is configured to control saturation of the second semiconductor region not to be biased by a deep forward voltage by supplying, to the first gate, a first gate potential to induce a channel or a current path on a surface of the first semiconductor region under the first gate, even when the second semiconductor region or a portion of the first semiconductor region close to the second semiconductor region is exposed to light.

8. A photoelectric converter according to claim 7, further comprising

a fourth semiconductor region of the first conductivity type provided to cover an upper part of the second semiconductor region and be self-aligned with the first gate.

9. A photoelectric converter according to claim 7, further comprising

a fifth semiconductor region of the first conductivity type is in contact with the second semiconductor region, so that a current having flowed through the second semiconductor region is amplified through the first or fifth semiconductor regions.

10. A photoelectric converter array comprising:

a plurality of the photoelectric converters according to claim 4, arranged in first and second directions intersecting with each other;

a plurality of first interconnections extending in the first direction;

a plurality of second interconnections extending in the second direction;

a third interconnection to supply the first gate potential; and

a fourth interconnection to supply the second potential, wherein:

the first to fourth interconnections are insulated with one another; and

the second gate of the second field-effect transistor is connected with one of the first interconnections extending in the first direction; and

the other of the second source and second drain of the second field-effect transistor is connected with one of the second interconnections extending in the second direction.

11. A photoelectric converter array according to claim 10, wherein  
the second drain is arranged to have a common portion in neighboring photoelectric converters.

12. An imaging device comprising:  
the photoelectric converter array according to claim 10;  
a drive circuit to scan the first interconnections;  
a current or charge sense circuit connected with the second interconnections;  
a third field-effect transistor for potential setting connected with the second interconnections at one of a source and a drain;  
a reference potential supplier connected with the other of the source and drain of the third field-effect transistor;

a first gate potential supplier connected with the third interconnection;  
and

a second potential supplier connected with the fourth interconnection,  
wherein

the current or charge sense circuit is of a differential type, having a first input terminal connected with the second interconnections and a second input terminal, and supplied with a reference potential at the second input terminal.

13. An imaging device according to claim 12, wherein

the third field-effect transistor is configured to supply a reference potential to the second interconnections after the sense circuit completes sensing and before the second field-effect transistor is turned off.

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FIG. 1

## PRIOR ART

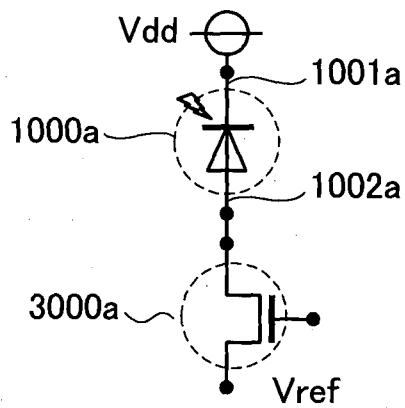
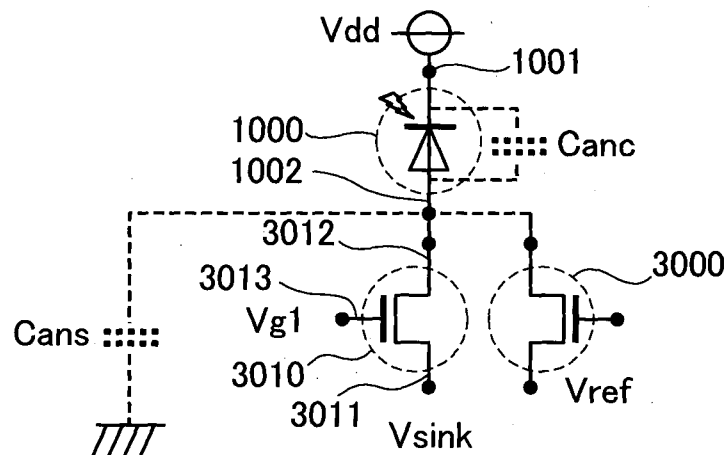
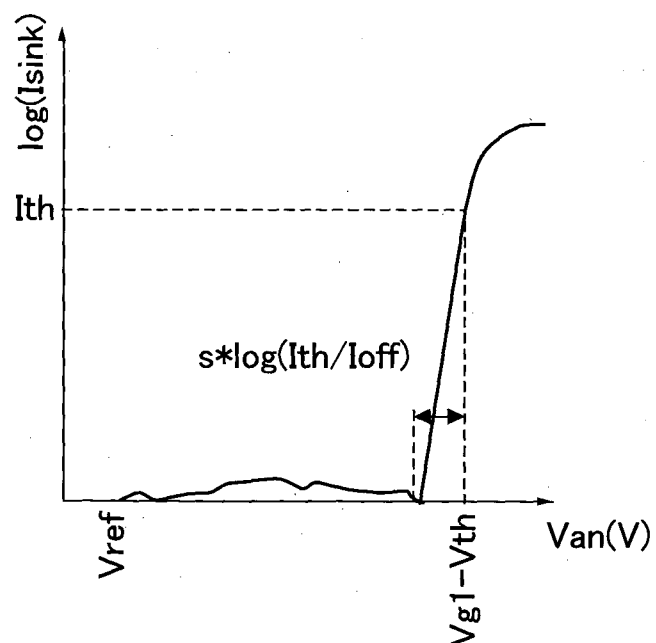


FIG.2

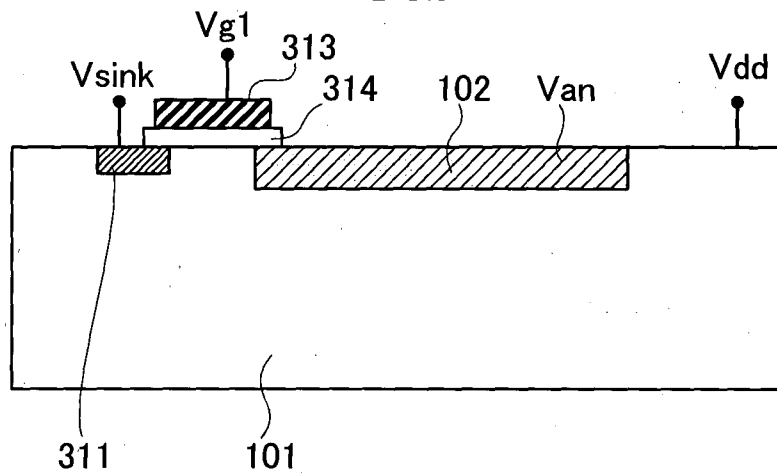


**FIG.3**



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**FIG.4**



**FIG.5A**

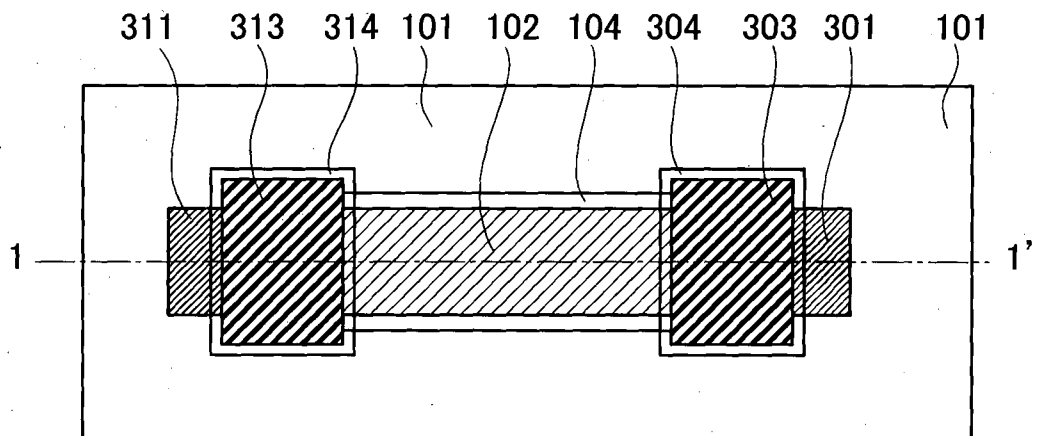
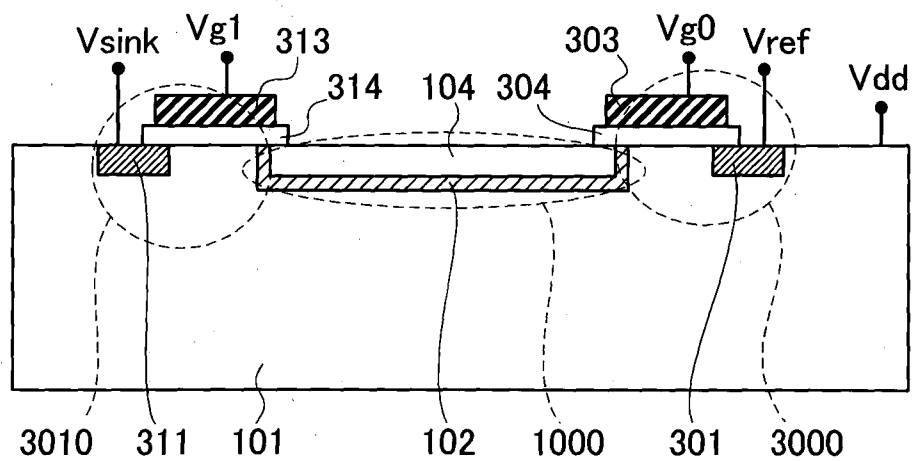


FIG.5B



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FIG.6

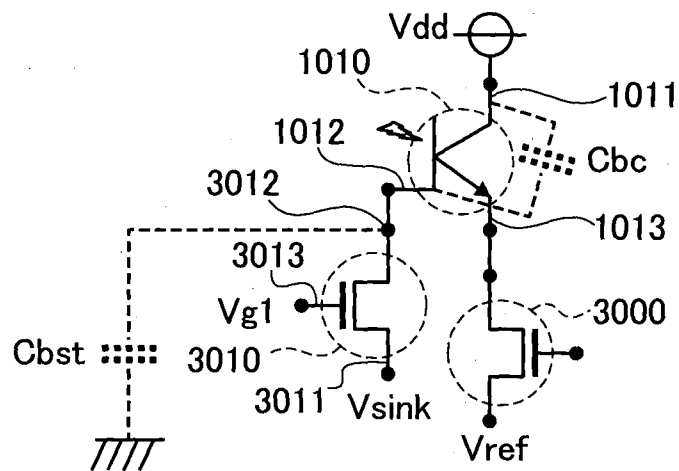
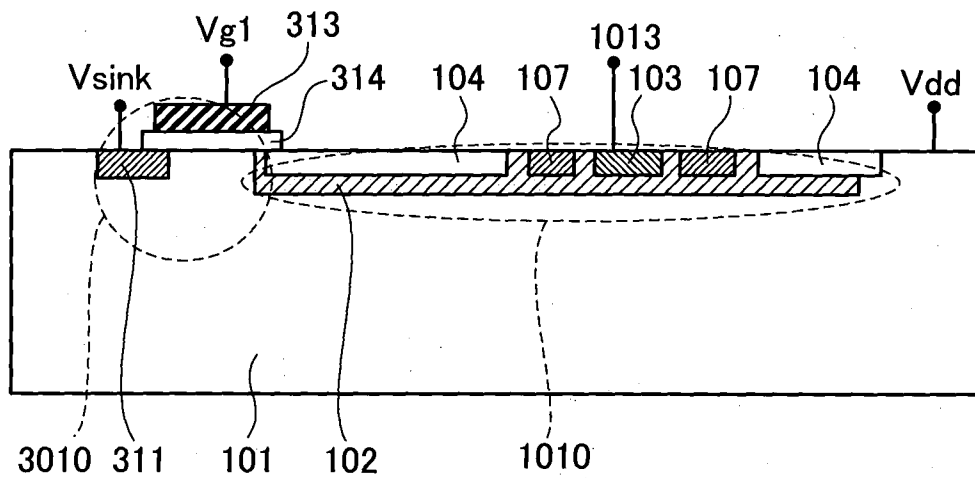


FIG.7

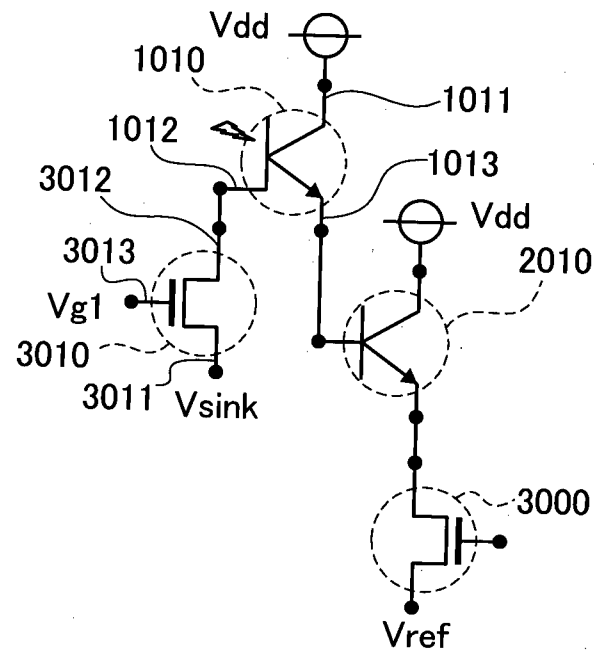




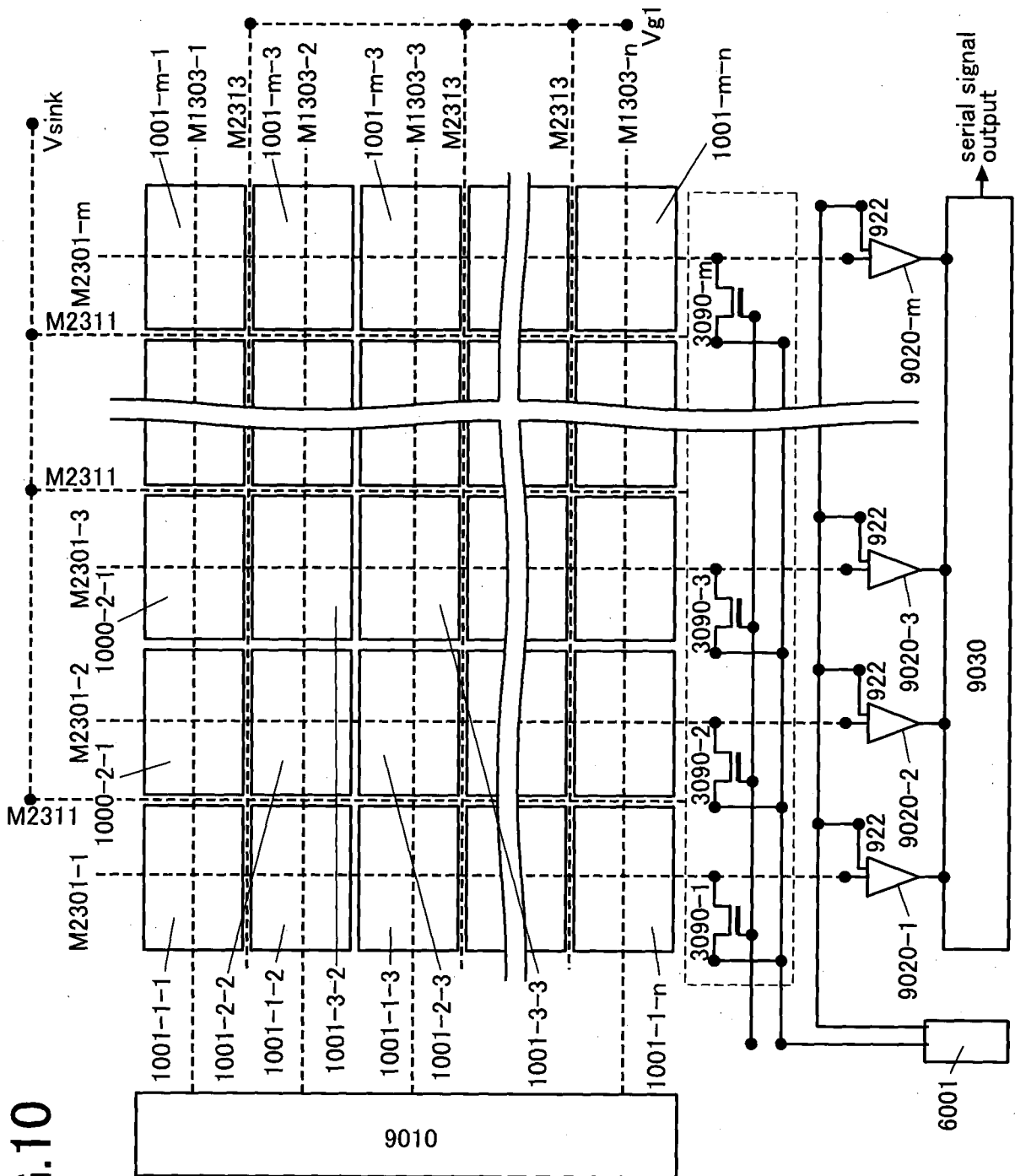


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FIG.9



**FIG. 10**



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2012/076557

## A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H04N5/3745 (2011.01) i, H01L27/146 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H04N5/3745, H01L27/146

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996  
 Published unexamined utility model applications of Japan 1971-2012  
 Registered utility model specifications of Japan 1996-2012  
 Published registered utility model applications of Japan 1994-2012

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2009-141419 A (Panasonic Corporation) 2009.06.25, claim7, paragraphs 11,22,57 (No Family)	1
A	JP 2011-135561 A (Sony Corporation) 2011.07.07, Full text; all drawings & US 2011/0128428 A1	1-13
A	JP 2011-040917 A (ROHM Co., Ltd.) 2011.02.24, Full text; all drawings (No Family)	1-13

☐ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

\* Special categories of cited documents:

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

29.10.2012

Date of mailing of the international search report

06.11.2012

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