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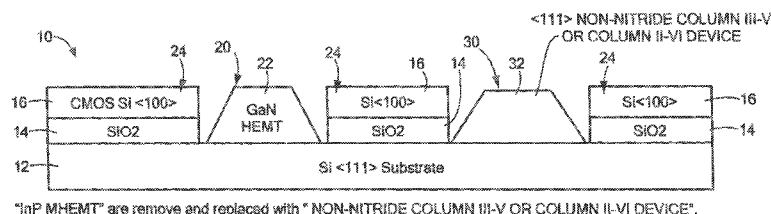


FIG. 2

(57) Abstract: A semiconductor structure having a silicon substrate having a <111> crystallographic orientation, an insulating layer disposed over a first portion of the silicon substrate, a silicon layer having a <100> orientation disposed over the insulating layer, and a non-nitride column III-V semiconductor layer or column II-VI semiconductor layer having the same <111> crystallographic orientation as the silicon substrate, the non-nitride column III-V semiconductor layer or column II-VI semiconductor layer being in direct contact with a second portion of the silicon substrate. A column III-nitride is disposed on the surface of the third portion of the substrate.



**SEMICONDUCTOR STRUCTURE HAVING SILICON DEVICES, COLUMN III-
NITRIDE DEVICES, AND COLUMN III-NON-NITRIDE OR COLUMN II-VI
DEVICES**

TECHNICAL FIELD

5 [0001] This disclosure relates generally to semiconductor structures and more particularly to semiconductor structures having silicon devices, column III-nitride devices, and *column III-non-nitride or column II-VI devices*.

BACKGROUND AND SUMMARY

10 [0002] As is known in the art, many electronics applications incorporate both silicon and column III-V circuits due to their unique performance characteristics. The silicon circuits are typically CMOS circuits used for digital signals and the column III-V circuits are for microwave, millimeter wave, and optical signals. Typically this integration is done by fabricating the silicon and column III-V circuits separately on different chips and then electrically connecting them, often with wire bonds. This process is expensive, limits
15 integration complexity, increases the footprint, and introduces parasitic resistances and inductances which degrade circuit performance.

[0003] It is also known in the art that transistors have been formed on silicon having <100> and <111> crystallographic orientations (i.e., where, as is well known, a <100>
20 crystallographic orientation is where the <100> axis of the crystalline silicon is normal (i.e., perpendicular) to the layer growing or depositing surface of the silicon and a <111> crystallographic orientation is where the <111> axis of the crystalline silicon is normal (i.e., perpendicular) to the layer growing or depositing surface of the silicon). Many years ago, CMOS was formed on silicon substrates having the <111> crystallographic
25 orientation; however this orientation is inferior for CMOS compared to the <100> crystallographic orientation due to a higher surface state density on the <111> crystallographic orientation.

30 [0004] One CMOS structure is formed on a silicon-on-insulator (SOI) structure. This SOI structure includes a silicon substrate having a <100> crystallographic orientation. An insulating layer of SiO₂ is formed on the silicon substrate. An upper device layer of silicon having a <100> crystallographic orientation is formed on the insulating layer; the

insulating layer being used to assist electrical isolation of the CMOS transistor devices formed in the upper silicon layer. Thus, both the upper device layer and the substrate have the same crystallographic orientation (i.e., a $\langle 100 \rangle$ crystallographic orientation).

[0005] It is also known that it is desirable to have silicon CMOS transistors and column III-V (e.g. GaN, GaAs or InP) transistors on a common substrate. One structure used to form CMOS transistors and column III-V transistors on a common substrate is shown in FIG. 1. There, a GaAs transistor is formed on the same substrate as the CMOS transistors. It is also known that GaAs may be grown on a growth layer having a $\langle 100 \rangle$ crystallographic orientation. It is also known in the art that a column III-V (such as a column III-N, for example, GaN, AlN, GaAlN, InGaN) device can be formed on a silicon substrate. Since it is preferable that the GaN device be formed with $\langle 111 \rangle$ crystallographic orientation to minimize crystal defects, the device is typically formed on a substrate (e.g., silicon) having a $\langle 111 \rangle$ crystallographic orientation. This device is shown in the middle portion of the structure shown in FIG. 1.

[0006] On July 3, 2012, U. S. Patent No. 8, 212, 294 was granted, entitled "Structure having silicon CMOS transistors with column III-V transistors on a common substrate", inventors Hoke et. al., assigned to the same assignee as the present patent application. As described therein, a starting wafer comprises a handle silicon substrate with a $\langle 111 \rangle$ orientation, a silicon dioxide insulating layer over a first portion of the $\langle 111 \rangle$ substrate, a silicon $\langle 100 \rangle$ layer disposed over the insulating layer, and a column III-V device having the same crystallographic orientation as the silicon layer disposed on the second portion of the silicon substrate. More particularly, the semiconductor structure includes a column III-As, column III-P, or column III-Sb device on the $\langle 100 \rangle$ silicon layer and is shown in FIG. 1. More particularly, CMOS transistors are formed on one portion of a $\langle 100 \rangle$ silicon layer and an MHEMT device, here an InP MHEMT device having column III-As layers, formed on another portion of the $\langle 100 \rangle$ silicon layer. It is noted that the InP MHEMT is in contact with, and is grown along, the $\langle 100 \rangle$ crystallographic axis of the silicon layer.

[0007] The inventor has recognized that further improvements can be made to the structure described in the above referenced U. S. Patent No. 8, 212, 294 (here shown in FIG. 1). More particularly, the inventor has recognized that:

1. The InP MHEMT is not nearly co-planar with the other device surfaces which complicates device processing.

2. The thermal resistance path for heat generated in the InP MHEMT to the substrate is increased by the presence of the silicon layer and SiO₂ layer.

3. The growth of III-V material such as the InP MHEMT on a Si <100> surface is improved by tilting the Si<100> surface several degrees. The CMOS process, however, is developed on <100> silicon layers that are not misoriented. Tilting the silicon layer can alter the CMOS process by changing the depths of implanted species.

4. The growth of III-V material such as the MHEMT on a tilted <100> silicon surface is improved by performing a high temperature (~900C) anneal to form bilayer steps in the surface. If bilayer steps are not formed, the growth of a binary III-V material on <100> elemental silicon results in antiphase boundary defects. A high temperature anneal could degrade the CMOS and possibly the GaN HEMT present on the wafer.

[0008] Having recognized these effects, the inventor discloses herein a non-nitride column III-V or column II-VI device structure, CdTe, HgCdTe or ZnO devices grown on a third portion of a silicon substrate instead of on the silicon <100> layer disposed over the insulating layer.

[0009] In one embodiment, a semiconductor structure is provided having: a silicon substrate having a <111> crystallographic orientation; an insulating layer disposed over a first portion of the silicon substrate; a silicon layer having a <100> orientation disposed over the insulating layer, a non-nitride column III-V or column II-VI semiconductor layer having the same <111> crystallographic orientation as the silicon substrate, the non-nitride column III-V or column II-VI semiconductor layer being in direct contact with a second portion of the silicon substrate, the non-nitride column III-V or column II-VI semiconductor layer having formed therein an active device.

[0010] In one embodiment, the non-nitride device is a column III-X device, where X is a non-nitride element.

[0011] In one embodiment, the column II-VI semiconductor layer is CdTe, HgCdTe or ZnO.

[0012] In one embodiment, the column III-X device is a column III-As, column III-P, or column III-Sb device or column III alloys of As, P, and Sb.

5 [0013] In one embodiment, the column III-X device is a InP device

In one embodiment, a III-N layer is in direct contact with a third portion of the substrate, where N is nitrogen.

10 [0014] In one embodiment, the silicon layer has active devices fabricated in it such as CMOS transistor devices formed therein.

[0015] With such a structure:

1. The surfaces of the 3 device types, silicon CMOS, GaN HEMT, and InP MHEMT are nearly coplanar.

15 2. The InP MHEMT is grown directly on the silicon substrate resulting in reduced thermal resistance.

3. The growth of the MHEMT on the substrate eliminates any the need to tilt to the CMOS silicon layer.

20 4. The steps in a <111> surface are naturally bilayer so the high temperature bilayer anneal is eliminated.

[0016] The details of one or more embodiments of the disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from
25 the claims.

DESCRIPTION OF DRAWINGS

[0017] FIG. 1 is a simplified cross sectional diagram of a semiconductor structure according to the PRIOR ART; and

30 [0018] FIG. 2 is a simplified cross sectional diagram of a semiconductor structure according to the disclosure.

[0019] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0020] Referring now to FIG. 2, a semiconductor structure 10 is shown having: a silicon substrate 12 having a <111> crystallographic orientation; an insulating layer, 14, here silicon dioxide, disposed over a first portion of the silicon substrate 12; and a silicon layer 16 having a <100> orientation disposed over the insulating layer 14, here silicon dioxide. Such structure to this point may be formed using any conventional process such as that described in the above referenced U. S. Patent No. 8, 212, 294.

[0021] Next, CMOS transistor devices 24 are formed in the silicon layer 16 over a first portion of substrate 12.

[0022] Next, a mask, not shown, is used to mask the formed CMOS transistor devices 24 for protection and a window in the mask is used to etch an opening 20 through the silicon layer 16 and the silicon dioxide layer 14 down to expose a second portion of the silicon substrate 12.

[0023] Next, a GaN transistor device 22 is formed on the exposed second portion of the silicon substrate 12, as shown.

[0024] Next, a mask not shown is used to protect the CMOS transistor devices 24 and the GaN device 22.

[0025] Next, a window in the mask is used to form an opening 30 through the exposed portion of the silicon layer 16 and underlying portion of the silicon dioxide layer 14 to expose a third portion of the silicon substrate 12. Next, a non-nitride device 32 is formed on the exposed third portion of the silicon substrate 12, as shown. More particularly, the non-nitride device 32 is: (a) a column III-X device, where X is a non-nitride element, for example, the column III-X device is a column III-As, column III-P, column III-Sb device, or alloys of As, P, and Sb; here an InP device, Other column III-X devices are possible such as the GaAs HEMT, InP HBT, GaInAs quantum well detector or laser, or InAsSb infrared detector. On the third portion of the silicon substrate column II-VI devices such

as CdTe-based solar cells, HgCdTe infrared detectors, or zinc oxide transparent conductors can also be formed.

[0026] It should now be appreciated, a semiconductor structure according to this disclosure includes: a silicon substrate having a $\langle 111 \rangle$ crystallographic orientation; an insulating layer disposed over a first portion of the silicon substrate; a silicon layer having a $\langle 100 \rangle$ orientation disposed over the insulating layer, a non-nitride column III-V semiconductor layer or column II-VI semiconductor layer having the same $\langle 111 \rangle$ crystallographic orientation as the silicon substrate, the non-nitride column III-V semiconductor layer or column II-VI semiconductor layer being in direct contact with a second portion of the silicon substrate.

[0027] The semiconductor structure may also include one or more of the following features: wherein the non-nitride device is a column III-X device, where X is a non-nitride element; wherein the column III-X device is a column III-As, column III-P, column III-Sb, or column III alloys of As, P, Sb device; including a III-N layer in direct contact with a third portion of the substrate, where N is nitrogen.

[0028] It should also be appreciated a semiconductor structure according to this disclosure includes: a silicon substrate having a $\langle 111 \rangle$ crystallographic orientation; an insulating layer disposed over a first portion of the silicon substrate; a silicon layer having a $\langle 100 \rangle$ orientation disposed over the insulating layer, a non-nitride column III-V semiconductor layer or column II-VI semiconductor layer having the same $\langle 111 \rangle$ crystallographic orientation as the silicon substrate, the non-nitride column III-V semiconductor layer or column II-VI semiconductor layer being in direct contact with a second portion of the silicon substrate, the column III-V semiconductor layer being column III-As, column III-P, column III-Sb, or column III alloys of As, P, Sb device and the column II-VI semiconductor being a column II-O, column II-S, column II-Se, column II-Te or column II alloys of O, S, Se, and Te.

[0029] The semiconductor structure may also include one or more of the following features: including a III-N layer in direct contact with a third portion of the substrate, where N is nitrogen; wherein the silicon layer has a transistor device formed therein;

wherein the silicon layer has CMOS transistor devices formed therein; wherein the column III-V semiconductor layer having formed therein an InP or GaAs or InSb device; wherein the column II-VI semiconductor layer is CdTe, HgCdTe or ZnO.

5 [0030] A number of embodiments of the disclosure have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure. For example, silicon circuits other than CMOS may be fabricated in the silicon layer, 16. Also the III-X layer 32 may contain two device structures grown in the layer stack. Accordingly, other embodiments are within the scope
10 of the following claims.

WHAT IS CLAIMED IS:

- 5 1. A semiconductor structure comprising:
a silicon substrate having a $\langle 111 \rangle$ crystallographic orientation;
an insulating layer disposed over a first portion of the silicon substrate;
a silicon layer having a $\langle 100 \rangle$ orientation disposed over the insulating
layer,
- 10 a non-nitride column III-V semiconductor layer or column II-VI
semiconductor layer having the same $\langle 111 \rangle$ crystallographic orientation as the silicon
substrate, the non-nitride column III-V semiconductor layer or column II-VI
semiconductor layer being in direct contact with a second portion of the silicon substrate.
- 15 2. The semiconductor structure recited in claim 1 where the non-nitride device is
a column III-X device, where X is a non-nitride element.
3. The semiconductor device recite in claim 2 wherein the column III-X device is
a column III-As, column III-P, column III-Sb, or column III alloys of As, P, Sb device.
- 20 4. The semiconductor structure recited in claim 1 including a III-N layer in direct
contact with a third portion of the substrate, where N is nitrogen.
5. The semiconductor structure recited in claim 2 including a III-N layer in direct
25 contact with a third portion of the substrate, where N is nitrogen.
6. The semiconductor structure recited in claim 3 including a III-N layer in direct
contact with a third portion of the substrate, where N is nitrogen.
- 30 7. A semiconductor structure comprising:
a silicon substrate having a $\langle 111 \rangle$ crystallographic orientation;
an insulating layer disposed over a first portion of the silicon substrate;
a silicon layer having a $\langle 100 \rangle$ orientation disposed over the insulating
layer,

a non-nitride column III-V semiconductor layer or column II-VI semiconductor layer having the same $\langle 111 \rangle$ crystallographic orientation as the silicon substrate, the non-nitride column III-V semiconductor layer or column II-VI semiconductor layer being in direct contact with a second portion of the silicon substrate, the column III-V semiconductor layer being column III-As, column III-P, column III-Sb, or column III alloys of As, P, Sb device and the column II-VI semiconductor being a column II-O, column II-S, column II-Se, column II-Te or column II alloys of O, S, Se, and Te.

8. The semiconductor structure recited in claim 7 including a III-N layer in direct contact with a third portion of the substrate, where N is nitrogen.

9. The semiconductor structure recited in claim 9 wherein the silicon layer has a transistor device formed therein.

10. The semiconductor structure recited in claim 9 wherein the silicon layer has CMOS transistor devices formed therein.

11. The semiconductor structure recited in claim 10 wherein the column III-V semiconductor layer having formed therein an InP or GaAs or InSb device.

12. The semiconductor structure recited in claim 1 wherein the column III-V semiconductor layer has formed therein a InP or GaAs or InSb device.

13. The semiconductor structure recited in claim 1 wherein the column II-VI semiconductor layer is CdTe, HgCdTe or ZnO.

14. The semiconductor structure recited in claim 10 wherein the column II-VI semiconductor layer is CdTe, HgCdTe or ZnO.

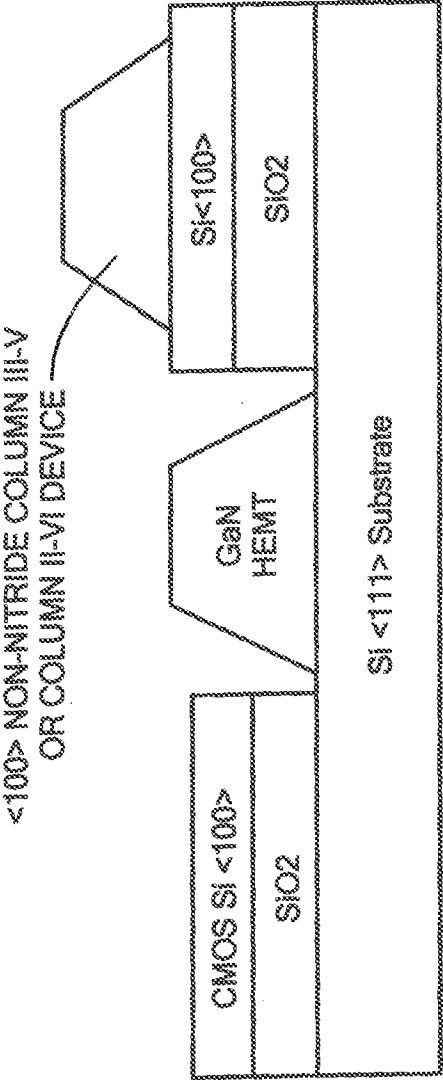
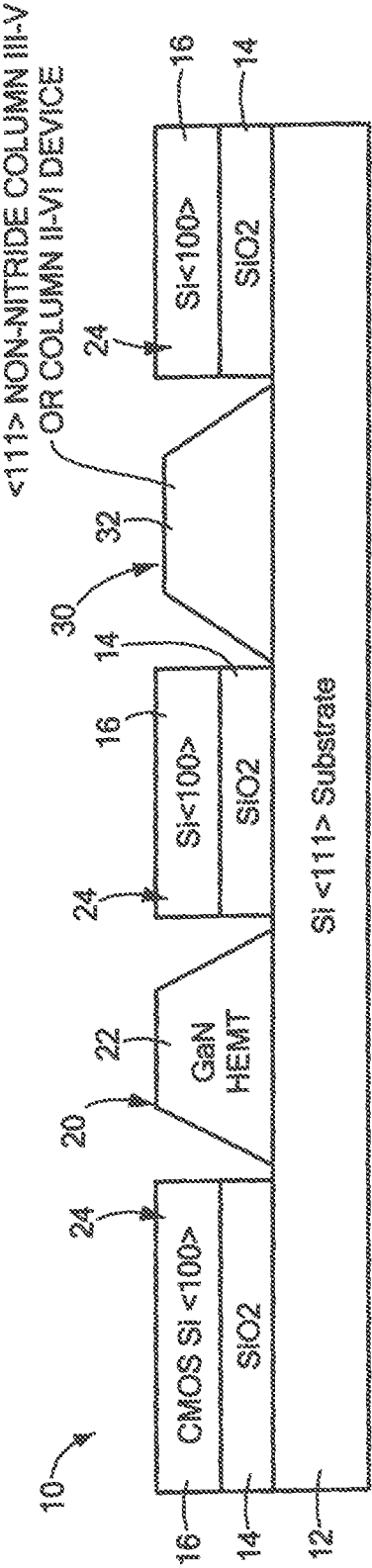


FIG. 1

PRIOR ART



"InP MHEMT" are remove and replaced with "NON-NITRIDE COLUMN III-V OR COLUMN II-VI DEVICE".

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/010397

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/8258 H01L27/06 H01L21/84 H01L27/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No

PCT/US2014/010397

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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Information on patent family members

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