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(54) Title: METHOD FOR SIMULATING AN INTEGRATED CIRCUIT

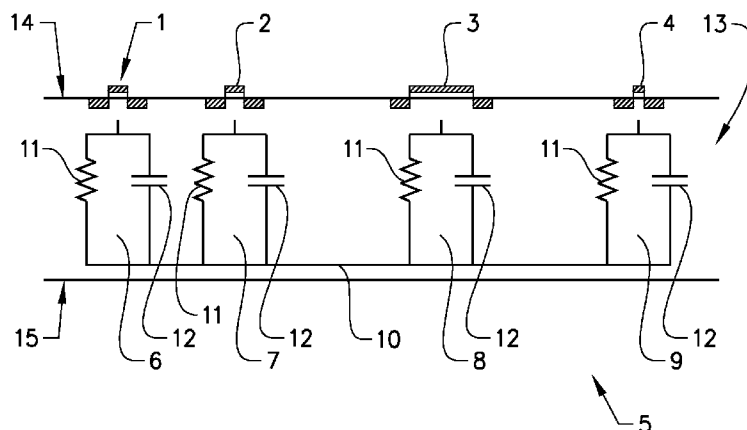


FIG. 1

(57) Abstract: The object of the present invention is to provide an inventive method for analysing an integrated circuit design including substrate coupling effects comprising the steps of providing a circuit schematic (22) of the integrated circuit, modelling the substrate coupling effect by means of an electrical substrate network (5) and analysing (23) the combined circuit schematic (22) and substrate network (5) to evaluate the substrate coupling effects, wherein said modelling and analysing (23) of the substrate coupling effects is performed before determining the relative position of the electrical components (1,2,3,4) on the chip, such that said substrate network (5) can be extracted prior to availability of component placement information.

TITLE

Method for simulating an integrated circuit

TECHNICAL FIELD

- 5 The present invention relates to a method for analysing an integrated circuit design including substrate coupling effects comprising the steps of: providing a circuit schematic of the integrated circuit, modelling the substrate coupling effect by means of an electrical substrate network, and analysing the combined circuit schematic and substrate network to evaluate the
- 10 substrate coupling effects.

BACKGROUND ART

- In integrated circuits all components are located on a common substrate and are interconnected by means of a metallisation network to achieve desired
- 15 function. The common substrate gives rise to unwanted electrical coupling between the electrical components on the substrate, which generates interference and noise between the different electrical components and between the electrical components and the substrate node. Another result of the substrate coupling is increased signal losses, because of the unwanted
- 20 currents through the substrate.

- This phenomenon has earned a lot of attention in semiconductor technology in connection with increased integration on system-on-chip (SOC) solutions. SOC designs can combine memories, processors, I/O interfaces and
- 25 dedicated application-specific logic on a single chip.

- There is a need to predict the substrate coupling effect on the performance of the integrated circuit. Certain computer aided design (CAD) tools which are used for the design of integrated circuits offer an analysis of the substrate
- 30 coupling effects in connection with the traditional design flow. This traditional design flow comprises four main steps:

- Design of circuit schematics which fulfil the requirements of the specification
- Physical design of the corresponding chip circuit layout
- Extraction of parasitic components
- 5 ◦ Analysis and simulation of the integrated circuit including extracted parasitic components

The parasitic components are extracted based on the physical circuit layout which includes placement information, i.e. information about the components' relative placement, in particular the distance between said components. Such a solution is for instance known from JP2207134661A.

The problem with the solution according to the prior art is that the analysis of the substrate coupling need a physical circuit layout to extract the parasitic components. This implies that the circuit analysis must be performed at the end of the design flow. If modifications of the schematics are necessary due to excessive substrate coupling effects, the schematics must be re-designed which implies time consuming and costly design iterations. Normally, several iterations of the steps 1-4 are needed to reach desired performance.

During the design of a circuit, different computer-aided design (CAD) tools are available to support the design process. These tools offer a wide range of services in the design phase like analysis, placement, simulation etc. The CAD tools have however built-in disadvantages. For instance, only physically small circuits can be analysed, because the entire substrate is meshed by the analysing tool into a large amount of small parts, where each part is represented by an equivalent electrical net. The topology of the substrate noise coupling model is also very complex since the relative positions of the electrical components are taken into account. The result is a big network of parasitic components, whereby the simulation time rapidly increases with increasing circuit size.

There is thus a need for an improved method for analysing integrated circuit designs including substrate coupling effects removing the above mentioned disadvantages, i.e. where the substrate coupling effect can be modelled and simulated earlier in the design flow, where the topology of the substrate network which models the noise coupling is less complex, and where the simulation of the integrated circuit can be conducted fast and with less processing resources.

SUMMARY

10 The object of the present invention is to provide an inventive method for analysing substrate coupling effects where the previously mentioned problems are avoided. The object is achieved by the features of the characterising portion of claim 1, wherein the modelling and analysing of the substrate coupling effects is performed before determining the relative positions of the electrical components on the chip, such that said substrate network can be extracted prior to availability of component placement information.

Preferable aspects of the invention are provided by the dependent claims.

20 The extraction of the substrate network prior to physical layout can for instance be performed in that the influence of the relative position of the electrical components on the substrate coupling effect is neglected in said modelling step.

25 According to further advantageous aspect of the invention can the extraction of the substrate network prior to physical layout be performed in that the substrate network is based exclusively on substrate characteristics and geometry of components, wherein the geometry of a component comprises at least the length and width of said component seen from a top side of the chip.

30

Moreover, according to further advantageous aspect of the invention can the physical layout of the integrated circuit design, defining the location of the electrical components on the chip, be produced only after the influence of the substrate coupling effect on the performance of the circuit is considered
5 acceptable.

According to further advantageous aspect of the invention can the substrate network comprise a plurality of connected equivalent impedance nets, each impedance net representing a single electrical component located on the
10 chip.

According to further advantageous aspect of the invention can the equivalent impedance net for at least one single component consist of a single impedance connecting said component with the common substrate node.
15

According to further advantageous aspect of the invention can the equivalent impedance net consist of a parallel-connected resistor and capacitor unit.

According to further advantageous aspect of the invention can the equivalent
20 impedance net consist of a plurality a parallel-connected resistor and capacitor units, and wherein said plurality of units are connected in series.

According to further advantageous aspect of the invention can the equivalent impedance net additionally comprise at least one inductor, preferably in
25 series with a resistor.

According to further advantageous aspect of the invention can the parameters of each single impedance be derived by means of analytical models.
30

According to further advantageous aspect of the invention can the parameters of each single impedance be derived by means of dedicated measurements of the substrate.

- 5 According to further advantageous aspect of the invention can the parameters of each single impedance be derived by means of electromagnetic simulations of the substrate.

- 10 According to further advantageous aspect of the invention can the substrate network comprise one imaginary element for each electrical component to be modelled on the chip, and wherein said imaginary element represents the substrate physics as a function of frequency.

- 15 According to further advantageous aspect of the invention can a computer-readable medium be provided, which stores computer-executable instructions for causing a computer system to perform the inventive method.

BRIEF DESCRIPTION OF THE DRAWINGS

- 20 Figure 1 shows a cross-section of an integrated circuit with several components located on the substrate and an impedance network modelling the substrate coupling according to the invention.

- Figure 2 shows an integrated circuit design flowchart according to the invention.

25

DETAILED DESCRIPTION

- The inventive method defines that an electrical equivalent substrate network representing the physical substrate, and thus the substrate coupling during use of the circuit, is created and incorporated already at the circuit schematic level in the beginning of the design flow, prior to design of the physical layout.
- 30

Said inventive method is based on the finding that the component relative position has less influence on the substrate noise coupling than the component geometry, i.e. length and width of the component. The component relative position is thus less important. When developing this finding another step forward, it can be concluded that the substrate coupling effect can be decided with good accuracy based exclusively on component geometry and substrate characteristics. Finally, as a result of this understanding, improvements of the design flow of integrated circuits are possible since the physical circuit layout is no longer needed to perform an analysis of the substrate coupling effect.

Physical layout or placement is the step where the exact locations for various components on the chip are determined for the first time in the design process. The placement information includes thus in particular the distances between individual components. Based on the physical layout, photomasks are generated which are used in the manufacturing process of the chip.

The design of the substrate network according to the invention, and the parameters of the included elements are based upon the impedance characteristics between a top surface of the semiconducting substrate and a common substrate node. In case of thick substrates, the substrate node represents the semiconductor deep in the substrate. If the backside of the substrate is biased, said backside is taken as the node.

For each component which interacts with the substrate, a unique impedance is calculated. This unique impedance is modelled by means of an equivalent impedance net. These separate equivalent impedance nets, each representing a specific component, are then subsequently connected via the common substrate node to a final impedance network, which is connected to the circuit schematic.

In the following only one embodiment of the invention is shown and described, simply by way of illustration of one mode of carrying out the invention.

- 5 Figure 1 shows a side view of a substrate 13 comprising a first MOS-transistor 1, a second MOS-transistor 2, a third MOS-transistor 3, and a fourth MOS-transistor 4 placed on a top surface 14 of said common substrate 13. Figure 1 further shows an equivalent impedance network 5 modelling the substrate impedance between said transistors 1, 2, 3, 4 located on the top
10 surface 14 and a common substrate node 10. Said equivalent impedance network 5 comprises a plurality of equivalent impedance nets 6, 7, 8, 9, each representing the impedance between respective transistor 1, 2, 3, 4 and the common substrate node 10. The impedance nets 6, 7, 8, 9 comprise a parallel-connected resistor 11 and capacitor 12 to properly represent the
15 resistivity and permittivity of the substrate, such that the substrate coupling can be analysed and simulated. The impedance network 5 is subsequently the result of connecting each single equivalent impedance net 6, 7, 8 and 9 together via the common substrate node 10.
- 20 The determination of the parameters in said impedance nets is for instance performed with aid of analytical models or measurements. It is also possible to use electromagnetic simulators which traditionally are used for other purposes. The impedance calculations and simulations require substrate characteristics in form of a resistivity profile, doping structure, etc. The
25 manufacturer of the semiconducting substrate can possibly provide this information. The resistivity profile can also be determined by measuring suitable test structures.

Analytical model

- 30 Determination of impedance parameters by means of analytical model: Equations for the resistance and capacitance are used. The simplest example is the resistance between a circular top surface and the backside

surface on a substrate with uniform resistivity. The equation reads $R = \frac{\rho}{4r}$

where ρ is the resistivity and r is the top surface radius. The capacitance C is then given from the relation $\rho\varepsilon = RC$ where ε is the substrate permittivity.

For noncircular surfaces more elaborate formulas must be used. Having

- 5 nonuniform substrates makes the analytical modelling approach progressively more difficult.

Measurements

Determination of impedance parameters by means of measurements:

- 10 Dedicated test structures are realized on a chip and subsequently characterised using appropriate measurement equipment. A simple structure to measure substrate impedance could thus be a substrate contact, by which a varying voltage and frequency is inputted, and wherein the substrate currents are measured. Having measurement data, an impedance network is
- 15 chosen and the impedance parameters are determined in such a way that the impedance behaviour matches the measurements as closely as possible.

Electromagnetic (EM) simulations

Determination of impedance parameters by means of electromagnetic

- 20 simulations: The desired geometries are defined as well as the substrate characteristics. The impedance is then simulated by solving Maxwell's equations in the structure using dedicated tools. The output is the impedance data similar to those obtained in the measurement. Having the impedance data, work identical to that described in the measurements method is
- 25 required.

The chosen substrate equivalent net should describe the frequency behaviour of the real impedance between component on the substrate top surface and the common substrate node. Therefore net topologies other than

30 the simple parallel resistor-capacitor unit might be required. From a physical point of view, such a simple model is only valid for a semiconductor substrate

having a uniform resistivity and capacity throughout the entire substrate. If the substrate characteristic is nonuniform, other net configurations of resistors and capacitors must be used to reflect the frequency behaviour. Since the electrical substrate coupling can be resistive, capacitive or inductive by nature, inductors might also need to be included in the net if required.

Another approach is to consider the substrate physics at all given data of the impedance as a function of frequency. Such data can be obtained from measurements and/or EM simulations. Next, an equivalent net consisting of resistors, capacitors, and/or inductors is designed to reproduce the measured impedance behaviour. The net topology and resistance, capacitance, and inductance parameters are chosen arbitrarily. The net and the parameters need however not have any physical interpretation as long as the behaviour is properly described. The elements in the equivalent net need also not be represented by resistors and capacitors, but merely a special imaginary component, which correctly represents the substrate impedance as a function of frequency.

Figure 2 shows the integrated circuit design flowchart according to an embodiment of the invention. The inventive method for simulating a circuit schematic including substrate parasitic elements before determining the physical layout comprises extraction and inclusion of the substrate parasitic components based on the circuit schematics. Said extraction comprises determining the substrate impedances between the components on the chip and their common substrate node, determining a suitable equivalent impedance net for each component on the chip, joining the equivalent impedance nets of each component to a complete impedance network representing the substrate impedance, and connecting the complete equivalent impedance network to the components in the circuit schematic.

Said circuit schematic 22 including the equivalent impedance network is subsequently analysed and simulated 23 to evaluate the effects the substrate coupling. If said effects are considered to negatively influence the performance 24 of the circuit to an unacceptable extent, the circuit

5 schematics 22 must be iteratively redesigned. If an acceptable performance 24 of the circuit schematics 22 is obtained, a physical layout 25 based on the circuit schematics 22 is produced. Optionally, based on said physical layout 25, further parasitic components can be extracted 26 and included in a more accurate and detailed subsequent analysis and simulation 27. If the substrate

10 coupling effect is considered to negatively influence the performance 28 of the circuit to an unacceptable extent, the designer can choose, depending on the extent and type of substrate coupling, to either amend the circuit schematics 22 or the physical layout 25. If an acceptable performance 28 of the physical layout 25 is obtained, the integrated circuit design can proceed

15 to production.

The results of the substrate coupling analysis performed before determining the physical layout is useful also in case further analysis is performed since a first optimisation is accomplished, and the results thereof will reduce

20 subsequent design iterations and increase analysis efficiency.

The invention is not limited to the specific design flowchart presented, but includes all variations within the scope of the present claims. The internal sequence of the steps for arriving at a circuit schematic including the

25 equivalent impedance network can of course be varied according to the demands of each specific design. After determining a suitable equivalent impedance net for a component, said impedance net can thus be directly joined to impedance network representing the substrate impedance, or be directly joined to the circuit schematic. Besides, the optional extraction of

30 remaining parasitic components and its associated simulation can be omitted.

The inventive method covers all equivalents to the term "circuit schematics". The basis for the extraction of substrate parasitic components includes thus all abstract electrical circuit representations, which symbolise the devices of the chip using graphical symbols, and which do not resemble the physical layout of the circuit. The schematics can for instance be a gate-level representation or a logic-level representation of the circuit. The only parameter which must be included in said schematics is the geometry of the electrical components on the chip. This requirement is however easily fulfilled, since to achieve desired circuit performance, the chip components must be correctly dimensioned, and in integrated circuits, the component geometry is the basic parameter over which the designer has control. For instance, to realise a transistor with a certain driving power, the designer must choose appropriate component length and width. Since this choice must be made already at the circuit schematic level, the geometry of the electrical components on the chip is available.

The term "electrical component" is considered to encompass all different kinds of components located on a chip and which is connected to the common substrate such that they can electrically interact with other electrical components through the substrate, and/or the substrate node. Examples of such components are transistors, diodes, substrate contacts, guard rings, resistors, capacitors, inductors.

The advantages with the inventive method are reduced number of time consuming and costly design iterations. The inventive method allows circuit analysis of substrate coupling effects already in the first step of the design flow, contrary to the method according to the prior art where said analysis is performed in the last step of the design flow. The inventive method is also not limited to analysis of small circuits, because the impedance network is relatively small and comprises only a single impedance for each component. The impedance network can thus easily be simulated.

The invention is not limited to the specific equivalent impedance network presented in figure 1, but includes all variations within the scope of the present claims. Inductors may for instance be included in the network if needed, in particular in series with the resistors. In case of a layered

5 substrate, i.e. where the substrate resistivity and capacity are assumed to be constant only in layers, and wherein the substrate comprises a plurality of such layers, the equivalent impedance net representing the substrate impedance of each component may comprise a plurality of parallel-

10 connected resistor and capacitor units, each such unit representing a specific layer. Said parallel-connected resistor and capacitor units, each representing a layer in the substrate, are consequently connected in series to model the layered substrate correctly.

As will be realised, the invention is capable of modification in various obvious

15 respects, all without departing from the scope of the appended claims. Accordingly, the drawings and the description thereto are to be regarded as illustrative in nature, and not restrictive.

CLAIMS

1. A method for analysing an integrated circuit design including substrate coupling effects comprising the steps of:
 - 5 providing a circuit schematic (22) of the integrated circuit design;
 modelling the substrate coupling effect by means of an electrical substrate network (5); and
 analysing (23) the combined circuit schematic (22) and substrate network (5) to evaluate the substrate coupling effects,
10 **characterised in that**
 said modelling and analysing (23) of the substrate coupling effects is performed before determining the relative position of the electrical components (1,2,3,4) on the chip, such that said substrate network (5) can be extracted prior to availability of component
15 placement information.
2. A method for analysing an integrated circuit according to claim 1,
wherein the influence of the relative position of the electrical components (1,2,3,4) on the substrate coupling effect is neglected in
20 said modelling step.
3. A method for analysing an integrated circuit according to any
proceeding claim, wherein the substrate network (5) is based
exclusively on substrate characteristics and geometry of components
25 (1,2,3,4).
4. The method according to claim 3, wherein the geometry of a
component (1,2,3,4) comprises at least the length and width of said
component (1,2,3,4) seen from a top side of the chip.
30
5. A method for analysing an integrated circuit according to any
proceeding claim, wherein a physical layout (25) of the integrated

circuit design, defining the location of the electrical components (1,2,3,4) on the chip, is produced only after the influence of the substrate coupling effect on the performance of the circuit is considered acceptable.

5

6. The method according to any proceeding claim wherein the substrate network (5) comprises a plurality of connected equivalent impedance nets (6,7,8,9), each impedance net (6,7,8,9) representing a single electrical component (1,2,3,4) located on the chip.

10

7. The method according to claim 6 wherein said equivalent impedance net (6,7,8,9) for at least one single component (1,2,3,4) consists of a single impedance connecting said component (1,2,3,4) with a common substrate node (10).

15

8. The method according to claim 7 wherein said equivalent impedance net (6,7,8,9) consists of a parallel-connected resistor (11) and capacitor (12).

20

9. The method according to claim 7 wherein said equivalent impedance net (6,7,8,9) consists of a plurality a parallel-connected resistor (11) and capacitor (12) units, and wherein said plurality of units are connected in series.

25

10. The method according to any of claims 7 - 9 wherein said equivalent impedance net (6,7,8,9) further comprises at least one inductor, preferably in series with a resistor (11).

30

11. The method according to any of claims 6 - 10 wherein the parameters of each single impedance is derived by means of analytical models.

12. The method according to any of claims 6 - 10 wherein the parameters of each single impedance is derived by means of dedicated measurements of the substrate (13).
- 5 13. The method according to any of claims 6 - 10 wherein the parameters of each single impedance is derived by means of electromagnetic simulations of the substrate (13).
- 10 14. The method according to any of claims 1 to 5 wherein the substrate network (5) comprises one imaginary element for each electrical component (1,2,3,4) to be modelled on the chip, and wherein said imaginary element represents the substrate physics as a function of frequency.
- 15 15. A computer-readable medium storing computer-executable instructions for causing a computer system to perform the method of any of claims 1 - 14.

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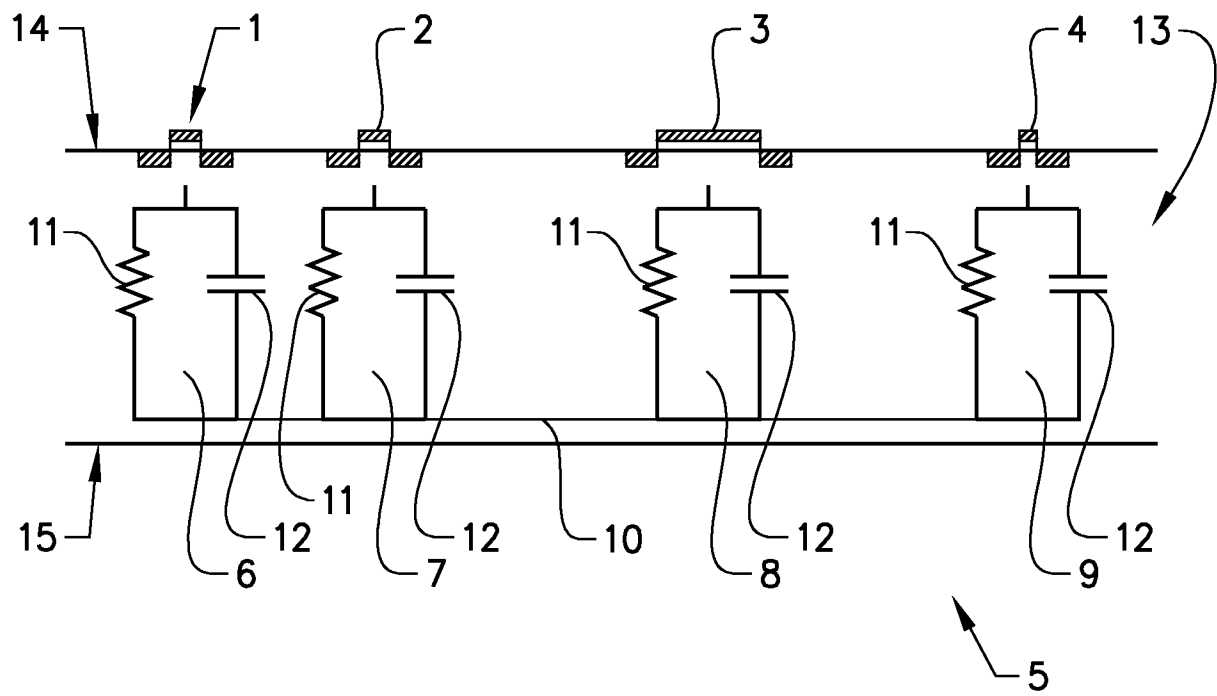


FIG. 1

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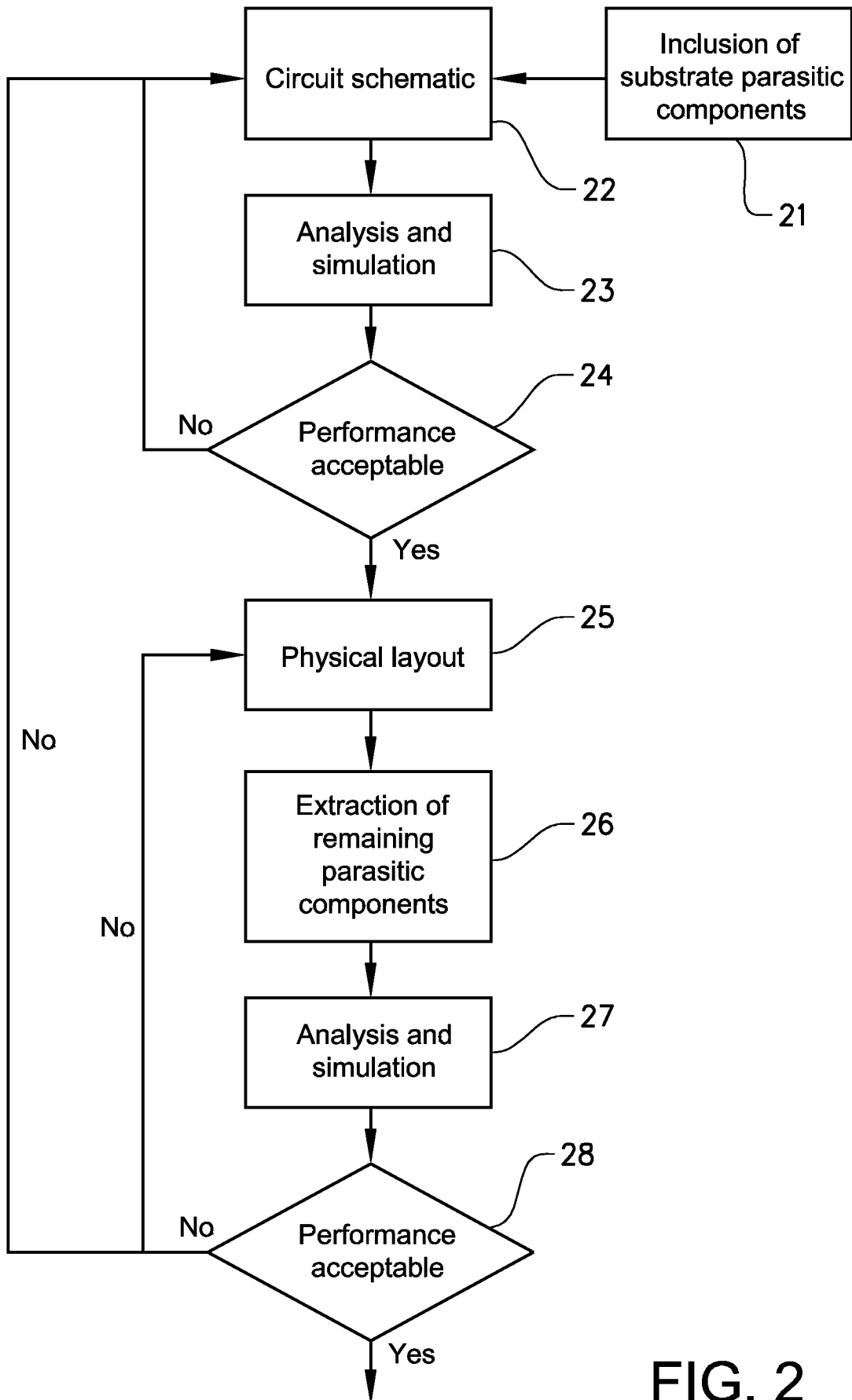


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE2009/050531

A. CLASSIFICATION OF SUBJECT MATTER

IPC: see extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ, NPL, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	"Schematic-driven substrate noise coupling analysis in mixed-signal IC design" - P. Birrer et al, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS--I: REGULAR PAPERS, VOL. 53, NO. 12, DECEMBER 2006; whole document --	1-15
A	"Noise constraint driven placement for mixed signal designs" - W.H. Kao and W.K. Chu, Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03, pp. IV-712- IV-715, 25-28 May 2003; whole document --	1-15
A	US 20040117162 A1 (D. OZIS ET AL), 17 June 2004 (17.06.2004), whole document --	6-14

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Date of the actual completion of the international search

5 February 2010

Date of mailing of the international search report

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Cited literature, if any, will be enclosed in paper form.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/SE2009/050531

US 20040117162 A1 17/06/2004 NONE
