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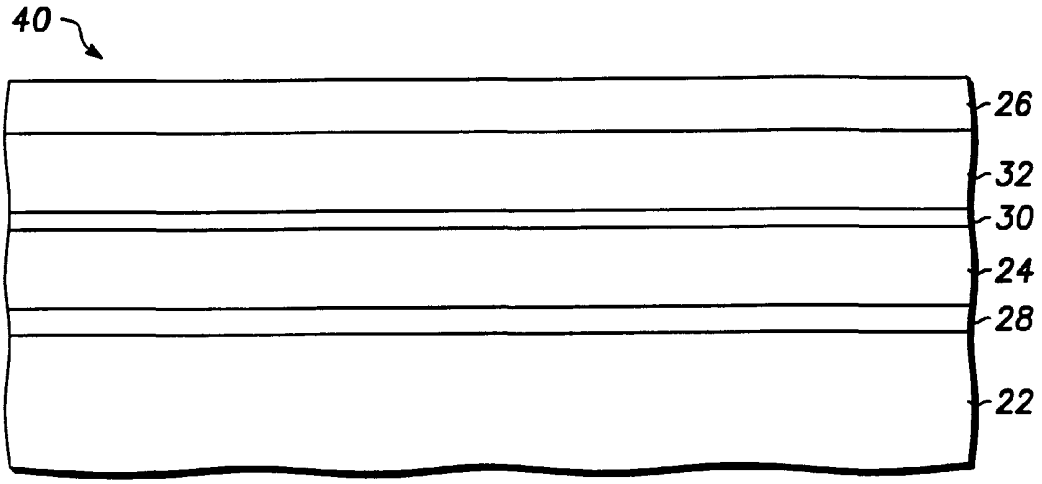
(54) **Title:** INTEGRATED RADIATION EMITTING SYSTEM AND PROCESS FOR FABRICATING SAME



(57) **Abstract:** High quality epitaxial layers of compound semiconductor materials can be grown overlying large silicon wafers by first growing an accommodating buffer layer on a silicon wafer. The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer. Radiation systems, including radiation sources such as light emitting diode or lasers and wave guides may be formed in the high quality epitaxial compound semiconductor material and above the oxide layers.

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INTEGRATED RADIATION EMITTING SYSTEM AND PROCESS FOR FABRICATING SAME

Field of the Invention

This invention relates generally to semiconductor structures and devices and to a method for their fabrication, and more specifically to integrated, monolithic radiation systems including an electromagnetic radiation source and a wave guide.

Background of the Invention

The vast majority of semiconductor discrete devices and integrated circuits are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. Other semiconductor materials, such as the so called compound semiconductor materials, have physical attributes, including wider bandgap and/or higher mobility than silicon, or direct bandgaps that make these materials advantageous for certain types of semiconductor devices. Unfortunately, compound semiconductor materials are generally much more expensive than silicon and are not available in large wafers as is silicon. Gallium arsenide (GaAs), the most readily available compound semiconductor material, is available in wafers only up to about 150 millimeters (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and are widely available at 200 mm. The 150 mm GaAs wafers are many times more expensive than are their silicon counterparts. Wafers of other compound semiconductor materials are even less available and are more expensive than GaAs.

Because of the desirable characteristics of compound semiconductor materials, and because of their present generally high cost and low availability in bulk form, for many years attempts have been made to grow thin films of the compound semiconductor materials on a foreign substrate. To achieve optimal characteristics of the compound semiconductor material, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow layers of a monocrystalline compound semiconductor material on germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting thin film of compound semiconductor material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline compound semiconductor material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in that film at a low cost compared to the cost of fabricating such devices on a bulk wafer of compound semiconductor material or in an epitaxial film of such material on a bulk wafer of compound semiconductor material. In addition, if a thin film of high quality monocrystalline compound semiconductor material could be realized on a bulk wafer such as a silicon wafer, an integrated device structure could be achieved that took advantage of the best properties of both the silicon and the compound semiconductor material.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline compound semiconductor film over another monocrystalline material and for a process for making such a structure.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 - 3 and 11 - 12 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer;

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer; and

FIGS. 9 - 10 and 13 - 21 include illustrations of cross-sectional views of a portion of various radiation systems in accordance with the present embodiment.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. For example, the material could be an oxide or nitride having a lattice structure substantially matched to the substrate and to the subsequently applied semiconductor material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24.

Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 26 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide

(AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials in the indium phosphide (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice structure of the compound semiconductor material exhibits a 45 degree rotation with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1),which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that tend to be polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material. For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26, may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In Accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template for the deposition of a compound semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIG. 9 illustrates a top view and FIG. 10 illustrates a side view of a monolithic, integrated system 90 for transmitting electromagnetic radiation in accordance with an exemplary embodiment of the present invention. System

90 includes a radiation emitting device 92, a wave guide 94, and a radiation detection device 96. In accordance with various aspects of this embodiment, emitting device 92 and detection device 96 may be configured to transmit and receive electromagnetic radiation of various wavelengths. However, the invention is conveniently described below in the context of transmitting light having a wavelength or wavelengths between the infra red and ultra violet regions of light. In this case, emitting device 92 is a laser or a light emitting diode, detection device 96 is a photo detector, and both are formed within a compound semiconductor region of system 90.

Laser 92, wave guide 94, and photo detector 96 are formed over a Group IV substrate 1002 and an amorphous oxide layer 1004 formed thereon, wherein amorphous oxide layer 1004 is formed according the method described above, for example, in connection with layer 36. In accordance with an alternate embodiment of the invention, laser 92, guide 94, and detector 96 may be formed over a monocrystalline oxide such as layer 24 discussed above in connection with FIGS. 1,2, and 5.

In accordance with one aspect of the embodiment illustrated in FIGS. 9 and 10, laser 92 includes an edge emitting laser, having a first cladding layer 1006, an active layer 1008; and a second cladding layer 1010. Layers 1006-1010 may be formed of any suitable semiconductor material such as the compound semiconductor materials discussed above in connection with layer 26. For example, first cladding layer 1006 may include n-type doped AlGaAs, active layer 1008 may include GaAs, and second cladding layer 1010 may include p-type doped AlGaAs, where each of layers 1006-1010 is epitaxially formed over substrate 1002. Although not illustrated in the drawing figures, laser 92 may also include insulating layers to facilitate electrical isolation of laser 92 or components thereof and/or conducting layers to facilitate coupling of laser 92 to other devices or components.

In general, wave guide 94 is configured to transmit and guide light transmitted by laser 92 to a location away from laser 92. More specifically, wave guide 94 guides light through a first portion or core 1012, which is surrounded by a second portion 1014 and a third portion 1016; second portion 1014 and third portion 1016 are know as cladding layers. Preferably, guide 94 is designed such that substantially all light received by a first end 1018 is confined within fist portion 1012 of guide 94 during light transmission toward a second end 1020 of guide 94. In other words, the light is preferably transmitted through guide 94 with total internal reflection.

To obtain total or at least substantial internal reflection, first portion 1012 is formed of a material having a different index of refraction than material used to form second and third portions 1014 and 1016. More particularly, the index of refraction of portion 1012 is greater than the index of refraction of portions 1014 and 1016, which may suitably be formed of the same material. In accordance with an exemplary embodiment, material selected for portion 1012 has an index of refraction, n1, material selected for portions 1014 and 1016 has an index of refraction of n2, and the difference between n1 and n2 is about 0.02.

Suitable materials for wave guide portions 1012-1016 include oxides such as alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, perovskite oxides, other suitable oxides, nitrides, and the like. For example, one or more of portions 1012-1016 may include a monocrystalline oxide such as that described above in connection with any of FIGS. 1-3. In accordance with one particular example, portion 1012 may include strontium titanate doped with a material (*e.g.*, an impurity), and portions 1014 and 1016 may include undoped strontium titanate such that the refractive index of portions 1014,1016 is lower than the refractive index of portion 1012.

Detector 96 is generally configured to convert light received from laser 92 into an electrical signal. In accordance with the exemplary embodiment illustrated in FIGS. 9 and 10, detector 96 includes an active region 1022 and contacts 1024 and 1026. Active region 1022 may be formed of a variety of crystalline, polycrystalline, or amorphous materials such as silicon, GaAs, and InGaAs; however, in accordance with one embodiment of the present invention, region 1022 is formed of the same material used to form region 1008 of laser 92, such as monocrystalline GaAs.

Monolithic system 90 may be formed on Group IV substrate 1002, which may include various devices such as CMOS circuits formed therein, by forming amorphous layer 1004, using a suitable cap layer that is not shown in FIGS. 9 or 10, as discussed above in connection with FIGS. 3 and 7. Suitable layers for cladding and active regions of a laser are then formed on the monocrystalline substrate. For example, as illustrated in FIG. 11, an AlGaAs layer 1102, a GaAs layer 1104, and an AlGaAs layer 1106 can be formed over now amorphous layer 1004. Alternatively, layers 1102, 1106 and active region 1104 can be formed over a monocrystalline oxide layer as discussed above in connection with FIGS. 1-2.

Next, a portion of layers 1102, 1104, and 1106 may be removed to form structure 1200, illustrated in FIG. 12, using suitable photolithographic and etching techniques. In accordance with the illustrated example, a portion of all of layers 1102-1106 is removed from a region 1202, and a portion of layer 1106 is removed from a region 1204 to define a portion of detector 96. Contacts 1024 and 1026 may then be formed on a surface of layer 1022, for example, using conductive material (*e.g.*, metal) deposition and etch techniques.

Wave guide 94 may then be formed on structure 1200 by depositing radiation transmissive material suitable for second portion 1014, forming a patterned portion 1012 over portion 1014 using, for example, photolithography techniques, and depositing material to form third portion 1016 of wave guide 94, such that one end of guide 94 is aligned to and preferably contacts an output section of source 92 and another end of guide 94 is in alignment with and preferably contacts an input of detector 96.

Although not illustrated in FIGS. 9-12, system 90 may suitably include electronic circuits coupled to emitter 92 and/or detector 96. For example, system 90 may include drive circuitry, for emitter 92 or detector 96, formed within either substrate 1002 and/or within compound semiconductor material epitaxially grown thereon.

FIGS. 13 and 14 illustrate a top view and a side view, respectively, of a planar system 1300, including a microelectronic circuit 1302, an emitter 1304 (*e.g.*, laser) coupled to circuit 1302, a wave guide 1306, and a detector 1308 in accordance with an alternate embodiment of the present invention. Emitter 1304, wave guide 1306, and detector 1308 of system 1300 may be formed using the process and materials described above in connection with system 90, except that the emitter, wave guide, and detector are formed within a trench 1310 created within a monocrystalline Group IV semiconductor substrate 1312, such that light can be transmitted from emitter 1304 toward detector 1308 along a path that is substantially parallel to a bottom surface of the groove formed in the substrate. Planar structure 1300 also includes a planarizing or filler compound 1404, which may include spin on glass or the like.

Trench 1310 may be formed by etching substrate 1312 along crystalline planes. For example, if substrate 1312 includes (100) silicon, trench 1310 may be formed by exposing substrate 1312 to a wet etch environment such that trench 1310 includes a substantially planar surface 1402 that is substantially parallel to the substrate surface, over which layer 1314 and laser 1304 may be formed, and sidewalls 1408 that are substantially parallel to other crystalline planes of substrate 1312.

As illustrated in FIGS. 13 and 14, circuit 1302 may be formed within substrate 1312 and coupled to source 1304 by, for example, using a conductive plug 1410 and a conductive line 1412 formed over planarizing material 1404. Alternatively, circuit 1302 could be formed within a monocrystalline compound semiconductor layer grown above an amorphous oxide layer using a suitable template layer to facilitate monocrystalline growth of the additional semiconductor layer.

Circuit 1302 may include any device suitable for driving laser 1304 and may be formed within any suitable semiconductor material. For example, the semiconductor material may include Group IV compounds such as silicon, germanium, silicon germanium, silicon germanium carbide, or compound semiconductor material such as GaAs and other materials discussed above in connection with examples 1-6 provided above.

Although not illustrated, both systems 90 and 1300 may include other electronic circuits in addition to circuit 1302. For example, systems 90 and 1300 may include tuning circuits, feedback control circuits, and the like, which are discussed in greater detail hereinbelow.

In accordance with an alternate embodiment of the invention, only laser 1304 is formed within a trench. In this case, light emitted from laser 1304 travels from laser 1304 to sloped sidewalls 1408, and at least a portion of the emitted light is reflected from the sidewalls toward the top of trench 1402. A fiber optic cable, a wave guide, or other suitable device may be attached to the top surface to capture the reflected light.

FIG. 15 illustrates a top view of a system 1500 in accordance with another exemplary embodiment of the present invention. System 1500 is configured to transmit electromagnetic radiation such as light from a source to a location "off chip." Generally, system 1500 includes an emitter 1502 as a radiation source, a wave guide 1504 (optional), and a fiber optic cable or optical fiber 1506. Emitter 1502 and wave guide 1504 are formed using the materials and processes described above in connection with emitters 92, 1304 and wave guides 94, 1306. In particular, emitter 1502 and guide 1504 are formed over a monocrystalline Group IV substrate, as described above.

A first end 1508 of cable 1506 is generally aligned with either an output end of a wave guide 1504 or an output of source 1502 (in which case wave guide 1504 is not required), such that substantially all radiation generated by source 1502 enters cable 1506. To facilitate coupling of cable 1506 to either of guide 1504 or source 1502, a V-shaped groove 1602, illustrated in FIG. 16, is formed in a substrate 1604. Cable 1506, which generally has a circular cross section having a diameter, can then be fixedly attached to substrate 1604 within groove 1602, such that at least a portion of cable 1506 resides within a portion groove 1602. In accordance with one aspect of this embodiment, groove 1602 is formed by etching substrate 1604, and a depth of groove 1602 is selected such that cable 1506 and output from guide 1504 or laser 1502 are substantially aligned, *e.g.*, a center of cable 1506 and a center of guide 1504 are aligned.

FIG. 17 illustrates another embodiment of the invention in which both a radiation emitting source and a fiber optic cable are located within a trench formed within a substrate. As illustrated, a system 1700 includes an edge emitting radiation source 1702, such as an edge emitting laser, formed within a first portion of a groove 1704, a fiber optic cable 1706 formed within a second portion 1708 of the groove, and a source control circuit 1710 formed within a substrate 1712 and coupled to source 1702 via conductive path 1714. In accordance with one aspect of this embodiment, source 1702 includes an edge emitting laser formed according to the process described above in connection with source 1304 and trench portions 1704 and 1708 are formed according to the process described above in connection with trench 1310. Depths of first and second portions 1704, 1708 are preferably selected such that radiation emitted from source 1702 is substantially aligned with a center of cable 1706. In accordance with one aspect of this embodiment, a depth of second portion 1708 is greater than a depth of first portion 1704 to facilitate alignment of radiation output from source 1702 and the center of cable 1706.

FIG. 18 illustrates a system 1800, including a feedback control loop, in accordance with yet another embodiment of the present invention. System 1800 includes a radiation emitter 1802, a radiation detector 1804, a feedback control circuit 1806, a driver 1808, an optical device 1810 (*e.g.*, a fiber optic cable), and a wave guide 1812 coupled to both device 1810 and radiation detector 1804. In accordance with the present invention, each of emitter 1802, detector 1804, circuit 1806, driver 1808, and guide 1812 are monolithically integrated on a Group IV substrate.

In general, system 1800 is configured to control an output from source 1802, for example, at a desired intensity level, using a feedback loop 1814, including a feedback path from detector 1804 to device 1802. In accordance with the illustrated example, detector 1804 (with appropriate receiver circuitry) converts radiation emission such as light received from source 1802 into an electrical signal, circuit 1806 manipulates the signal from detector 1804 with an appropriate gain, and driver circuit 1808 sends a signal to source 1802 in response to a signal received from circuit 1806.

Detector 1804 circuitry, feedback circuit 1806, and driver circuit 1808 may be formed in any suitable semiconductor layer. For example, circuit 1808 may be formed within the Group IV (*e.g.*, silicon) substrate or within any semiconductor material deposited thereon.

FIG. 19 illustrates a monolithic multiplexing system 1900 in accordance with another exemplary embodiment of the present invention. System 1900 includes a radiation source 1916, which includes one or more light sources (*e.g.*, light emitting diodes or lasers) 1902, 1904, 1906, 1908, and 1910, wherein each light source is capable of producing radiation having, respectively; a wavelength of 81, 82, 83, 84, and 85; a wave guide 1912; and a fiber optic cable 1914.

Light sources 1902-1910 and guide 1912 may be formed and cable 1914 may be attached to a substrate 1919 according to the methods described above in connection with FIGS. 9-17, except that in the embodiment illustrated in FIG. 19, guide 1912 includes multiple branches extending to a plurality of sources. For example, in accordance with one aspect of this embodiment, sources 1902-1910 are formed over an amorphous oxide layer such as layer 36, illustrated in FIG. 3, or a monocrystalline oxide layer such as layer 24, illustrated in FIG. 1, and guide 1912 is formed within or above the amorphous or monocrystalline layers.

In accordance with an alternate aspect of this embodiment, source 1916 includes a radiation emitting source capable of emitting radiation over a spectrum of wavelengths and a grating coupled to the source for separating a plurality of wavelengths from the spectrum of wavelengths, such that a desired wavelength or wavelengths may be selected. For example, source 1916 may include a fiber optic cable coupled to a grating to selectively transmit light of a desired wavelength or wavelengths to a portion or portions of guide 1912.

FIG. 20 illustrates a top view of a monolithic demultiplexing system 2000 in accordance with another exemplary embodiment of the present invention. System 2000 includes a radiation source which brings radiation having a plurality of wavelengths onto the chip and/or a radiation transmission medium such as a fiber optic cable 2004, a demultiplexer 2006, wave guides 2008, 2010, and 2012, and radiation detectors 2016, 2018, and 2020. The source may include a plurality of radiation emitting devices (*e.g.*, in an array) or a fiber optic cable carrying radiation having a plurality of wavelengths. System 2000 is generally configured to transmit radiation of multiple wavelengths from source 2002 through a cable 2004, separate the radiation according to wavelength at demultiplexer 2006, and send radiation of a particular wavelength to each of detectors 2016-2020.

In accordance with one aspect of the present embodiment, demultiplexer 2006 includes one or more directional couplers epitaxially formed over an oxide such an oxide described above in connection with FIGS. 1-3. Each decoupler includes a grating and is configured to separate radiation of one wavelength from a stream of radiation including radiation of one or more wavelengths. The separated light may then be transmitted to one of detectors 2016-2020 through one of wave guides 2008-2012 and/or directed toward one of detectors 2016-2020 using beveled, reflective surfaces to direct the light toward the detector.

System 2000 may also suitably include a circuit 2022 configured to tune one or more of the directional couplers within demultiplexer 2006. In accordance with one aspect of the invention, circuit 2022 may be formed within the Group IV substrate. Alternatively, circuit 2022 may be formed within one or more of the epitaxial compound semiconductor layers formed above the Group IV substrate.

Source 2002, guides 2008-2012, and detectors 2016-2020 may be formed in accordance with processes described above in connection with source 92, guide 94, and detector 96, and source 2002 may be formed on a separate substrate than the substrate that includes guides 2008-2012 and detectors 2016-2020. Further, cable 2004 may be coupled to source 2002 and demultiplexer 2006 according to the method described above in connection with attaching cable 1506 to source 1502.

FIG. 21 illustrates a system 2100, including a vertical cavity surface emitting laser (VCSEL) 2102 in accordance with another exemplary embodiment of the invention. VCSEL 2102 includes bottom mirror layers 2104; a laser cavity region 2106; an upper mirror region 2108; a ring-shaped contact 2110; and a wave guide 2112, having cladding layers 2114 and a core layer 2116. Although wave guide 2116 is illustrated as formed above VCSEL 2102, in accordance with an alternative embodiment of the present invention, VCSEL 2102 may be formed over a monocrystalline oxide layer (which may have been exposed to an anneal process to cause the oxide to become amorphous), which oxide layer serves as a portion of the wave guide. In other words, VCSEL 2102 may suitably be formed on top of or over a portion of the wave guide.

VCSEL 2102 is formed by epitaxially growing lower mirror layers 2104, laser cavity region 2106 layers, and upper mirror layers 2108 over a Group IV substrate 2122 (which may include various devices such as CMOS circuits formed therein) and an amorphous oxide layer 2124, as discussed above in connection with FIGS. 3 and 7. Alternatively, mirror layers 2104, 2108 and active region 2106 may be formed over a monocrystalline oxide layer as discussed above in connection with FIGS. 1-2.

Lower mirror layers 2104 include alternating layers of compound semiconductor materials. For example, the first, third, and fifth films within the optical laser may include a material such as gallium arsenide, and the second, fourth, and sixth films within the lower mirror layer 2104 may include aluminum gallium arsenide or vice versa.

Upper mirror layers 2108 are formed in a similar manner to the lower mirror layer 2104 and include alternating films of compound semiconductor materials. In one particular embodiment, the upper mirror layer 2108 may be p-type doped compound semiconductor materials, and the lower mirror layer 2104 may be n-type doped compound semiconductor materials, and each layer within mirror layers 2104 and 2108 have a thickness of about 8/4, where 8 is the wavelength of light emitted from the laser source.

After the appropriate layers have been grown, laser 2102 can be formed by photolithographically patterning the layers and using a suitable etchant to remove a portion of the layers.

Wave guide 2116 may then be formed over VCSEL 2102 by depositing radiation transmissive material, patterning the material, and removing a portion of the material. In accordance with one aspect of this embodiment, the transmissive material may include any material discussed above in connection with guide 94, and the material is patterned such that a portion of the material is aligned or coupled to an output of VCSEL 2102. In accordance with a further aspect of this embodiment, wave guide 2112 is patterned such that an edge 2118 of the guide is beveled to facilitate transmission of light through core 2116, as illustrated by arrow 2120.

System 2100 may also include a detector 2126, coupled to or aligned with wave guide 2116. Detector 2126 may include any suitable radiation detector such as the photo detector described above in connection with FIG. 9. In addition or in the alternative, VCSEL 2102 may be directly coupled to a fiber optic cable or other device.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

We claim:

1. A monolithically integrated optical system comprising:

a monocrystalline semiconductor substrate;

an oxide layer formed overlying the substrate;

a monocrystalline compound semiconductor laser; and

an optical wave guide deposited in alignment with the compound semiconductor laser and configured to transmit emissions from the laser.

2. The monolithically integrated optical system of claim 1 further comprising a photo detector coupled monolithically to the wave guide and configured to receive the emissions from the laser.

3. The monolithically integrated optical system of claim 1 wherein the optical wave guide comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

4. The monolithically integrated optical system of claim 3 wherein the optical wave guide comprises a monocrystalline oxide.

5. A monolithically integrated system comprising:

a silicon substrate;

an alkali earth metal oxide layer formed overlying the substrate;

a radiation emitting device formed of compound semiconductor material epitaxially deposited overlying the oxide layer; and

a wave guide deposited overlying the oxide layer and configured to receive and transmit radiation emitted from the radiation emitting device.

6. The system of claim 5 further comprising a radiation detector monolithically formed overlying the oxide layer and coupled to receive radiation transmitted by the wave guide.

7. The system of claim 6 wherein the radiation detector is formed of material epitaxially grown overlying the oxide layer, the material selected from the group consisting of silicon, III-V compound semiconductor materials and II-VI compound semiconductor materials.

8. The system of claim 7 wherein the radiation detector comprises a material selected from silicon, gallium arsenide, and indium gallium arsenide.

9. The system of claim 5 further comprising a V-shaped groove formed in the silicon substrate in alignment with the wave guide.

10. The system of claim 9 further comprising an optical fiber positioned in the V-shaped groove and configured to receive radiation transmitted by the wave guide.

11. The system of claim 10 wherein the optical fiber has a substantially circular cross section having a diameter and the V-shaped groove has a depth predetermined in response to the diameter of the optical fiber.

12. The system of claim 5 wherein the wave guide comprises a first branch coupled to an optical device and a second branch coupled to a radiation detector.

13. The system of claim 12 wherein the radiation detector is coupled to sample the radiation emitted from the radiation emitting device.

14. The system of claim 13 further comprising a control circuit coupled to the radiation detector.

15. The system of claim 14 wherein the control circuit comprises:

a radiation emitting device drive circuit operatively coupled to the radiation emitting device to control the output of the radiation emitting device; and a feedback path from the radiation detector to the radiation emitting device drive circuit.

16. The system of claim 15 wherein the radiation emitting device drive circuit is operated to maintain a substantially constant radiation emitting device output.

17. The system of claim 15 wherein the radiation emitting drive circuit is formed in the silicon substrate.

18. The system of claim 15 further comprising a radiation detector receiver circuit.

19. The system of claim 18 wherein the radiation detector receiver circuit is formed in the silicon substrate.

20. The system of claim 5 wherein the wave guide comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

21. The system of claim 5 wherein the wave guide comprises a monocrystalline alkali earth metal oxide.

22. The system of claim 5 wherein the wave guide comprises a monocrystalline material.

23. The system of claim 5 wherein the wave guide is photolithographically aligned to the radiation emitting device.

24. The system of claim 5 wherein the radiation emitting device comprises a device selected from the group consisting of lasers and light emitting diodes.

25. An optical multiplexer circuit comprising:

a monocrystalline Group IV substrate;

an oxide layer overlying the substrate;

a radiation emitting source epitaxially formed overlying the oxide layer and configured to emit radiation having a plurality of wavelengths;

a wave guide having a plurality of branches formed overlying the oxide and coupled to the radiation emitting source, each of the plurality of branches configured to carry one of the plurality of wavelengths; and

a multiplexed wave guide coupled to each of the plurality of branches, the multiplexed wave guide configured to carry all of the plurality of wavelengths.

26. The optical multiplexer circuit of claim 25 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

27. The optical multiplexer circuit of claim 26 wherein the oxide layer comprises a monocrystalline oxide.

28. The optical multiplexer circuit of claim 26 wherein the oxide layer comprises an amorphous oxide formed by annealing a monocrystalline oxide.

29. The optical multiplexer of claim 25 wherein the radiation emitting source comprises a plurality of radiation emitting sources epitaxially formed overlying the oxide layer.

30. The optical multiplexer of claim 29 wherein the plurality of radiation emitting sources comprise compound semiconductor lasers epitaxially grown overlying the oxide layer.

31. The optical multiplexer of claim 29 wherein the plurality of radiation emitting sources comprise compound semiconductor light emitting diodes epitaxially grown overlying the oxide layer.

32. The optical multiplexer of claim 25 wherein the radiation emitting source comprises:

a radiation emitting source capable of producing a spectrum of wavelengths; and

a grating coupled to the radiation emitting source for selecting a plurality of wavelengths from the spectrum of wavelengths.

33. The optical multiplexer of claim 32 wherein the radiation emitting source comprises an optical fiber carrying a plurality of wavelengths.

34. The optical multiplexer of claim 25 wherein the radiation emitting source comprises a compound semiconductor light emitting diode epitaxially grown overlying the oxide layer.

35. The optical multiplexer of claim 25 wherein the wave guide having a plurality of branches comprises an alkali earth metal titanate.

36. The optical multiplexer of claim 35 wherein the wave guide having a plurality of branches comprises impurity doped strontium titanate.

37. The optical multiplexer of claim 25 wherein the wave guide having a plurality of branches comprises a core layer of alkali earth metal oxide having a first index of refraction and a cladding layer of alkali earth metal oxide having a second index of refraction less than the first index of refraction.

38. The optical multiplexer of claim 37 wherein the alkali earth metal oxide comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

39. The optical multiplexer of claim 25 wherein the wave guide having a plurality of branches comprises a monocrystalline alkali earth metal oxide epitaxially grown overlying the oxide layer.

40. An optical integrated circuit comprising:

a monocrystalline silicon substrate having a surface with a 100 surface orientation;

a groove etched in the surface, the groove comprising a first portion having a substantially planar bottom parallel to the surface and sides parallel to crystalline planes in the monocrystalline silicon substrate;

an oxide layer overlying the substrate including the planar bottom of the groove; and

a compound semiconductor edge emitting laser epitaxially grown overlying the oxide layer, the laser positioned overlying the planar bottom of the groove.

41. The optical integrated circuit of claim 40 further comprising laser control circuitry formed in the substrate and coupled to the laser.

42. The optical integrated circuit of claim 40 wherein the edge emitting laser is configured to emit radiation in a direction to impinge upon one of the sides, the side reflecting the radiation away from the surface.

43. The optical integrated circuit of claim 42 further comprising an optical fiber coupled to the surface to collect the radiation reflected away from the surface.

44. The optical integrated circuit of claim 40 wherein the edge emitting laser is configured to emit radiation in a direction parallel to the groove.

45. The optical integrated circuit of claim 44 further comprising an optical fiber positioned in the groove to collect the radiation emitted parallel to the groove.

46. The optical integrated circuit of claim 44 further comprising:

a second portion of the groove, the second portion etched to a greater depth than the first portion; and

an optical fiber positioned in the second portion of the groove to collect the radiation emitted parallel to the groove.

47. The optical integrated circuit of claim 44 further comprising a wave guide formed in the groove overlying the amorphous oxide and in alignment with the laser to collect the radiation emitted parallel to the groove.

48. The optical integrated circuit of claim 47 wherein the wave guide comprises a monocrystalline oxide.

49. The optical integrated circuit of claim 47 wherein the wave guide comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

50. The optical integrated circuit of claim 49 wherein the wave guide comprises a monocrystalline oxide.

51. The optical integrated circuit of claim 44 wherein the wave guide comprises a core of alkali earth metal oxide doped to have a first refractive index and a cladding layer of alkali earth metal oxide doped to have a second refractive index less than the first refractive index.

52. The optical integrated circuit of claim 51 wherein the alkali earth metal oxide comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

53. The optical integrated circuit of claim 40 further comprising a filler material applied overlying the laser and forming a substantially planar upper surface.

54. The optical integrated circuit of claim 53 further comprising:

control circuitry formed in the substrate; and

interconnect metallization coupled between the laser source and the control circuitry, the interconnect metallization formed in part on the planar upper surface.

55. The optical integrated circuit of claim 40 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth

metal ruthenates, alkali earth metal niobates, and perovskite oxides.

56. An optical integrated circuit comprising:

a silicon substrate;

a layer of oxide overlying the substrate;

an optical radiation source, the source emitting radiation comprising a plurality of wavelengths;

a radiation transmission medium coupled to the source;

a demultiplexer formed on the layer of oxide and coupled to the radiation transmission medium to separate the radiation into a plurality of radiation streams each characterized by substantially a single wavelength; and

a plurality of wave guides each formed on the oxide layer and coupled to receive one of the plurality of radiation streams.

57. The optical integrated circuit of claim 56 wherein the demultiplexer comprises a plurality of directional couplers.

58. The optical integrated circuit of claim 57 further comprising control circuitry formed in the silicon substrate and configured to tune the plurality of directional couplers.

59. The optical integrated circuit of claim 56 wherein the plurality of wave guides each comprise an alkali earth metal oxide epitaxially grown overlying the layer of oxide.

60. The optical integrated circuit of claim 59 wherein the alkali earth metal oxide comprises a monocrystalline oxide.

61. The optical integrated circuit of claim 56 further comprising a plurality of photo detectors, each photolithographically aligned to one of the plurality of wave guides.

62. The optical integrated circuit of claim 61 wherein the plurality of photo detectors each comprise a monocrystalline semiconductor material epitaxially grown overlying the amorphous oxide.

63. The optical integrated circuit of claim 56 wherein the layer of oxide comprises an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

64. A process for fabricating an optical integrated circuit comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a monocrystalline oxide layer overlying the monocrystalline semiconductor substrate;

epitaxially growing a monocrystalline compound semiconductor layer overlying the monocrystalline oxide layer;

photolithographically patterning the monocrystalline compound semiconductor layer to form a radiation emitting device;

depositing a radiation transmissive material overlying the substrate and contacting the radiation emitting device; and

photolithographically patterning the radiation transmissive material to form a wave guide in alignment with and coupled to the radiation emitting device.

65. The process of claim 64 further comprising the step of thermally annealing the monocrystalline oxide layer to convert the monocrystalline oxide layer to an amorphous oxide layer.

66. The process of claim 65 wherein the step of thermally annealing comprises the step of rapid thermal annealing.

67. The process of claim 66 wherein the step of rapid thermal annealing comprises rapid thermal annealing at a temperature between about 700° C and about 1000° C.

68. The process of claim 64 wherein the step of epitaxially growing a monocrystalline oxide layer comprises the step of growing by a process selected from the group consisting of molecular beam epitaxy, chemical vapor deposition, physical vapor deposition, pulsed laser deposition and chemical solution depostion an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

69. The process of claim 68 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises the step of epitaxially growing a monocrystalline layer of compound semiconductor material selected from the group consisting of InP, InGaAs, GaAs, AlGaAs, ZnSe, and ZnSSe.

70. The process of claim 64 wherein the step of depositing a radiation transmissive material overlying the substrate comprises the step of depositing a second oxide layer overlying the monocrystalline oxide layer.

71. The process of claim 70 wherein the step of depositing a second oxide layer comprises the step of depositing a layer of alkali earth metal oxide.

72. The process of claim 71 wherein the step of epitaxially depositing comprises epitaxially depositing a layer of alkali earth metal titanate.

73. The process of claim 64 wherein the step of depositing radiation transmissive material overlying the substrate comprises the step of depositing an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

74. The process of claim 64 further comprising the step of photolithographically patterning the monocrystalline semiconductor layer to form a photo detector device.

75. The process of claim 74 further comprising the step of photolithographically patterning the optically transmissive material to form a wave guide in alignment with and optically coupling the photo detector device and the radiation emitting device.

76. The process of claim 64 wherein the step of photolithigraphically patterning the monocrystalline compound semiconductor layer comprises patterning to form a device selected from the group consisting of lasers and light emitting diodes.

77. A process for fabricating an optical integrated circuit comprising the steps of:

providing a monocrystalline silicon substrate having a surface;

forming a CMOS circuit at least partially within the substrate;

etching a groove extending into the substrate from the surface, at least a portion of the groove having a bottom substantially parallel to the surface;

epitaxially growing a monocrystalline alkali earth metal oxide overlying the surface and the bottom;

epitaxially growing a monocrystalline compound semiconductor layer overlying the monocrystalline alkali earth metal oxide;

forming a laser device and a photo detector device, at least the laser device formed overlying the bottom;

forming a wave guide optically connecting the laser device and the photo detector device;

depositing an insulating material to substantially fill the groove; and

forming an interconnect metallization overlying the insulating material to connect the CMOS circuit to the laser device and to the photo detector device.

78. The process of claim 77 further comprising the step of securing an optical fiber in the groove in alignment with the wave guide.

79. The process of claim 77 further comprising the step of securing an optical fiber in the groove in alignment with the laser device.

80. The process of claim 77 wherein the step of forming a laser device and a photo detector device comprise the step of patterning the monocrystalline compound semiconductor layer.

81. The process of claim 77 wherein the step of forming a wave guide comprises the steps of:

depositing a second layer of alkali earth metal oxide contacting the laser device and the photo detector device, the second layer having a first index of refraction;

patterning the second layer to form a wave guide core; and

depositing a third layer of alkali earth metal oxide overlying the second layer of alkali earth metal oxide, the third layer having a second index of refraction less than the first index of refraction.

82. The process of claim 81 wherein the step of forming a wave guide wherein the step of depositing a second layer comprises the step of depositing a layer comprising $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

83. The process of claim 82 further comprising the step of impurity doping the layer of $Sr_xBa_{1-x}TiO_3$ to control the first refractive index.

84. The process of claim 77 further comprising the step of annealing the alkali earth metal oxide to convert the alkali earth metal oxide to an amorphous structure.

85. A process for fabricating an optical integrated circuit comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a monocrystalline oxide layer overlying the substrate;

forming a first amorphous oxide layer underlying the monocrystalline oxide layer during the step of epitaxially growing a monocrystalline oxide;

epitaxially growing a first seed layer of monocrystalline semiconductor material overlying the layer of monocrystalline oxide layer;

epitaxially growing a monocrystalline compound semiconductor layer overlying the first seed layer;

thermally annealing the monocrystalline oxide layer to convert the monocrystalline oxide layer to an additional amorphous oxide layer;

forming a light emitting device at least partially within the compound semiconductor layer;

forming a photo detector device at least partially within the compound semiconductor layer;

depositing a radiation transmissive layer overlying the light emitting device;

patterning the radiation transmissive layer to form a wave guide in alignment with and coupled to the light emitting device and the photo detector device.

86. The process of claim 85 wherein the step of thermally annealing is carried out after the step of epitaxially growing a first seed layer.

87. The process of claim 85 wherein the step of thermally annealing is carried out after the step of epitaxially growing a monocrystalline compound semiconductor layer.

88. The process of claim 85 wherein the step of depositing a radiation transmissive layer comprises the step of depositing an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

89. The process of claim 85 wherein the step of depositing a radiation transmissive layer comprises the step of depositing $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

90. The process of claim 85 wherein the step of epitaxially growing a monocrystalline oxide layer comprises the step of epitaxially depositing an oxide selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth

metal hafniates, alkali earth metal tantalates, alkali earth metal ruthenates, alkali earth metal niobates, and perovskite oxides.

91. The process of claim 90 wherein the step of epitaxially growing a monocrystalline oxide layer comprises the step of depositing $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

92. The process of claim 85 further comprising the step of forming a template layer overlying the monocrystalline oxide layer.

93. A process for fabricating an optical integrated circuit comprising the steps of:

providing a monocrystalline silicon substrate having a surface;

forming a CMOS circuit at least partially within a first portion of the substrate;

etching a groove extending into the substrate from the surface, the groove having a first portion having a bottom substantially parallel to the surface;

epitaxially growing a monocrystalline alkali earth metal oxide layer overlying the bottom and a second portion of the surface;

forming a first amorphous oxide layer underlying the monocrystalline alkali earth metal oxide layer;

epitaxially growing a monocrystalline compound semiconductor layer overlying the bottom and a second portion of the surface;

thermally annealing the monocrystalline alkali earth metal oxide layer to convert the monocrystalline alkali earth metal oxide to an additional amorphous oxide layer;

forming a laser device and a photo detector device at least partially within the monocrystalline compound semiconductor layer, at least the laser device formed overlying the bottom;

depositing a first layer of alkali earth metal titanate contacting the laser device and the photo detector device, the first layer having a first index of refraction;

photolithographically patterning the first layer to form a wave guide core aligned with and optically coupling the laser device and the photo detector device, at least a portion of the wave guide core positioned in the groove;

depositing a second layer of alkali earth metal titanate overlying the first layer, the second layer having a second index of refraction less than the first index of refraction;

depositing a planarizing insulative material to substantially fill the groove; and

forming an interconnect metallization overlying the planarizing insulative material to connect the CMOS circuit to the laser device and to the photo detector device.

94. The process of claim 93 further comprising the step of securing an optical fiber in a second portion of the groove in alignment with the laser device, the second portion configured to have a V-shape.

95. The process of claim 93 further comprising the step of securing an optical fiber in a second portion of the groove in alignment with the wave guide, the second portion configured to have a V-shape.

96. The process of claim 93 wherein the step of epitaxially growing a monocrystalline earth metal oxide comprises the step of epitaxially growing monocrystalline $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

97. The process of claim 93 wherein the step of depositing a first layer of alkali earth metal titanate comprises the step of depositing $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

98. The process of claim 97 wherein the step of depositing $Sr_xBa_{1-x}TiO_3$ comprises depositing impurity doped $Sr_xBa_{1-x}TiO_3$ to determine the first index of refraction.

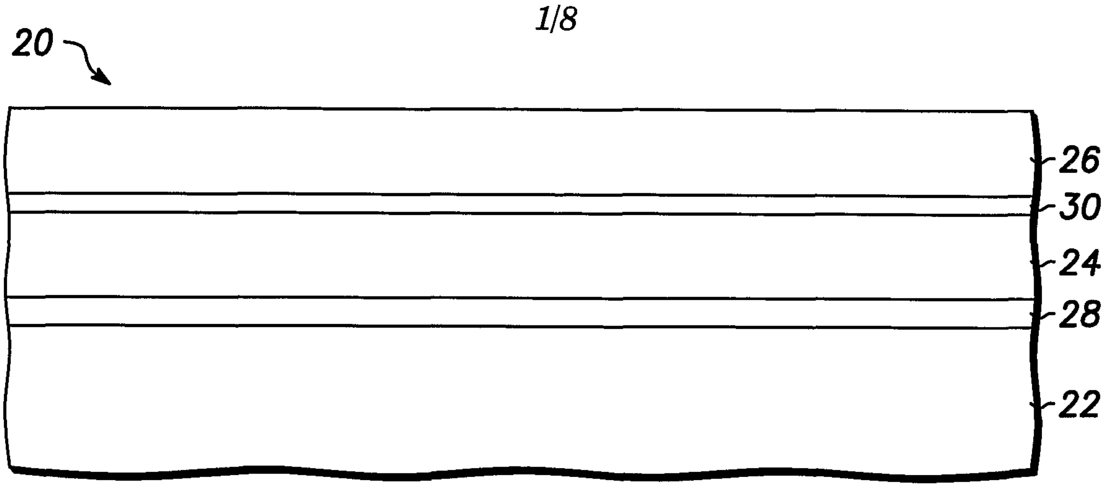


FIG. 1

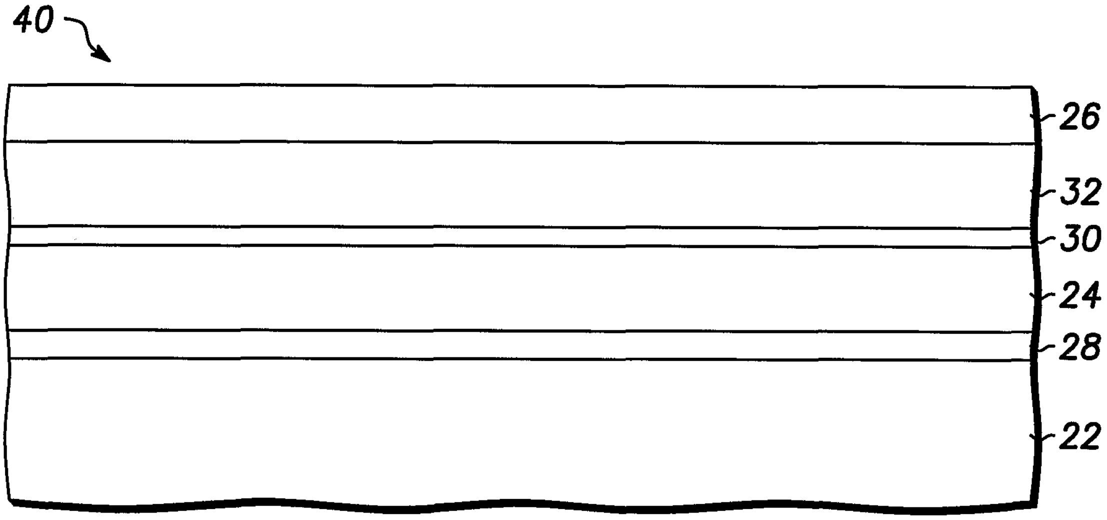


FIG. 2

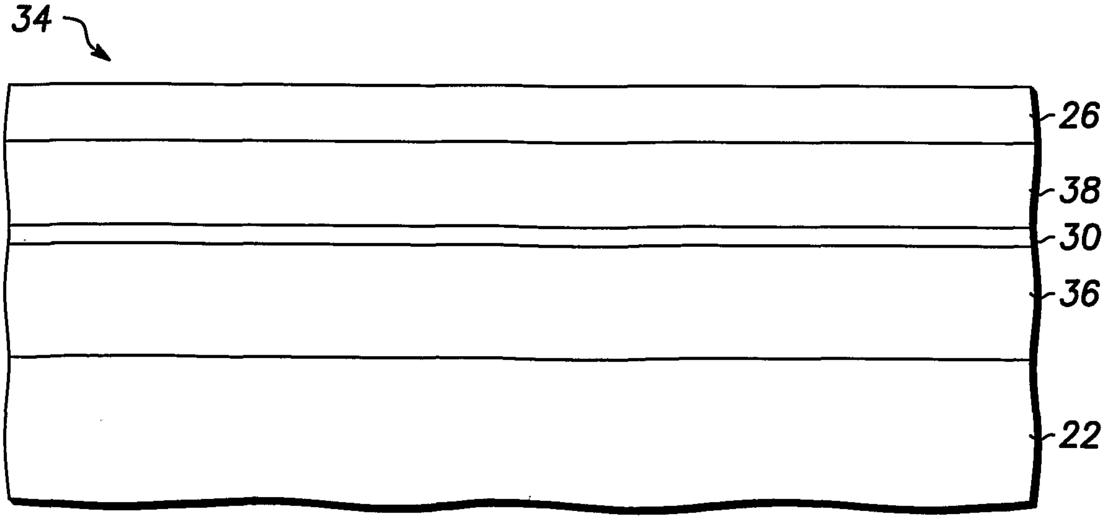


FIG. 3

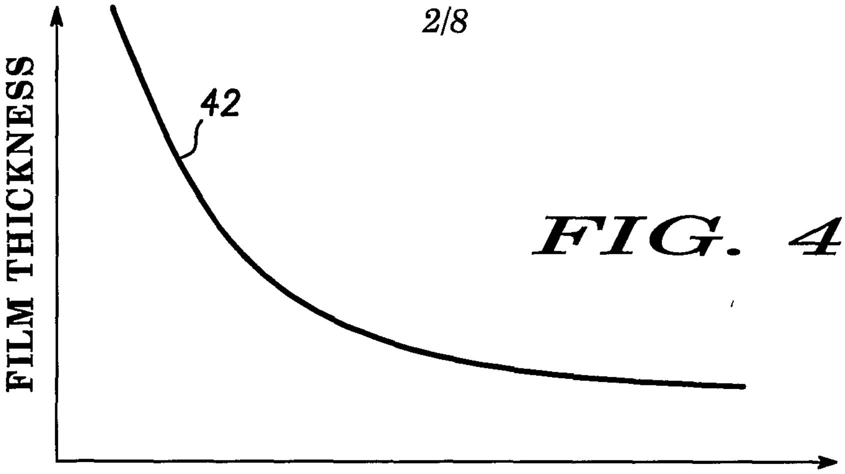


FIG. 4

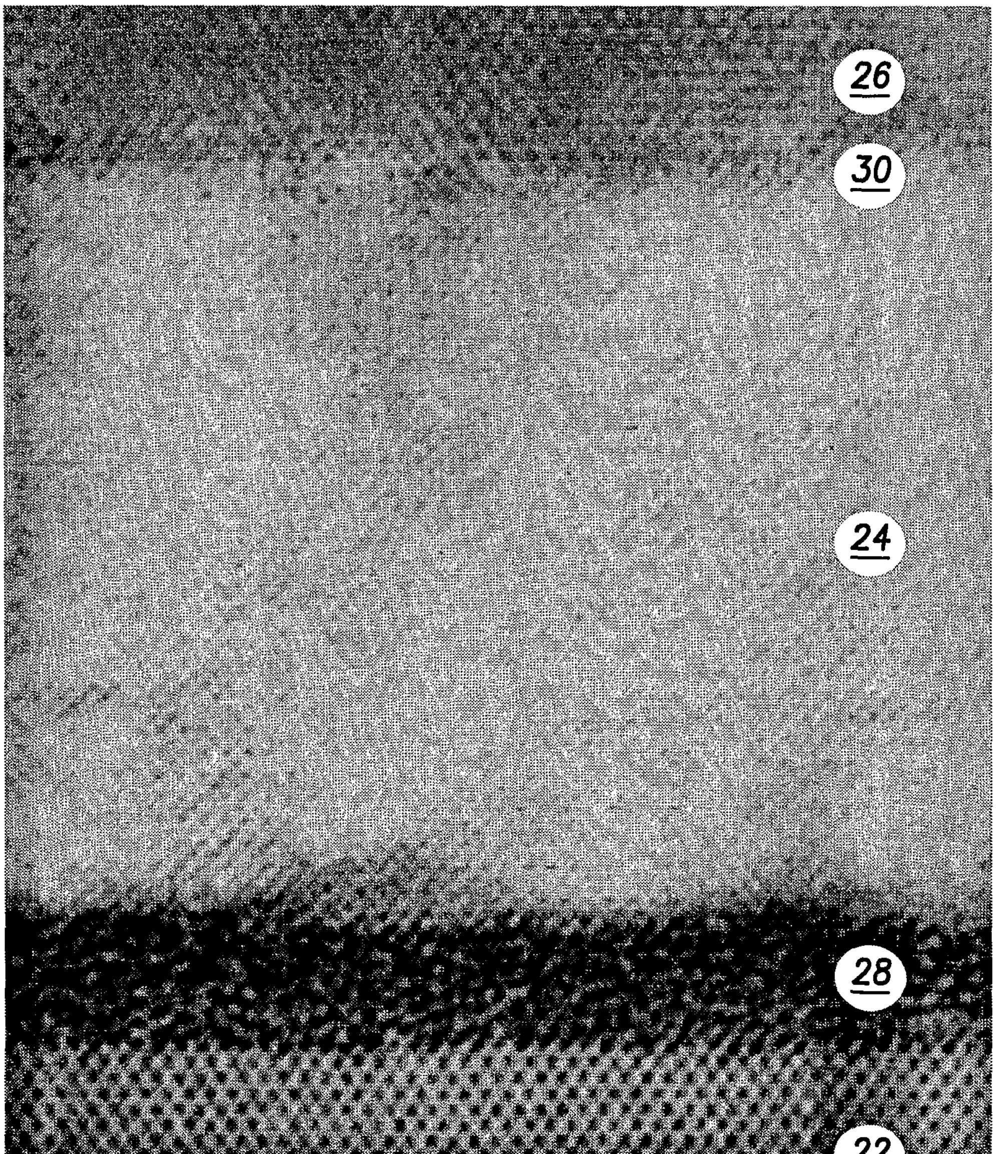
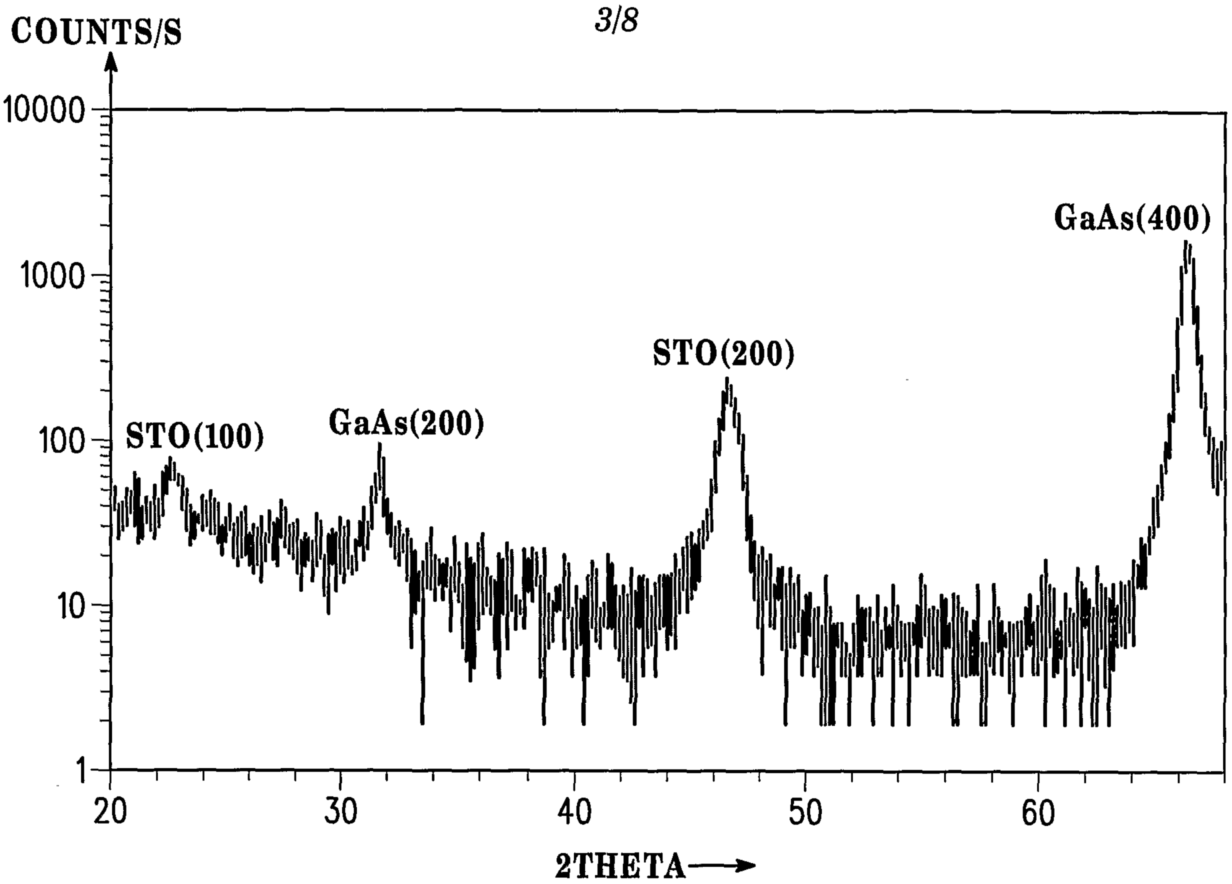


FIG. 5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1000
100
10
1
STO(100)
GaAs(200)
STO(200)
GaAs(400)
20
30
40
50
60
2THETA⟶

FIG. 6

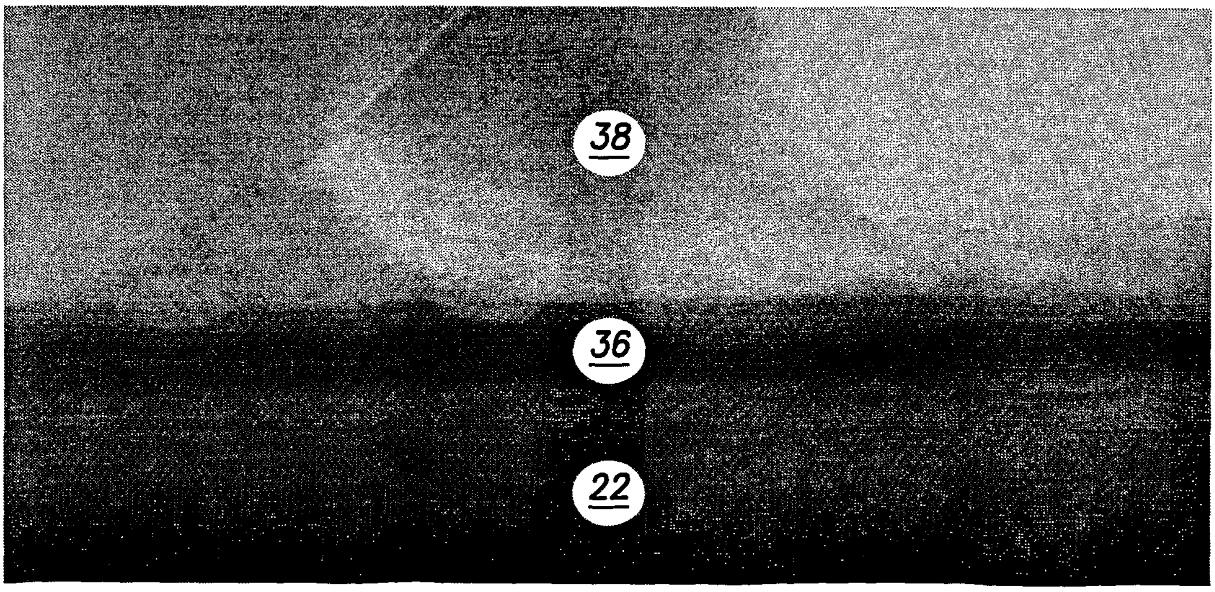

38
36
22

FIG. 7

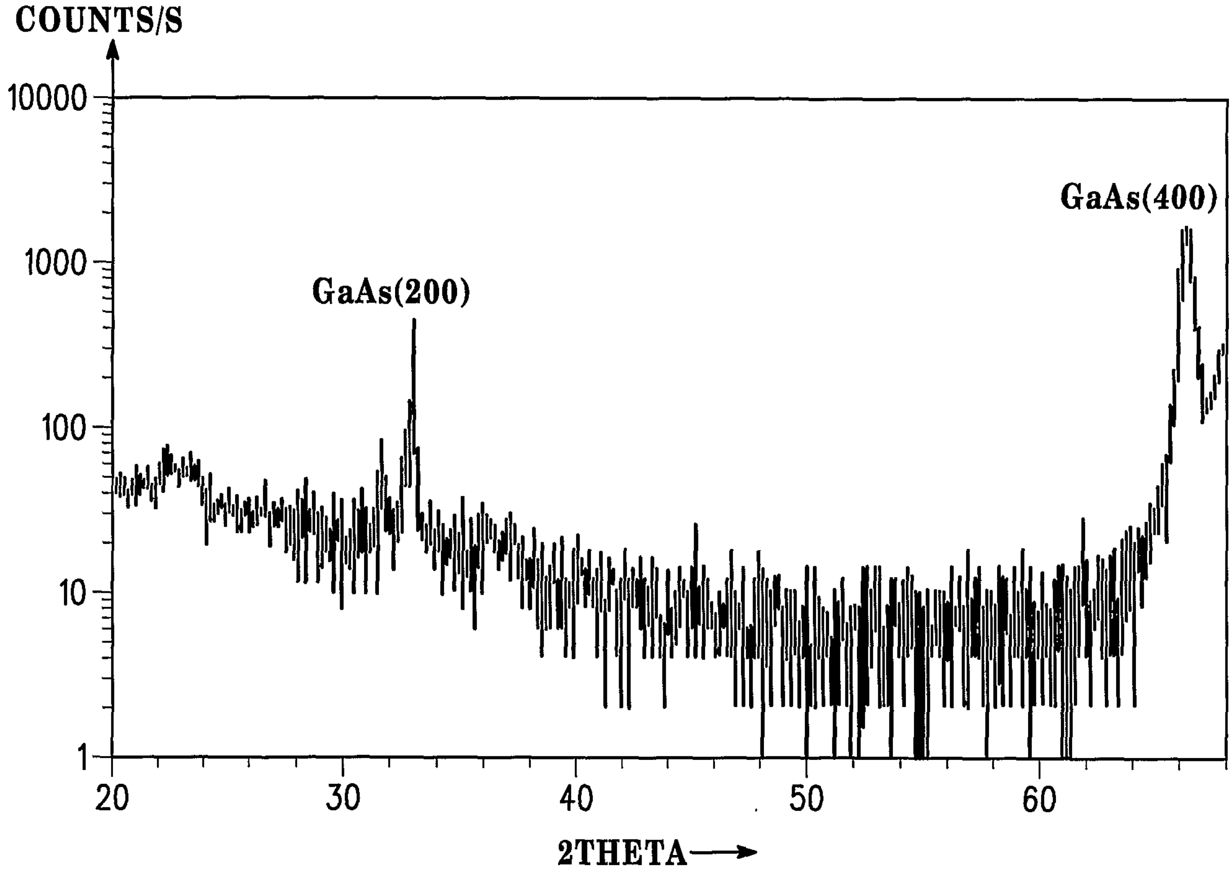

COUNTS/S
10000
1000
100
10
1
GaAs(200)
GaAs(400)
20
30
40
50
60
2THETA⟶

FIG. 8

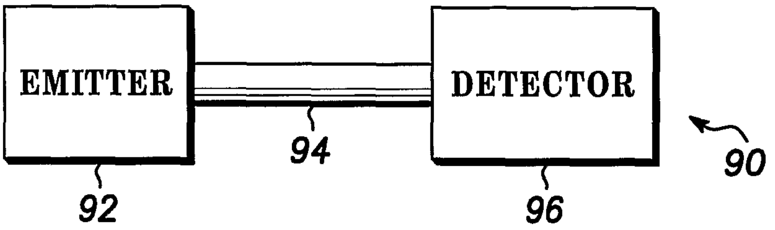


FIG. 9

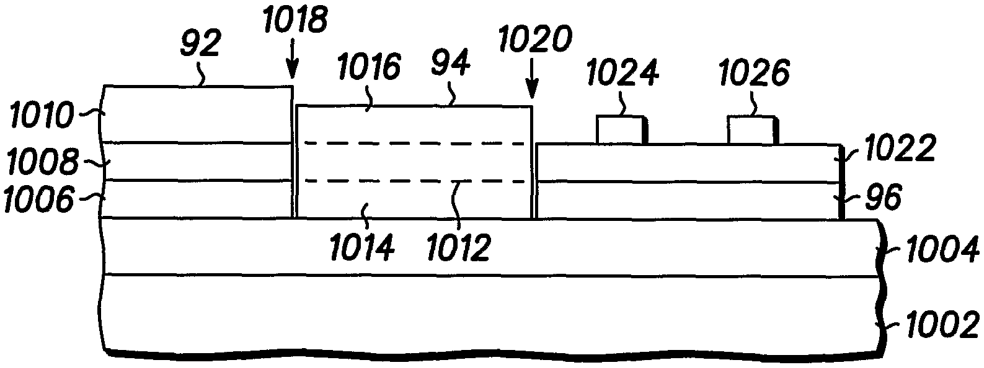


FIG. 10

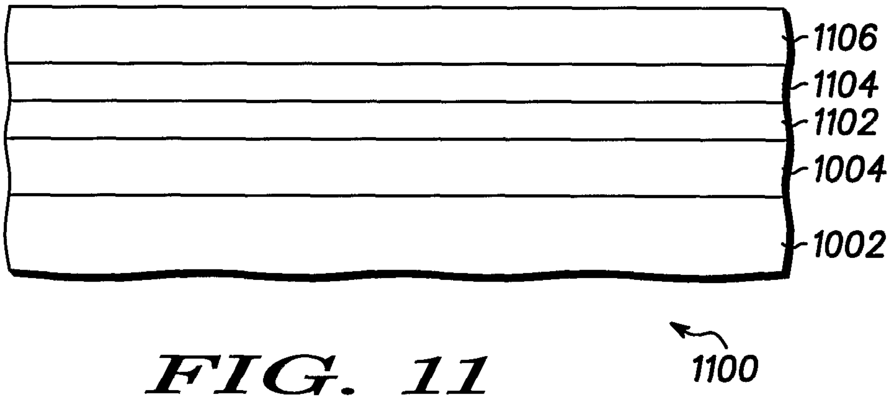


FIG. 11

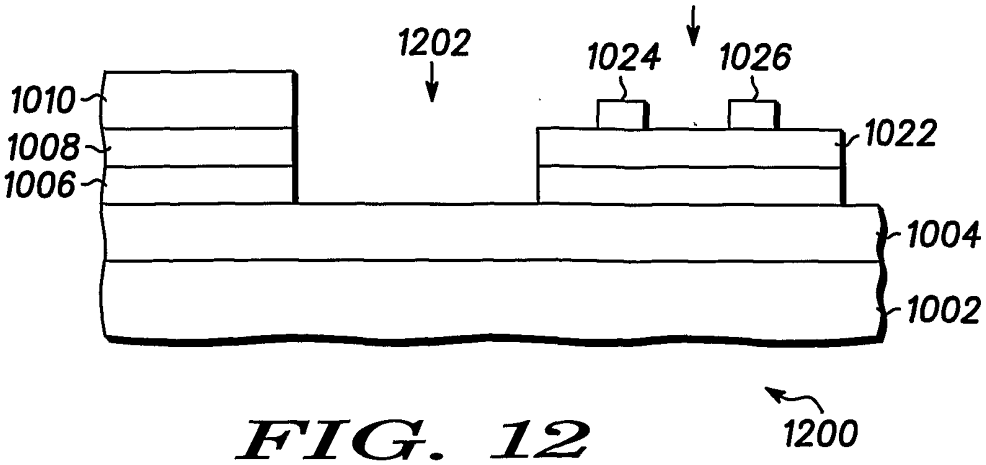


FIG. 12

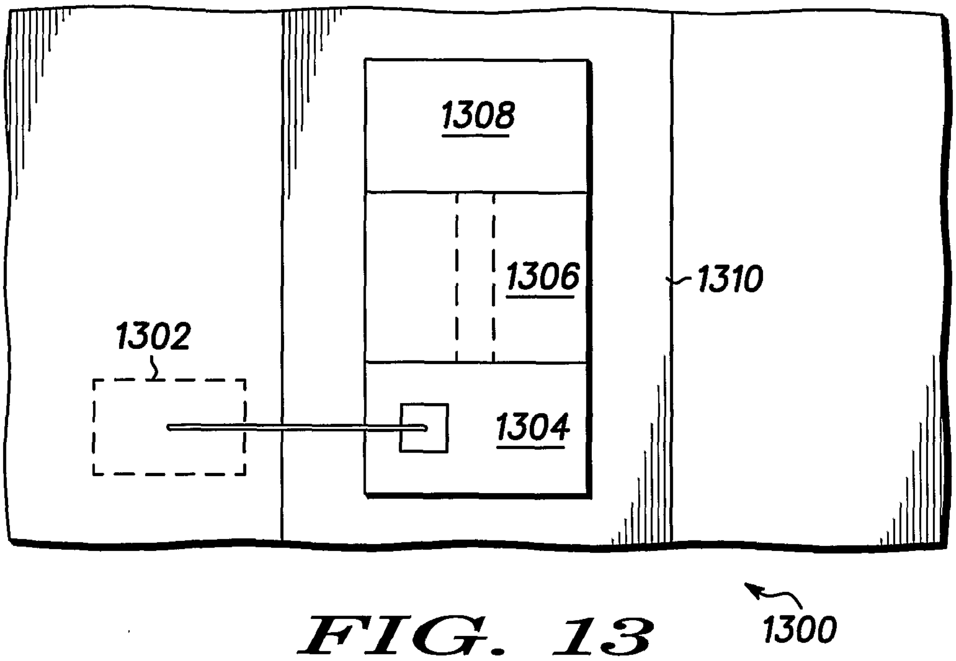


FIG. 13

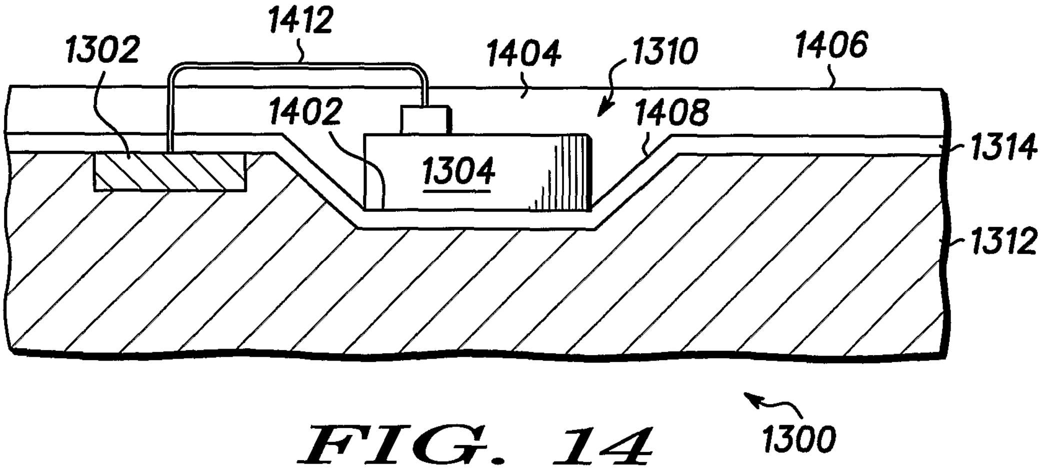


FIG. 14

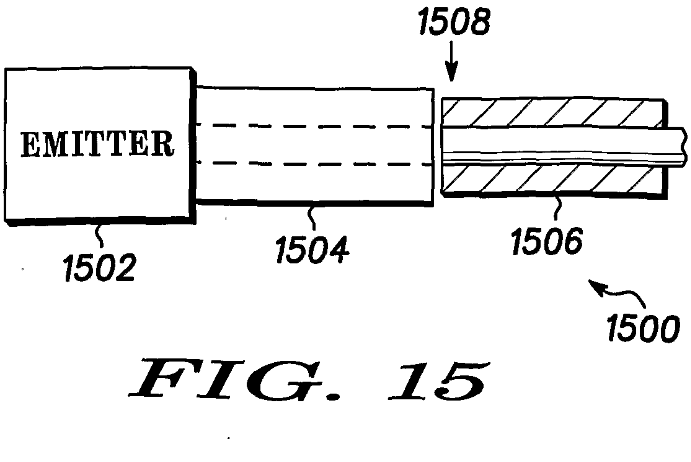


FIG. 15

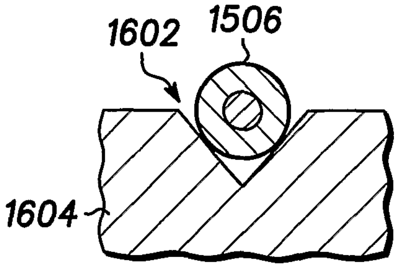


FIG. 16

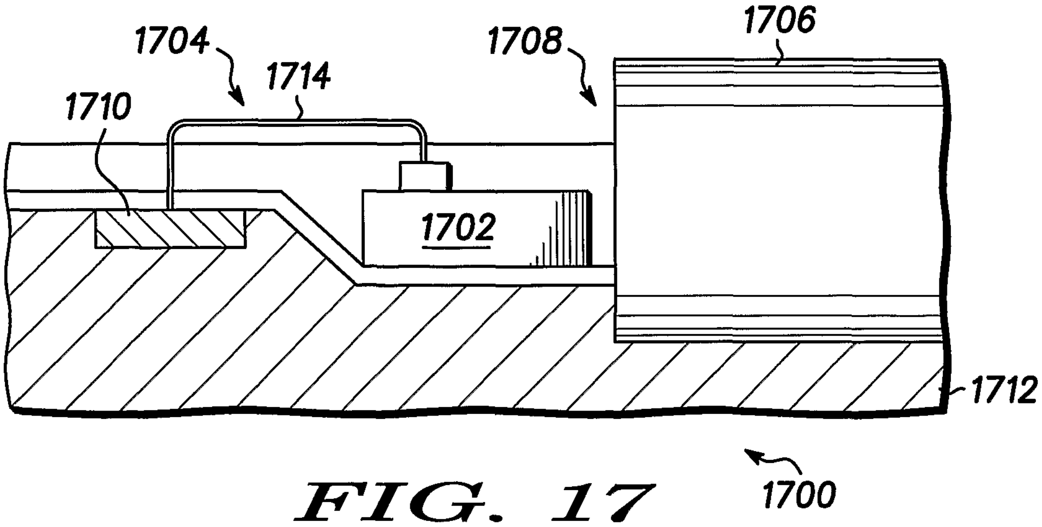
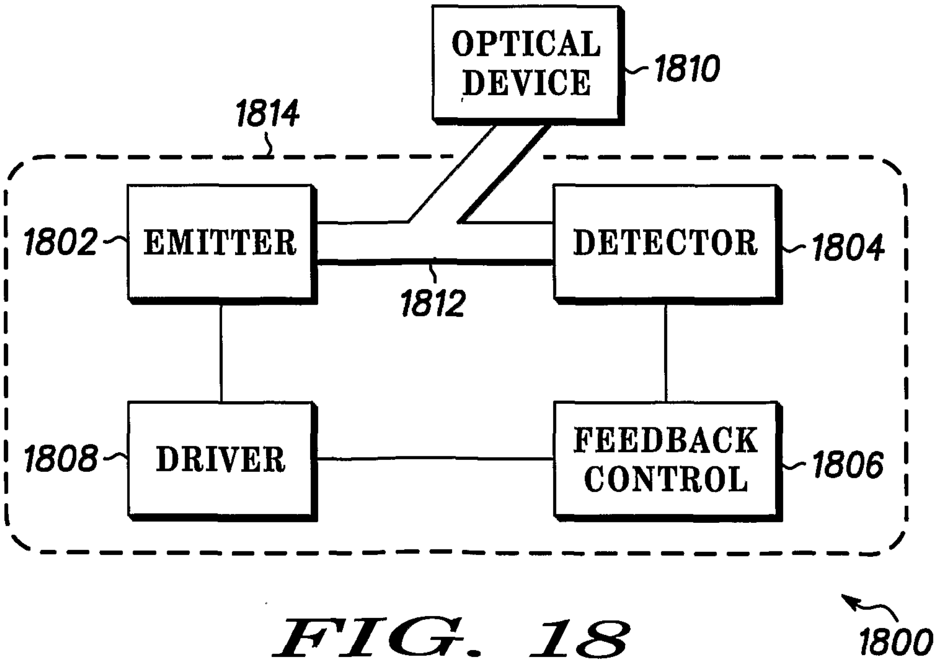

1704
1714
1710
1708
1706
1702
1712
1700

FIG. 17


OPTICAL DEVICE
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1814
1802
EMITTER
DETECTOR
1804
1812
1808
DRIVER
FEEDBACK CONTROL
1806
1800

FIG. 18

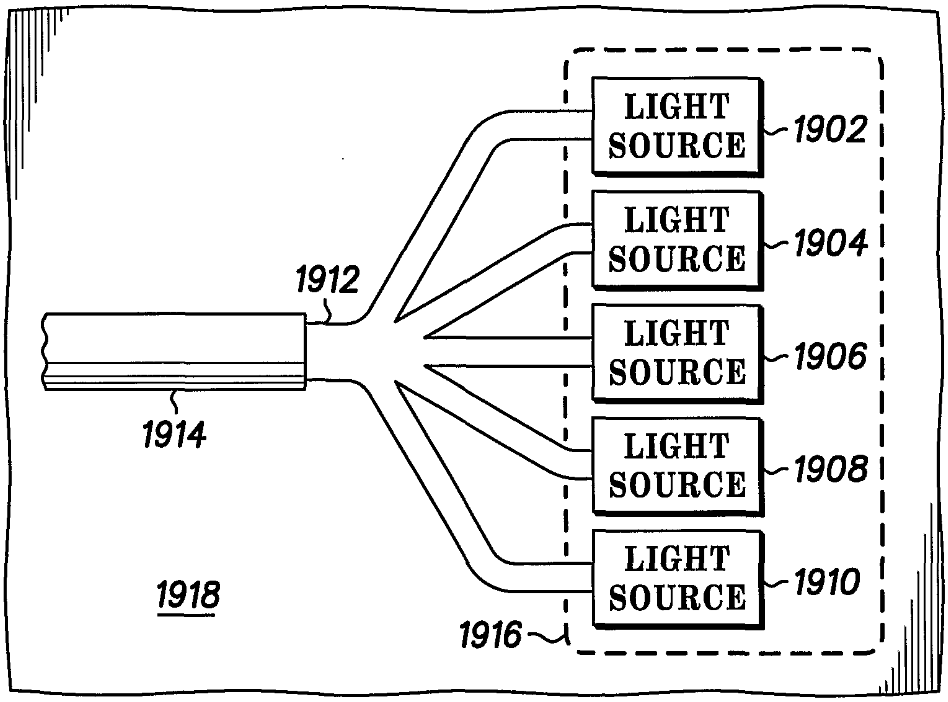
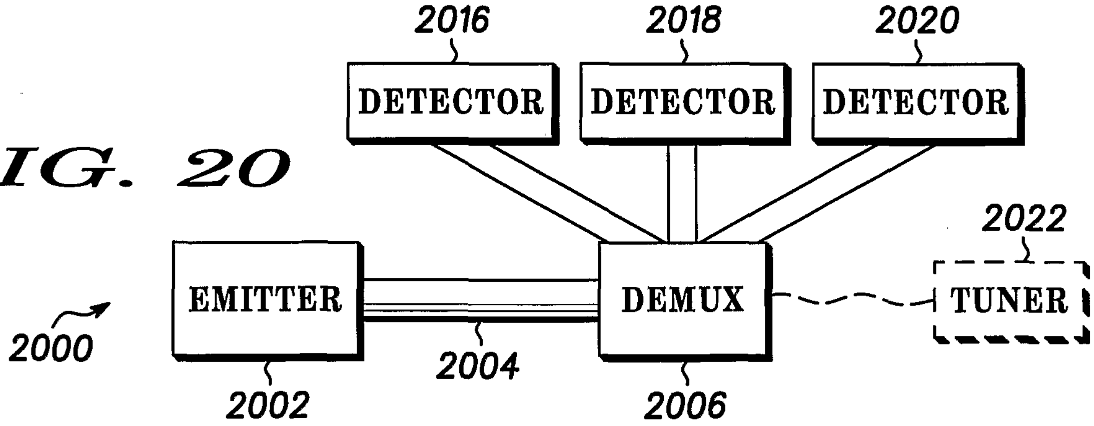


FIG. 19

FIG. 20



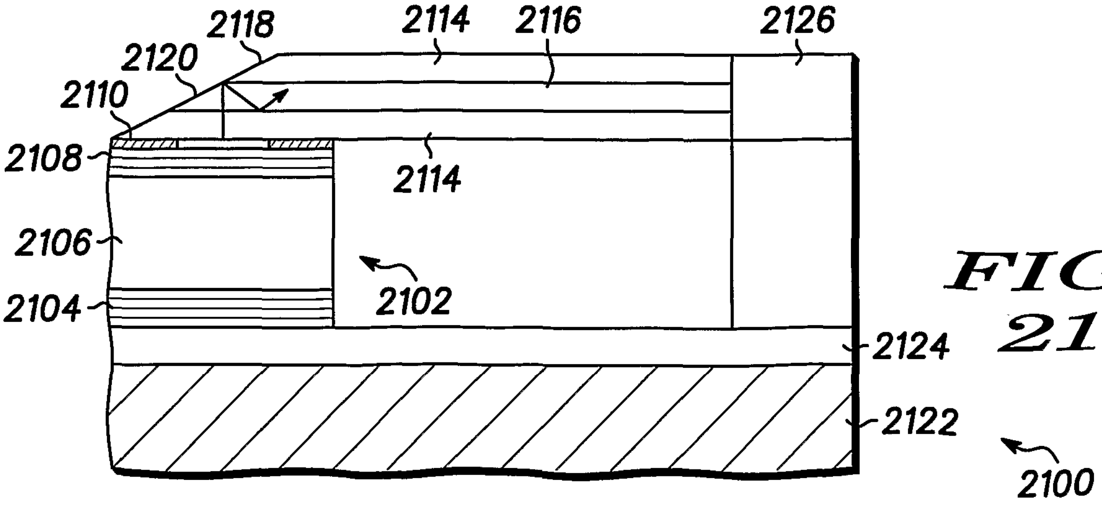


FIG. 21