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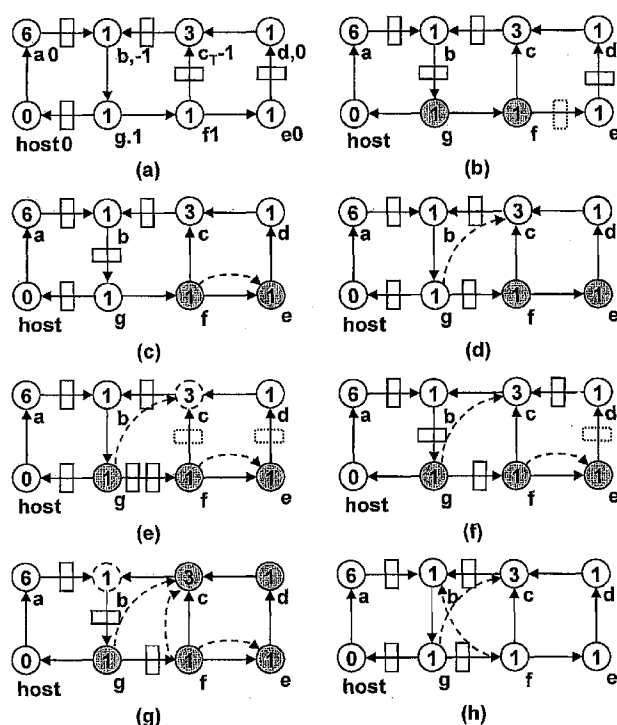
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(54) Title: SYSTEM AND METHOD FOR EFFICIENT AND OPTIMAL MINIMUM AREA RETIMING



(57) Abstract: A method for use in electronic design software efficiently and optimally produces minimized or reduced register flip flop area or number of registers/flip flops in a VLSI circuit design without changing circuit timing or functionality. The method dynamically generates constraints; maintains the generated constraints as a regular tree; and incrementally relocates registers/flip flops and/or the number of registers/flip flops in the circuit design.

FIG. 2



CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN,  
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## SYSTEM AND METHOD FOR EFFICIENT AND OPTIMAL MINIMUM AREA RETIMING

CROSS-REFERENCE TO RELATED APPLICATIONS/INCORPORATION BY  
REFERENCE

**[0001]** This patent application makes reference to, claims priority to and claims benefit from United States Provisional Patent Application Serial No. 61/025,548 filed on February 1, 2008, and United States Patent Application Serial No. 12/361,845, filed January 29, 2009. The above stated provisional application is hereby incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED  
RESEARCH OR DEVELOPMENT

**[0002]** This work was supported by the National Science Foundation (NSF) Grant No. CCR-0238484.

## FIELD OF THE INVENTION

**[0003]** The present invention relates to a system and method for use in electronic design software to perform minimum area retiming to relocate registers or flip-flops in a circuit design through sequential transformation wherein circuit functionality is preserved and more particularly to such a retiming system and method that is optimal, efficient and minimizes memory usage.

## BACKGROUND OF THE INVENTION

**[0004]** Retiming is one of the most powerful sequential transformations that relocates the registers or flip-flops (FFs) in a circuit while preserving its functionality. Since relocating the FFs could balance the longest combinational paths and reduce the circuit states, the clock period and the FF area or number of FFs in a circuit can be reduced through retiming optimizations. As the minimum clock period retiming minimizes the clock period, and thus might significantly increase the FF area, the minimum area retiming minimizes the FF area under a given clock period, and thus could be used to minimize the FF area even under the minimum clock period. Therefore, the min-area retiming problem is more important for sequential circuit design, but of higher complexity. See, e.g. N. Shenoy and R. Rudell, "Efficient implementation of retiming" ICCAD, pages 226-233 (1994).

**[0005]** All known and provable approaches to min-area retiming follow the basic ideas of C. E. Leiserson and I. B. Saxe "Retiming synchronous circuitry," Algorithmica 6(1):5-35 (1991). Given a circuit represented as a graph of  $n$  vertices and  $m$  edges, the minimum number of FFs between any two vertices and the maximum delay over the paths of the minimum number of FFs are first computed. Then, besides one constraint for each edge requiring that the FF number to be nonnegative, for each pair of the vertices whose computed path delay is larger than the given clock period, i.e. the timing critical path, a constraint is generated requiring that there be at least one FF between

them. Minimizing the FF area under those constraints formulates a dual of the min-cost network flow problem. Since each constraint forms an arc in the flow network, the number of arcs in the network is usually  $\theta(n^2)$ . Even though polynomially solvable, min-cost network flow computation, such as described in R. K. Ahuja, T. L. Magnanti, and J. B. Orlin "Network Flows: Theory, Algorithms, and Application," Prentice Hall (1993), over a dense circuit graph is usually expensive on large problems.

**[0006]** N. Shenoy and R. Rudell, in "Efficient implementation of retiming," ICCAD, pages 226-233 (1994), were among the first to consider a practical implementation of the min-area retiming algorithm. They found that the storage requirement to compute the timing critical paths and the number of constraints are the bottleneck and proposed techniques to reduce memory usage and to prune some redundant constraints. Minaret, proposed by N. Maheshwari and S S. Sapatnekar in "Efficient retiming of large circuits," IEEE TVLSI, 6(1):74-83, (March 1998), further pruned redundant constraints to reduce the size of the flow network by exploring the equivalence of retiming and clock skew optimization as proposed in ASTRA. See S. S. Sapatnekar and R. B Deokar "Utilizing the retiming-skew equivalence in a practical algorithm for retiming large circuits," IEEE TCAD, 15(10):1237-1248 (October 1996). However, even with these pruning techniques, as experimental results indicate, the flow networks could still be very dense compared to the original circuit graphs. Experiments have shown that for a circuit with more than 180K gates Minaret had to formulate and

solve a minimum cost network flow problem with more than 122M arcs, which used up more than 2GB of virtual memory.

**[0007]** H. Zhou, in "Deriving a new efficient algorithm for min-period retiming," Asia and South Pacific Design Automation Conference, Shanghai, China (January 2005) proposed an efficient incremental algorithm for minimum period retiming that iteratively moves FFs to decrease the clock period while the optimal solution is found in a short time. To overcome the expenses of existing approaches to minimum area retiming, D. P. Singh, V. Manohararajah, and S D Brown, in "Incremental retiming for FPGA physical synthesis," DAC, pages 433-438, Anaheim, CA (June 2005) also proposed that FFs be incrementally moved in the circuit. However, since only those moves that are better in cost and feasible in timing are allowed, these approaches are heuristic and may end up with a suboptimal solution. An efficient incremental algorithm for minimum area retiming with provably optimal solution has been evasive.

#### BRIEF SUMMARY OF THE INVENTION

**[0008]** In accordance with the present invention the disadvantages of prior retiming methods has been overcome. The method of retiming registers or flip flops in a circuit design in accordance with the present invention performs minimum area retiming to relocate the registers/flip flops in a circuit design in an efficient and optimal manner.

**[0009]** More particularly, the method of the present invention dynamically generates constraints; maintains the constraints as a regular forest; and incrementally relocates registers in the circuit to reduce the register area in the circuit and/or the number of registers in the circuit.

**[0010]** In accordance with one embodiment of the present invention the method includes determining whether there is a cluster of gates in the circuit wherein each gate of the cluster has a number of fanouts that is greater than the number of fanins of the gate and relocating the flip flops by iteratively moving a flip flop over the cluster.

**[0011]** In accordance with another embodiment of the present invention a constraint is generated only if it is directed to a path in the circuit that can lead to a reduction in the register area and/or number of registers in the circuit.

**[0012]** These and other advantages and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and the drawings.

#### BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

**[0013]** FIG. 1 is an illustration of a software routine for incremental minimum area retiming in accordance with one embodiment of the present invention;

**[0014]** FIGS. 2a-2h are illustrations of the iterative retiming of a circuit represented as a graph of vertices and edges in accordance with the routine of FIG. 1;

**[0015]** FIG. 3 is a diagram illustrating regular trees utilized in accordance with the present invention;

- [0016] FIG. 4 is an illustration of a subroutine ChangeRoot;
- [0017] FIG. 5 is an illustration of a subroutine UpdateForest;
- [0018] FIG. 6 is an illustration of a subroutine ZeroCut; and
- [0019] FIG. 7 is an illustration of a software routine for optimal, incremental minimum area retiming in accordance with another embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

[0020] A synchronous sequential circuit is modeled by a directed graph  $\mathcal{G} = (\mathcal{V}, \mathcal{E})$  whose vertices  $\mathcal{V}$  represent combinational gates and whose edges  $\mathcal{E}$  represent signals between vertices. Nonnegative gate delays are given as vertex weights  $d : \mathcal{V} \rightarrow \mathcal{R}^*$  and the nonnegative numbers of FFs on the signals are given as edge weights  $w' : \mathcal{E} \rightarrow \mathcal{N}$ . Given such a graph, the min-area retiming problem asks for an FF relocation  $w' : \mathcal{E} \rightarrow \mathcal{N}$  such that the total FF area in the circuit is minimized while it works under a given clock period  $\phi$ .

[0021] Conventionally, to guarantee that  $w'$  is a relocation of  $w$ , a retiming is given by a vertex labeling  $r : \mathcal{V} \rightarrow \mathcal{Z}$  representing the number of FFs moved backward over each gate from fanouts to fanins. Given  $r$ , the FF number on the edge  $(u, v)$  after retiming is  $w_r(u, v) = w(u, v) + r(v) - r(u)$ . A retiming  $r$  is valid if the FF number of every edge is nonnegative,

$$\mathcal{P}0(r): (\forall (u, v) \in \mathcal{E} : w_r(u, v) \geq 0).$$

**[0022]** For a circuit to work under a given clock period  $\phi$ , the maximum combinational path delay in the circuit can be at most  $\phi$ . To compute the maximum path delay, a vertex labeling of  $t : \mathcal{V} \rightarrow \mathcal{R}$  is used to represent the arrival time at the output of each gate. A valid  $r$  retiming  $r$  is feasible for  $\phi$  if the following condition holds for some arrival times  $t$ ,

$$\begin{aligned} \mathcal{P}1(r, \phi) : (\forall (u, v) \in \mathcal{E} : (w_r(u, v) > 0) \vee (t(v) \geq d(v) + t(u))) \\ \wedge (\forall v \in \mathcal{V} : d(v) \leq t(v) \leq \phi). \end{aligned}$$

**[0023]** The total FF number is  $\sum_{e \in \mathcal{E}(\mathcal{G})} w_r(e)$ . For any vertex  $v \in \mathcal{V}$ , let  $\mathcal{FI}(v)$  and  $\mathcal{FO}(v)$  be the sets of the fanins and the fanouts of  $v$  respectively. To minimize, the total FF number is equivalent to maximizing the quantity  $\sum_{v \in \mathcal{V}} (|\mathcal{FO}(v)| - |\mathcal{FI}(v)|) r(v)$ . More generally,  $b : \mathcal{V} \rightarrow \mathcal{R}$  is defined to be the labeling that represents the reduction in FF area if one FF is moved from the fanouts of the given vertex to its fanins. Then the FF area reduction for the retiming  $r$  is  $\sum_{v \in \mathcal{V}(\mathcal{G})} b(v) r(v)$ . With these notations, the min-area retiming problem can be formally stated as follows.

$$\text{Maximize} \quad \sum b(v) r(v),$$

$$\sum b(v) r(v),$$

$$v \in \mathcal{V}(\mathcal{G})$$

$$\text{st} \quad \mathcal{P}0(r) \wedge \mathcal{P}1(r, \phi)$$

For ease of presentation,  $b$  is extended to any graph  $X = (\mathcal{V}_X, E_X)$  with  $\mathcal{V}_X \subseteq \mathcal{V}$  and any  $I \subseteq \mathcal{V}$  by defining  $b(X)$  that  $b(X) = \sum_{v \in \mathcal{V}_X} b(v)$ ,  $b(I) = \sum_{v \in I} b(v)$ , and  $b(\emptyset) = 0$ . It is assumed that  $b(G) = 0$  without loss of generality and that the min-area retiming problem is bounded.

**[0024]** More complicated retiming problems can be solved in the same formulation of the problem stated above. One example is to consider the sharing of the FFs at the fanouts of a gate. As proposed by C. E. Leiserson and I. B Saxe in "Retiming synchronous circuitry," Algorithmica, 6(1):5-35 (1991), this scenario is handled by including additional constraints in  $\mathcal{P}0(r)$  and setting the labeling  $b$  accordingly. Let

$wmax(u) = \max_{(u,v) \in E} w(u, v)$  and assume that all the fanout edges of  $u$  have the same breadth  $\beta(u)$ , which is the costs of adding a FF along each edge. For each vertex  $u$

where the FFs at the fanouts of  $u$  should be shared, a dummy vertex  $u_m$  is introduced

For each fanout  $v$  of  $u$ , the breadth of the edge  $(u, v)$  is changed to  $\frac{\beta(u)}{|FO(u)|}$  and one

constraint is added to  $\mathcal{P}0(r)$  by introducing the edge  $(v, u_m)$  to  $G$  with  $w(v, u_m) = wmax(u) -$

$w(u, v)$  and the breadth  $\frac{\beta(u)}{|FO(u)|}$

**[0025]** In Leiserson and Saxe's approach to the minimum-area retiming, two  $n \times n$  matrices  $\mathcal{W}$  and  $\mathcal{D}$  are first computed to capture the critical timing constraints, and

based on them, a dual of the min-cost network flow problem is formulated and solved. For any vertex pair  $(u, v)$ ,  $\mathcal{W}(u, v)$  is the minimum number of FFs along any path from  $u$  to  $v$ , and  $\mathcal{D}(u, v)$  is the maximum delay of the paths from  $u$  to  $v$  with  $\mathcal{W}(u, v)$  FFs. If  $\mathcal{D}(u, v) > \phi$ , then there is a timing critical path from  $u$  and  $v$  and a critical timing constraint requiring at least one FF on the path should be generated. The dual of the minimum cost network flow problem is formulated to maximize the FF area reduction subject to the nonnegative FF number requirement and all the critical timing constraints. As  $\mathcal{W}$  and  $\mathcal{D}$  would usually be much denser than the circuit graph, the flow network would be dense when the given clock period is tight. Despite the many efforts as described in N. Shenoy and R. Rudell, "Efficient implementation of retiming," ICCAD, pages 226-233 (1994) and N. Maheshwari and S S. Sapatnekar, "Efficient retiming of large circuits," IEEE TVLSI, 6(1):74-83 (March 1998) to reduce the storage requirement for computing the critical timing constraints and to prune the redundant constraints, the large number of constraints is still the bottleneck for solving the min-area retiming problems.

**[0026]** To totally avoid the bottleneck, the method of the present invention does not compute the matrices  $\mathcal{W}$  or  $\mathcal{D}$  at all. The feasibility of clock period  $\phi$  is checked by dynamically updating the gate arrival times and comparing them with  $\phi$ , as in C. E. Leiserson and I. B Saxe "Retiming synchronous circuitry" Algorithmica, 6(1):5-35 (1991) and H. Zhou "Deriving a new efficient algorithm for min-period retiming," Asia and South

Pacific Design Automation Conference, Shanghai, China (January 2005). The objective in the retiming problem stated above indicates that, in order to improve a given solution, some vertices with  $b > 0$  must have their  $r$  increased. However, a vertex may not be independent if  $w_r(u, v) = 0$  and increasing  $r(u)$  requires that  $r(v)$  be increased at the same time. It is not hard to maintain such a relation. However, a more involved case happens when the increase of  $r$  over a path extends it to be longer than  $\phi$ . Incremental arrival time updating is used to identify such a situation, and the relation between the source  $u$  and sink  $v$  of the violating path is maintained as a constraint. It is revealing to note that  $\mathcal{D}(u, v) > \phi$  and  $r(v) + \mathcal{W}(u, v) - r(u) = 1$  for such  $u$  and  $v$ . In other words, the method of the present invention dynamically identifies timing arcs in Leiserson and Saxe's flow network but only identifies the currently tight ones that "lie on the road to improvement." The relations thus identified on normal circuit edges and on tight timing arcs are called active constraints. They force vertices with  $b(I) > 0$  to be bundled with vertices with  $b < 0$ . When there is still a bundle  $I$  with  $b(I) > 0$ , the objective can be improved by increasing  $r$  on  $I$ ; otherwise, the current retiming is already optimal.

**[0027]** Figure 1 depicts the incremental minimum area retiming method of the present invention that is implemented as a software routine by at least one processor of a computer system having preferably 65 MB of memory. The method is used for

sequential circuit design to relocate the registers or FFs in a circuit to reduce the register or FF area and/or number of registers or FFs in the circuit. The method of the present invention directly addresses the register or FF area minimization problem instead of its dual network flow problem. The method starts by finding a feasible retiming  $r$  for the clock period  $\phi$  wherein a set of active constraints  $\mathcal{A}$  are maintained throughout the algorithm. An initial feasible retiming  $r$  to obtain a minimum clock period  $\phi$  on line 1 of the method can be obtained by any efficient fixed period retiming algorithm such as described in C. E. Leiserson and I. B. Saxe "Retiming Synchronous Circuitry," Algorithmica, 6(1):5-35 (1991) or H. Zhou "Deriving A New Efficient Algorithm For Min-Period Retiming," Asia and South Pacific Design Automation Conference, Shanghai, China (January 2005). After the initial circuit design satisfying the clock period constraint is found at line 1, the method implements a loop to iteratively reduce the number of registers/FFs by moving the registers/FFs backwards over some gates with fanouts larger than fanins. If a fanout edge currently has no register/FF or is on a timing critical path requesting at least one register/FF, such a move may require register/FF moves over other gates. The method of the present invention maintains such relations among the gates, i.e. constraints, as a forest. If there is a cluster of gates, i.e., vertices whose fanouts are larger than its fanins, the number of FFs can be reduced by moving one FF over the cluster and if not, the current design is optimal. An important advantage of the method is that a critical timing constraint is dynamically

generated only when it is needed. Because the method maintains a forest on the gates, it only requests linear storage on top of the circuit graph. The method is extremely efficient in handling large circuits. For example, for a circuit design having more than 180K gates, the method of the present invention provided optimal retiming with a 65 MB memory in less than one minute. As such the method was at least 100 times faster than the prior art Minaret method and it used 1/30<sup>th</sup> of the memory used by Minaret.

**[0028]** More specifically, as shown in Fig. 1, after a feasible retiming  $r$  under clock period  $\phi$  is found, the first step of the loop at line 4 is to find a positive vertex set  $I$  that is closed under the set of active constraints  $\mathcal{A}$ . If no such  $I$  exists, the loop stops and  $r$  is determined to be optimal. A vertex set  $I$  is closed under active constraints  $\mathcal{A}$  if  $\mathcal{A}$  if  $\forall (u, v) \in \mathcal{A}, u \in I \Rightarrow v \in I$ . A vertex set  $I$  is positive if  $b(I) > 0$  so that the increment of  $r$  on  $I$  will reduce the FF area. The new retiming after the increment is denoted by  $r_I$ . However, if such an increase violates the nonnegative FF number requirement on an edge leaving  $I$  as determined at line 7, an active constraint  $(u, v)$  is added to  $\mathcal{A}$  in line 8 of the method. An increase can also violate the timing constraint if a path longer than  $\phi$  is created. The method uses incremental arrival time updating to

identify such a situation and keeps a relation between the source  $u$  and sink  $v$  of the violating path wherein  $\mathcal{D}(u, v) > \phi$  and  $r(v) + \mathcal{W}(u, v) - r(u) = 1$  for such  $u$  and  $v$ . As such, the method of the present invention dynamically identifies timing arcs that lie on the road to improvement in a flow network. More particularly,  $q(v)$  is used to record the source of the critical path to  $v$ . If  $t(v) > \phi$  in  $r_I$  for some vertex  $v$  as determined at line 9, then the method adds an active constraint  $(q(v), v)$  to  $\mathcal{A}$  at line 10. If a positive vertex set  $I$  is found at line 4 that will not generate more active constraints, the FF area is reduced by increasing  $r$  on  $I$  and updating  $\mathcal{A}$  at line 12. If because of the increase in active constraints in set  $\mathcal{A}$ , there is no positive  $I$  closed under  $\mathcal{A}$ , then the retiming  $r$  is determined to be optimal at line 6.

**[0029]** Figure 2 illustrates an example of the incremental minimum area retiming of a circuit in accordance with the method of Fig. 1, wherein the labeling  $\hat{b}$  is shown in Fig 2a after the gate names and the gate delays are inside of each gate. In this example, the clock period is 6. Active constraints are shown as dotted arcs in Fig. 2. Moreover, one FF is moved from the fanouts of the gates shaded gray to their fanins. Detailed execution information is listed in the following Table.

|    | $\mathcal{A}, I$                                        | <i>Comments</i>              |
|----|---------------------------------------------------------|------------------------------|
| 1. | $\phi, \{g, f\}$                                        | $w(f, e) + r(e) - r(f) = 0.$ |
| 2. | $\{(f, e)\}, \{g, f, e\}$                               | $t(c) = 7 > 6, q(c) = g.$    |
| 3. | $\{(f, e), (g, c)\}, \{f, e\}$                          | $r \leftarrow r_1.$          |
| 4. | $\{(f, e), (g, c)\}, \{f, e\}$                          | $w(f, c) + r(c) - r(f) = 0.$ |
| 5. | $\{(f, e), (g, c), (f, c)\}, \{f, e, g, c\}$            | $w(e, d) + r(d) - r(e) = 0.$ |
| 6. | $\{(f, e), (g, c), (f, c), (e, d)\}, \{f, e, g, c, d\}$ | $t(b) = 7 > 6, q(b) = f.$    |
| 7. | $\{(g, c), (f, b)\}, \mathcal{N}_O \text{ positive } I$ | $r \text{ is optimal.}$      |

**[0030]** It is noted that keeping every identified active constraint in  $\mathcal{A}$  is not efficient since it might make  $|\mathcal{A}|$  very large. On the other hand, if not careful, removing some active constraints from  $\mathcal{A}$  may not lead to algorithm convergence, since it is possible to have active constraints cycling in and out of  $\mathcal{A}$ . The method of the present invention successfully overcomes the difficulty by maintaining  $\mathcal{A}$  as a regular forest, which is a forest as discussed below, wherein  $|\mathcal{A}|$  is at most  $n - 1$  while the termination of the algorithm is guaranteed. Because the method

incrementally handles dynamically generated constraints in a regular forest, which can not be done by any existing algorithm, the method of the present invention is much more efficient when it is expensive to generate all of the constraints.

**[0031]** With regard to regular forests, a forest  $\mathcal{F}$  with vertices  $\mathcal{V}$  consists of rooted trees. For any vertex  $v \in \mathcal{V}$ , let  $\mathcal{T}_v$  be the subtree rooted at  $v$  for any non-root vertex  $v \in \mathcal{V}$ , let  $p_v$  be its parent. A labeling  $\mathcal{B}: \mathcal{V} \rightarrow \mathcal{R}$  is maintained such that  $\mathcal{B}(v) = \mathcal{B}(\mathcal{T}_v)$ . For any non-root vertex  $v \in \mathcal{V}$ , a direction is assigned to the edge  $\{p_v, v\}$  such that an active constraint can be derived from the edge. A labeling  $\mathcal{U}(v)$  is used to maintain the direction: if  $\mathcal{U}(v) = \text{true}$ , then  $(v, p_v)$  is the active constraint; and if  $\mathcal{U}(v) = \text{false}$ , then  $\{p_v, v\}$  is the active constraint. Let  $\mathcal{A}(\mathcal{F})$  be the set of the active constraints derived from the edges of  $\mathcal{F}$ . A tree  $\mathcal{T}$  is defined to be regular if for any vertex  $v$  of  $\mathcal{T}$  that is not the root of  $\mathcal{T}$ , the following conditions hold, which are illustrated in Fig. 3.

1. if  $b(\mathcal{T}) > 0$ , then  $(\mathcal{U}(v) \wedge (\mathcal{B}(v) > 0)) \vee (\neg \mathcal{U}(v) \wedge (\mathcal{B}(v) \leq 0))$ ;
2. if  $b(\mathcal{T}) = 0$ , then  $(\mathcal{U}(v) \wedge (\mathcal{B}(v) > 0)) \vee (\neg \mathcal{U}(v) \wedge (\mathcal{B}(v) < 0))$ ;
3. if  $b(\mathcal{T}) < 0$ , then  $(\mathcal{U}(v) \wedge (\mathcal{B}(v) \geq 0)) \vee (\neg \mathcal{U}(v) \wedge (\mathcal{B}(v) < 0))$ ;

A tree is defined to be almost regular if the inequalities  $\mathcal{B}(v) < 0$  and  $\mathcal{B}(v) > 0$  in the above conditions are substituted with  $\mathcal{B}(v) \leq 0$  and  $\mathcal{B}(v) \geq 0$  respectively. Further, the forest  $\mathcal{F}$  is defined to be regular if any tree  $\mathcal{T}$  in the forest is regular.

**[0032]** A tree  $T$  is positive if  $b(T) > 0$ . A tree  $T$  is respectively zero and negative if  $b(T) = 0$  and  $b(T) < 0$  respectively. Let  $\mathcal{P}(\mathcal{F})$  be the set of all of the positive trees,  $\mathcal{Z}(\mathcal{F})$  be the set of all of the zero trees and  $\mathcal{N}(\mathcal{F})$  be the set of all of the negative trees in  $\mathcal{F}$ . Let the vertices in  $\mathcal{P}(\mathcal{F})$  be  $\mathcal{V}_{\mathcal{P}(\mathcal{F})}$ . If  $\mathcal{P}(\mathcal{F}) \neq \emptyset$ , then  $I = \mathcal{V}_{\mathcal{P}(\mathcal{F})}$  is positive and closed under  $\mathcal{A}(\mathcal{F})$ .

**[0033]** Lemma states 1 and 2 are as follows.

LEMMA 1. Let  $I'$  be a vertex set that is closed under  $\mathcal{A}(\mathcal{F})$

Then  $b(I') \leq b(I)$  for  $I = \mathcal{V}_{\mathcal{P}(\mathcal{F})}$ .

On the other hand, if  $\mathcal{P}(\mathcal{F}) = \emptyset$ , optimality can be claimed as in the following lemma.

LEMMA 2. Suppose that  $\mathcal{A}(\mathcal{F})$  is a set of the active constraints of a feasible retiming  $r$  for the clock period  $\phi$ , i.e.,  $\forall (u, v) \in \mathcal{A}(\mathcal{F})$ , either  $w_r(u, v) = 0$ , or  $(\mathcal{D}(u, v) > \phi) \wedge (r(v) + \mathcal{W}(u, v) - r(u) = 1)$ . If  $\mathcal{P}(\mathcal{F}) = \emptyset$ , then  $r$  is the optimal solution of the min-area retiming problem.

**[0034]** The forest  $\mathcal{F}$  is stored in an adjacency list data structure using  $O(n)$  storage. It is assumed that there are two operations that can be completed with  $O(n)$  time and space. The first one is  $\text{CreateTree}(\mathcal{F}, v)$ , which either removes the edge  $\{pu, v\}$  from the forest if  $v$  is not a root, or keeps  $\mathcal{F}$  unchanged if  $v$  is a root. The second one is  $\text{MergeTree}(\mathcal{F}, u, v)$ , which assumes that  $v$  is the root of a tree not containing  $u$  and

makes  $u$  the parent of  $v$ . The subroutine  $\text{ChangeRoot}(\mathcal{F}, v)$  as show in Fig. 4 updates the regular forest  $\mathcal{F}$  in order to make  $v$  the root of a tree without introducing additional active constraints into  $\mathcal{A}(\mathcal{F})$ . In each iteration of the For loop on line 2,  $v_{i-1}$  is the root of the tree containing  $v$ ,  $v_i$  is a children of  $v_{i-1}$ , and  $v$  is the subtree rooted at  $v_i$ . The subtree rooted at  $v_i$  is cut off from the tree rooted at  $v_{i-1}$  on line 4. In order to keep the vertices of  $\mathcal{P}(\mathcal{F})$ ,  $\mathcal{Z}(\mathcal{F})$ , and  $\mathcal{N}(\mathcal{F})$  unchanged,  $v_{i-1}$  is assigned to be a child of  $v_i$  on line 7 if necessary. The correctness of the  $\text{ChangeRoot}$  subroutine is stated in the following lemma.

LEMMA 3. The invariants of the For loop on line 2 are that, first, the regular forest  $\mathcal{F}$  is regular; second,  $\mathcal{A}(\mathcal{F})$  contains no new active constraint; third, the vertices of  $\mathcal{P}(\mathcal{F})$ ,  $\mathcal{Z}(\mathcal{F})$ , and  $\mathcal{N}(\mathcal{F})$  are not changed. When the subroutine terminates,  $v$  is the root of a tree in  $\mathcal{F}$ .

**[0035]** A forest with no edge may be designated as  $\mathcal{F}_0$ . That is, every vertex is a tree in  $\mathcal{F}_0$ . The method of Fig. 1 suggests that to start, the forest  $\mathcal{F}$  is  $\mathcal{F}_0$  and  $\mathcal{P}(\mathcal{F}) = \emptyset$  is eventually satisfied with additional active constraints.

**[0036]** Note that  $b(\mathcal{P}(\mathcal{F})) \geq 0$  always holds and  $\mathcal{P}(\mathcal{F}) = \emptyset$  is equivalent to  $b(\mathcal{P}(\mathcal{F})) = 0$ . Intuitively, either a positive tree is combined with a negative tree to reduce

$b(\mathcal{P}(\mathcal{F}))$ , or a positive tree is combined with a zero tree in order to expand  $\mathcal{P}(\mathcal{F})$  such that  $b(\mathcal{P}(\mathcal{F}))$  can be reduced later. Such progress is captured by a potential tuple,

$$\Psi(\mathcal{F}) \sqsubseteq (b(\mathcal{P}(\mathcal{F})), n - |\mathcal{V}_{\mathcal{P}(\mathcal{F})}|),$$

with the lexicographic ordering, i.e., for  $\Psi(\mathcal{F}) = (\chi, y)$  and  $\Psi(\mathcal{F}') = (\chi', y')$ ,  $\Psi(\mathcal{F}) \preceq \Psi(\mathcal{F}')$  if  $\chi < \chi'$  or  $(\chi = \chi') \wedge (y < y')$ . Assuming that the additional active constraint is  $(u, v)$  satisfying  $u \in \mathcal{V}_{\mathcal{P}(\mathcal{F})}$  and  $v \notin \mathcal{V}_{\mathcal{P}(\mathcal{F})}$ , the UpdateForest subroutine as shown in Fig 5 will decrease  $\Psi(\mathcal{F})$  by adding  $(u, v)$  to  $\mathcal{A}(\mathcal{F})$  and removing active constraints from  $\mathcal{A}(\mathcal{F})$  if necessary. It is noted that such an active constraint must exist eventually as we move FFs from the fanouts of  $\mathcal{V}_{\mathcal{P}(\mathcal{F})}$  to their fanins; otherwise the minimum area retiming problem is unbounded. In this subroutine, the problem is simplified by the ChangeRoot subroutine on line 1 in order to make  $v$  a root in the regular forest. If  $v$  is the root of a zero tree,  $v$  is assigned to be a child of  $u$  on line 3. Otherwise, the problem is simplified by ChangeRoot on line 5 in order to make  $u$  a root. Then  $v$  is assigned to be a child of  $u$  on line 7. Since after line 7, the tree rooted at  $u$  will not always be regular but will always be almost regular, the ZeroCut subroutine is called on line 8 to recover  $\mathcal{F}$  as a regular forest.

**[0037]** The ZeroCut subroutine as shown in Fig. 6, recursively cuts off the subtrees that do not satisfy the conditions of a regular tree. The correctness of the ZeroCut and the UpdateForest subroutines are stated in the following lemmas:

LEMMA 4. Assume that every tree in  $\mathcal{F}$  is regular except  $\mathcal{T}$  which is almost regular. Let  $u$  be the root of  $\mathcal{T}$ . Then after we apply  $\text{ZeroCut}(\mathcal{F}, u, b(\mathcal{T}))$ ,  $\mathcal{F}$  becomes regular and  $b(\mathcal{P}(\mathcal{F}))$  remains unchanged.

LEMMA 5. Assume that  $\mathcal{F}$  is a regular forest,  $u \in \mathcal{V}_{\mathcal{P}(\mathcal{F})}$ , and  $u \notin \mathcal{V}_{\mathcal{P}(\mathcal{F})}$ . Then after we apply  $\text{UpdateForest}(\mathcal{F}, u, v)$ ,  $\mathcal{F}$  remains a regular forest,  $\Psi'(\mathcal{F})$  is strictly decreased, and  $(u, v)$  is the only active constraint added to  $\mathcal{A}(\mathcal{F})$ .

**[0038]** The method of Fig. 1 can be combined with subroutines of Figs. 4, 5 and 6 to provide the incremental minimum area retiming method shown in Fig. 7. The invariants of the loop on line 3 of Fig. 7 are stated in the following lemma.

LEMMA 6. At the beginning of each iteration of the loop on line 3,  $r$  is a feasible retiming for  $\Phi$ ,  $\mathcal{F}$  is a regular forest,  $\mathcal{A}(\mathcal{F})$  is the set of the active constraints of  $r$ .

**[0039]** The preconditions for lines 9 and 10 are established by the following lemma.

LEMMA 7      If  $w_r(u, v) \neq 0$  for any fanout edge  $(u, v)$  of  $I$ , then  $r_I$  is valid. If  $t(v) > \phi$  in  $r_I$  for some vertex  $v$  on line 9, then  $q(v) \in \mathcal{V}_{P(\mathcal{F})}$  and  $v \notin \mathcal{V}_{P(\mathcal{F})}$ .

[0040]      When optimality is not determined at line 6, either the FF area of  $r$  will be strictly decreased by  $b(I) > 0$  for some  $I \subset \mathcal{V}$  and  $\Psi(\mathcal{F})$  remains the same on line 12, or  $\Psi(\mathcal{F})$  will be strictly decreased and the FF area of  $r$  remains the same on line 8 and 10 according to Lemma 5. Since the problem is bounded, the number of the subsets of  $\mathcal{V}$  is finite, and the number of the regular forests with vertices  $\mathcal{V}$  is finite, we can terminate the method where  $r$  is an optimal solution of the minimum area re-timing problem. Together with Lemma 2 and 6, we have the following theorem,

THEOREM 1.      The method of Fig. 7 will terminate and when it terminates,  $r$  is an optimal solution of the min-area retiming problem.

[0041]      The method of Fig. 7 requires  $O(m)$  storage for the circuit graph and  $O(n)$  storage for the auxiliary data structures. The time complexity of each iteration of the loop on line 3 is  $O(m)$ . The number of iterations can be bounded for reasonable practical VLSI circuits as stated in the following theorem,

THEOREM 2.      The space complexity of the method of Fig. 7 is  $O(m)$ . If the labeling  $b$  is assumed to be an integer-value; that the FF area in the initial feasible retiming is bounded by  $O(m)$ ; and that

$b(\mathcal{P}(\mathcal{F}_o)) = \sum_{(v \in \mathcal{V}) \wedge (b(v) > 0)} b(v)$  is bounded by  $O(n)$ , then the time complexity of the method of Fig. 7 is  $O(n^2 m)$

**[0042]** It is noted that it is not necessary to generate  $I$  on line 4 of Fig. 7 from scratch every time. It can be proved that the UpdateForest subroutine changes  $\mathcal{V}_{\mathcal{P}(\mathcal{F})}$  by either inserting vertices or removing vertices but not both. The UpdateForest subroutine can be modified to provide such information so that  $I$  can be constructed to be  $\mathcal{V}_{\mathcal{P}(\mathcal{F})}$  incrementally. Let the inserted vertices or the removed vertices be  $Q$ . They will be used later when the constraints on line 7 and 9 are checked incrementally.

**[0043]** It is also not efficient to check every fanout edge of  $I$ , to compute the labelings  $t$  and  $q$  in  $r_I$ , and to check every vertex every time when the algorithm reaches line 7 and 9. The constraints should be checked incrementally, i.e. the constraints that are known to hold should be excluded from being checked, and the labelings  $t$  and  $q$  should be updated incrementally. Two vertex queues  $\mathcal{J}$  and  $\mathcal{K}$  are maintained for such purpose. For any vertex  $u \notin \mathcal{J}$ , if  $u \in I$ , then for any edge  $(u, v)$ , either  $v \in I$ , or  $w_r(u, v) > 0$ . For any vertex  $u \notin \mathcal{K}$  and any vertex  $v$  in the

combinational fanin cone of  $u$  (including  $u$ ) in  $r_I$ ,  $t(v)$  and  $q(v)$  are up-to-date, and  $t(v) \geq \phi$ . On line 7, a vertex  $u$  is repeatedly removed from  $\mathcal{J}$  until an edge  $(u, v)$  leaving  $I$  satisfying  $w_r(u, v) = 0$  is found or  $\mathcal{J}$  is empty. On line 9 of Fig. 7, the method repeatedly removes a vertex and its combinational fanin cone from  $\mathcal{K}$  and computes  $t(v)$  and  $q(v)$  for any vertex  $v$  in the cone, until  $t(v) > \phi$  for some vertex  $v$  or  $\mathcal{K}$  is empty. The queues  $\mathcal{J}$  and  $\mathcal{K}$  are updated incrementally when  $I$  is changed. When  $I$  is changed by inserting the vertex set  $Q$ , it is sufficient to insert every vertex in  $Q$  to  $\mathcal{J}$  and to insert every vertex in the combinational fanout cone of  $Q$  in  $r_I$  to  $\mathcal{K}$ . Computing the cone can be time consuming when  $|Q|$  is large. In such case every vertex of  $\mathcal{G}$  is inserted into  $\mathcal{K}$ . When  $I$  is changed by removing the vertex set  $Q$ , it is sufficient to insert to  $\mathcal{J}$  the vertices  $u \in I$  that fanouts to a vertex  $v \in Q$  satisfying  $w_r(u, v) = 0$ . Identifying such vertices could be inefficient when  $|Q|$  is large. In such case, every vertex of  $\mathcal{G}$  is inserted to  $\mathcal{J}$ . For the queue  $\mathcal{K}$  every vertex of  $\mathcal{G}$  is inserted to it.

**[0044]** If the sharing of the FFs at the fanouts of gates is considered, redundant constraints can be introduced to  $\mathcal{PO}$ . Let  $u$  be any vertex with the

dummy vertex  $u_m$  and let  $v$  be a fanout of  $u$ . In  $\mathcal{PO}(r)$ , we should have  $w(u,v)+r(v) - r(u) \geq 0$  and  $w_{\max}(u) - w(u, v) + r(u_m) - r(v) \geq 0$ . Thus,  $w_{\max}(u) + r(u_m) - r(u) \geq 0$ . This redundant constraint is inserted to  $\mathcal{PO}$  and is checked first on line 7 after  $u$  is removed from the vertex queue  $\mathcal{J}$ . The effect is that when both  $(u, v)$  and  $(v, u_m)$  are active constraints,  $(u, u_m)$  are directly identified as an active constraint and thus  $u$  and  $u_m$  are included in one regular tree without requiring a detour to  $v$ . As  $b(u) > 0$  and  $b(u) + b(u_m) = 0$  for most  $u$ ,  $b(\mathcal{P}(\mathcal{F}))$  is reduced more frequently without the necessity to expand  $\mathcal{P}(\mathcal{F})$  first and the method runs faster.

**[0045]** The retiming method of the present invention has been found to be substantially faster than prior methods and it uses considerably less memory. Moreover, because the method is incremental, it can be stopped at any time that the circuit designer is satisfied with the register/FF area or number of registers/FFs.

**[0046]** Many further modifications and variations of the present invention are possible in light of the above teachings. Thus, it is to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than are described here in above.

## CLAIMS

What is claimed is:

1. A method of relocating registers in a circuit design, the method being implemented as one or more routines executed by a processor and comprising:
  - iteratively generating constraints related to the relocation of registers in the circuit design to form a set of constraints;
  - maintaining the constraints as a regular forest; and
  - incrementally relocating registers in the circuit design to reduce the register area and/or the number of registers in the circuit design.
2. The method of relocating registers in a circuit design as recited in claim 1, wherein the registers are flip flops.
3. The method of relocating registers in a circuit design as recited in claim 1, including determining whether there is a cluster of gates in the circuit wherein each gate of the cluster has a number of fanouts that is greater than the number of fanins of the gate and relocating the registers by iteratively moving a register over the cluster.
4. The method of relocating registers in a circuit design as recited in claim 1, wherein the forest is stored as an adjacency list data structure.
5. The method of relocating registers in a circuit design as recited in claim 1, including
  - representing the circuit as a graph with a plurality of vertices representing gates and a plurality of edges representing signals between vertices; and

updating the regular forest to make a vertex a root of a tree without generating a constraint.

6. The method of relocating registers in a circuit design as recited in claim 5, including cutting off a subtree if the subtree is not a regular forest.

7. The method of relocating registers in a circuit design as recited in claim 1, wherein a constraint is generated when an increase in the number of registers moved over a path extends the path to be longer than a given clock period.

8. The method of relocating registers in a circuit design as recited in claim 1, wherein a constraint is generated only if it is directed to a path in the circuit that can lead to a reduction in the area of registers and/or number of registers in the circuit.

9. The method of relocating registers in a circuit design as recited in claim 1, including dynamically updating gate arrival times and comparing the gate arrival times to a given clock period.

10. A method of relocating flip flops in a circuit design, the method being implemented as one or more routines executed by a processor and comprising:  
dynamically generating timing constraints;  
maintaining the dynamically generated timing constraints as regular forest;  
and  
incrementally retiming the circuit design to reduce the flip flop area and/or number of flip flops in the circuit.

11. The method of relocating flip flops in a circuit design as recited in claim 10, including determining whether there is a cluster of gates in the circuit wherein each gate

of the cluster has a number of fanouts that is greater than the number of fanins of the gate and relocating flip flops by iteratively moving a flip flop over the cluster.

12. The method of relocating flip flops in a circuit design as recited in claim 10, wherein the absolute value of the number of constraints in the set maintained as a forest is at most  $n-1$  where  $n$  is the number of vertices in the circuit when represented as a graph.

13. The method of relocating flip flops in a circuit design as recited in claim 12, wherein the vertices in the graph represent combinational gates in the circuit.

14. The method of relocating flip flops in a circuit design as recited in claim 10, including dynamically updating gate arrival times and comparing the gate arrival times to a given clock period.

15. The method of relocating flip flops in a circuit design as recited in claim 10, wherein a timing constraint is generated when an increase in the number of flip flops moved over a path extends the path to be longer than a given clock period.

16. The method of relocating flip flops in a circuit design as recited in claim 10, wherein a timing constraint is generated only if it is directed to a path in the circuit that can lead to a reduction in the flip flop area and/or number of flip flops in the circuit.

17. A method of relocating registers in a circuit design, the method being implemented as one or more routines executed by a processor and comprising:

dynamically generating constraints related to the relocation of registers in the circuit design to form a set of constraints, wherein a constraint is generated

only if it is directed to a path in the circuit design that can lead to a reduction in the register area and/or number of registers in the circuit design;

maintaining the constraints as a regular forest; and

incrementally relocating registers in the circuit to reduce the register area and/or the number of registers in the circuit design.

18. The method of claim 17, wherein the registers are flip flops.

19. The method of claim 17, including determining whether there is a cluster of gates in the circuit wherein each gate of the cluster has a number of fanouts that is greater than the number of fanins of the gate and relocating the registers by iteratively moving a register over the cluster.

20. The method of claim 17, wherein a constraint is generated when an increase in the number of registers moved over a path extends the path to be longer than a given clock period.

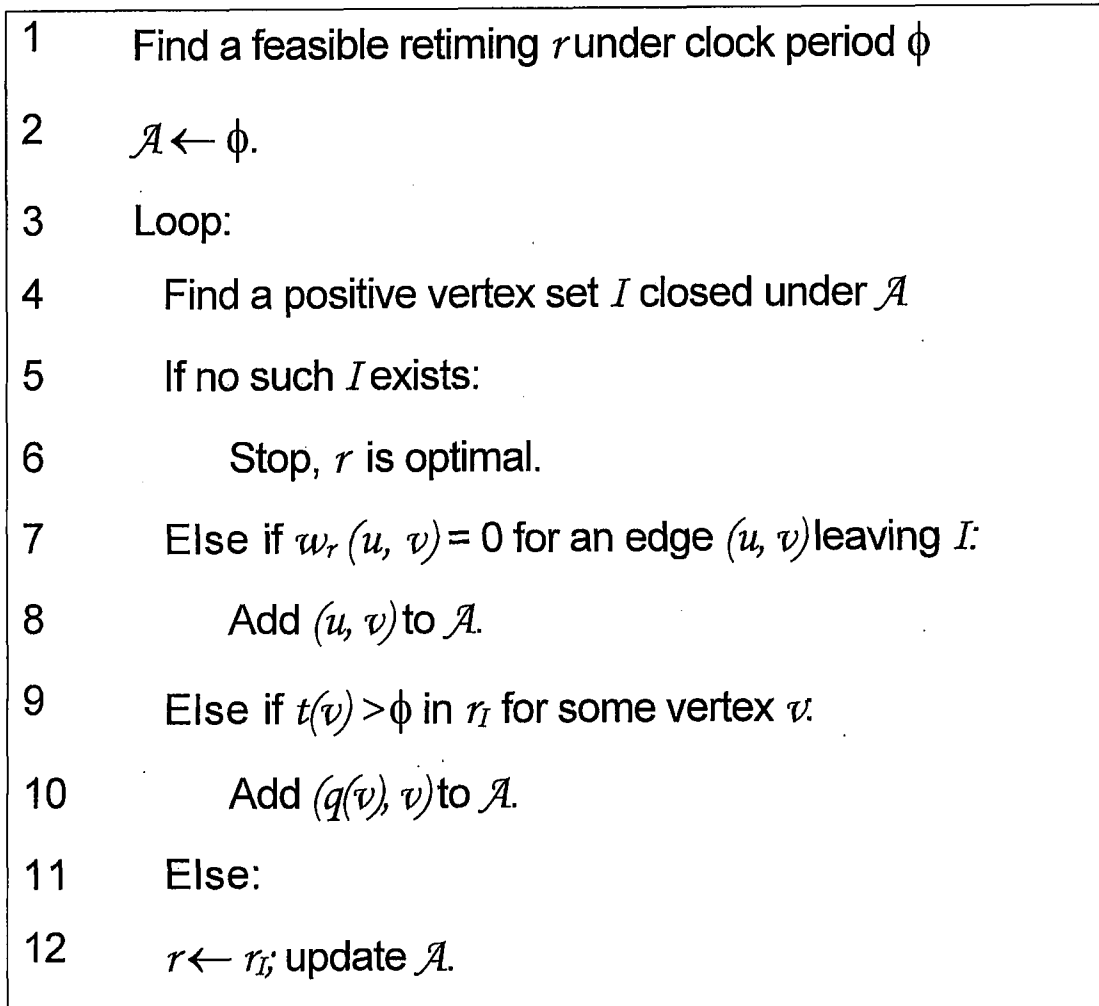


FIG. 1

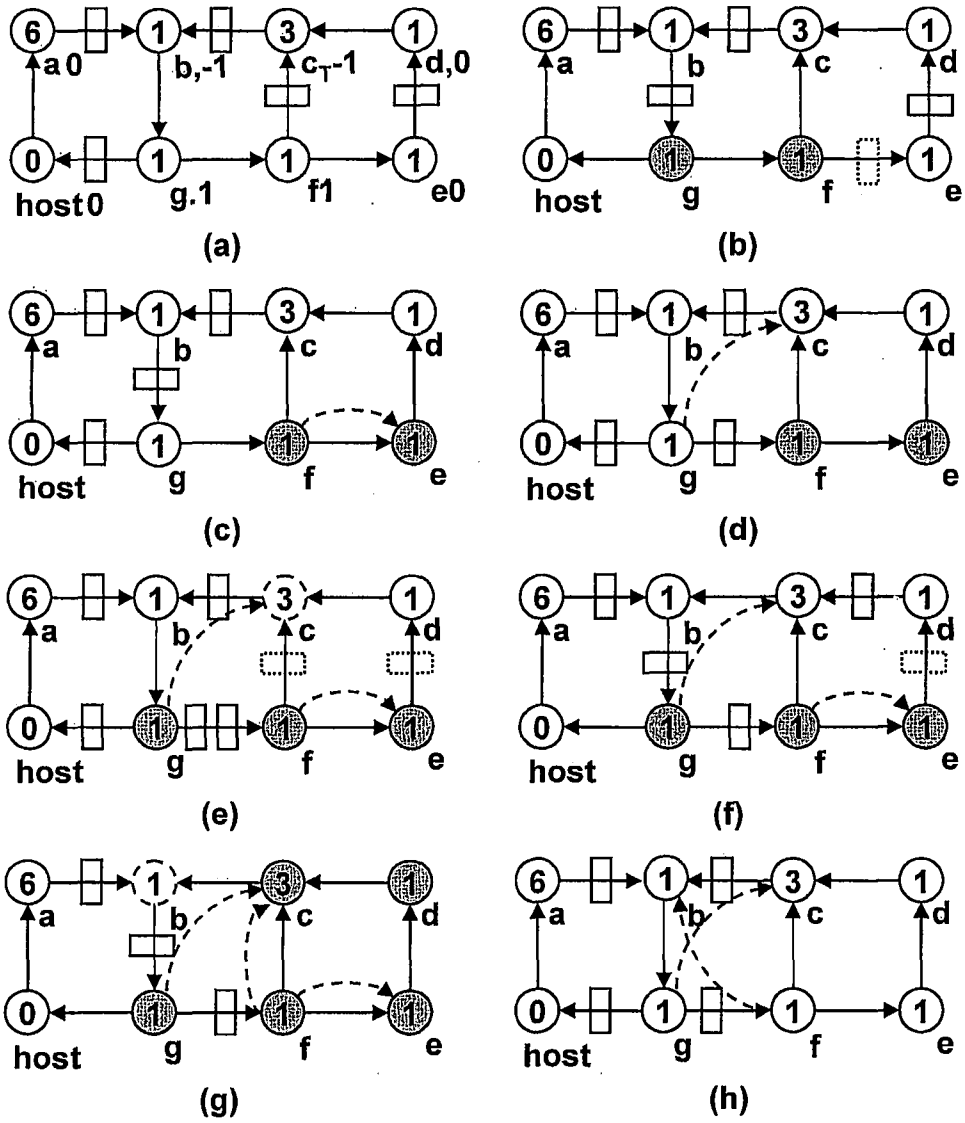


FIG. 2

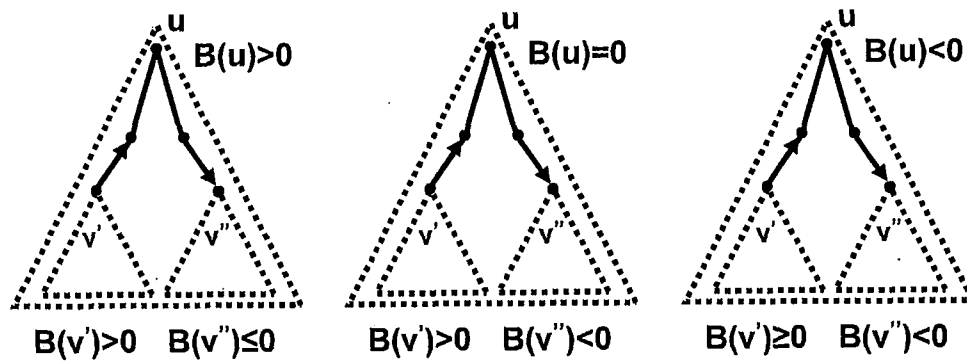


FIG. 3

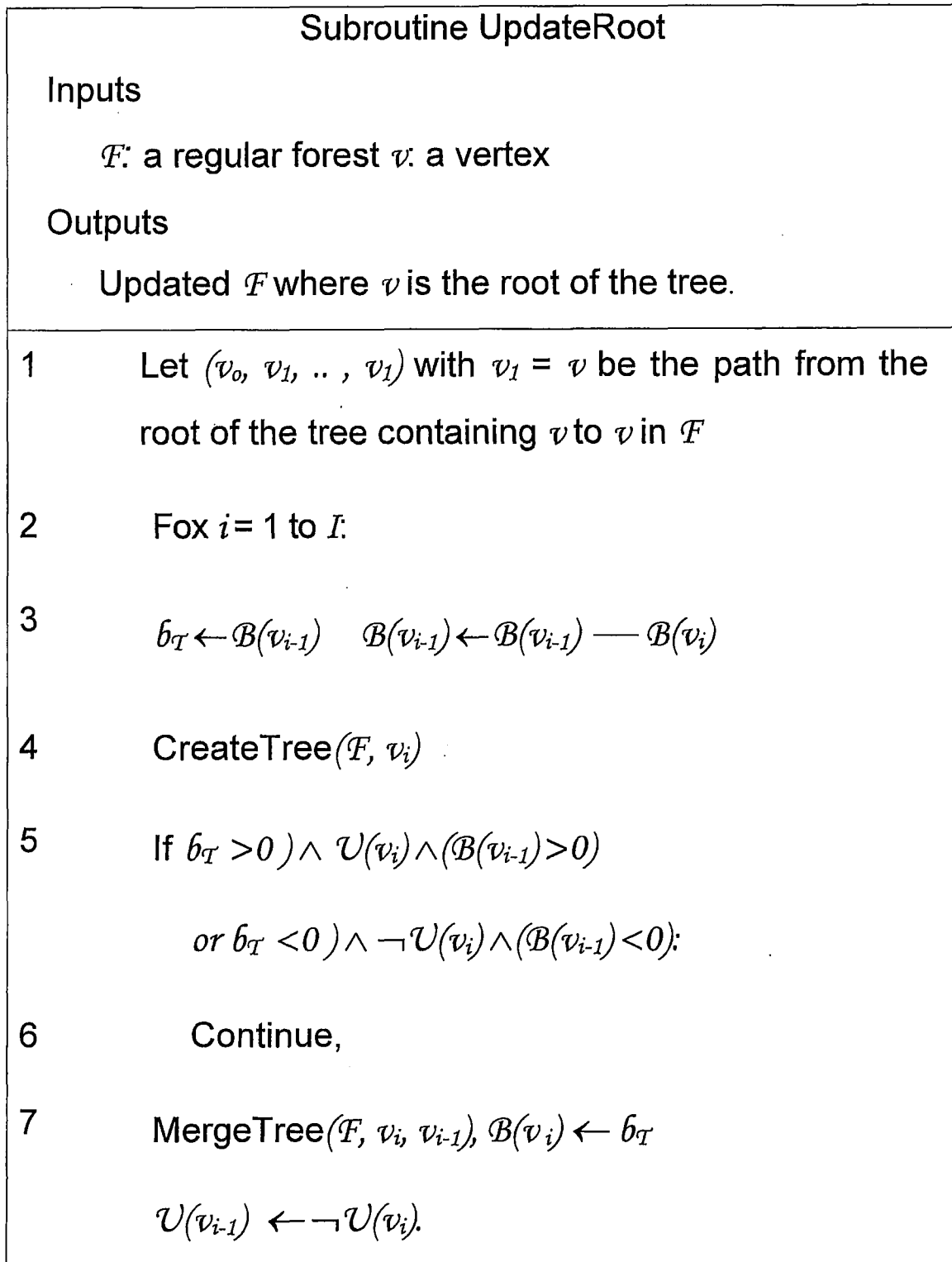


FIG. 4

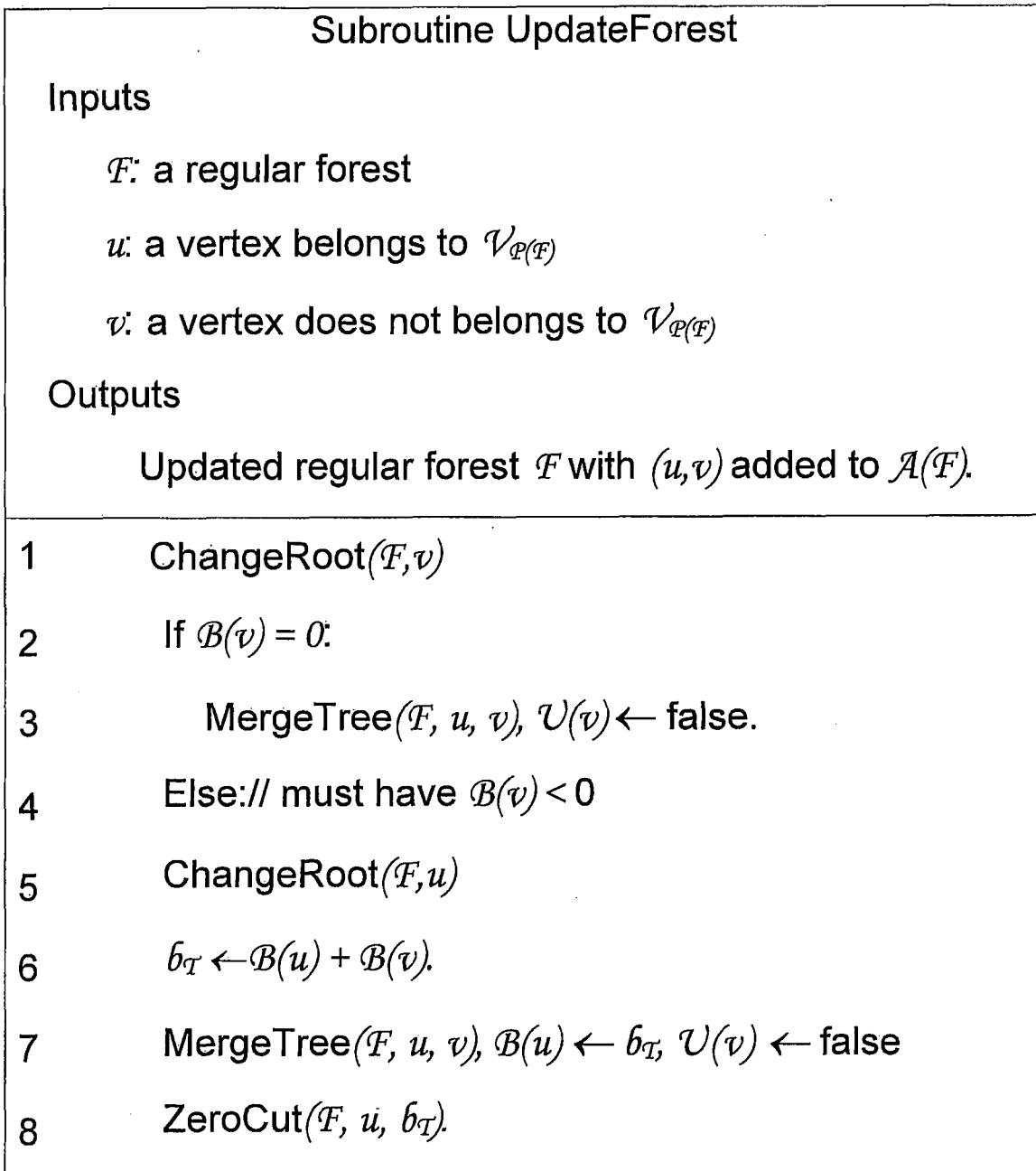


FIG. 5

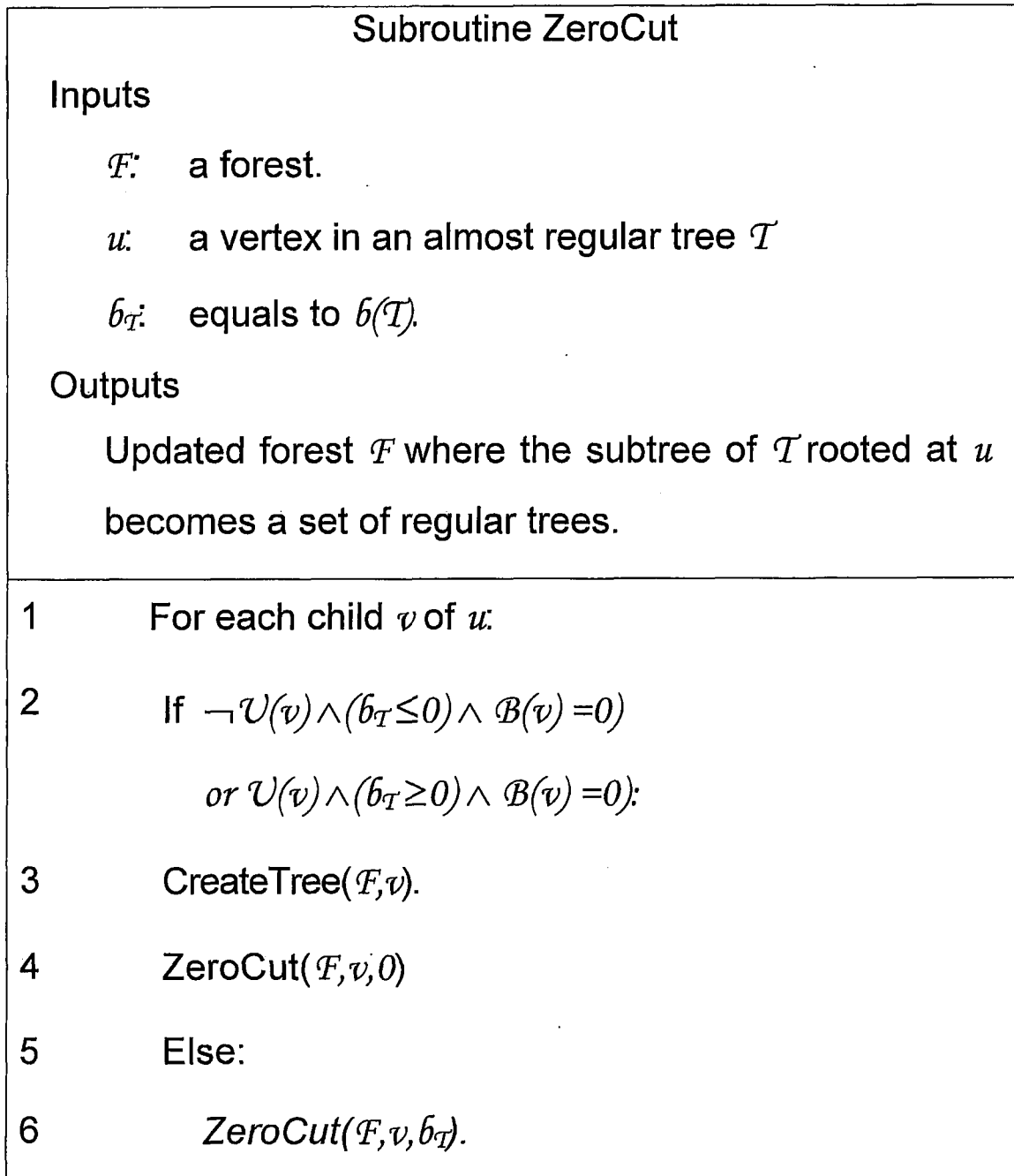


FIG. 6

### Algorithm iMinArea

#### Inputs

$\phi$ : the clock period

#### Outputs

The optimal feasible retiming  $r$  for  $\phi$

```

1   Initialize a feasible retiming  $r$  under clock period  $\phi$ 
2   Initialize  $\mathcal{F}$  to be a forest with no edge.
3   Loop:
4        $I \leftarrow \mathcal{V}_{\mathcal{P}(\mathcal{F})}$ 
5       If  $I = \phi$ :
6           Stop,  $r$  is optimal.
7       Else if  $w_r(u, v) = 0$  for an edge  $(u, v)$  leaving  $I$ :
8           UpdateForest( $\mathcal{F}, u, v$ ).
9       Else if  $t(v) > \phi$  in  $r_I$  for some vertex  $v$ :
10          UpdateForest( $\mathcal{F}, q(v), v$ ).
11      Else:
12           $r \leftarrow r_I$ .
```

**FIG. 7**

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 09/32810

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 17/50 (2009.01)

USPC - 716/2

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC - 716/2

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC: 716/1-2, 6, 8-10

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST (PGPB, USPT, EPAB, JPAB); Google

Search Terms: Electronic design software, efficient, reduce, minimize, register, flip flop, VLSI, circuit, tree, quantity, number, constraints, forest, cluster gates, fan outs, fan ins, adjacency list, data structure, vertices, vertex, root, subtree, clock period, gate arrival

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                           | Relevant to claim No. |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 7,296,246 B1 (Kuehlmann, et al) 13 November 2007 (13.11.2007) entire document especially Fig. 1A-1E, col 3 ln 35-63, col 5 ln 1-64, col 5 ln 1-64, col 6 ln 48-col 7 ln 55, col 7 ln 32-55, col 8 ln 15-64, col 9 ln 60 to col 10 ln 24, col 11 ln 24-36. | 1-20                  |
| A         | US 7,200,822 B1 (McElvain) 03 April 2007 (03.04.2007) entire document.                                                                                                                                                                                       | 1-20                  |

☐ Further documents are listed in the continuation of Box C.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

16 March 2009 (16.03.2009)

Date of mailing of the international search report

23 MAR 2009

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