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[56]		References Cited	
		UNITED STATES PATENTS	
2,811,698	10/1957	Slate.....	333/73 S
2,751,558	6/1956	Grieg et al.	333/84 M
3,199,054	8/1965	Holland.....	333/31
3,419,813	12/1968	Kamnitsis.....	333/84 M
3,458,837	7/1969	Ngo.....	333/73
3,509,495	4/1970	Morton.....	333/22

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[54] **MICROSTRIP DELAY LINE**
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333/84 (M)
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H03h 7/34
[50] Field of Search..... **333/30, 84**
M, 29, 73 S

ABSTRACT: The characteristic impedance of a microstrip delay line is controlled by altering the effective area of the ground plane. Reducing the effective ground plane area increases the characteristic impedance and improves the output rise time while maintaining a nearly constant time delay.

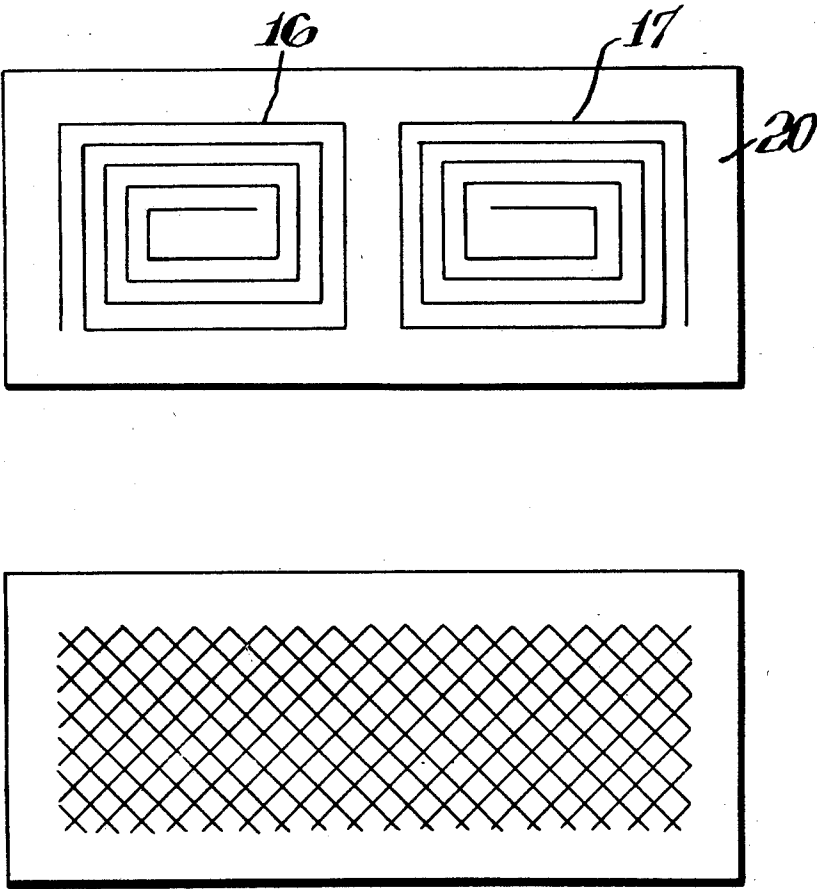


Fig. 1.

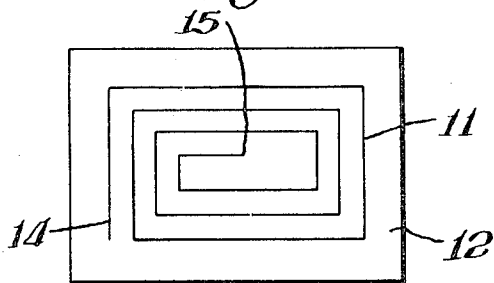


Fig. 3.

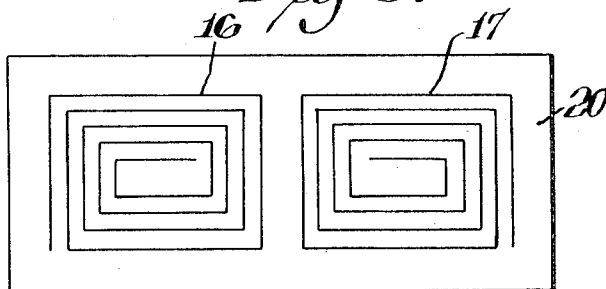


Fig. 2.

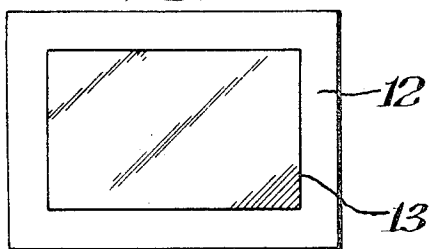


Fig. 4.

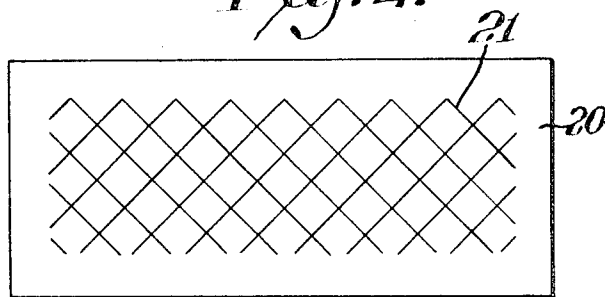
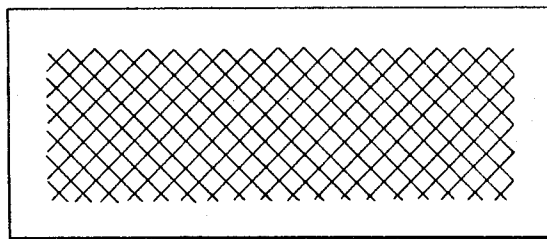


Fig. 5.



MICROSTRIP DELAY LINE

BACKGROUND OF THE INVENTION

This invention relates to microstrip delay lines and in particular to such lines having a less than solid ground plane.

The rapid advancement in the field of high speed digital integrated circuits has produced a requirement for miniaturized delay lines having the requisite high frequency characteristics. A response to this need has been the parallel plate microstrip delay line in which an active line comprising a series inductance is formed by deposition of a conductive spiral on one surface of a ceramic substrate. A distributed shunt capacitance is provided by a conductive ground plane deposited on the opposing substrate surface and in proximate capacitive relation to the spiral. The conductors are deposited by printing techniques well known in integrated and thick film circuit technology.

The microstrip line meets the high frequency requirements by providing time delays up to 10 nsec. (on one-half inch cubes), delay to rise time ratios of up to 5:1 and characteristic impedances of 25 to 100 ohms. In addition, these lines are of small bulk and weight and can be economically manufactured in quantity by the recent printing processes.

Delay line performance parameters for these lines are normally controlled, for a given dielectric, by varying the inductor spiral length and pitch and/or the dielectric thickness. It is an object of this invention to add an additional control variable. It is a further object to improve the rise time characteristics over those attainable with the present lines.

SUMMARY OF THE INVENTION

Broadly, a delay line constructed in accordance with this invention comprises a distributed series inductance formed as a conductive spiral on the surface of a ceramic substrate and a distributed series capacitance provided by depositing a conductive ground plane on the opposing substrate surface and in proximate capacitive relation to the spiral.

In a more limited sense, the effective area of such a deposited ground plane is variable; that is, for a ground plane which is designed to occupy a given area in relation to the active line, the effective area of such a plane may be effectively reduced by etching away selected portions of the plane. Heretofore, full ground planes only have been used for these lines. Changes in the lines' characteristic impedance necessitated redesigning the spiral (by changing width or pitch) or altering the substrate thickness. It has been discovered, however, that reductions in the ground plane area of up to 75 percent have the following effect: line impedance increases by about 50 percent; the line delay remains nearly constant and the rise time improves.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the active plane of a conventional microstrip line;

FIG. 2 shows the ground plane for the delay line of FIG. 1;

FIG. 3 shows the active plane of one embodiment of the invention;

FIG. 4 shows the ground plane for the delay line of FIG. 3 wherein the effective ground area is reduced by 75 percent; and

FIG. 5 shows the ground plane of another embodiment of the invention wherein the effective ground area is reduced by 50 percent.

DESCRIPTION OF THE INVENTION

A microstrip delay line is essentially a parallel plate transmission line wherein an "active" inductance line is separated from a parallel ground line by a dielectric material.

FIGS. 1 and 2 show a conventional microstrip delay line where the active line is formed by screening a spiral conductor 11 onto the surface of a substrate 12 and by screening a

ground plane 13 on the opposing surface. The ground plane is uniformly spaced along the length and width of the active line thus affording a characteristic impedance along the length of the delay line. The input pulse is applied between terminal 14 and the ground plane and the output pulse is measured between terminal 15 and the ground plane. The spiral design (number of turns, segment width) and the substrate qualities (permittivity, strength) are determined by particular design requirements.

FIGS. 3 and 4 show one embodiment of the invention. The delay line is designed for a 6 nanosecond delay and the active line requires the deposition of 0.25 inch square conductive spirals 16 and 17 joined in series. These spirals are formed by screening a thin film (0.2 to 0.4 mil) conductive material such as silver onto the surface of ceramic substrate 20. The substrate is 0.020 inch thick titanium dioxide having a dielectric constant of 40. The ground plane 21, a thin film (0.2 to 0.4 mil) of silver is screened onto the opposite surface of the substrate to form the pattern shown in FIG. 4. While the ground plane is still uniformly spaced within the same area encompassed within the spiral perimeters, its effective conductive area is only 25 percent of that which a solid conductive plane would occupy. FIG. 5 shows another embodiment of the invention wherein the ground plane area has been uniformly reduced 50 percent.

Delay line characteristics of the two embodiments were measured and compared to a line physically identical except for a conventional solid ground plane (100 percent of ground area metallized). Table 1 summarizes these results.

TABLE 1
Delay line parameters

	100% ground	50% ground	25% ground
Delay time, nanoseconds...	6	6	5.2
Rise time, nanoseconds.....	3.2	2.0	1.8
Capacitance, pf.....	189	151	86.5
Impedance, Ω	40	45	63

Referring to Table 1, it is seen that the impedance has increased from 40 ohms at full ground to 63 ohms with 75 percent of the ground area removed. While capacitance has decreased from 189 to 86.5 pf, the delay time has only decreased 0.8 nanosecond. The reason for this time delay constancy is that, while the delay is a function of the length of the line and the square root of the permittivity of the dielectric, the impedance is a function of the square root of the product of permittivity and the line dimensions. As a consequence, the delay changes at a much lower rate than the impedance.

The relation between the percentage of ground area removed and impedance increase is not directly proportional due to a fringing effect. Hence an empirical approach is required to design a ground area such that a required impedance is obtained.

Since it is obvious that many changes and modifications can be made in the above-described details without departing from the nature and spirit of the invention it is to be understood that the invention is not limited to said details except as set forth in the appended claims.

As an example, other ground patterns can be used besides those shown in FIGS. 4 and 5. The only requirements are regularity in pattern over the superimposed length and width of the parallel active line. Also, barium titanate could be used as the substrate material.

What I claim is:

1. A delay line comprising a substantially planar dielectric substrate, a first electrical conductor disposed to form a distributed inductance pattern on one surface of said dielectric substrate, and a second electrical conductor disposed on the opposite surface of said dielectric substrate in capacitive relation to said first conductor so as to encompass the surface area directly opposing the perimeter of said distributed inductance pattern, and wherein the second conductor is patterned by uniformly dispersed holes therethrough such that said second conductor covers less than the entire surface area opposing

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the perimeter of the distributed inductance thereby increasing the line impedance and improving the rise time characteristics with substantially no change in delay time.

2. A delay line as described in claim 1 wherein said first electrical conductor is a thin film of a conductive material screened onto the surface of a ceramic substrate in a spiral pattern and wherein said second electrical conductor is a thin film of conductive material screened onto the opposing surface of the ceramic substrate over an area equal to that bounded by the spiral perimeters, said conductive film covering more than 25 percent of said area.

3. A delay line as described in claim 2 wherein said ceramic base is selected from the group consisting of titanium dioxide and barium titanate.

5 4. The delay line of claim 1 wherein said first electrical conductor is disposed to form at least two distributed inductance spiral patterns coupled in series enhancing mode.

10 5. The delay line of claim 1 wherein said second conductor comprises a first series of uniformly spaced parallel conducting lines and a second series of uniformly spaced parallel conducting lines wherein the lines of said second series contact the lines of said first series at substantially right angles.

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