(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 November 2007 (29.11.2007)

PCT

(10) International Publication Number
WO 2007/136539 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2007/011017

(22) International Filing Date: 7 May 2007 (07.05.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/437,536 19 May 2006 (19.05.2006) US

(71) Applicant *(for all designated States except US)*: **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, New York 14650-2201 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PARKS, Christopher** [US/US]; 113 Kentucky Crossing, Rochester, New York 14612 (US). **HUNT, Howard Marc** [US/US]; 500 Lakeview Terrace, Webster, New York 14580 (US).

(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, New York 14650-2201 (US).

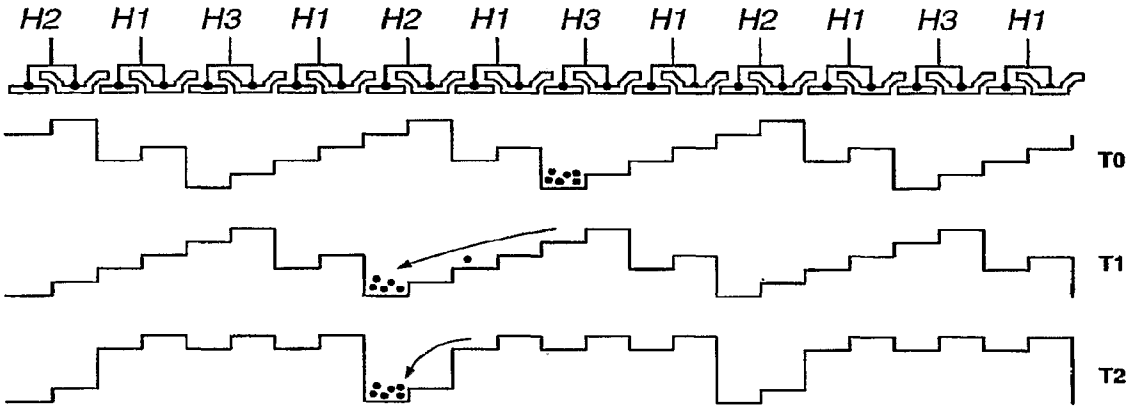
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** CCD WITH IMPROVED CHARGE TRANSFER



(57) **Abstract:** A charge coupled device having a plurality of non-adjacent first gate electrode pairs; a plurality of second gate electrode pairs placed in every second space between the first gate electrode pairs; a plurality of third gate electrode pairs placed in the spaces between the first gate electrode pairs not occupied by the second gate electrode pairs; wherein, in a full resolution mode, the first gate electrode pairs are clocked substantially 180 degrees out of phase with respect to the second and third gate electrode pairs and the second and third gate electrode pairs are clocked substantially equally; and wherein, in a half resolution, double speed mode, the second and third gate electrode pairs are clocked substantially 180 degrees out of phase with respect to each other and substantially 50% duty cycle and the first gate electrode pairs are clocked with 25% or less duty cycle and 90 degrees out of phase with respect to the second gate electrode pairs.

WO 2007/136539 A2

CCD WITH IMPROVED CHARGE TRANSFER

FIELD OF THE INVENTION

The invention relates generally to the field of charge-coupled devices and, more particularly, to improving the charge transfer electric field in a CCD operating in a half resolution mode.

BACKGROUND OF THE INVENTION

Fig. 1 shows a prior art charge coupled device (CCD) operable in two modes. The first mode is a full-resolution image read out mode and the second mode is a half-resolution double speed read out mode. In the double speed read out mode, two adjacent charge packets are summed together and are transferred two times faster than in full resolution mode. These two modes allow for a two-dimensional pixel array to be read out in a full resolution still photography imaging mode and a reduced resolution video-imaging mode. Examples of this prior art can be found in patents US Patent Nos. 6,452,634 and 6,462,779.

In Fig. 1, a pseudo-2-phase CCD is shown with every other gate pair connected to timing signal H1. The gate pairs between H1 alternate between timing signals H2 and H3. Fig. 2 shows the timing signals for the full-resolution read out of Fig. 1. In full-resolution mode, H2 and H3 are clocked the same and with the opposite phase of H1. This timing causes the charge packets in the CCD to be advanced by two gate pairs for each clock cycle.

Fig. 3 shows the transfer of charge in the half-resolution double speed read out mode and Fig. 4 shows the timing signals for Fig. 3. H1 is held at a constant DC voltage. H2 and H3 are now clocked with opposite phase. The amplitude of the clock signals H2 and H3 is double the full-resolution mode amplitude shown in Fig. 2. This double speed timing advances the charge packets four gate pairs in one clock cycle, twice as far as the full-resolution mode. The double speed timing mode also sums together two adjacent charge packets to reduce the resolution by one half.

One deficiency of the charge transfer shown in Fig. 3 is the voltage potential steps are small and the distance the charge travels is long. Consequently, it is desirable to increase the voltage between adjacent gate pairs to increase the electric field strength in the CCD. An increased electric field will improve the charge transfer efficiency.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the present invention, the method resides in a charge coupled device having a plurality of non-adjacent, first gate electrode pairs; a plurality of second gate electrode pairs placed in every second space between the first gate electrode pairs; a plurality of third gate electrode pairs placed in the spaces between the first gate electrode pairs not occupied by the second gate electrode pairs; wherein, in a full resolution mode, the first gate electrode pairs are clocked substantially 180 degrees out of phase with respect to the second and third gate electrode pairs and the second and third gate electrode pairs are clocked substantially equally; wherein, in a half resolution, double speed mode, the second and third gate electrode pairs are clocked substantially 180 degrees out of phase with respect to each other and substantially 50% duty cycle and the first gate electrode pairs are clocked with 25% or less duty cycle and 90 degrees out of phase with respect to the second gate electrode pairs.

The above and other objects of the present invention will become more apparent when taken in conjunction with the following description and drawings wherein identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

Advantageous Effect Of The Invention

The present invention has the following advantages of increasing the voltage between adjacent gate pairs to increase the electric field strength in the CCD. An increased electric field will improve the charge transfer efficiency.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is prior art showing full resolution CCD charge transfer;

Fig. 2 is the prior art timing diagram for Fig. 1;

Fig. 3 is prior art showing half resolution double speed CCD charge transfer;

Fig. 4 is the prior art timing diagram for Fig. 3;

Fig. 5 is a charge transfer in a half resolution double speed CCD with increased electric field for improved charge transfer efficiency;

Fig. 6 is the timing diagram for Fig. 5;

Fig. 7 is a charge transfer for the full resolution mode;

Fig. 8 is the timing diagram for Fig. 7;

Fig. 9 is the invention implemented with a true-2-phase CCD; and

Fig. 10 is a digital camera using an image sensor employing a half resolution double speed CCD with increased electric field for improved charge transfer efficiency.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 5 shows an image sensor CCD 10 with improved half resolution double speed mode charge transfer efficiency. It consists of three gate pairs H1, H2, and H3. Every other gate pair is connected to timing signal H1. The gate pairs between H1 alternate between timing signals H2 and H3. The timing signals for Fig. 5 are shown in Fig. 6. In half-resolution double speed mode, the CCD timing signals H2 and H3 are clocked 180 degrees or substantially 180 degrees out of phase with respect to each other and with double the amplitude of timing signal H1. The H2 and H3 timing signals have a 50% duty cycle. Unlike the prior art, timing signal H1 is clocked with less than a 50% duty cycle and 90 degrees out of phase from timing signal H2. This sets up the situation in Fig. 5 at time step T2. Here the channel potential voltage difference from gate pairs H1 to H2 is twice as large as the prior art. This will double the electric field strength within the CCD and improve charge transfer efficiency. It also causes charge to transfer through four gate pairs in one clock cycle and it sums together

two adjacent charge packets. This allows for a reduced resolution image sensor with a faster frame rate.

Fig. 7 shows the charge transfer when the CCD is clocked in full-resolution read out mode. The timing diagram for Fig. 7 is shown in Fig. 8. Here the normal two-phase clocking is applied to the gate pairs. H2 and H3 are clocked in phase with respect to each other and with half the amplitude of the half resolution double speed mode. The H1 timing signal is clocked 180 degrees out of phase or substantially 180 degrees out of phase with respect to H2 or H3. The amplitude of the timing signals can be the same as the half resolution double speed mode or they can be set to one half amplitude (as shown in Fig. 8). Normally the clock voltage amplitude in full-resolution mode would be set to one half to conserve power.

The invention thus far has been described in the context of a pseudo-2-phase CCD where adjacent gate pairs are connected together. The invention will work equally well with a CCD of the true-2-phase design as shown in Fig 9. The extra channel potential adjusting implant 30 creates a step in the channel potential under each gate. The timing signals applied to the gates H1, H2, and H3 are the same as in Fig. 6.

Fig. 10 illustrates a digital camera 20 having the CCD image sensor 10 disposed therein for illustrating a typical commercial embodiment to which the ordinary consumer is accustomed.

PARTS LIST

10	image sensor CCD
20	digital camera
30	extra channel potential adjusting implant

WHAT IS CLAIMED IS:

1. A charge coupled device comprising:

(a) a plurality of non-adjacent, first gate electrode pairs;

(b) a plurality of second gate electrode pairs placed in every second space between the first gate electrode pairs;

(c) a plurality of third gate electrode pairs placed in the spaces between the first gate electrode pairs not occupied by the second gate electrode pairs;

wherein, in a full resolution mode, the first gate electrode pairs are clocked substantially 180 degrees out of phase with respect to the second and third gate electrode pairs and the second and third gate electrode pairs are clocked substantially equally;

wherein, in a half resolution, double speed mode, the second and third gate electrode pairs are clocked substantially 180 degrees out of phase with respect to each other and substantially 50% duty cycle and the first gate electrode pairs are clocked with 25% or less duty cycle and 90 degrees out of phase with respect to the second gate electrode pairs.

2. The charge coupled device of claim 1, wherein one or more of the plurality of gate electrode pairs are a single gate electrode with a channel potential adjusting implant partially under each gate electrode.

3. A method of clocking a charge coupled device, the method comprising the steps of:

(a) providing a plurality of non-adjacent first gate electrode pairs;

(b) providing a plurality of second gate electrode pairs placed in every second space between the first gate electrode pairs;

(c) providing a plurality of third gate electrode pairs placed in the spaces between the first gate electrode pairs not occupied by the second gate electrode pairs;

(d) clocking, in a full resolution mode, the first gate electrode pairs substantially 180 degrees out of phase with respect to the second and third gate electrode pairs and clocking the second and third gate electrode pairs substantially equally; and

(e) clocking, in a half resolution, double speed mode, the second and third gate electrode pairs substantially 180 degrees out of phase with respect to each other and substantially 50% duty cycle and clocking the first gate electrode pairs with 25% or less duty cycle and 90 degrees out of phase with respect to the second gate electrode pairs.

4. The method as in claim 3 further comprising providing one or more of the plurality of gate electrode pairs as a single gate electrode with a channel potential adjusting implant partially under each gate electrode.

5. A camera comprising:

a charge coupled device comprising:

(a) a plurality of non-adjacent, first gate electrode pairs;

(b) a plurality of second gate electrode pairs placed in every second space between the first gate electrode pairs; and

(c) a plurality of third gate electrode pairs placed in the spaces between the first gate electrode pairs not occupied by the second gate electrode pairs;

wherein, in a full resolution mode, the first gate electrode pairs are clocked substantially 180 degrees out of phase with respect to the second and third gate electrode pairs and the second and third gate electrode pairs are clocked substantially equally;

wherein, in a half resolution, double speed mode, the second and third gate electrode pairs are clocked substantially 180 degrees out of phase with respect to each other and substantially 50% duty cycle and the first gate electrode pairs are clocked with 25% or less duty cycle and 90 degrees out of phase with respect to the second gate electrode pairs.

6. The camera as in claim 5, wherein one or more of the plurality of gate electrode pairs are a single gate electrode with a channel potential adjusting implant partially under each gate electrode.

5

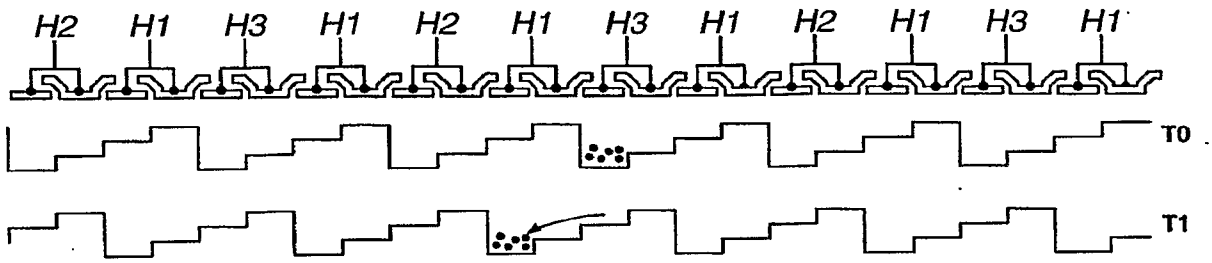


FIG. 1
(PRIOR ART)

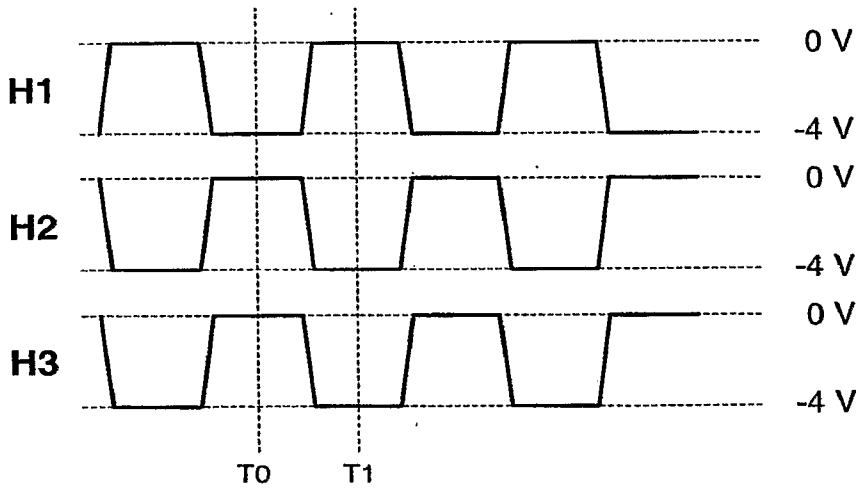


FIG. 2
(PRIOR ART)

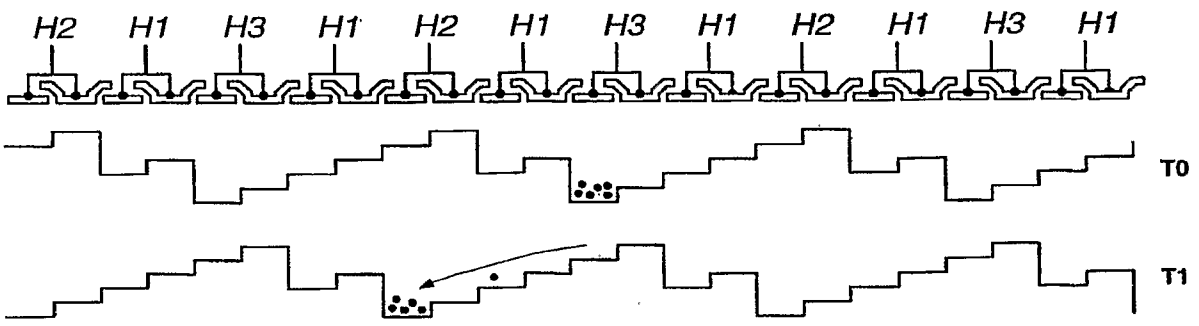


FIG. 3
(PRIOR ART)

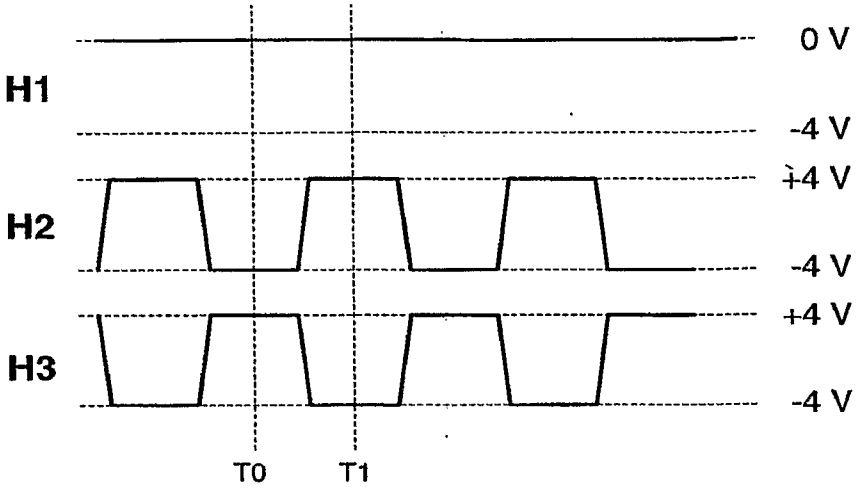


FIG. 4
(PRIOR ART)

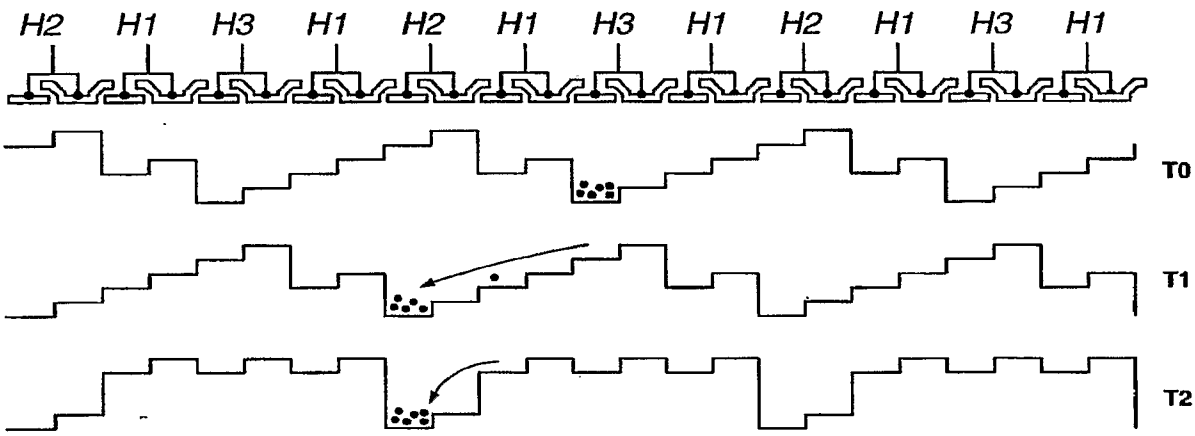


FIG. 5

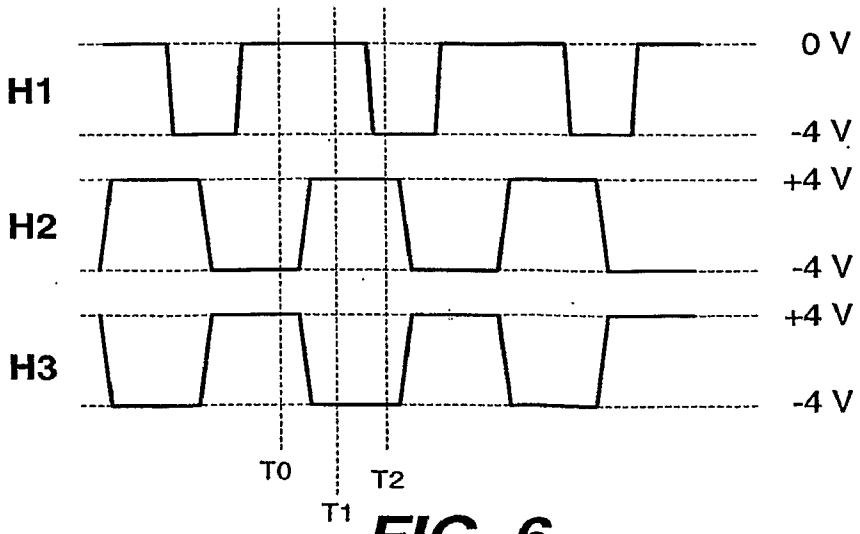


FIG. 6

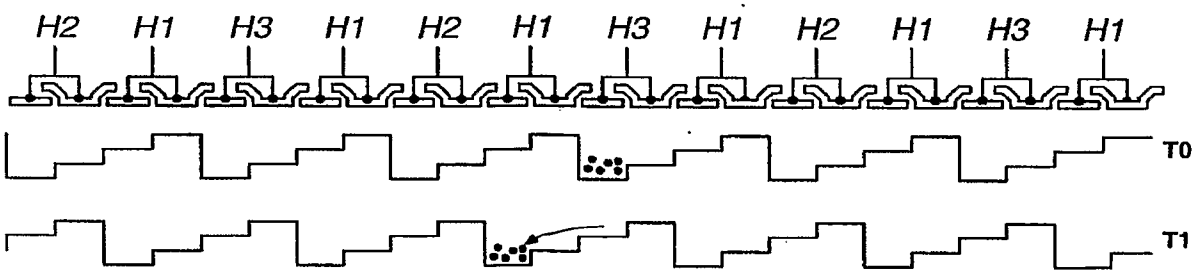


FIG. 7

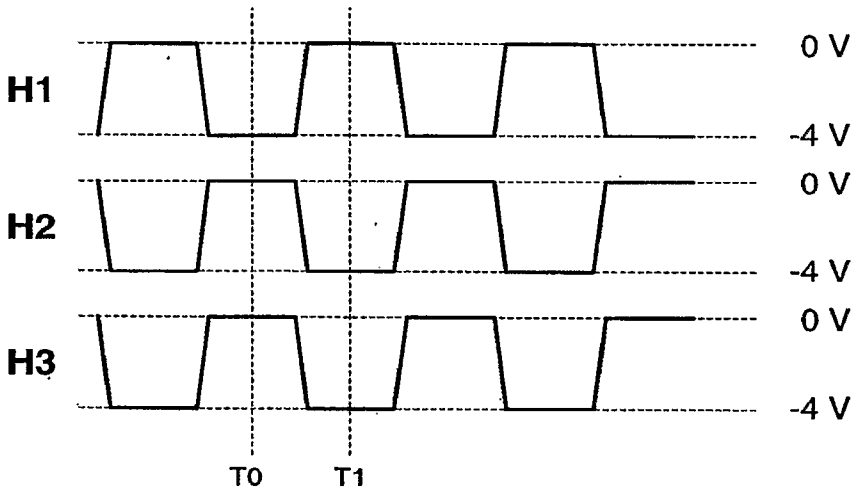


FIG. 8

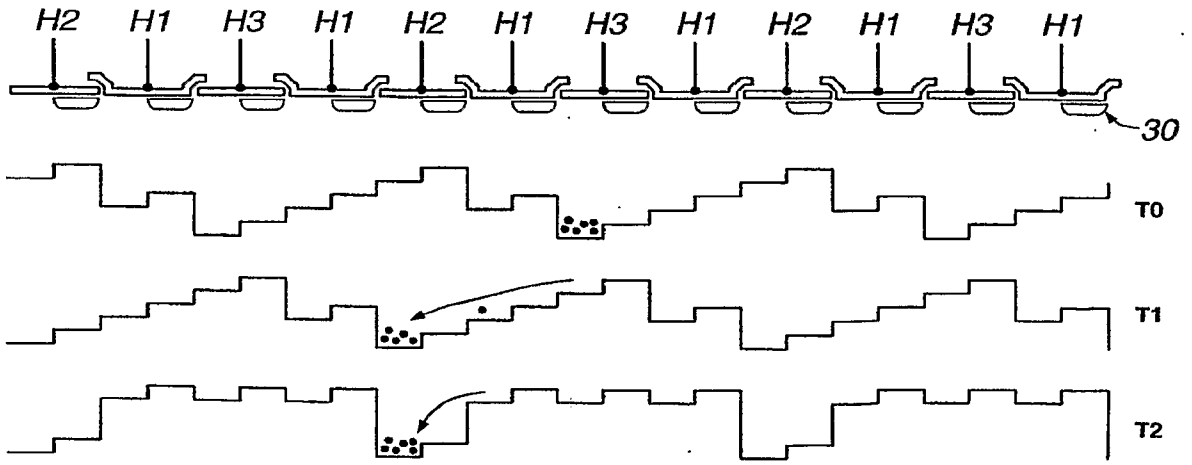


FIG. 9

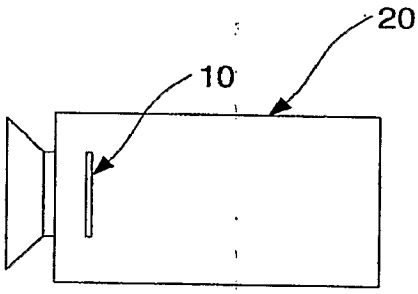


FIG. 10