

Sept. 6, 1966

E. A. CARACCILO

3,271,625

ELECTRONIC PACKAGE ASSEMBLY

Filed Dec. 9, 1963

Fig. 8

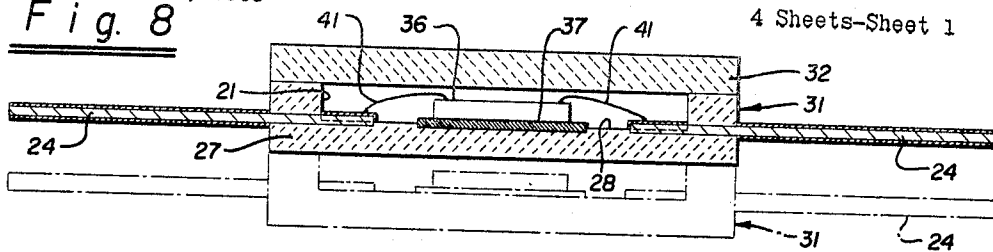


Fig. 9

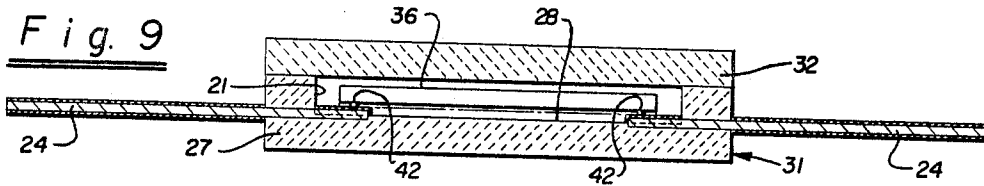


Fig. 10

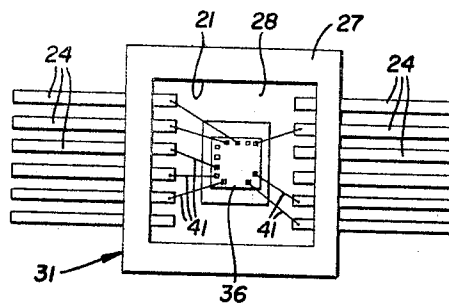
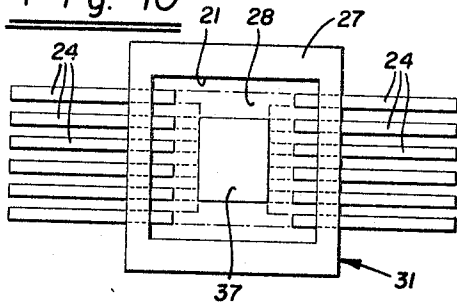


Fig. 12

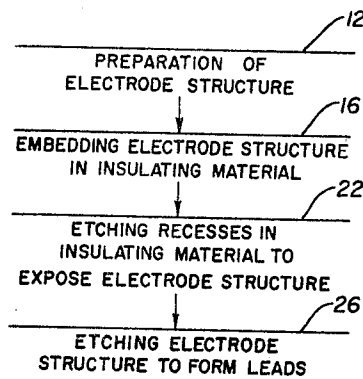


Fig. 1

INVENTOR

Edward A. Caracciolo

BY

Fleh & Swain

Attorneys

Sept. 6, 1966

E. A. CARACCILO
ELECTRONIC PACKAGE ASSEMBLY

3,271,625

Filed Dec. 9, 1963

4 Sheets-Sheet 2

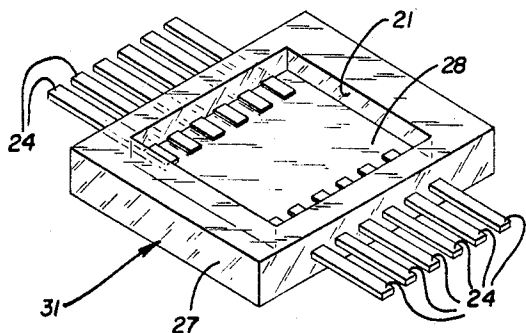


Fig. 2

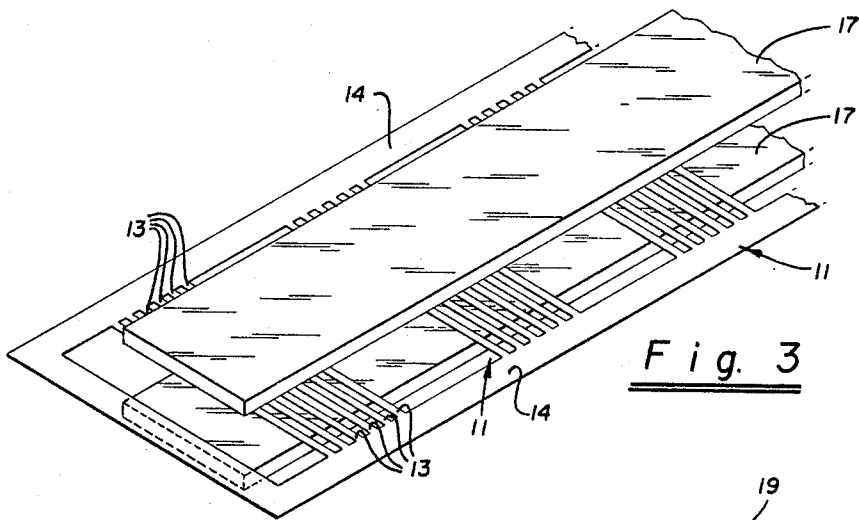


Fig. 3

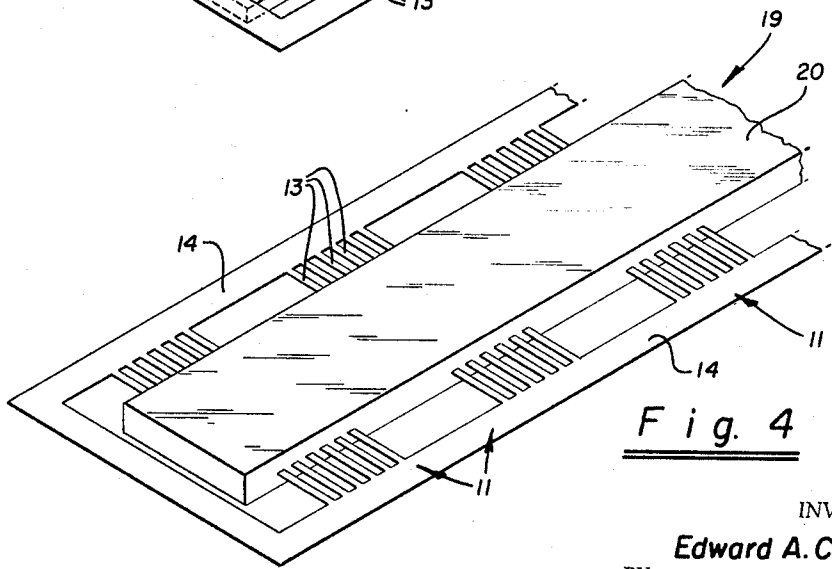


Fig. 4

INVENTOR.
Edward A. Caracciolo
BY *Fleh & Swain*
Attorneys

Sept. 6, 1966

E. A. CARACCIOLO

3,271,625

ELECTRONIC PACKAGE ASSEMBLY

Filed Dec. 9, 1963

4 Sheets-Sheet 3

Fig. 5

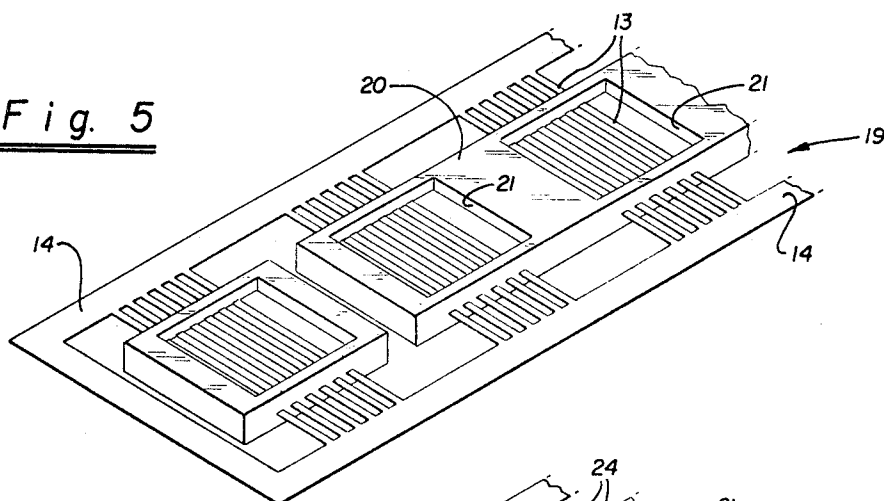


Fig. 6

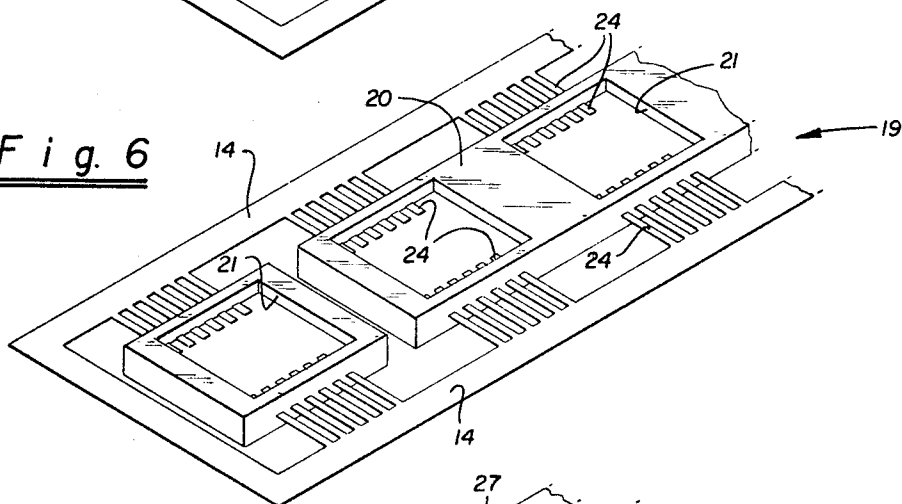
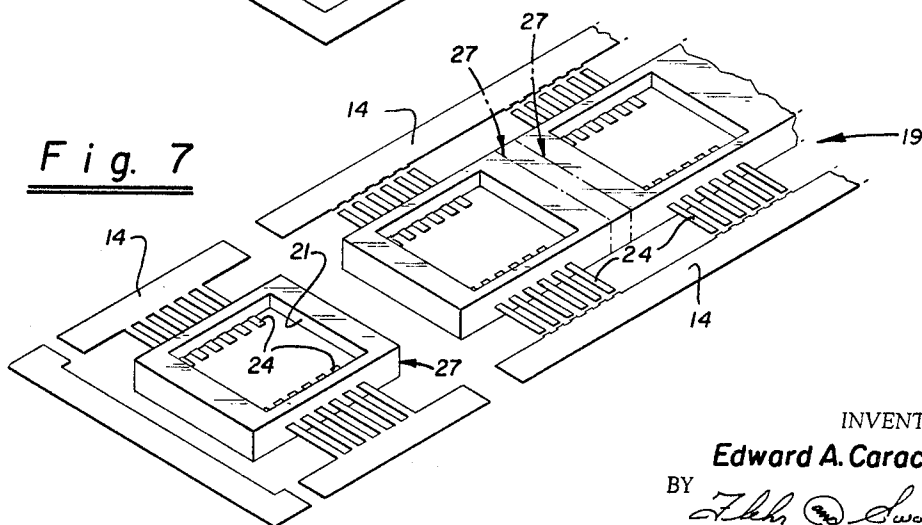


Fig. 7



INVENTOR

Edward A. Caracciolo

BY

John A. Swain

Attorneys

Sept. 6, 1966

E. A. CARACCILO
ELECTRONIC PACKAGE ASSEMBLY

3,271,625

Filed Dec. 9, 1963

4 Sheets-Sheet 4

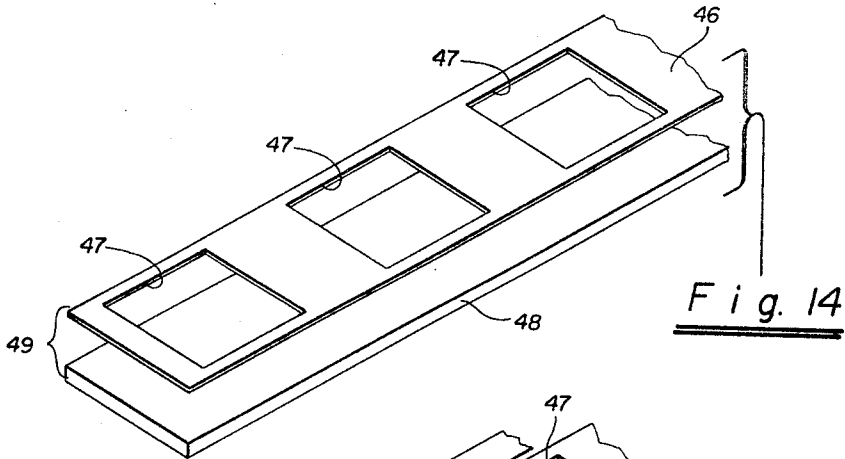


Fig. 14

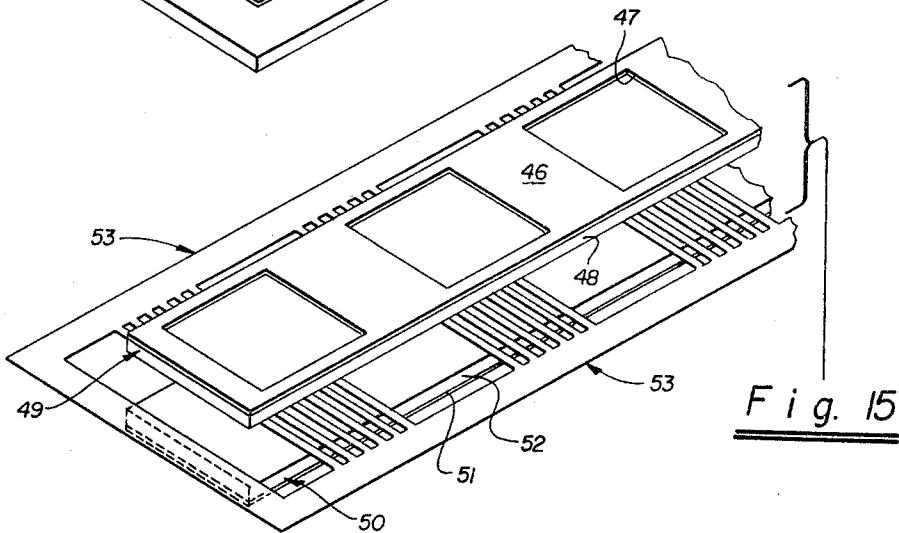


Fig. 15

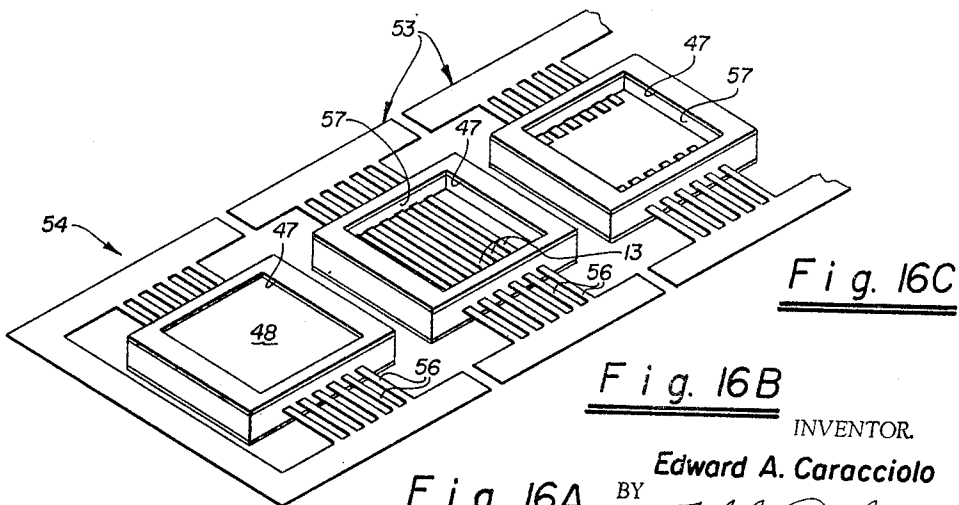


Fig. 16B

INVENTOR.

Edward A. Caracciolo

BY

John E. Swain

Attorneys

Fig. 16A

1

3,271,625

ELECTRONIC PACKAGE ASSEMBLY

Edward A. Caracciolo, Santa Clara, Calif., assignor to Signetics Corporation, Sunnyvale, Calif., a corporation of California

Filed Dec. 9, 1963, Ser. No. 329,190

1 Claim. (Cl. 317-101)

This application is a continuation-in-part of my earlier filed application Serial No. 213,912, filed August 1, 1962, now abandoned.

This invention relates to an electronic package assembly particularly adapted for semiconductor and miniature electronic devices.

At the present time, attempts are being made to provide packages for semiconductor devices and miniature electronic devices which have high mechanical and thermal shock reliability. One approach has been to take glass in a powder or frit form and forming the same into a type of package utilizing a suitable mold. However, this approach suffers from conventional handicaps of molded wares, that is, difficulty or impossibility of obtaining repetitive dimensional resolution. In addition, there are the problems of cyclic deterioration of the mold, mold release, and mold replacement costs. This technique or approach also encounters difficulties because in this process, a great number of particles are fused or sintered together to form the article with the inherent problems of interstitial gases, voids and impurities which seriously affect the quality of the article. There is, therefore, a need for a new and improved package for semiconductor and electronic devices and a method of manufacture for the same as well as an improved electronic assembly.

In general, it is an object of the present invention to provide an electronic assembly, package and method of manufacture which overcomes the above named disadvantages.

Another object of the invention is to provide an electronic assembly which is hermetically sealed and which has high mechanical and thermal shock reliability.

Another object of the invention is to provide a package of the above character which has great mechanical strength.

Another object of the invention is to provide a package of the above character in which a chemically inert material is utilized as a dielectric.

Another object of the invention is to provide a package which is homogeneous.

Another object of the invention is to provide a method of manufacture which utilizes chemical action rather than mechanical action for making the package.

Another object of the invention is to provide a method of the above character which can be readily and economically performed.

Another object of the invention is to provide a method of the above character in which multiple packages can be formed at the same time.

Additional objects and features of the invention will appear from the following description in which the preferred embodiments are set forth in detail in conjunction with the accompanying drawings.

Referring to the drawings:

FIGURE 1 is a chart showing my method for the manufacture of my package.

FIGURE 2 is an isometric view of the base portion of a package incorporating my invention.

FIGURE 3 is an isometric view showing an electrode structure disposed between two thin sheets of a dielectric material.

FIGURE 4 is an isometric view showing the assembly after the sheets have been bonded together with heat and pressure to provide a sandwich.

2

FIGURE 5 is an isometric view similar to FIGURE 4 showing recesses etched into the dielectric material to expose the internal electrode structure.

FIGURE 6 is an isometric view of the assembly shown in FIGURE 5 showing certain portions of the exposed electrodes etched away.

FIGURE 7 is an isometric view showing how the electrode structure and the dielectric sheets cut apart in blocks to provide separate packages.

FIGURE 8 is a side elevational view in cross-section of a semiconductor assembly incorporating my invention.

FIGURE 9 is a side elevational view in cross-section of another semiconductor assembly incorporating my invention.

FIGURE 10 is a plan view of another embodiment of my package with a centrally disposed pad.

FIGURE 11 is a plan view showing the electrode structure is masked to provide the pad.

FIGURE 12 is a plan view of the semiconductor assembly shown in FIGURE 8.

FIGURE 13 is a plan view of another embodiment of a semiconductor assembly incorporating my invention.

FIGURE 14 is an isometric view showing a sheet of conducting material ready to be bonded to a sheet of dielectric material.

FIGURE 15 is an exploded isometric view of a plurality of sheets of material ready to be bonded together into a unitary structure.

FIGURE 16A is an isometric view of a portion of the assembly shown in FIGURE 15 bonded together.

FIGURE 16B is an isometric view showing a portion of the dielectric material etched away to expose the leads.

FIGURE 16C is an isometric view showing certain portions of the leads etched away.

The method or process for making the package which is shown in FIGURE 2 is shown in FIGURES 3-7 and is set forth in the chart shown in FIGURE 1. As shown in FIGURE 1, an electrode structure 11 is first formed as indicated by step 12. The electrode structure can be formed in any suitable manner and of any suitable conducting material. However, for reasons hereinafter explained, material having certain thermal expansion characteristics or coefficient of expansion such as Kovar is utilized. A sheet of Kovar or other suitable metal is punched as shown in FIGURE 3 to provide a plurality of laterally extending spaced parallel strips 13 which are maintained in a predetermined spaced relationship by a remaining outer portion 14 of the sheet which extends around the entire perimeter of the electrode structure. Since the sheet shown in FIGURE 3 had a rectangular configuration, the outer remaining portion 14 also has a rectangular configuration. The invention may be practiced by forming only one group of strips at a time. However, in order to facilitate production and to make possible the production of a number of packages at the same time, the strips 13 are arranged in groups of six strips each with the spacing between each group being substantially greater than the spacing between the individual strips of the group.

After the electrode structure 11 has been punched, it is thoroughly cleaned in a suitable manner. For example, it can be immersed in a bath of acetic acid, nitric acid and hydrochloric acid with the following proportions:

	Milliliters
Acetic acid	750
Nitric acid	250
Hydrochloric acid	15

The electrode structure is retained in this bath for a suitable period of time such as 20 seconds with the bath having a room temperature or temperature of approxi-

mately 70° F. After the bath, the electrode structure is thoroughly rinsed in a suitable manner such as by use of an ultrasonic bath utilizing first tap water, then deionized water and then acetone in that order. The electrode structure is then passed through a stream of burning hydrogen gas and heated to a low redness for a period of approximately 5 seconds.

After preparation of the electrode structure 11 has been completed, the electrode structure is embedded in an insulating or dielectric material as shown in step 16 in FIGURE 1. As shown in FIGURES 3 and 4, this can be accomplished by placing the electrode structure 11 between a pair of rectangular sheets 17 of a suitable insulating or dielectric material such as #7052 glass (Corning Code) in such a manner that a sandwich is formed with the electrode structure 11 being disposed between the two sheets 17. The sheets 17 can have any desired thickness such as, for example, .040 inch. The sheets 17 also can be of any desired dimensions. However, as shown in FIGURES 3 and 4, the sheets should have a width which is substantially less than the length of the strips 13 provided in the electrode structure 11 so that the strips will extend beyond the side edges of the sheets.

The entire sandwich assembly is then fired in a suitable manner to form the same into a unitary assembly such as by placing the sandwich in a furnace and maintaining the furnace at a temperature of approximately 1650° F. for a period of approximately 7 minutes. The assembly 19 is then removed and annealed in a suitable manner such as for a period of 5 minutes at 950° F., after which it is cooled to room temperature. As can be seen from FIGURE 4, the two glass sheets 17 have been bonded together to provide a single glass sheet 20 with the electrode structure 11 embedded within the same.

After this has been completed, recesses 21 of a suitable configuration, such as the rectangular recesses shown in FIGURE 5, are formed in the insulating material as indicated by step 22 in FIGURE 1. These recesses are formed in a suitable manner such as by masking the upper surface of the sheet of insulating or dielectric material 20 with an etch-resistant material. The mask is so formed on the upper surface of the sheet of insulating material so that regions of the upper surface of the sheet 20 are exposed which generally overlie the groups of metal strips 13 embedded in the sheet 20.

A suitable etchant such as full strength hydrofluoric acid is then applied to the upper surface of the sheet 20 which selectively attacks the glass but does not attack the electrode structure 11. If desired, instead of just masking the upper surface of the sheet of insulating material 20, all the surfaces of the dielectric material 20 can be masked in a suitable manner so that the entire assembly may be placed in an etching bath. When this is done, the etchant can be utilized for peripheral shaping of the sheet 20.

With my invention, it is only desirable to etch the recesses 21 to a depth so that the strips 13 will be exposed within the recess. I have found that this is relatively easy to accomplish by taking advantage of the electro-conductivity of the hydrofluoric acid which is used for the etchant. By connecting an electrical circuit from the etchant to the electrode structure 11, it is possible to ascertain when the etchant has first etched away sufficient glass to come in contact with the strips 13 to establish an electrical contact. As soon as this initial circuit has been established, a time delay device is used in the circuitry so that the etching will continue for a sufficient period of time to expose all of the strips 13 and to take into account any small variances in depth of the strips 13 within the sheet 20. The electrical apparatus is then utilized to arrest any further etching action. Thus, a suitable buffer such as ammonium bifluoride can be added to the hydrofluoric acid to inhibit any further reaction. Thereafter, the circuitry can

actuate a mechanism to transfer the entire assembly 19 into a rinsing bath.

After the assembly or assemblies have been thoroughly washed, a mask is applied over the portions of the strips 13 within the recesses 21 to expose a centrally disposed rectangular area overlying the strips. A suitable etchant such as Kovar etch is then placed within the recesses to selectively attack the Kovar but which does not attack the glass to remove the central portion of each of the strips to form leads 24 as indicated by step 26. After the etching has been completed, the assembly is again rinsed and dried. Thereafter, the portions 14 are cut away as shown in FIGURE 7 to separate the other ends of the leads 24. The assembly 19 is then cut apart as also shown in FIGURE 7 to provide rectangular blocks 27 of insulating or dielectric material with centrally disposed recesses 21 with two sets of leads 24. This completes the manufacture of the base 31 of the package incorporating my invention.

As can be seen from FIGURE 2, this base 31 consists of the body 27 of insulating or dielectric material of a suitable configuration such as the rectangular configuration shown in FIGURE 2. This body is formed with a centrally disposed recess 21 which also has a suitable configuration such as the rectangular configuration shown in FIGURE 2. The recess is formed so that there is a relatively large planar bottom wall 28. The leads 24 are mounted in opposite side walls of the body and are permanently bonded therein. Portions of each of the leads 24 are disposed within the recess and are bonded in the bottom wall but have their upper surfaces exposed within the recess. In the arrangement shown, the leads are rectangular in cross-section and are arranged so that they all lie in the same horizontal plane. The leads on each side are also spaced so that they are parallel to each other. The leads have been formed of Kovar and Corning 7052 glass has been used so that the glass and the leads have substantially the same coefficient of expansion.

In utilizing the base 31 to form a package, a cover 32 of a suitable insulating or dielectric material and preferably the same insulating material which is utilized for the base is mounted on top of the base 31 as shown in FIGURE 8. The edge areas between the base 31 and the cover 32 are then subjected to heat and pressure to permanently bond the cover 32 to the base 31. If desired, this sealing operation can taken place within a vacuum chamber or within a chamber containing an inert atmosphere. At the same time that the heat and pressure are being applied to the side edges, means may be attached to the leads 24 to drain off any excess heat to thereby prevent damage to the electronic device 36 being encapsulated within the package.

If desired, the bases 31 can be stacked one above the other as also shown in FIGURE 8 and bonded together in a similar manner with the base of the unit above serving as a cover for the base below.

As is readily apparent to those skilled in the art, my package is such that it can be utilized for encapsulating miniature electronic devices and particularly semiconductor devices. Thus, as is preferable in the mounting of semiconductor devices, a metal pad 37 is mounted on the bottom wall 28 and is centrally disposed between the inner ends of the leads 24. This pad 37 may be placed in the base 31 after the leads have been formed in the manner hereinbefore described. However, alternatively, it can be formed with the leads by stamping an electrode structure 38 of the type shown in FIGURE 11 and then utilizing a suitable mask 39 and etchant to selectively remove the undersired metal from within the recess to provide a centrally disposed metal pad 37 which is securely bonded to the bottom wall 28 of the insulating body 27.

The semiconductor device 36 mounted on the base 31 can be of any suitable type, as for example, it can be an integrated circuit such as a NAND gate. Connections

between the circuitry of the device 36 and the inner ends of the leads 24 can be accomplished in any suitable manner such as by the use of gold wire which is bonded to the device 36 and to the leads 24 by suitable means such as thermocompression bonding as described in United States Patent No. 3,006,067 and as shown in FIGURES 8 and 12.

Alternatively, the pad 37 can be omitted and the semiconductor device can be inverted as shown in FIGURE 9. When the semiconductor device is inverted, the leads 24 and the portions of the electronic device to which connections are to be made are arranged so that they will overlies each other. Bonds can be formed between the leads 24 and the desired areas of the semiconductor device 36 by utilization of beads of a suitable material such as gold and then utilizing pressure and temperature to again form the thermocompression bonds between the leads 24 and the gold balls 42 and between the gold balls and the semiconductor device. In order to enhance the formation of good bonds, it may be desirable to first bathe the leads 24 in an electroless gold bath. In FIGURE 13, I have shown a different arrangement of electrodes or leads 24 in which the semiconductor device is bonded to the leads 24 in much the same way as shown in FIGURE 9.

It is apparent from the foregoing that I have provided a new and improved electronic assembly, package and method of manufacture for the package and the assembly. The leads are sealed in the insulating material which makes the leads easier to handle and also makes the entire package vibration resistant. The package is also constructed in such a way that the semiconductor devices or miniature electronic devices can be readily mounted within the same. The packages are also formed so that they can be readily stacked one above the other to thereby obtain a very high packing density.

If desired, the cover 32 can be eliminated and after the electrical connections between the semiconductor device and the leads 24 have been made, the recess 21 can be filled with a potting compound to provide a hermetically sealed device which is also vibration and shock resistant.

In describing the fabrication of the embodiment shown in FIGURES 2-7, I have disclosed that the recesses formed in the dielectric material can be formed in a suitable manner such as by masking the upper surface of the sheet of dielectric material with an etch-resistant material. Such etch-resistant material can be in the form of a tape consisting of a strip of Mylar coated on one side with a solvent-resistant adhesive. Such a tape is perforated to provide areas which correspond to the areas which it is desired be recessed. With the use of such tape, it is necessary that graphite or similar high temperature release material be utilized in the furnace during processing of the assembly. Such high temperature release materials are relatively expensive and tend to erode away during the repeated cycling of the furnace.

It is for this reason I have disclosed in FIGURES 14, 15, 16, 16A, 16B and 16C, an electronic assembly, package and method of manufacture which does not require the use of a mask of this type which must be removed. Thus, as shown in FIGURE 14, in place of a removable mask, I have provided a strip 46 of suitable conducting material such as Kovar which is pre-punched with an array of holes 47 which correspond to the areas which must be etched out to provide access to the leads as hereinafter described. After the strip 46 has been prepared, one side of the strip 46 is then coated with a suitable dielectric material such as No. 7052 glass (Corning Code). This can be accomplished in any number of ways. For example, as shown in FIGURE 14, a sheet 48 of this dielectric material of the same general dimensions as the strip 46 can be provided. This assembly can then be fired in a suitable manner so that the Kovar strip is firmly bonded to the glass sheet 48. This firing can be accomplished in the

manner hereinbefore described. Thereafter, the completed assembly 49 can be annealed in a suitable manner as hereinbefore described.

The Kovar strip 46 can also be provided with a covering of dielectric material on one side by covering one side with a suitable masking material and then dipping the strip into a slurry of powdered glass (No. 7052 glass or any other glass having similar physical characteristics in an aqueous suspension). If desired, two strips 46 can be dipped at the same time by utilizing double-faced adhesive tape and bonding two of the strips back to back. After the strips have been dipped in the slurry, they can be separated and fired and annealed in a manner hereinbefore described. Alternatively, both sides can be covered with the slurry and fired, after which the dielectric covering on one side of the sheet 46 can be etched away.

In FIGURE 15, another assembly 50 similar to assembly 49 is provided which consists of a strip 51 of conducting material such as Kovar which is bonded to a plate 52 of dielectric material such as No. 7052 glass (Corning). However, in this case, the conducting material 51 is not provided with apertures such as the strip 46. An electrode structure 53 substantially identical to the electrode structure 11 hereinbefore described is disposed between the assemblies 50 and 49. The assemblies 50 and 49 with the electrode structure 53 are then fired in a suitable manner and annealed as hereinbefore described to provide a unitary assembly.

A portion of the completed assembly 53 is shown in FIGURE 16A. Thereafter, a suitable etchant is applied to the upper surface of the sheet 48 as exposed by the openings 47 in the strip 46. As hereinbefore described, the etching operation is continued until the strips 56 lying in a plane are exposed within the opening 47 as shown in FIGURE 16B.

As hereinbefore described, a mask is then applied over portions of the strips 13 within the recess 57. Thereafter, a suitable etchant such as Kovar etch is placed in the recesses 57 to selectively attack the Kovar to remove the central portion of each of the strips to form separate leads in the manner hereinbefore described. The outer portions of the electrode structure 53 can then be removed as also hereinbefore described to provide base portions for a package which can be utilized as also hereinbefore described.

The primary difference between the base formed by the method shown in FIGURES 14-16 and the method shown in FIGURES 2-7 is that the bases formed by the method shown in FIGURES 14-16 are provided with a metal top and a metal back which serves as a conducting material. If neither of these is desired, they can be easily stripped away. The use of the metal strips 46 with the perforations is advantageous in performing the etching operation for forming the recesses 57 as hereinbefore described, but in addition they have the further advantage in that these strips of Kovar material serve as a release material built into the package itself. No graphite or similar furnace release material is required to remove it from the mold upon removal from the furnace. There is a further advantage in that the entire assembly can be processed more rapidly because as it comes from the furnace, it can be dropped directly into the etchant which removes the glass exposed by the openings 47.

In many practical applications, the metal conducting tops and backs have advantages. For example, the metal top can be used as a common connector for a number of leads, or it can serve as a ground. Similarly, the metal back can be used as a heat sink for the package. The metal back may also make it easier to affix the package to the assembly of which it is to form a part as, for example, the metal back can be directly soldered to a chassis or framework containing other electronic components. Where photosensitive devices are utilized, the metal back may also be advantageous because it is opaque.

I claim:

In an electronic package assembly adapted to receive a semiconductor device having contact areas, a body, a plurality of conducting metallic leads having inner and outer end portions, the inner end portions of the leads being embedded in the body and having exposed upper surfaces, the outer end portions of the leads extending outwardly away from the body and being free of the body, portions of the leads intermediate the inner and outer end portions being surrounded on all sides by the body, at least the portion of the body in contact with and surrounding the leads being formed of a material having a coefficient of expansion which is substantially identical to that of the leads and serving to electrically insulate the leads from each other, all portions of said leads in said body being in physical contact with and supported by said body, the exposed upper surfaces of the inner portions of the leads lying in a substantially common plane and being disposed in a predetermined pattern adjacent the perimeter of the body, a substantially planar metal conducting pad mounted on the body in a generally central position and being out of contact with at least certain of the exposed upper surfaces of the inner end portions of the leads, said body being adapted to receive the semiconductor device so that the semiconductor device can be mounted directly upon the pad and so that the contact areas of the semiconductor device can be connected to the upper exposed surfaces of the inner portions of the leads, cover means mounted on said body and means forming a hermetic seal between the cover means and the body so that a semiconductor device mounted in the body is hermetically sealed therein, said body having a substantially planar outer surface and said cover means having a sub-

stantially planar outer surface parallel to the outer surface of the body to permit one package to be stacked with another package with surfaces in juxtaposition.

References Cited by the Examiner

UNITED STATES PATENTS

2,934,814	4/1960	Williams	29—155.5
2,994,121	8/1961	Shockley	317—235 X
3,029,368	4/1962	Wulc	317—101
3,029,495	4/1962	Doctor	317—101
3,040,213	6/1962	Byer et al.	317—101
3,081,525	3/1963	Delbove	29—155.5
3,118,016	1/1964	Stéphanson	317—101 X
3,179,854	4/1965	Luedicke et al.	317—101
3,184,831	5/1965	Seibertz	317—101

FOREIGN PATENTS

19,919 11/1893 Great Britain.

References Cited by the Applicant

UNITED STATES PATENTS

2,875,387	2/1959	Randels.
2,905,744	9/1959	Rayburn.
3,072,832	1/1963	Kilby.
3,006,067	10/1961	Anderson et al.

FOREIGN PATENTS

19,919 11/1893 Great Britain.

ROBERT K. SCHAEFER, *Primary Examiner.*

KATHLEEN H. CLAFFY, *Examiner.*

H. J. RICHMAN, W. C. GARVERT,

Assistant Examiners.