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(71) Applicant: **MASSACHUSETTS INSTITUTE OF TECHNOLOGY** [US/US]; 77 Massachusetts Avenue, Cambridge, MA 02139 (US).

(72) Inventors; and

(71) Applicants *(for US only)*: **SHULAKER, Max** [US/US]; 162 Brookline St, Cambridge, MA 02139 (US). **SRIMANI, Tathagata** [US/US]; 77 Massachusetts Ave., Cambridge, MA 02139 (US). **FULLER, Samuel** [US/US]; 77 Massachusetts Ave., Cambridge, MA 02139 (US). **STEIN, Yosi** [US/US]; One Technology Way, Norwood, MA 02062 (US). **MURPHY, Denis** [US/US]; One Technology Way, Norwood, MA 02062 (US).

(74) Agent: **COLICE, Christopher Max** et al.; Smith Baluch LLP, 376 Boylston St., Suite 401, Boston, MA 02116 (US).

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(54) **Title:** BACK-GATE FIELD-EFFECT TRANSISTORS AND METHODS FOR MAKING THE SAME

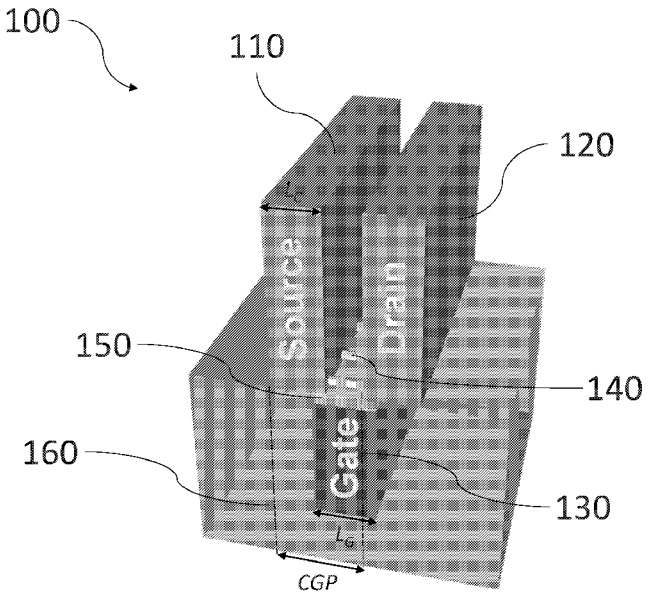


FIG. 2B

(57) **Abstract:** A back-gate carbon nanotube field effect transistor (CNFETs) provides: (1) reduced parasitic capacitance, which decreases the energy-delay product (EDP) thus improving the energy efficiency of digital systems (e.g., very-large-scale integrated circuits) and (2) scaling of transistors to smaller technology nodes (e.g., sub-3 nm nodes). An exemplary back-gate CNFET includes a channel. A source and a drain are disposed on a first side of the channel. A gate is disposed on a second side of the channel opposite to the first side. In this manner, the contacted gate pitch (CGP) of the back-gate CNFET may be scaled down without scaling the physical gate length ($L_G$) or contact length ($L_C$). The gate may also overlap with the source and/or the drain in this architecture. In one example, an exemplary CNFET was demonstrated to have a CGP less than 30 nm and 1.6x improvement to EDP compared to top-gate CNFETs.

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*[Continued on next page]*

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# BACK-GATE FIELD-EFFECT TRANSISTORS AND METHODS FOR MAKING THE SAME

## CROSS-REFERENCE TO RELATED PATENT APPLICATION

**[0001]** This application claims priority, under 35 U.S.C. § 119(e), to U.S. Application No. 62/623,277, filed on January 29, 2018, entitled "BACK-GATE CARBON NANOTUBE FIELD-EFFECT TRANSISTORS", which is incorporated herein by reference in its entirety.

## BACKGROUND

**[0002]** The development of progressively smaller transistor technology nodes has led to increasing technical and economical challenges. In particular, a roadmap towards scaling transistors beyond sub-3 nm technology nodes remains elusive given present manufacturing capabilities. For instance, if the contacted gate pitch (CGP) scales at its historical pace as dictated by Moore's Law, the shrinking of the physical spacing between the metal gate and the metal source/drain of the field effect transistor (FET) (i.e., the spacer thickness) results in increased parasitic capacitances, degrading potential energy delay product (EDP) benefits.

**[0003]** This is driving the search for beyond-silicon emerging nanotechnologies to supplement silicon CMOS. For instance, carbon nanotubes (CNTs) can be used to form carbon nanotube field effect transistors (CNFETs), whereby multiple CNTs in parallel comprise the channel of the FET with lithographically defined source, drain, and gate regions. It is projected that digital very-large-scale integrated (VLSI) circuits fabricated from CNFETs can achieve an order of magnitude improvement in EDP vs. silicon complementary metal oxide semiconductor (CMOS).

## SUMMARY

**[0004]** The development of new transistor architectures that utilize nanomaterials as a substitute for silicon is one promising approach to scale transistors to progressively smaller technology nodes without increasing the EDP or raising costs of manufacture in an unsustainable manner. The present disclosure is thus directed to various back-gate field effect transistors (FET) and methods for making the back-gate FETs, which can be scaled down to sub-3 nm technology nodes with lower EDP than conventional top-gate and gate-all-around (GAA) FETs at the same CGP. The design architecture of the back-gate FETs described herein may be used to substantially reduce the

CGP, which is a key metric defining the area of a FET and consequently the technology node. In one exemplary design, carbon nanotubes (CNTs) are used as the channel to form a back-gate carbon nanotube field effect transistor (CNFET) with a CGP of about 30 nm. Multiple CNFETs may then be assembled to form a CNFET digital logic circuit. Such CNFETs may (1) improve the energy efficiency (i.e., the energy delay product EDP) of digital VLSI circuits as well as provide an approach to scale CGP digital logic to smaller technology nodes (e.g., sub-3 nm technology nodes).

**[0005]** These CNFETs may take the form of a transistor comprising a channel, a source, a drain, and a gate. The channel has a first side and a second side opposite the first side, with the source disposed on the first side of the channel. The drain is disposed on the first side of the channel and spaced apart from the source by a physical channel length of less than about 10 nm. And the gate is disposed on the second side of the channel and has a gate length greater than the physical channel length. This transistor may have a contacted gate pitch of 30 nm or less and a parasitic capacitance of less than 0.1 femtofarads/micron.

**[0006]** Another inventive transistor also includes a channel, a source, a drain, and a gate. Again, the channel has a first side and a second side opposite the first side, with the source and the drain on the first side of the channel. The gate is disposed on the second side of the channel and overlaps with the source, the drain, or both the source and the drain. This transistor has a contacted gate pitch of 30 nm or less.

**[0007]** In these transistors, the channel may include a (carbon) nanotube in electrical communication with the source and the drain, in which case there may be a dielectric disposed between the gate and the nanotube. The gate may overlap with the source, the drain, or the source and the drain. And the transistor may be configured to operate at a clock frequency ranging between about 0.1 GHz and about 10 GHz.

**[0008]** These transistors can be made by forming a gate, depositing a dielectric on the gate, depositing a carbon nanotube over the dielectric to form a channel, and patterning a source and a drain on the channel opposite the gate with a physical channel length less than a length of the gate and less than about 10 nm. Depositing the carbon nanotube may occur at a temperature of less than about 400 °C. Patterning the source and the drain may involve lithographically etching with physical channel length at a minimum feature size and/or overlapping the source, the drain, or both

the source and the drain with the gate. Before forming the gate, a trench may be patterned into a substrate such that the gate, when formed, is embedded in the substrate.

**[0009]** All combinations of the foregoing concepts and additional concepts discussed in greater detail below (provided such concepts are not mutually inconsistent) are contemplated as being part of the inventive subject matter disclosed herein. In particular, all combinations of claimed subject matter appearing at the end of this disclosure are contemplated as being part of the inventive subject matter disclosed herein. Terminology explicitly employed herein that also may appear in any disclosure incorporated by reference should be accorded a meaning most consistent with the particular concepts disclosed herein.

## BRIEF DESCRIPTION OF DRAWINGS

**[0010]** The skilled artisan will understand that the drawings primarily are for illustrative purposes and are not intended to limit the scope of the inventive subject matter described herein. The drawings are not necessarily to scale; in some instances, various aspects of the inventive subject matter disclosed herein may be shown exaggerated or enlarged in the drawings to facilitate an understanding of different features. In the drawings, like reference characters generally refer to like features (e.g., functionally similar and/or structurally similar elements).

**[0011]** FIG. 1A shows a FET with a top-gate FET geometry.

**[0012]** FIG. 1B shows a FET with a gate-all-around FET geometry.

**[0013]** FIG. 2A shows an exemplary FET where CNTs are used as the FET channel in a back-gate FET geometry with a negative spacer length, $L_{SP}$.

**[0014]** FIG. 2B shows an exemplary FET where CNTs are used as the FET channel in a back-gate FET geometry.

**[0015]** FIG. 3 shows a process flow diagram of a back-gate CNFET. While back-gates are not embedded within the substrate, a conventional damascene process may be used to reduce parasitics for back-gate FET geometries. E-beam photoresist thickness (< 40 nm) limits the metal thickness in this experimental demonstration to <10 nm.

**[0016]** FIG. 4 shows three-dimensional schematics of the back-gate CNFET based on the process flow diagram of FIG. 3 with corresponding scanning electron microscopy(SEM) images of the back-gate CNFET.

**[0017]** FIG. 5A shows a top view of a probe pad layout for a CNFET digital logic (inverter).

**[0018]** FIG. 5B shows a magnified view of a typical CNFET inverter. Note the image shows an inverter before the pads in FIG. 4 are deposited, since the pads cover some of these features.

**[0019]** FIG. 5C shows a magnified view of a typical 30 nm CGP back-gate CNFET in the CNFET inverter shown in FIG. 5B.

**[0020]** FIG. 5D shows a magnified view of the CNFET channel region. The contact length, $L_C$, is 20 nm and the physical channel length, $L_{CH}$, is 10 nm, resulting in a 30 nm CGP. The gate length, $L_G$, is 18 nm, and overlaps both with the source (left contact) and drain (right contact) by ~4 nm.

**[0021]** FIG. 5E shows a cross-sectional transmission electron microscopy image of a back-gate CNFET with nominal 30 nm CGP.

**[0022]** FIG. 6A shows the $I_D$-$V_{GS}$ characteristics of multiple 30 nm CGP CNFETs, achieving subthreshold-swings (SS) of ~125 mV/dec (at a drain-source voltage $V_{DS}$=-0.5V).

**[0023]** FIG. 6B shows the $I_D$-$V_{DS}$ characteristic of an exemplary 30 nm CGP CNFET.

**[0024]** FIG. 6C shows the voltage transfer curve of a 30 nm CGP CNFET inverter, implemented using depletion load PMOS logic with an output high voltage $V_{OH}$ = 0.4V and an output low votlage $V_{OL}$= 0.05V, respectively.

**[0025]** FIG. 7 shows a chart comparing the current work with respect to contacted gate pitch across best reported scaled technologies in the literature.

**[0026]** FIG. 8A shows the parasitic capacitances (gate-to-plug capacitance, $C_{GTP}$ in FIGS. 1A-1E) for back-gate vs. top-gate and gate-all-around (GAA) FET. Back-gate FETs reduces parasitics by >2.5× vs. top-gate FETs and by >2.8× vs. GAA FETs for a 30 nm CGP (suitable for a sub-3 nm node). Benefits of parasitic reduction increases as CGP scales. Intrinsic parasitics are determined using TCAD Sentaurus (Synopsys) and verified using COMSOL Multiphysics (COMSOL, Inc.) (with a discrepancy of <0.3% across all simulations).

**[0027]** FIG. 8B shows a table of the device parameters used for analysis. CGP values of 30 nm, 42 nm, 90 nm, and 180 nm correspond to 3 nm, 7 nm, 22 nm, and 45 nm technology nodes, respectively.

**[0028]** FIG. 9A shows a perspective view of a back-gate CNFET, with labelled parasitic components.

**[0029]** FIG. 9B shows different components of input capacitance for a highly scaled 30 nm CGP back-gate CNFET (see device parameters in FIG. 8B).

**[0030]** FIG. 10 shows the optimized EDP (normalized with respect to the optimized EDP for the GAA CNFET for each module) across modules from the OpenSparc T2 core and a 32-bit commercial processor core. Average EDP benefit of back-gate vs. GAA is 2.18×, and 1.6× vs. top-gate. All simulations were done with respect to a 30nm CGP device with parameters listed in FIG. 8B. EDP benefits are maintained even with low-k spacers (e.g., with a k=4.4 spacer) with EDP benefits decreasing by <10% ( from the "dec" module of OpenSparcT2). Moreover, for many existing standard cell libraries, the same physical layouts can be used for FETs with back-gate geometries without any adjustments to the locations of FETs or to the metal routing within standard library cells (specifically for standard cell layouts in which vias to contact FET gates are located outside of the active region of the FETs).

**[0031]** FIG. 11 shows the total energy vs. frequency of the 32-bit commercial processor core, showing the pareto-optimal EDP trade-off curves for back-gate, top-gate, and GAA CNFETs. FIG. 10 shows values extracted from these EDP trade-off curves.

**[0032]** FIG. 12 shows the EDP benefits resulting from reduced parasitics outweigh potential gains stemming from improved electrostatic control for GAA geometries. Subthreshold swing (SS) can degrade by > 58% (resulting in SS = 100 mV/dec), while still maintaining the EDP benefits compared to GAA CNFETs with an assumed preferred SS approaching 60 mV/dec. Importantly, experimental demonstrations of CNFETs with $L_{CH}$ = 9nm have leveraged back-gate geometries and reported a SS better than 100 mV/dec (94 mV/dec), highlighting feasibility of this approach.

**[0033]** FIG. 13A shows a chart of the parasitic capacitance ($C_{GTP}$) as a function of the spacer length $L_{SP}$ for a top-gate FET and back-gate FETs with a 5 nm, a 3 nm, and a 1.5 nm overlap between the gate and source/drain. The chart indicates how the back-gate FET geometry may be used to realize a 15 nm CGP. Even with overlap, back-gates yield >3× reduced parasitic capacitances at scaled nodes.

**[0034]** FIG. 13B shows a table with device parameters used for extracting capacitances in FIG. 13A.

**[0035]** FIG. 14 shows a comparison of relative EDP of a fan-out 4 (FO-4) inverter (normalized to EDP of CGP 30nm top-gate CNFET) versus CGP of back-gate CNFETs. These devices have a contact length $L_c$ of 9 nm and a gate length $L_g$ of 9 nm. The spacer length $L_{SP}$ is varied to reduce CGP.

## DETAILED DESCRIPTION

**[0036]** FIG. 1A shows a schematic of a top-gate CNFET 80. The top-gate CNFET 80 includes a channel 40. A source 10 and a drain 20 are disposed on a first side of the channel 40 such that electric current flows from the source 10 to the drain 20 through the channel 40. A gate 30 disposed on the first side of the channel 40 between the source 10 and the drain 20 controls the flow of current through the channel 40. A dielectric 50 may be disposed between the gate 30 and the channel 40. A substrate 60 may provide mechanical support for manufacture and handling.

**[0037]** FIG. 1B shows a schematic of a gate-all-around (GAA) CNFET 90. Similar to the top-gate CNFET 80, the GAA CNFET 90 includes a source 10, a drain 20, and a channel 42 disposed on a first side of the channel 42. In this case, a gate 32 surrounds the channel 42 on all sides. As shown in FIG. 1B, the gate 32 is between the source 10 and the drain 20. A dielectric 52 may also be disposed between the channel 40 and the gate 30. Once again, a substrate 62 may provide mechanical support for manufacture and handling.

**[0038]** Generally, the size of the transistor and, hence, the corresponding technology node may be quantified using a contacted gate pitch (CGP). The CGP may be defined as equal to the gate pitch between two FETs 100 connected in series with a shared source 110/drain 120 contact. For the top-gate CNFET 80 and the GAA CNFET 90, the CGP is thus equal to the sum of the source 110/drain 120 contact length ($L_C$), the physical gate length ($L_G$) of the gate 130, and the two spacer regions ($2L_{SP}$) that separate the gate 130 from the source 110/drain 120:

$$\mathrm{CGP} = L_C + L_G + 2L_{SP} \quad (1)$$

This CGP is illustrated in FIG. 1A.

**[0039]** A physical channel length ($L_{CH}$), may also be defined using the above parameters as follows,

$$L_{CH} = \mathrm{CGP} - L_C \quad (2)$$

**[0040]** For comparison, FIGS. 2A and 2B show a schematic of an exemplary back-gate CNFET 100. CNFETs have previously used both a back-gate FET geometry and sophisticated FET geometries (such as GAA CNFETs). However, a rigorous analysis of the relative benefits (e.g., both energy efficiency and area scaling) of these sophisticated geometries compared to back-gate FET geometries was not performed. Here, back-gate FET geometries are shown to provide several benefits that have not been exploited for highly scaled technologies. For example, back-gate FETs enable physical scaling beyond the limits of both top-gate and gate-all-around FET geometries.

Back-gate FETs also provide additional EDP benefits owing to a reduction in parasitic capacitances compared to top-gate and GAA FETs.

**[0041]** The back-gate CNFET 102 in FIG. 2A includes a channel 142 that allows electric current to flow from a source 110 to a drain 120. As shown, the source 110 and the drain 120 may be disposed on a first side of the channel 142. The back-gate FET 100 also includes a gate 132 to control the flow of current with application of a voltage. The gate 132 may be disposed on a second side of the channel 142 opposite to the first side of the channel 142, hence the back-gate geometry. The gate 132 may be embedded in a substrate 162 that supports the back-gate FET 100. A dielectric 152 may also be disposed between the gate 132 and the channel 142.

**[0042]** Compared to the top-gate CNFET 80 and the GAA CNFET 90, the back-gate CNFET 102 in FIG. 2A can support a shorter CGP to enable more highly-scaled technology nodes. For instance, the spacer regions, which are used to avoid unwanted electrical contact (electrical shorts) between the gate 132 and the source 110/drain 120 are not necessary for the back-gate FET 100 since the back-gate 132 is on a plane beneath the source 110/drain 120. Therefore, the spacer regions may be eliminated entirely, thus enabling a smaller CGP and a physical channel length, $L_{CH}$, in transistors that would otherwise be constrained by design and/or fabrication limitations. For example, foundries typically impose a minimum feature size for a device layer as defined by the foundry's process development kit, which constrains conventional top-gate FETs and GAA FETs due to the need for the aforementioned spacer regions. And lithographical processes have resolution limitations that constrain the dimensions and relative spacing between features in the transistor. In both examples, the removal of the spacer regions allows the source 110 and the drain 120 to be positioned more closely resulting in a smaller $L_{CH}$.

**[0043]** For the back-gate FET 102, parasitic capacitances between the gate 132 and the source 110 and the gate 132 and the drain 120 may also be reduced, in part, by the reduced electrical coupling between the gate 132 and the source 110/drain 120 in the back-gate architecture. For example, the back-gate FET 100 may exhibit a total parasitic capacitance (gate-to-plug capacitance) less than about 0.1 femtofarads/micron.

**[0044]** Some back-gate CNFETs, including the back-gate CNFET 100 shown FIG. 2B, have a gate 130 that partially overlaps with the source 110 and/or the drain 120 while maintaining parasitic capacitances less than a corresponding top-gate or GAA FET at the same CGP. For designs having an overlap, a channel 140 and/or a dielectric 150 may be used to separate the gate 130 from the

source 110/drain 120. This overlapping gate 130 may be supported by or embedded in a substrate 160, e.g., for mechanical stability and support.

**[0045]** FIG. 2B shows an exemplary back-gate FET 100 with an overlap between the gate 130 and the source 110/drain 120. Such an overlap corresponds to a spacer length $L_{SP} < 0$ in Eq. 1. In this manner, the CGP can be reduced by decreasing $L_{SP}$ (e.g., below zero) – even without improving fabrication techniques to scale $L_C$ and $L_G$ to smaller dimensions.

**[0046]** In general, the back-gate FET 100 in FIG. 2B may have a CGP less than about 30 nm. The back-gate FET 100 may also have a $L_{CH}$ less than about 10 nm. The CGP and $L_{CH}$ may vary by +/- 1-5 nm due, in part, to variability and tolerances in fabrication. An overlap between the gate 130 and the source 110/drain 120 may be used to enable such reductions in CGP and $L_{CH}$, particularly given present limitations in fabrication. Future improvements in fabrication processes may also enable reductions in CGP and $L_{CH}$ without an overlap between the gate 130 and the source 110/drain 120.

**[0047]** As described below, the manufacture of the back-gate FET 100 may involve modifications to the process flow conventionally used for top-gate FETs or GAA FETs due, in part, to temperature considerations and material compatibility. Such modifications may include use of different materials/structures for the channel 140. For example, the channel 140 may be formed of one or more CNTs, which may be deposited at temperatures below 400 °C to avoid damaging the gate 130. As shown in FIG. 2B, several CNTs may be used as the channel 140 in order to support a higher electric current.

**[0048]** The dielectric 150 may be formed from various high-κ dielectrics including, but not limited to, silicon oxide, hafnium oxide, or any other dielectrics known to one of ordinary skill in the art. The source 110 and the drain 120 may be formed from various electrical conducting materials including, but not limited to, platinum, titanium, tungsten, tantalum, copper, any alloys of the foregoing, or any electrical conductors known to one of ordinary skill in the art. The substrate 160 may be in the form of wafer formed from various materials including, but not limited to, silicon, silicon oxide, aluminum nitride, or any other semiconductor or insulating materials known to one of ordinary skill in the art.

**[0049] CNFETS & CNFET Digital Logic with a Back-Gate Geometry having a CGP less than 30 nm**

**[0050]** The realization of the scaling benefits enabled by the back-gate FET 100 may involve some modifications to the front-end-of-line (FEOL) FET fabrication for conventional silicon-based technologies. As illustrated in FIGS. 3 and 4, the FET gate stack (e.g., gate 132 in FIG. 2A or gate 130 in FIG. 2B) is initially fabricated on the substrate. Subsequently, the semiconducting channel 140 of the FET 100 is deposited over this gate stack 130. To avoid damaging the gate stack 130 (*e.g.*, by crystallizing the high-*k* gate dielectric 150 or destroying the embedded metal gate 130), the channel 140 deposition – and all subsequent FEOL processing - should preferably be performed at low temperatures (*e.g.*, < 400 °C). This may be particularly challenging for silicon-based technologies, which use processing temperatures >1000 °C. In contrast, many emerging nanotechnologies use low processing temperatures (<400 °C), and thus naturally enable back-gate FET geometries. As a demonstration, CNTs may be used because CNTs may be deposited above the gate stack 130 at room temperature (*e.g.*, through solution-based processing or a transfer process). Additionally, CNFETs may also improve the EDP for digital VLSI circuits by an order of magnitude compared to silicon FETs.

**[0051] Fabrication**

**[0052]** As an exemplary experimental demonstration, back-gate CNFETs 100 and CNFET digital logic were fabricated that exhibit a record scaled CGP of 30 nm. The fabrication flow for a back-gate CNFET 100 is shown in FIG. 3 and described as follows: (1) the starting substrate for the 30 nm CGP CNFETs 100 is a silicon substrate, (2) the silicon substrate is coated with a 800 nm thermal oxide, and (3) the gate 130 is patterned on the wafer 160 by first coating the wafer 160 with a single layer of PMMA positive resist (~45 nm PMMA A1). Electron-beam (e-beam) lithography is used to define the gate electrode ($L_G$ ~18 nm). PMMA is then developed at -3.5 °C forming the pattern. Electron beam (e-beam) evaporation is used to deposit 3 Å of titanium followed by 4 nm of platinum. A lift-off process is then performed. The preferred area dose for e-beam lithography is chosen, in part, by simulating the electron back-scattering effects in a stack of PMMA-$SiO_2$ and PMMA-$HfO_2$ in TRACER. This is followed by (4) deposition of a 3.5 nm thick $HfO_2$ dielectric 150 having an equivalent oxide thickness (EOT) of 0.9 nm using atomic layer deposition.

**[0053]** While the back-gates 130 are not embedded within the substrate 160, a conventional damascene process may be used to realize an embedded gate stack 130 in order to achieve the reduced parasitics afforded by back-gate FET geometries. For example, the substrate 160 may

initially be patterned and etched to form a trench or recess along the surface of the substrate 160. Subsequent deposition of the materials used in the gate 130 (and the dielectric 150) may then fill the trench or recess in the substrate 160. A polishing process (e.g., chemical mechanical polishing) may then be used to remove excess gate material and/or to planarize the substrate 160 and gate 130 before subsequent fabrication processes are performed.

**[0054]** Following gate-stack 130 fabrication, PMMA and e-beam lithography are again used to pattern contact holes to the gate metal electrodes, and a dry $Cl_2$-based plasma etch is used to etch through the $HfO_2$. The PMMA is stripped in hot acetone followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface is functionalized with hexamethyldisilazane (HMDS, a common photoresist adhesion promoter). The wafer 160 is then submerged in a solution of 1,2-dichloroethane (DCE) containing >99.9% pure semiconducting CNTs (modified IsoNanotubes-S supplied by Nanointegris) for 10 minutes.

**[0055]** This is followed by (5) dispersing CNTs in DCE. The CNTs go through several sonication steps to wrap the CNTs in a polymer to disperse them within the DCE, followed by several ultracentrifugation steps to remove non-dispersed CNTs and excess polymer. Following CNT deposition, the wafer 160 is rinsed in hot toluene for 60 minutes, followed by vacuum annealing at $<10^{-5}$ Torr for >30 minutes.

**[0056]** Next, (6) the source 110 and (7) the drain 120 are defined and patterned similar to the gate electrode. The source 110 and the drain 120 are patterned in two separate steps in order to decrease the minimum resolution. (8) After deposition of the CNT channel 140, PMMA is patterned to cover the transistor channel regions 140, and oxygen plasma is used to remove excess CNTs (i.e., CNTs outside of the transistor channel region 140, and therefore not protected by the PMMA). This is followed by (9) an e-beam lithography step, e-beam evaporation, and lift-off to define larger probe pads and interconnect wires.

**[0057]** The fabrication process flow described above is one exemplary process that may be used to form back-gate CNFETs 100. The various processes, parameters, and materials used may be modified or removed depending on the design of the back-gate FET 100. Additional processing steps may also be introduced, such as additional patterning and etching steps for embedding the gate 130 into the substrate 160 as described above.

**[0058] Experimental Results**

**[0059]** To achieve CNFETs 100 that fit within a CGP of 30 nm, the exemplary CNFETs 100 were patterned with $L_C$ = 20 nm, $L_G$ = 18 nm, $L_{SP}$ = -4 nm (*i.e.*, 4 nm intentional overlap of the back-gate 130 with the source 110 and the drain 120), with a physical channel length ($L_{CH}$ = CGP – $L_C$) of 10 nm. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of the fabricated CNFETs 100 are shown in FIG. 5A-5E. Importantly, this scaled CGP is achieved without additional scaling of $L_G$ and $L_C$. This highlights how this approach can decouple the conflicting constraints on $L_C$ and $L_G$ (longer $L_C$ and $L_G$ can result in improved contact resistance and electrostatic control) from the constraints imposed by needing to aggressively scale CGP (ideally scaling both $L_C$ and $L_G$). FIGS. 6A-6C shows electrical characterization of a typical CNFET 100 and the measured voltage transfer curve from a CNFET inverter fabricated from 30 nm CGP CNFETs 100, illustrating functional operation.

**[0060] VLSI System-Level Energy-Efficiency Benefits**

**[0061]** In addition to the benefits that back-gate CNFETs 100 provide in terms of scaling, back-gate FET geometries may also simultaneously reduce parasitic capacitances (*e.g.*, gate-to-source/drain capacitance (see *gate-to-source/drain spacer capacitance*: $C_{GTP}$ in FIG. 2A)), resulting in additional EDP benefits for digital very-large-scale integrated (VLSI) circuits. The reduced parasitic capacitances are due to the decreased electrical coupling between the gate 130 beneath the source 110 and drain 120 (*i.e.*, considering the physical separation and overlap area between the gate 130 and the source 110 and/or the drain 120; see FIGS. 2A and 2B). In contrast, the gate is located directly between the source and drain for top-gate and GAA geometries forming large "parallel plate" capacitors.

**[0062]** FIG. 8A shows that at a CGP of 30 nm, the parasitic capacitance for the back-gate FET 100 is 0.1 fF/μm. By comparison, the parasitic capacitance for the top-gate FET and the GAA FET are 0.25 fF/μm and 0.28 fF/μm, respectively. Thus, the parasitic capacitance of the top-gate FET and the GAA FET are > 2.5x larger compared to the back-gate FET 100. Additionally, FIG. 8A shows the beneficial reduction in parasitic capacitance for back-gate FETs 100 increases as CGP continues to scale smaller. Such reduction in parasitic capacitances results in a lower EDP, which benefits digital VLSI circuits.

**[0063]** To quantify these EDP benefits, physical designs of digital VLSI circuits from the processor core of OpenSPARC T2 and a 32-bit commercial processor core were analyzed using standard cell layouts as well as industry-standard tools for synthesis, placement and routing, and

parasitic extraction. These processor cores incorporate many effects present in realistic VLSI circuits that do not appear in small-scale circuit benchmarks, ranging from physical placement and routing congestion, to wire parasitics and buffer insertion to meeting circuit-level timing constraints.

**[0064]** CNFET-level capacitance components are determined using a commercial 3D field solver (Synopsys Sentaurus), to extract values for the parasitic capacitors shown in FIG. 9A. In particular, these parasitic capacitances include: $C_{GS,sp}$ and $C_{GD,sp}$ (gate-to-source/drain contact capacitance), $C_{GS,fr}$ and $C_{GD,fr}$ (fringe capacitance from the gate the CNTs in the spacer region on both the source/drain sides), and $C_{SD}$ (direct source-to-drain capacitance between the metal contacts). Each of these capacitances is extracted separately for each CNFET geometry (top-gate, back-gate, gate-all-around). Intrinsic gate-to-channel capacitance ($C_{GC}$ in FIG. 9A) is computed using a SPICE-compatible CNFET compact model. These CNFET level capacitances are used in conjunction with standard cell-level capacitances (e.g., for local metal interconnects, extracted using Mentor Graphics Calibre) to characterize standard cell library power/timing, and then metal routing parasitics are extracted during place-and-route (Synopsys IC Compiler).

**[0065]** The physical design flow for VLSI circuits is as follows: the circuit-level performance metrics for physical designs for each VLSI-scale circuit module (*i.e.*, from the OpenSparc T2 processor core and for the 32 bit commercial processor core) are quantified at the 3 nm node (details in FIG. 8B) across multiple device-level performance metrics, including (but not limited to): supply voltage ($V_{DD}$ = 375 mV to 500 mV), sub-threshold slope ($SS$) degradation (from 0% to 60%), and interconnect simulator to model extrinsic elements based on the CNFET geometry and material properties (*e.g.*, on the dimensions and resistivity of the source/drain metal contact plugs). For each combination of parameters (*e.g.*, for each $V_{DD}$, $SS$, top-gate vs. bottom-gate), the following design flow is used to quantify relative EDP (*e.g.*, as in FIG. 10) for all VLSI circuit modules:

**[0066]** 1. *Standard cell library characterization*: using standard cell layouts (derived from the 15 nm node Nangate Open Cell Library) are used to extract standard cell parasitics, and then the extracted netlists are used in conjunction with the experimentally calibrated compact transistor models to characterize power and timing (using Cadence Spectre) for each standard library cell

**[0067]** 2. *Synthesis*: using Synopsys Design Compiler, synthesize each circuit module over a range of target clock frequencies (from 1 GHz to 10 GHz), since operating clock frequency after optimizing circuit EDP can vary depending on the device-level parameters (*e.g.*, $V_{DD}$).

**[0068]** 3. *Placement & routing*: using Synopsys IC Compiler perform placement and routing for each synthesized netlist (for each target frequency), allowing for physical circuit optimization such as buffer insertion to meet circuit timing constraints.

**[0069]** 4. *Power/timing analysis*: perform power and timing analysis for each physical design (using Synopsys PrimeTime) placed and routed above, over several *retargeted* clock frequencies spanning the range from 0.1 GHz up to 10 GHz in 0.1 GHz increments (*i.e.*, readjust the timing constraints in steps 2 and 3 targeting a different clock frequency), since it can be potentially more energy efficient to operate at a separate clock frequency than that was specified during synthesis and place and route.

**[0070]** FIG. 10 shows the reduced EDP (normalized with respect to the improved EDP for the GAA CNFET for each module) across modules of OpenSparc T2 and the 32-bit commercial processor core. Owing to reduced parasitic capacitances, back-gate CNFETs 100 provide an average of 2.2× EDP benefit vs. GAA CNFETs and 1.6× vs. top-gate CNFETs. Importantly, these benefits are *in addition* to the substantial EDP benefits that top-gate CNFETs offer vs. Si FETs.

**[0071]** FIG. 11 shows the energy per cycle as a function of the clock frequency for back-gate CNFETs 100 in comparison to top-gate and GAA CNFETs. Generally, a lower EDP corresponds to a lower energy per cycle at a higher clock frequency. As shown, the back-gate CNFETs 100 exhibit a lower energy per cycle than the top-gate and GAA CNFETs at a given clock frequency. This corresponds directly to the EDP benefit shown in FIG. 10.

**[0072] Additional Considerations**

**[0073]** The reduced parasitics that result in lower EDP may also outweigh potential gains stemming from improved electrostatic control for GAA geometries. For example, the subthreshold-swing (SS) for the back-gate CNFET 100 may degrade from ~60 mV/decade to ~100 mV/decade, while still maintaining EDP benefits compared to GAA CNFETs with nearly ideal SS approaching 60 mV/decade as demonstrated in FIG. 12.

**[0074]** In addition to showing scalability to a 30 nm CGP, this approach allows scaling to sub-20 nm CGP, using technology parameters that have already been achieved experimentally (FIG. 13). For instance, a 9 nm $L_G$, a 9 nm $L_C$, and an overlap of the gate and the source and drain ($-L_{SP}$) of 3

nm would result in a CGP of 15 nm. Importantly, even when assuming an overlap of the gate with the source and drain for back-gate FETs 100, the parasitics may still be less than a conventional top-gate FET at the same CGP (FIG. 13). The overlap of 3 nm (1) enables 15 nm CGP given experimentally realized dimensions for $L_C$ and $L_G$ and (2) exceeds the projected lithographic overlap accuracy, ensuring that some section of the gate is under the entire channel to maintain electrostatic control. For such aggressively scaled sub-20 nm CGPs, EDP benefits degrade compared to 30 nm CGP, though still maintain EDP benefits compared to 30 nm CGP top-gate CNFETs (FIG. 14).

**[0075]** As described above, the back-gate FET 100 architecture described herein provides an approach to realize scaled technology nodes, which may enable continued scaling to sub-3 nm technology nodes. In one exemplary back-gate FET 100, low-temperature solution processing of CNTs may be used to realize back-gate FETs 100. This approach not only enables additional scaling, but promises significant energy efficiency benefits by combining the EDP benefits afforded by CNTs with the EDP benefits associated with reducing parasitic capacitances in back-gate FETs. This approach is applicable to a broad range of emerging channel materials, such as one-dimensional and two-dimensional nanomaterials, especially if the channel materials satisfy: (1) the constraints of < 400 °C channel deposition and subsequent FET processing and (2) thin body thickness (to maintain good electrostatic control of the channel). Moreover, CGP scaling may be achieved in back-gate FETs 100 without requiring scaling of the physical gate length ($L_G$) or contact length ($L_C$), and is complementary to other paths for maintaining area reduction per node. Therefore, beyond demonstrating a FET scaling of a 30 nm CGP using materials and processing suitable for a sub-3 nm technology node, this work also illustrates a promising and feasible path for continued scaling beyond the limits of silicon-based technologies.

**[0076] Conclusion**

**[0077]** All parameters, dimensions, materials, and configurations described herein are meant to be exemplary and the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used. It is to be understood that the foregoing embodiments are presented primarily by way of example and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or

method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

**[0078]** Also, various inventive concepts may be embodied as one or more methods, of which at least one example has been provided. The acts performed as part of the method may in some instances be ordered in different ways. Accordingly, in some inventive implementations, respective acts of a given method may be performed in an order different than specifically illustrated, which may include performing some acts simultaneously (even if such acts are shown as sequential acts in illustrative embodiments).

**[0079]** All publications, patent applications, patents, and other references mentioned herein are incorporated by reference in their entirety.

**[0080]** All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

**[0081]** The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

**[0082]** The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, *i.e.*, elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, *i.e.*, "one or more" of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

**[0083]** As used herein in the specification and in the claims, "or" should be understood to have the same meaning as "and/or" as defined above. For example, when separating items in a list, "or" or "and/or" shall be interpreted as being inclusive, *i.e.*, the inclusion of at least one, but also

including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such as "only one of" or "exactly one of," or, when used in the claims, "consisting of," will refer to the inclusion of exactly one element of a number or list of elements. In general, the term "or" as used herein shall only be interpreted as indicating exclusive alternatives (*i.e.* "one or the other but not both") when preceded by terms of exclusivity, such as "either," "one of," "only one of," or "exactly one of." "Consisting essentially of," when used in the claims, shall have its ordinary meaning as used in the field of patent law.

**[0084]** As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

**[0085]** In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, *i.e.*, to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

# CLAIMS

1. A transistor comprising:

a channel having a first side and a second side opposite the first side;

a source disposed on the first side of the channel;

a drain disposed on the first side of the channel and spaced apart from the source by a physical channel length of less than about 10 nm; and

a gate disposed on the second side of the channel and having a gate length greater than the physical channel length.

2. The transistor of claim 1, wherein the transistor has a contacted gate pitch of 30 nm or less.

3. The transistor of claim 1, wherein the transistor has a parasitic capacitance of less than 0.1 femtofarads/micron.

4. The transistor of claim 1, wherein the channel comprises a nanotube in electrical communication with the source and the drain.

5. The transistor of claim 4, further comprising:

a dielectric disposed between the gate and the nanotube.

6. The transistor of claim 1, wherein the gate overlaps at least one of the source or the drain.

7. The transistor of claim 1, wherein the transistor is configured to operate at a clock frequency ranging between about 0.1 GHz and about 10 GHz.

8. A transistor comprising:

a channel having a first side and a second side opposite the first side;

a source disposed on a first side of the channel;

a drain disposed on the first side of the channel; and

a gate, disposed on the second side of the channel, overlapping at least one of the source or the drain,

wherein the transistor has a contacted gate pitch of 30 nm or less.

9. The transistor of claim 8, wherein the transistor has a parasitic capacitance of less than 0.1 femtofarads/micron.

10. The transistor of claim 8, wherein the channel comprises a nanotube in electrical communication with the source and the drain.

11. The transistor of claim 10, further comprising:
a dielectric disposed between the gate and the nanotube.

12. The transistor of claim 8, wherein the transistor operates at a clock frequency ranging between about 0.1 GHz and about 10 GHz.

13. A method of making a transistor, the method comprising:
forming a gate;
depositing a dielectric on the gate;
depositing a carbon nanotube over the dielectric to form a channel; and
patterning a source and a drain on the channel opposite the gate with a physical channel length less than a length of the gate and less than about 10 nm.

14. The method of claim 13, wherein depositing the carbon nanotube occurs at a temperature of less than about 400 degrees Celsius.

15. The method of claim 13, wherein patterning the source and the drain comprises lithographically etching with physical channel length at a minimum feature size.

16. The method of claim 13, wherein patterning the source and the drawn comprises overlapping at least one of the source or the drain with the gate.

17. The method of claim 13, further comprising:
before forming the gate, patterning a trench into a substrate such that the gate, when formed, is embedded in the substrate.

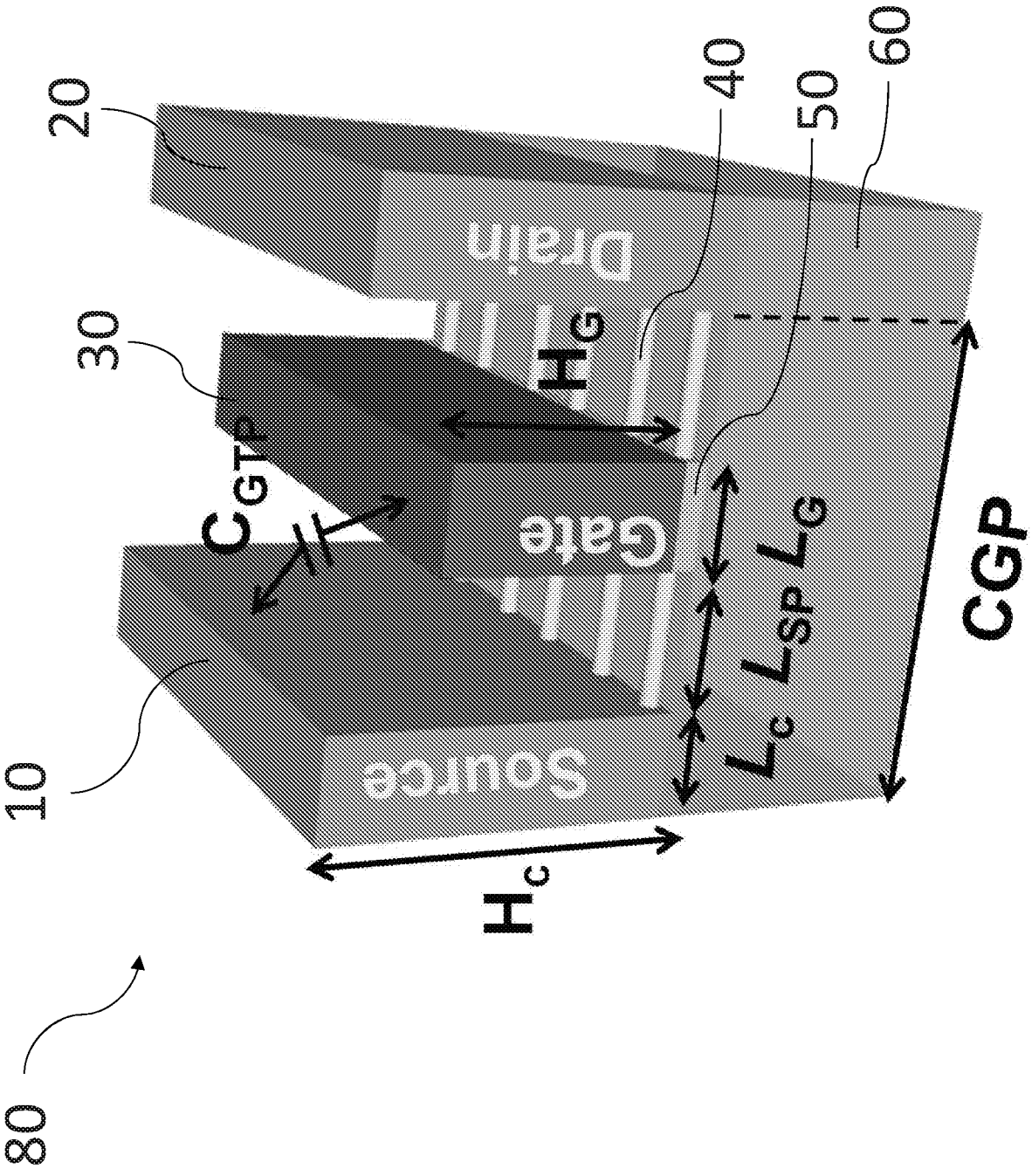



FIG. 1A

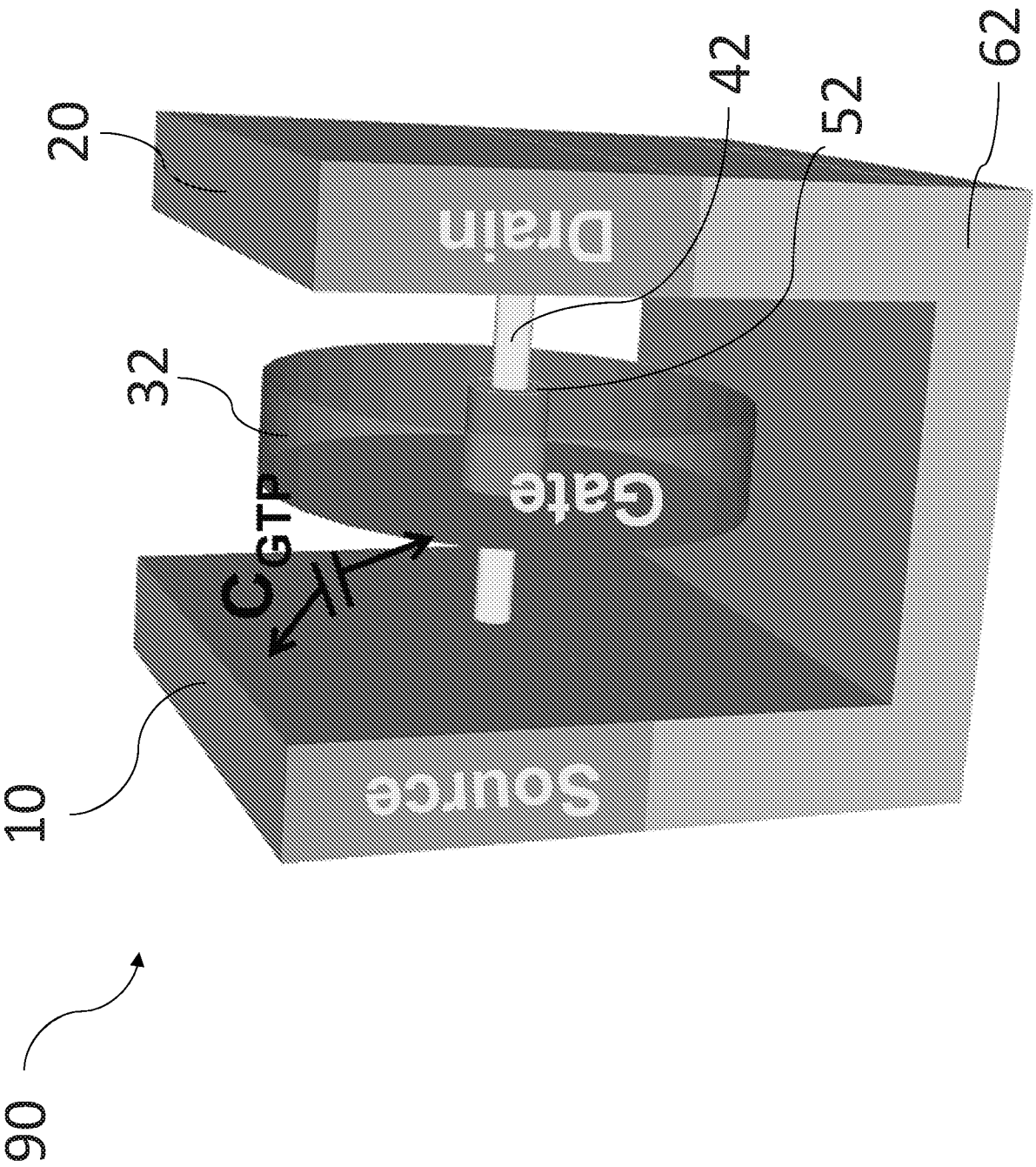



FIG. 1B

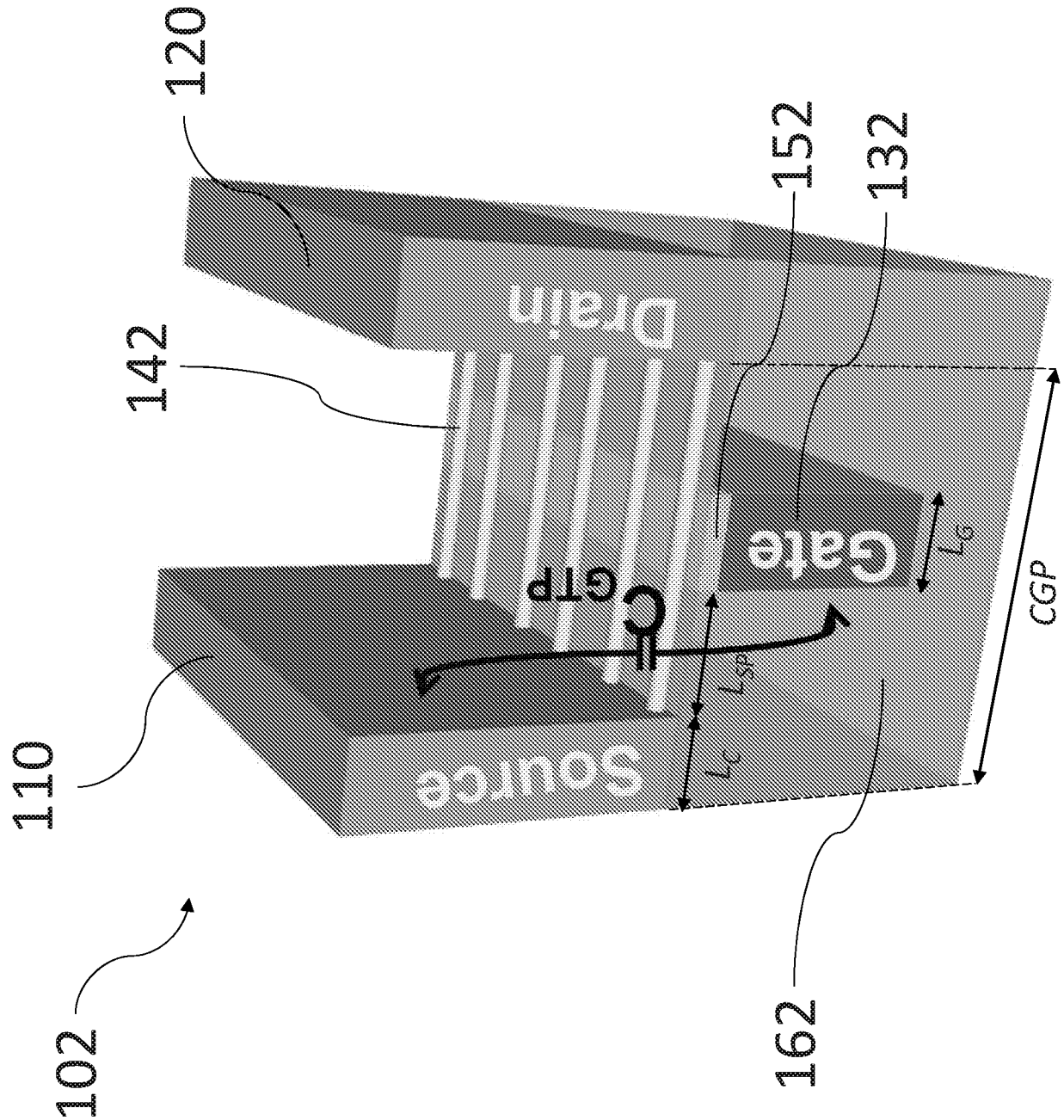



FIG. 2A

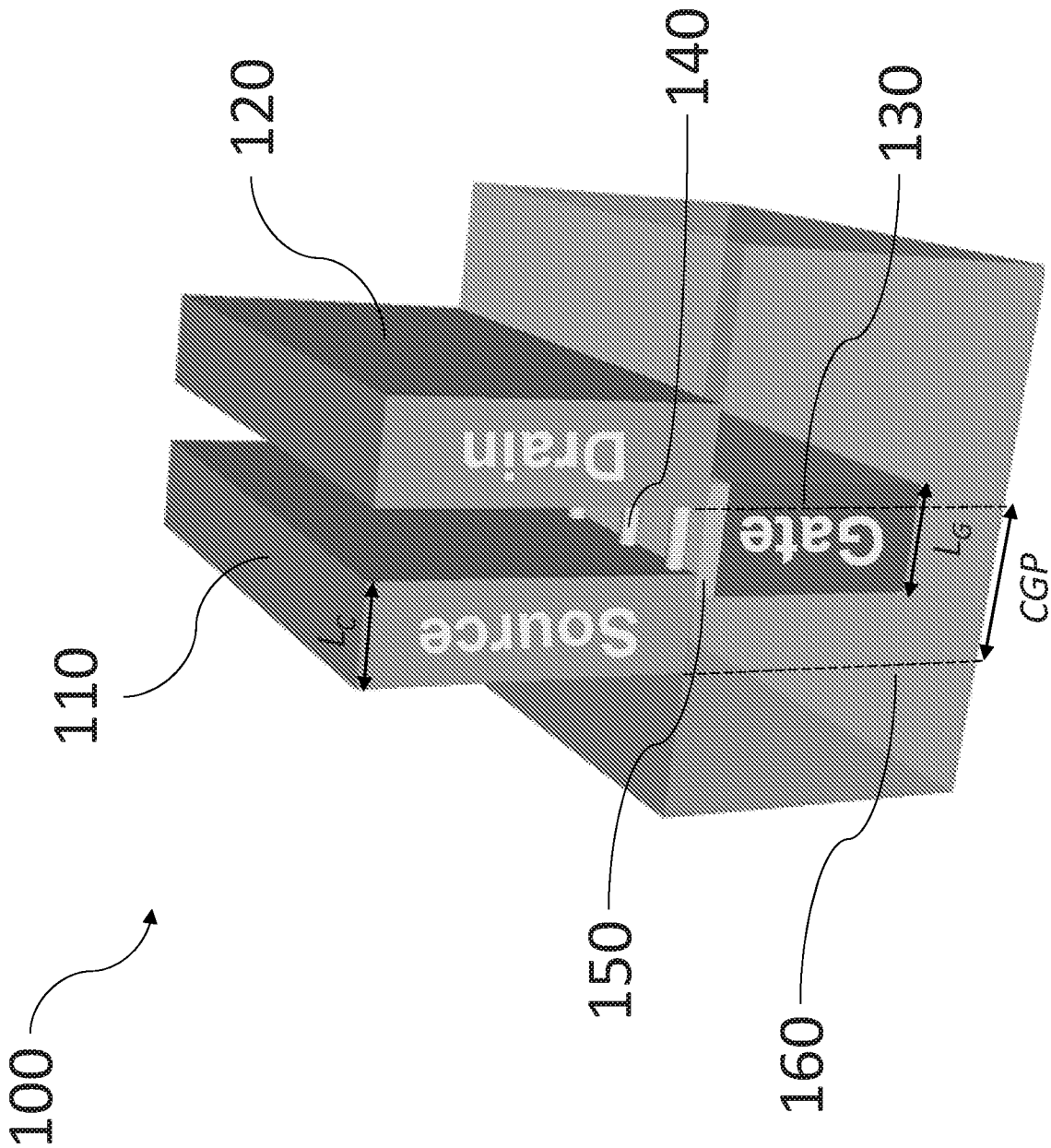
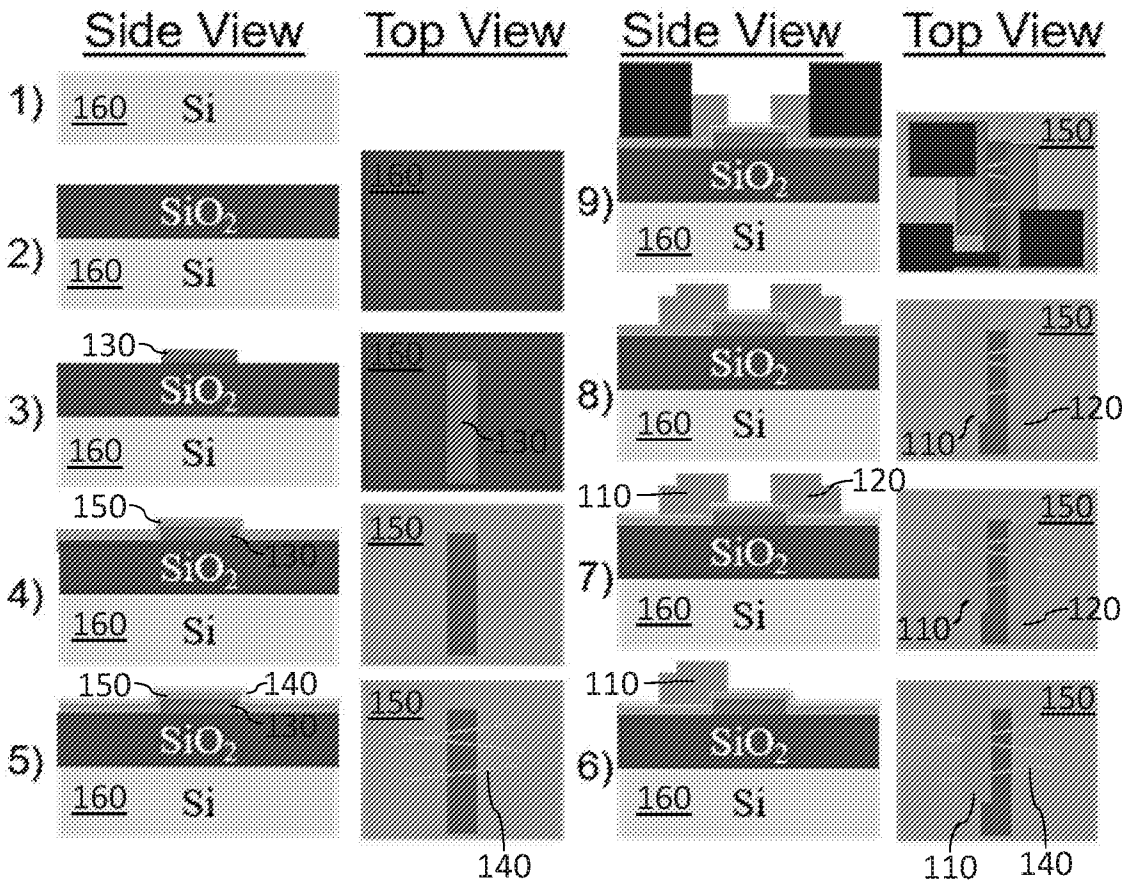



FIG. 2B




(1) Si substrate

(2) Si/SiO2 substrate

(3) E-beam Lithography for back gate (0.3nm Ti/ 4 nm Pt)

(4) ALD $HfO_2$ 3.5nm (EOT 0.9 nm)

(5) Spin Coat 99.99% semiconducting CNTs followed by toluene rinse and anneal at 400 C

(6-7) E-beam Lithography Source and Drain (1 nm Ti/ 8 nm Pt)

(8) E-beam patterning active area definition and $O_2$ plasma active etch to remove CNTs outside channel

(9) E-beam Lithography Contact Pads (1 nm Ti/ 20 nm Pt)



FIG. 3

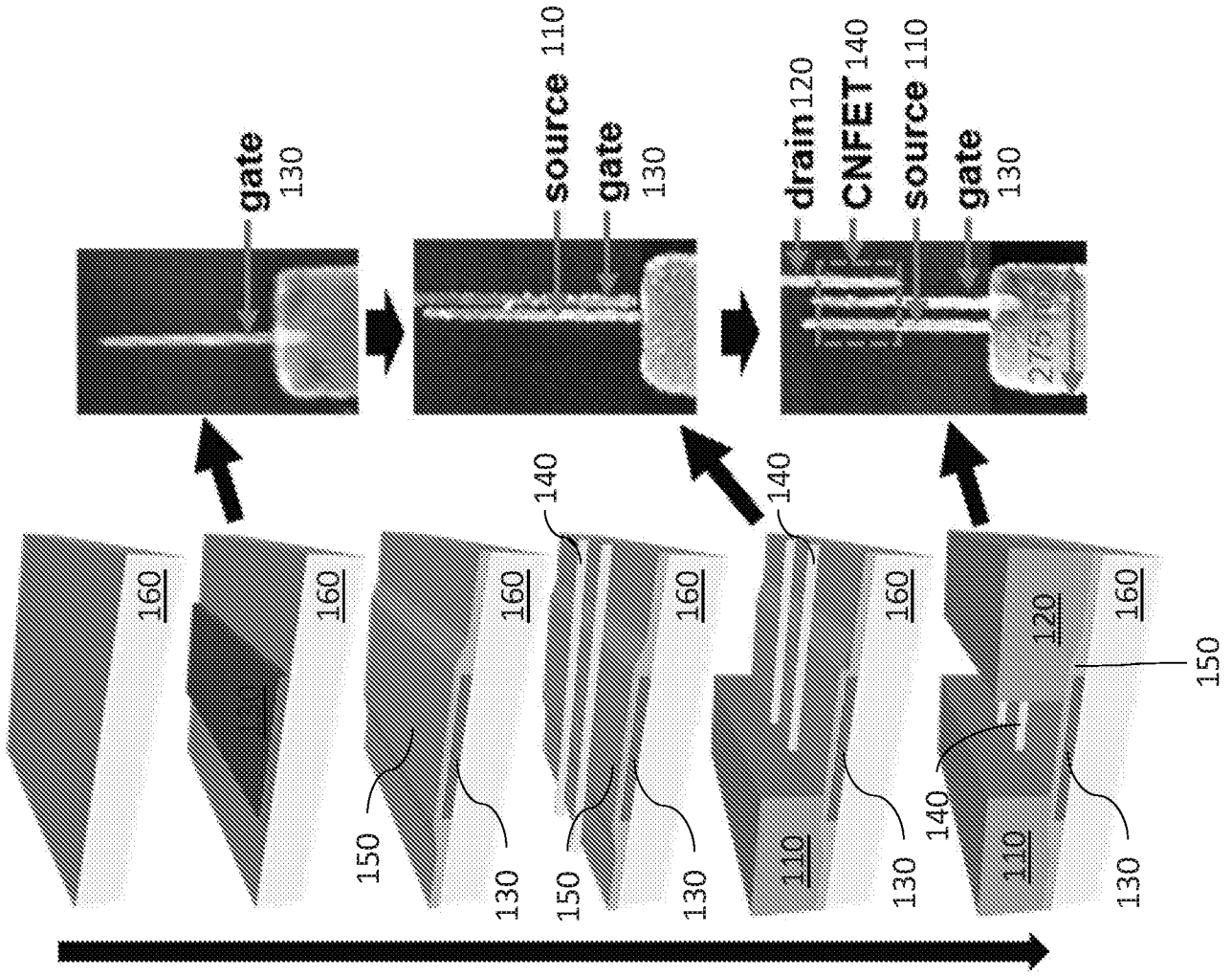

gate 130
source 110
gate 130
drain 120
CNFET 140
source 110
gate 130
160
150
130
140
110
120

FIG. 4

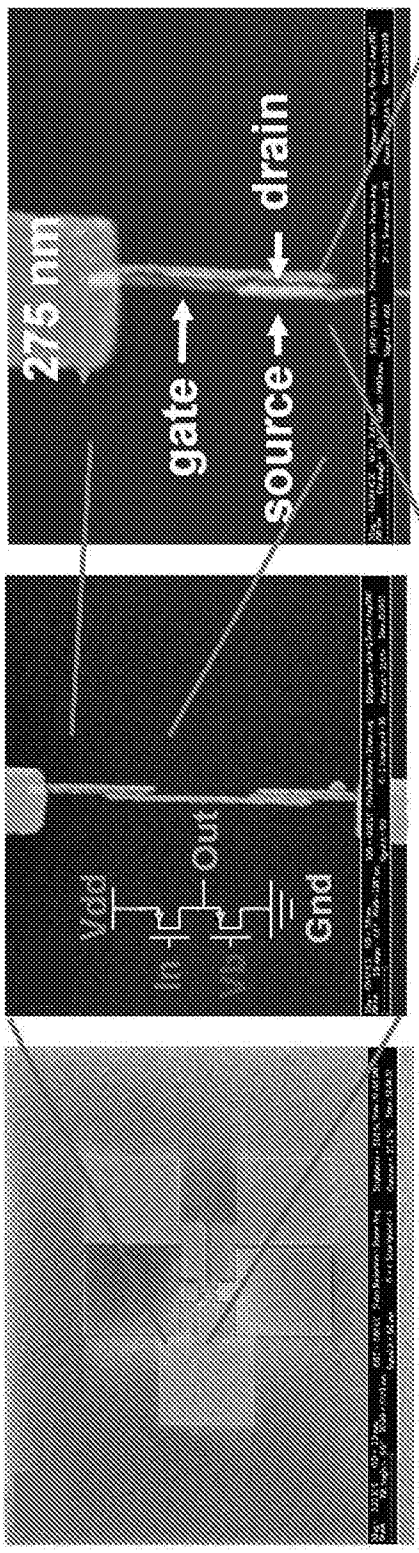



FIG. 5A



FIG. 5B




FIG. 5C

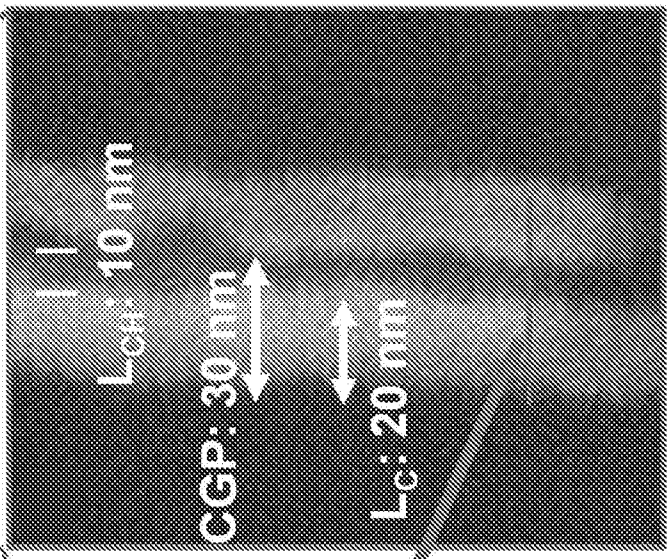



FIG. 5D

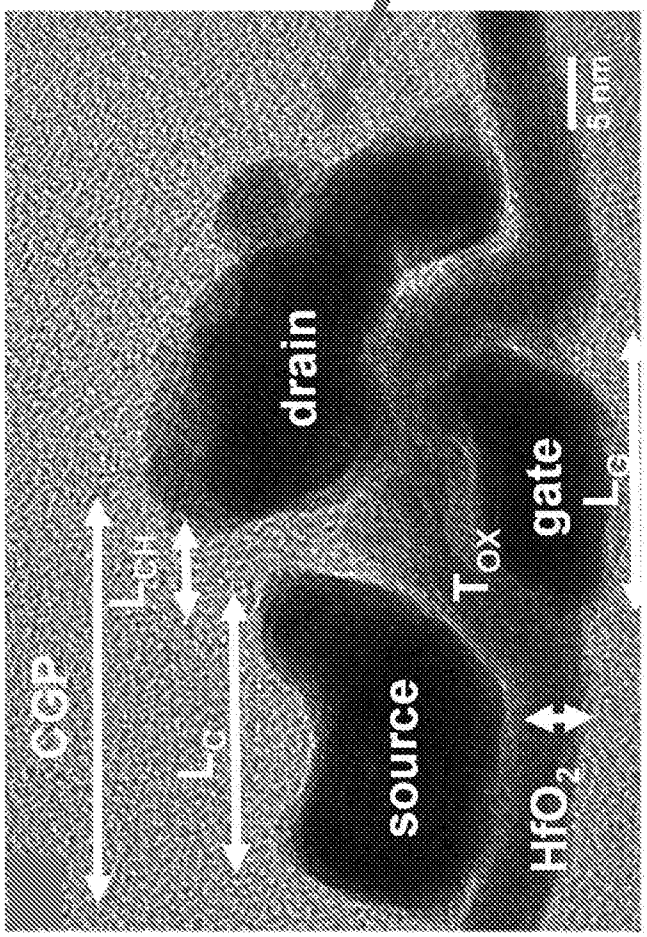



FIG. 5E

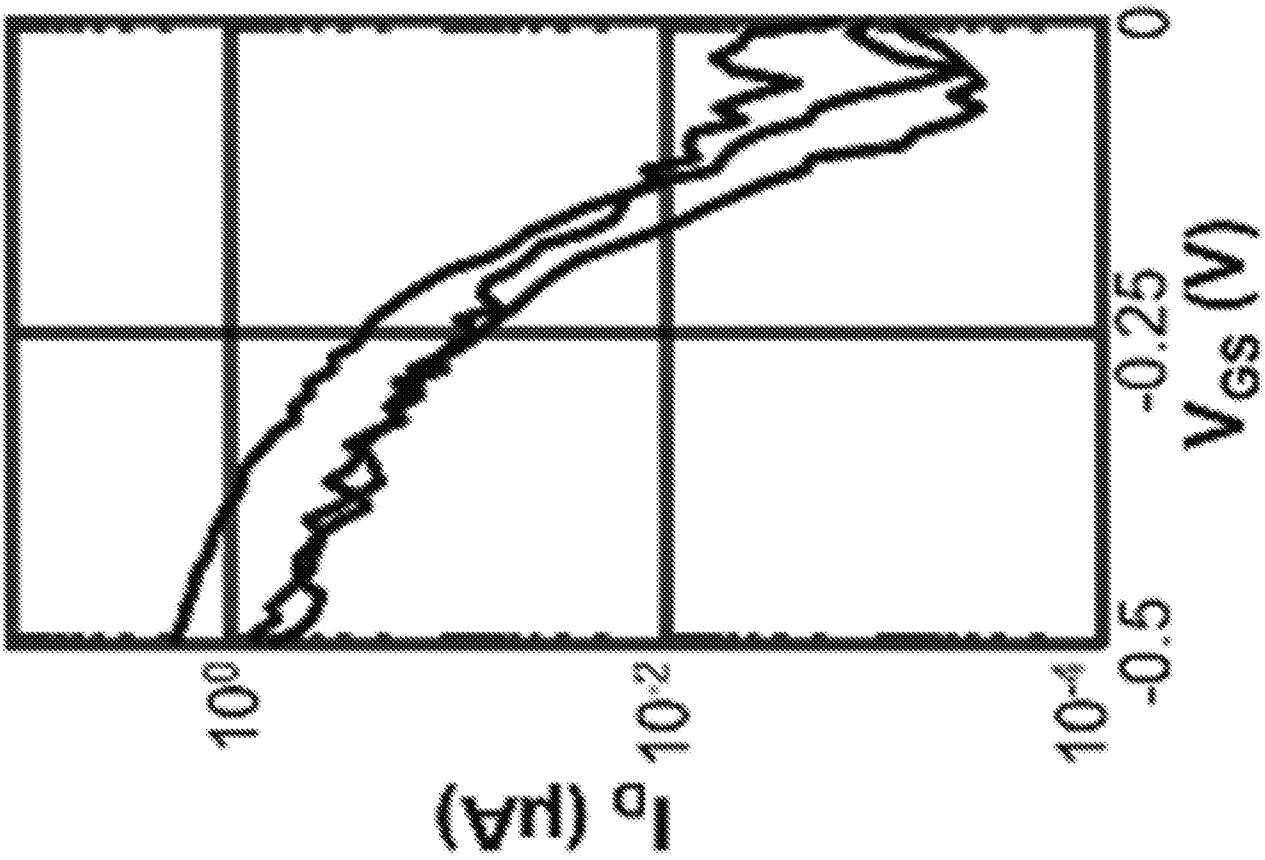



FIG. 6A

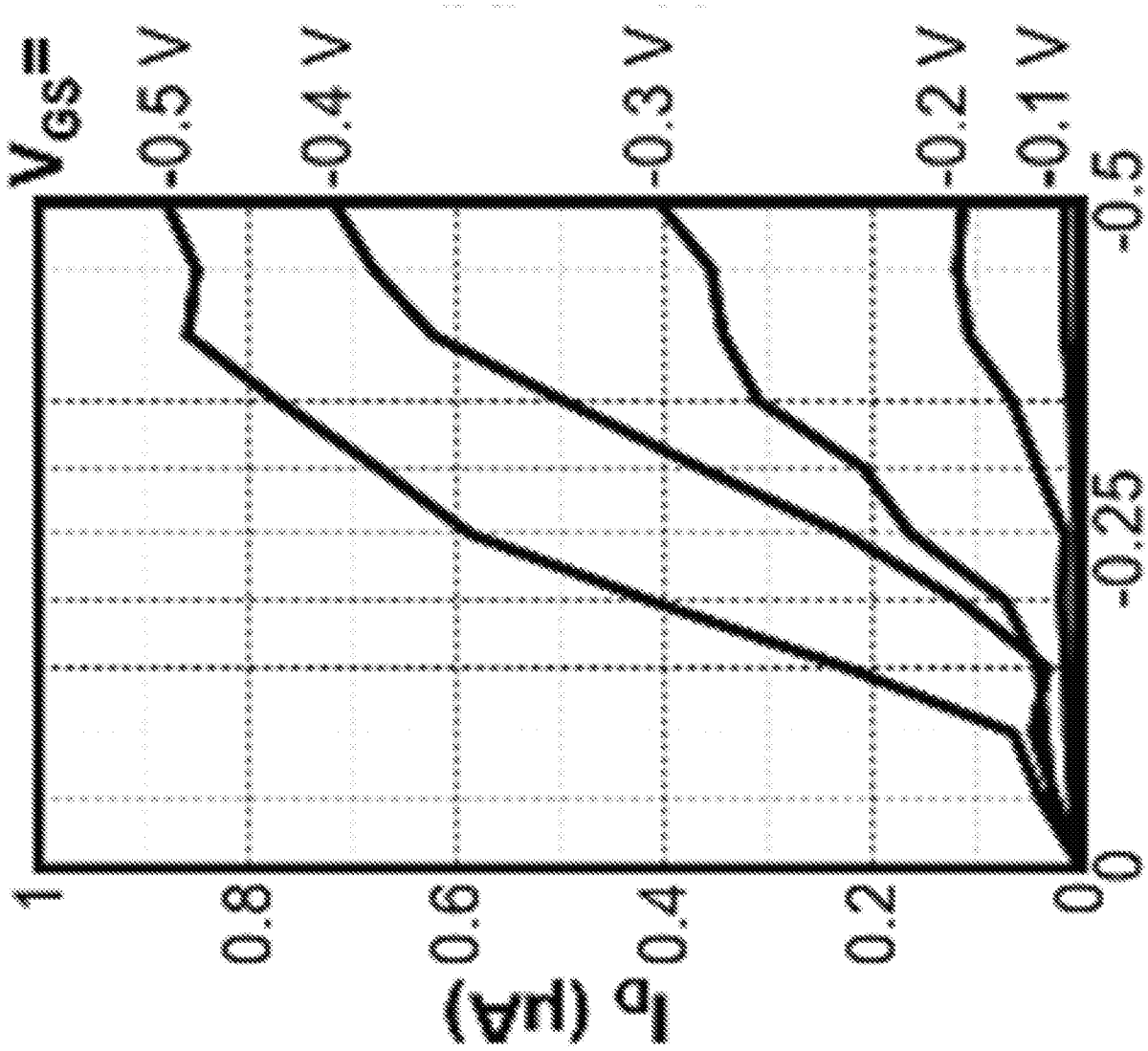



FIG. 6B

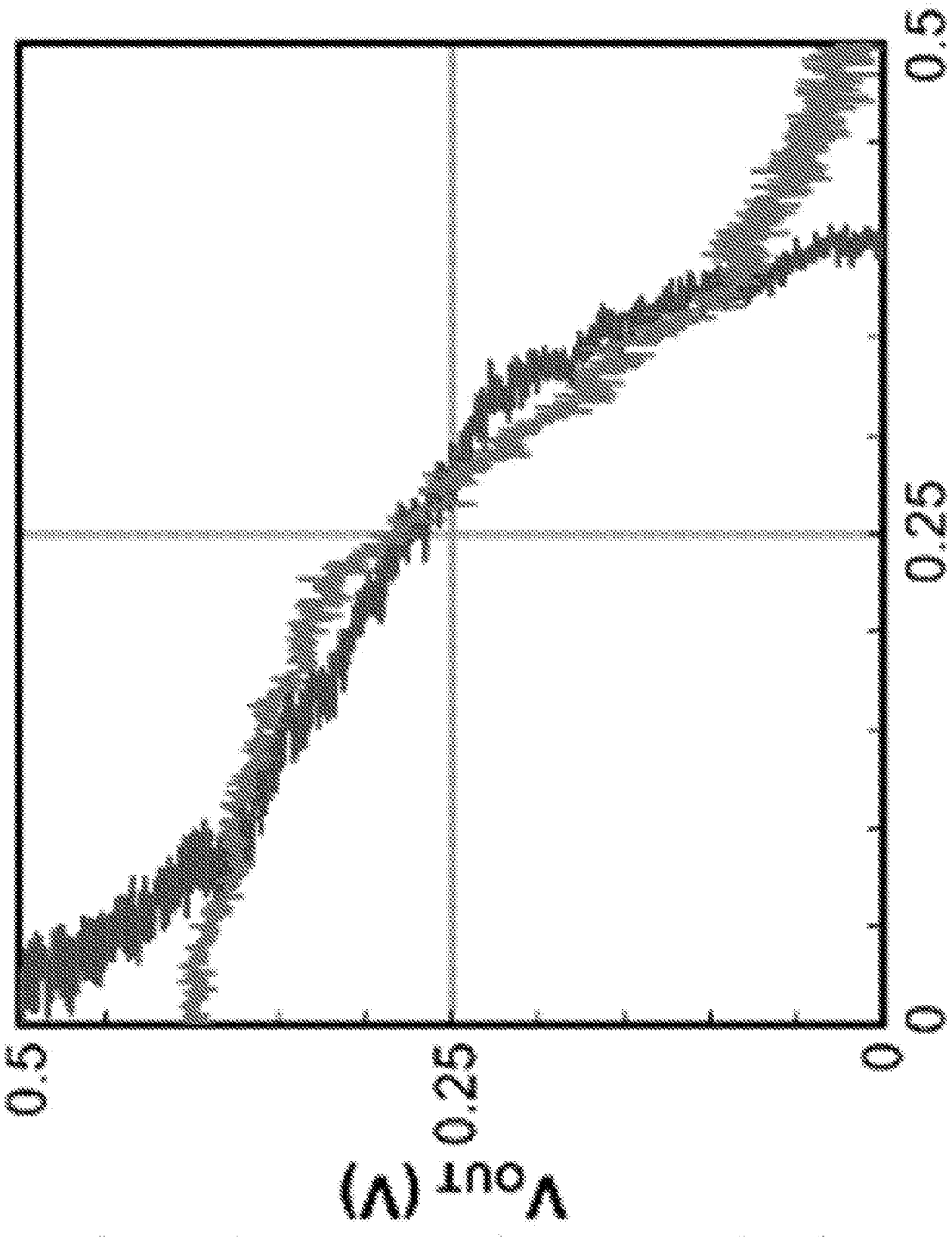



FIG. 6C

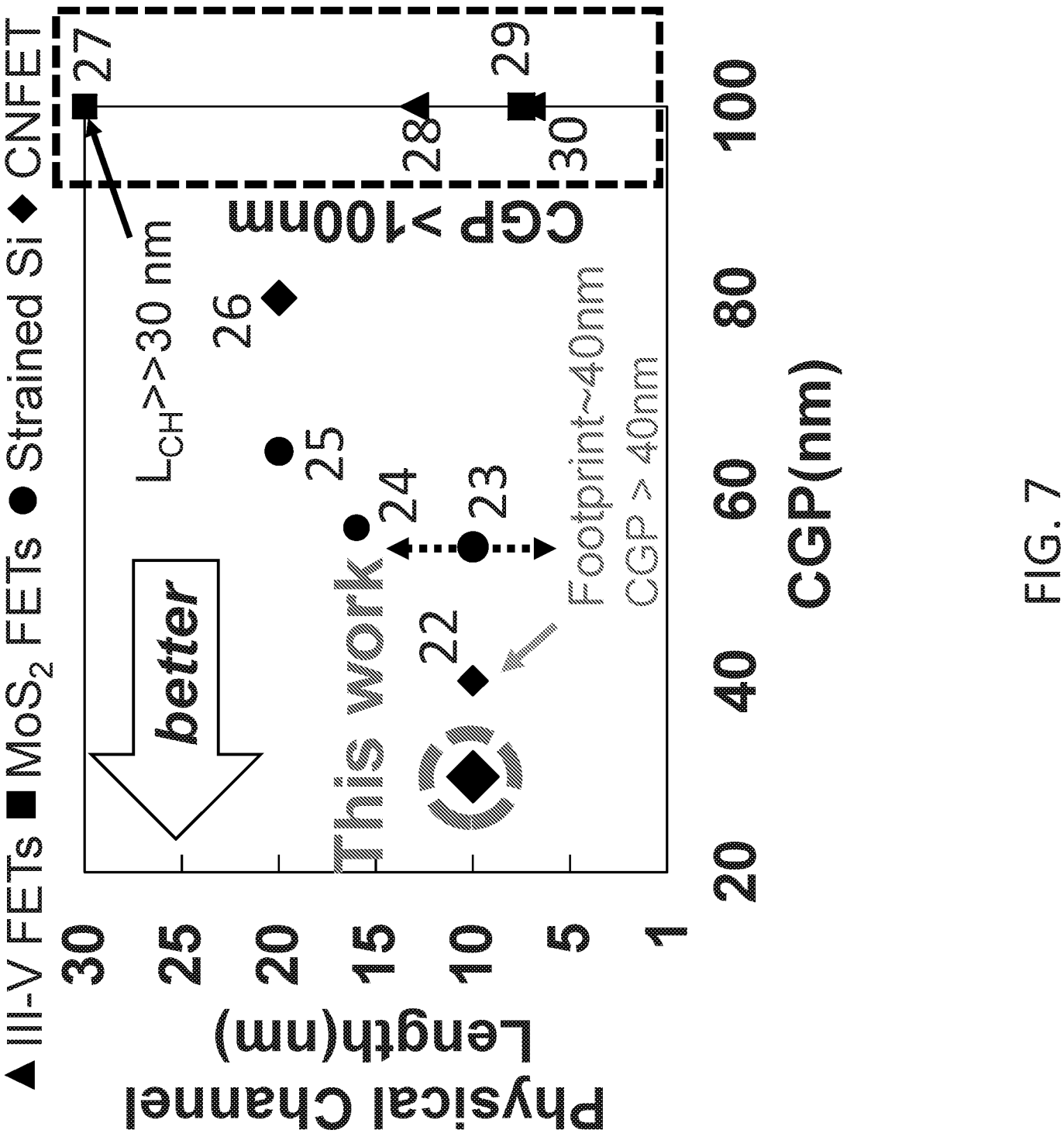

▲ III-V FETs ■ MoS2 FETs ● Strained Si ◆ CNFET
Physical Channel Length(nm)
30
25
20
15
10
5
1
20
40
60
80
100
CGP(nm)
better
This work
22
23
24
25
26
27
28
29
30
LCH>>30 nm
CGP >100nm
Footprint~40nm
CGP ~ 40nm

FIG. 7

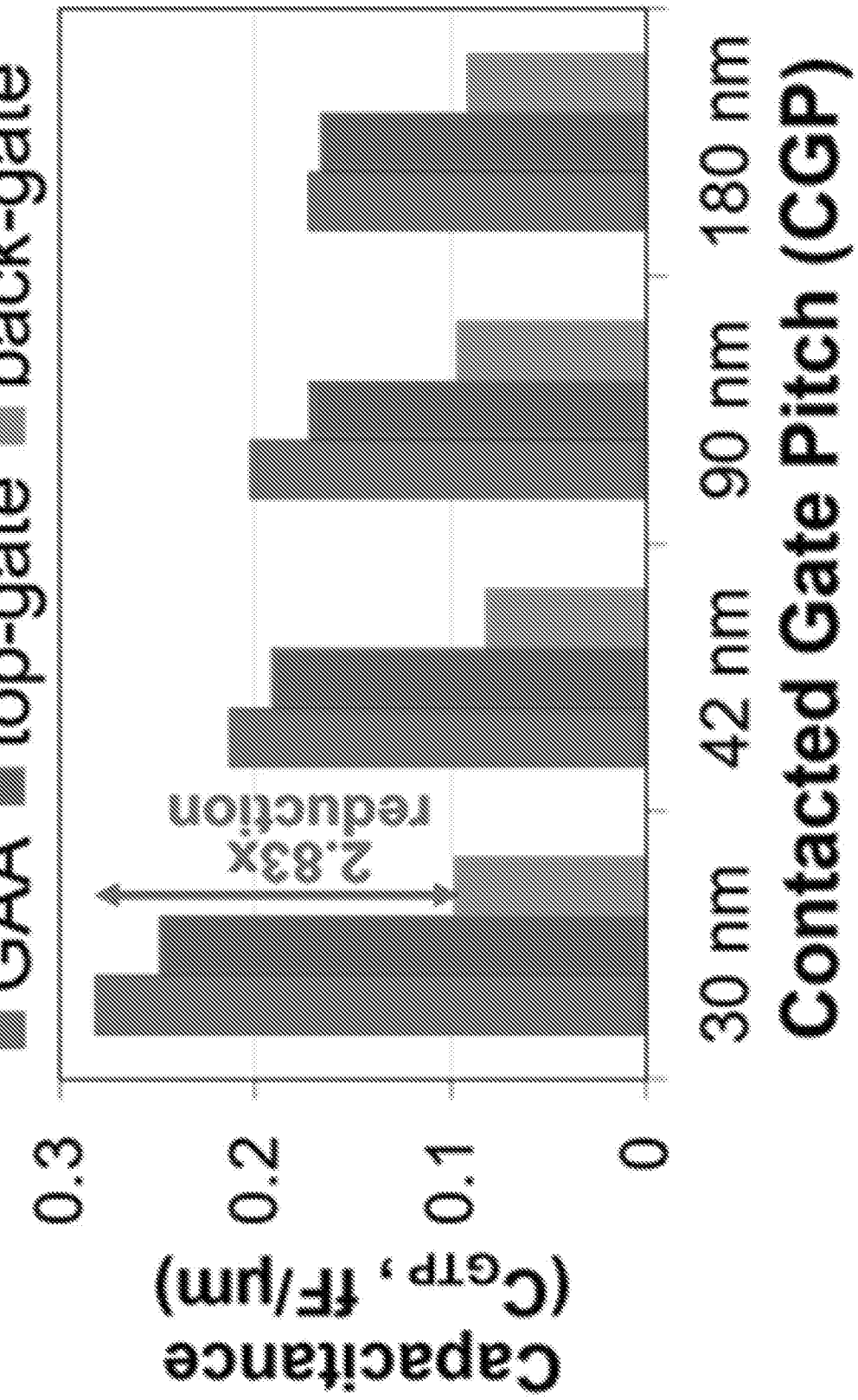

GAA
top-gate
back-gate
Capacitance
($C_{gtp}$, fF/μm)
0.3
0.2
0.1
0
2.83x
reduction
30 nm
42 nm
90 nm
180 nm
Contacted Gate Pitch (CGP)

FIG. 8A

| CGP (nm) | 30 | 42 | 90 | 180 |
|---|---|---|---|---|
| $L_G$ (nm) | 9 | 9 | 24 | 45 |
| $L_{SP}$ (nm) | 6 | 12 | 20 | 45 |
| $L_C$ (nm) | 9 | 9 | 26 | 45 |
| $H_G$ (nm) | 20 | 30 | 40 | 90 |
| $H_C$ (nm) | 40 | 60 | 80 | 180 |
| $T_{OX}$ (nm) | 2 | 2 | 3 | 4 |
| $K_{SPACER}$ | 5.5 | 5.5 | 5.5 | 5.5 |
| $K_{OX}$ | 10.3 | 10.3 | 10.3 | 10.3 |

FIG. 8B

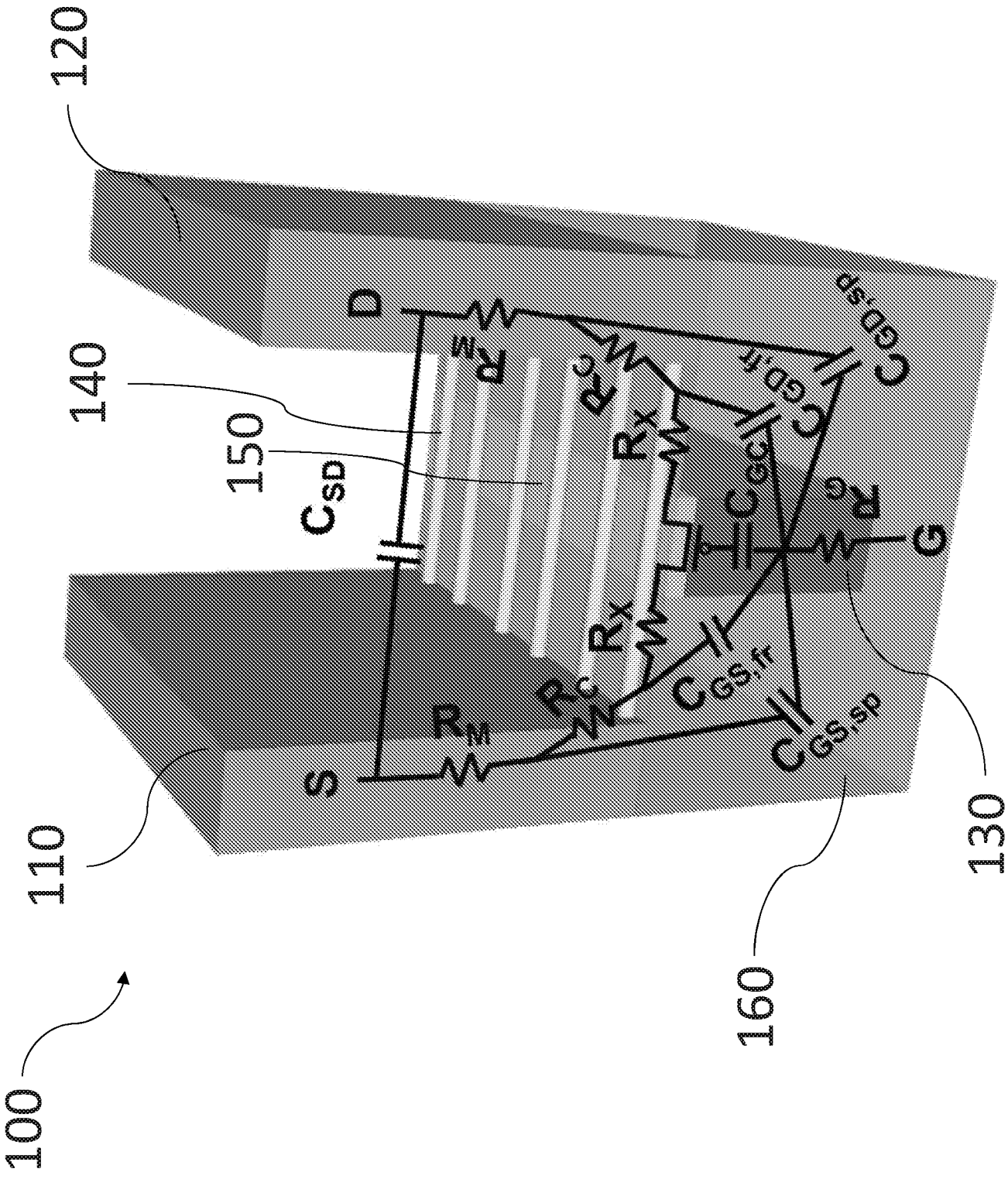

100
110
120
130
140
150
160
D
S
G
$R_E$
$R_C$
$R_X$
$R_X$
$R_C$
$R_M$
$R_G$
$C_{SD}$
$C_{GD,sp}$
$C_{GD,fj}$
$C_{GG}$
$C_{GS,f}$
$C_{GS,sp}$

FIG. 9A

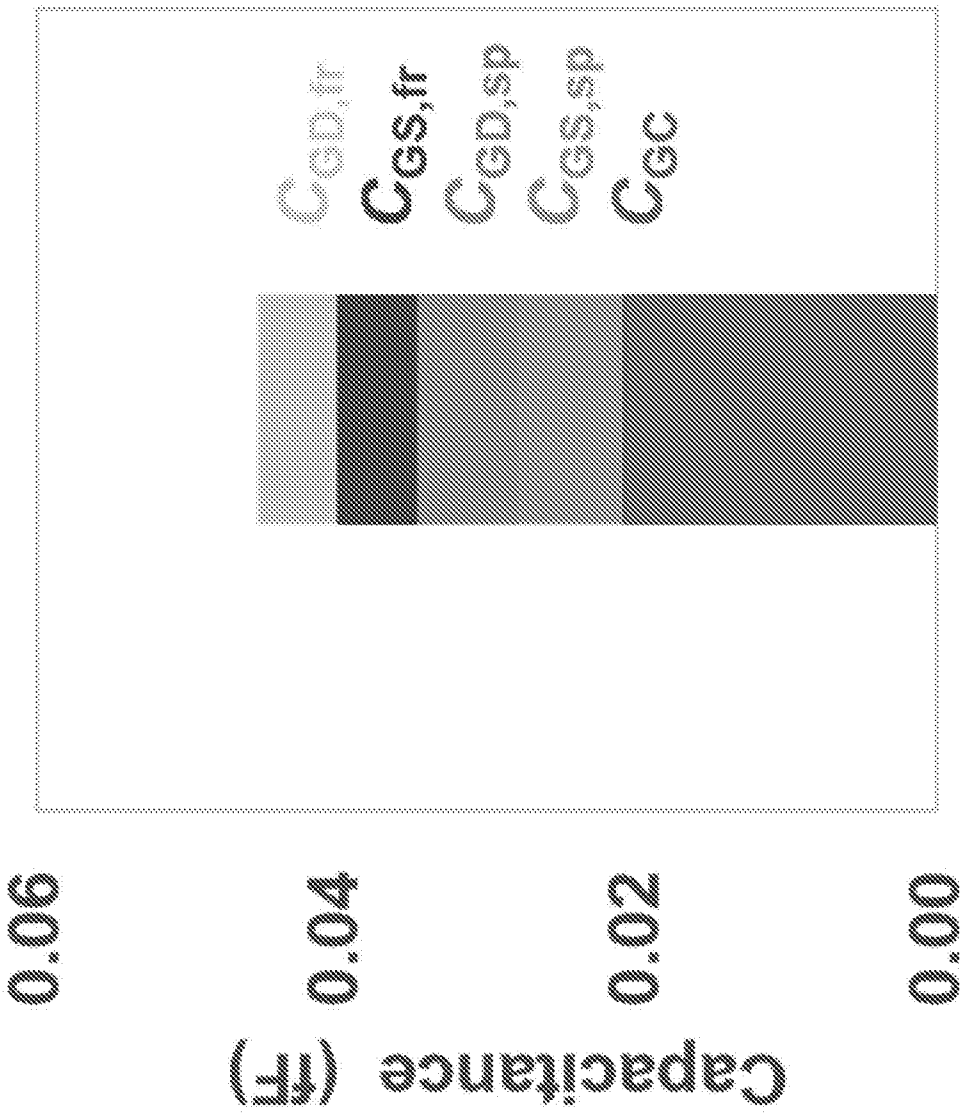



FIG. 9B

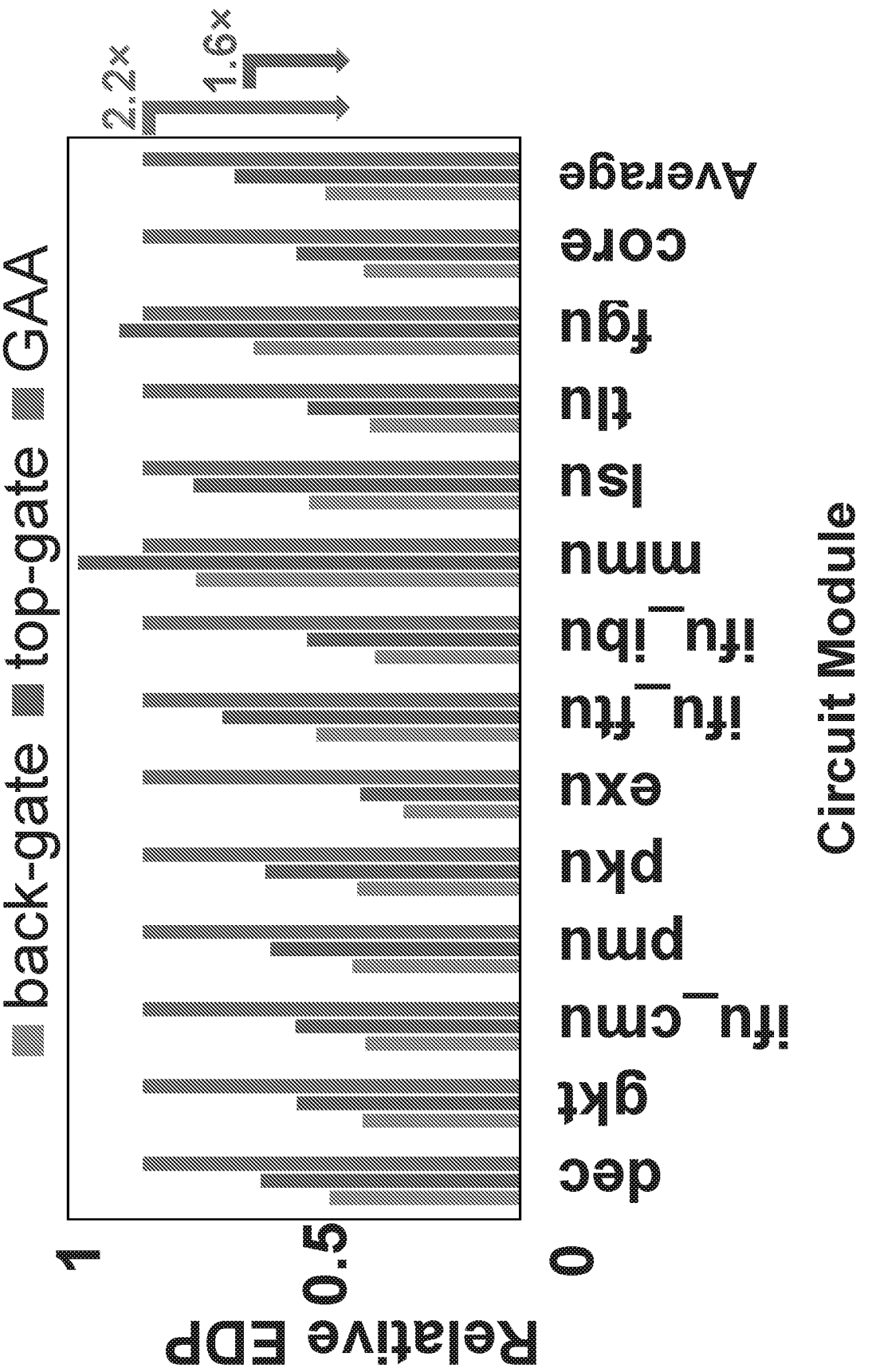

back-gate
top-gate
GAA
2.2x
1.6x
Relative EDP
1
0.5
0
dec
gkt
ifu_cmu
pmu
pku
exu
ifu_ftu
ifu_ibu
mmu
lsu
tlu
fgu
core
Average
Circuit Module

FIG. 10

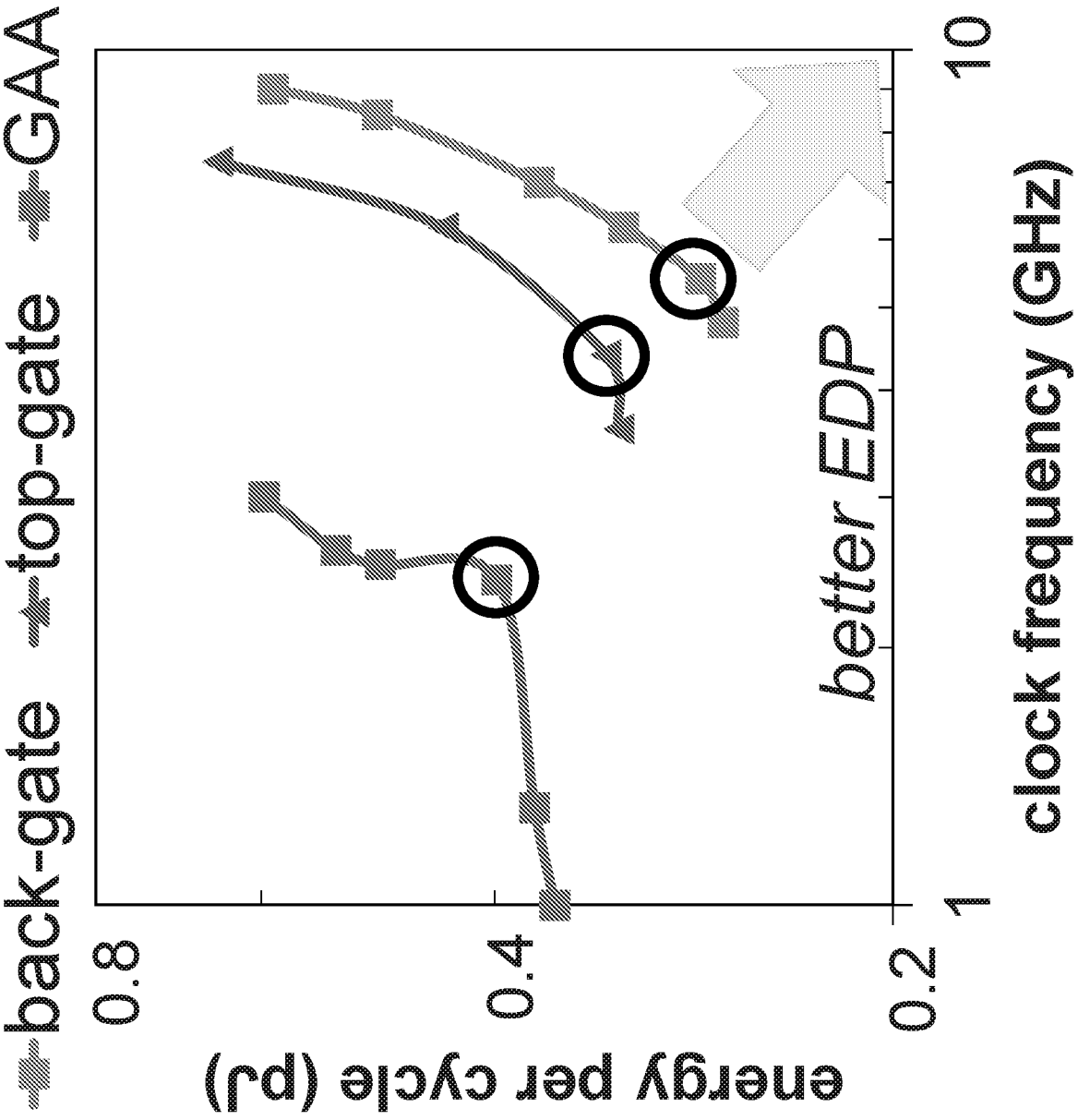

back-gate
top-gate
GAA
energy per cycle (pJ)
0.8
0.4
0.2
1
10
clock frequency (GHz)
better EDP

FIG. 11

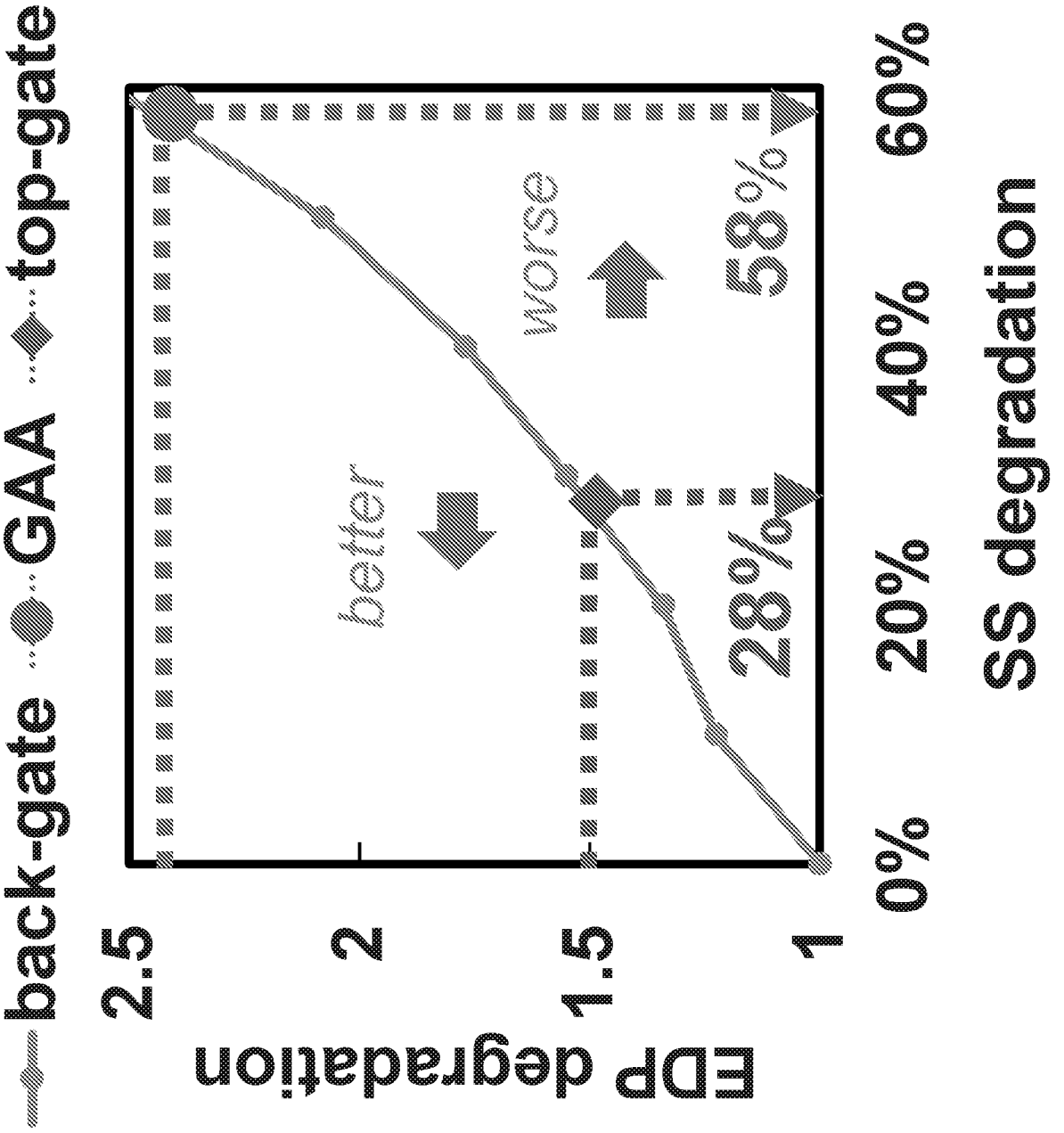

back-gate
GAA
top-gate
EDP degradation
2.5
2
1.5
1
0%
20%
40%
60%
SS degradation
better
worse
28%
58%

FIG. 12

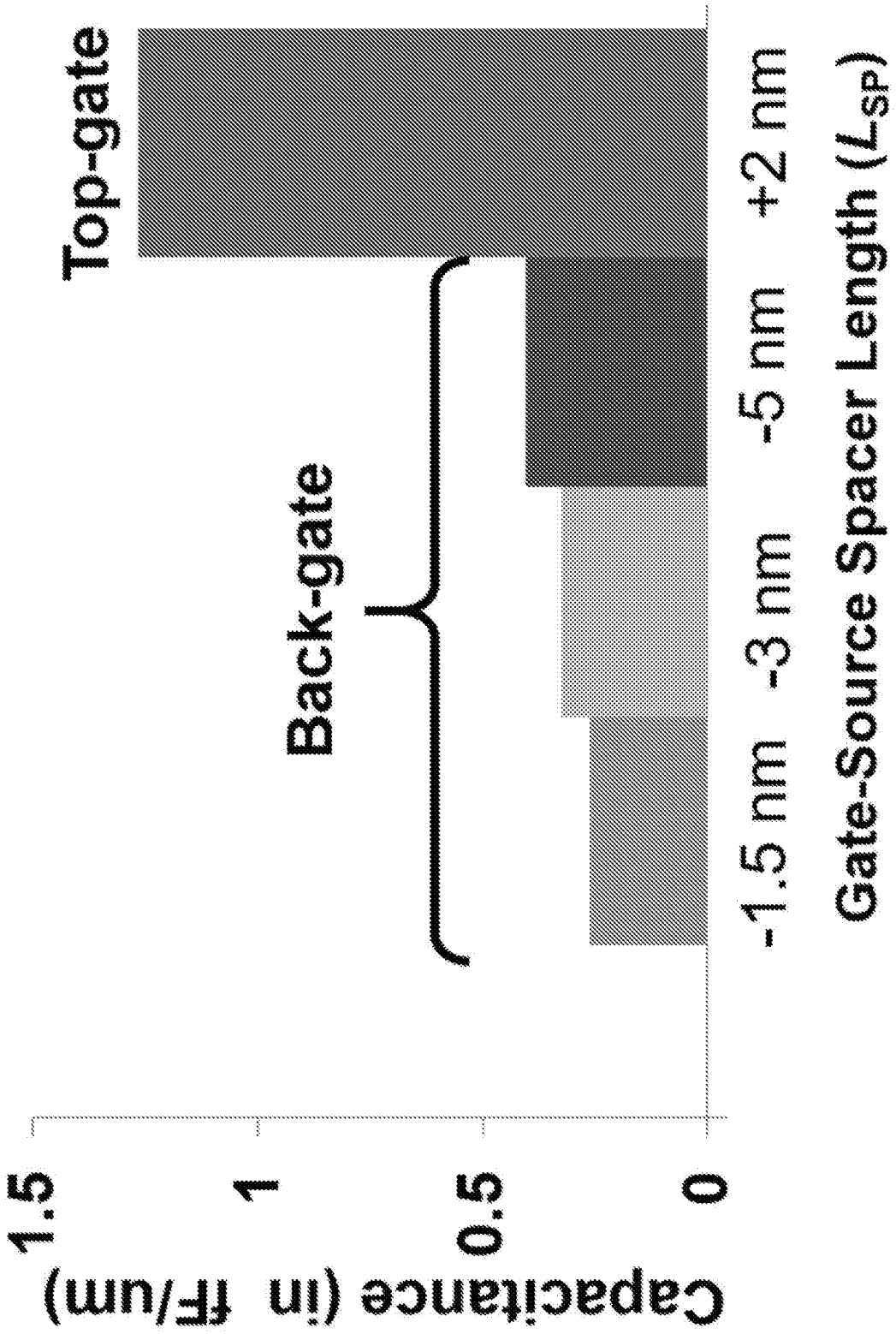

Capacitance (in fF/um)
1.5
1
0.5
0
Top-gate
Back-gate
-1.5 nm
-3 nm
-5 nm
+2 nm
Gate-Source Spacer Length ($L_{SP}$)

FIG. 13A

| CGP (nm) | 15 | 15 | 15 | 15 |
|---|---|---|---|---|
| $L_G$ (nm) | 9 | 12 | 16 | 5 |
| $L_{SP}$ (nm) | -1.5 | -3 | -5 | +2 |
| $L_C$ (nm) | 9 | 9 | 9 | 6 |
| $H_G$ (nm) | 15 | 15 | 15 | 15 |
| $H_C$ (nm) | 30 | 30 | 30 | 30 |
| $T_{OX}$ (nm) | 2 | 2 | 2 | 2 |
| $K_{SPACER}$ | 5.5 | 5.5 | 5.5 | 5.5 |
| $K_{OX}$ | 10.3 | 10.3 | 10.3 | 10.3 |

FIG. 13B

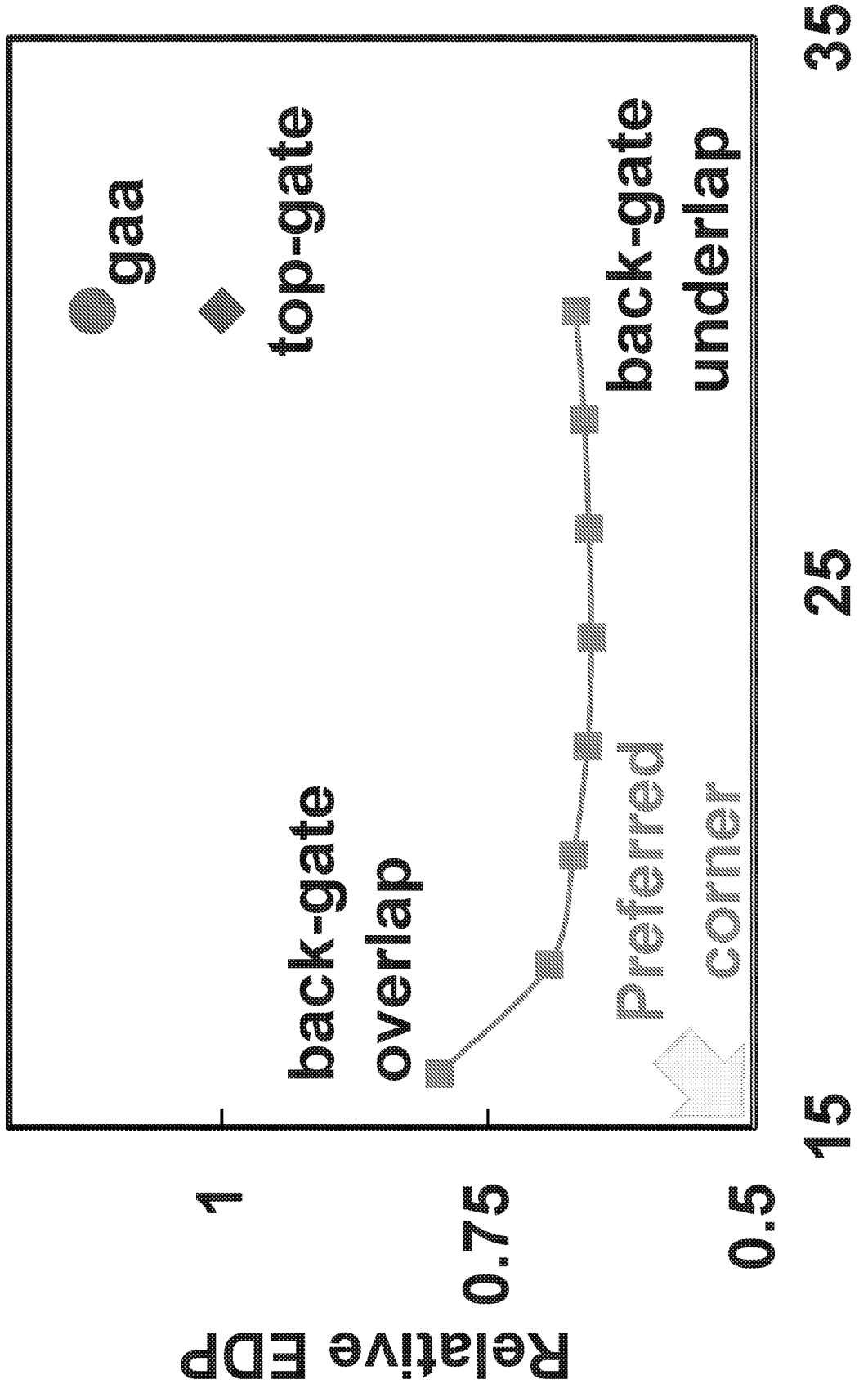

Relative EDP
1
0.75
0.5
15
25
35
CGP (nm)
gaa
top-gate
back-gate overlap
back-gate underlap
Preferred corner

FIG. 14