(12) UK Patent Application (19) GB (11) 2 095 877 A

(21) Application No **8208954**
(22) Date of filing **26 Mar 1982**
(30) Priority data
(31) **228620**
(32) **26 Mar 1981**
(33) **Dem. Rep. of Germany (DD)**
(43) Application published **6 Oct 1982**
(51) **INT CL³ G06F 11/18**
(52) Domestic classification **G4A** 12T 13E 17B 5X 9X EC
(56) Documents cited **None**
(58) Field of search **G4A**
(71) Applicants **VEB Werk fur Signal-und Sicherungstechnik Berlin, 1193 Berlin, Elsenstrasse 87/96, German Democratic Republic.**
(72) Inventors **Richter Karl, Kickbusch Michael, Henning Heinz, Brunecke Kurt, Nikolaizik Jurgen.**
(74) Agents **D. Young and Co., 10 Staple Inn, London WC1V 7RD.**

(54) **Hierarchical data processing system**

(57) A circuit arrangement for process automation by means of a hierarchical data processing system can be used in fields where high reliability and security are required. Enhancement is effected of the reliability and security of a hierarchical data processing system wherein single and multiple errors in different 'm-from-n' computer structures in a level or plane and multiple errors in different levels or planes are tolerated. Multiple errors which are not tolerated can be detected. Data transmission between the individual levels or planes is included in the majority decision. Using modular 'm-from-n' decision means ensures universal application of the redundancy principle within the hierarchy. Each computer has an input/output unit (4) arranged at an input thereof, the unit (4) comprising first and second direction switching means (1,3) and an 'm-from-n' decision means (2).

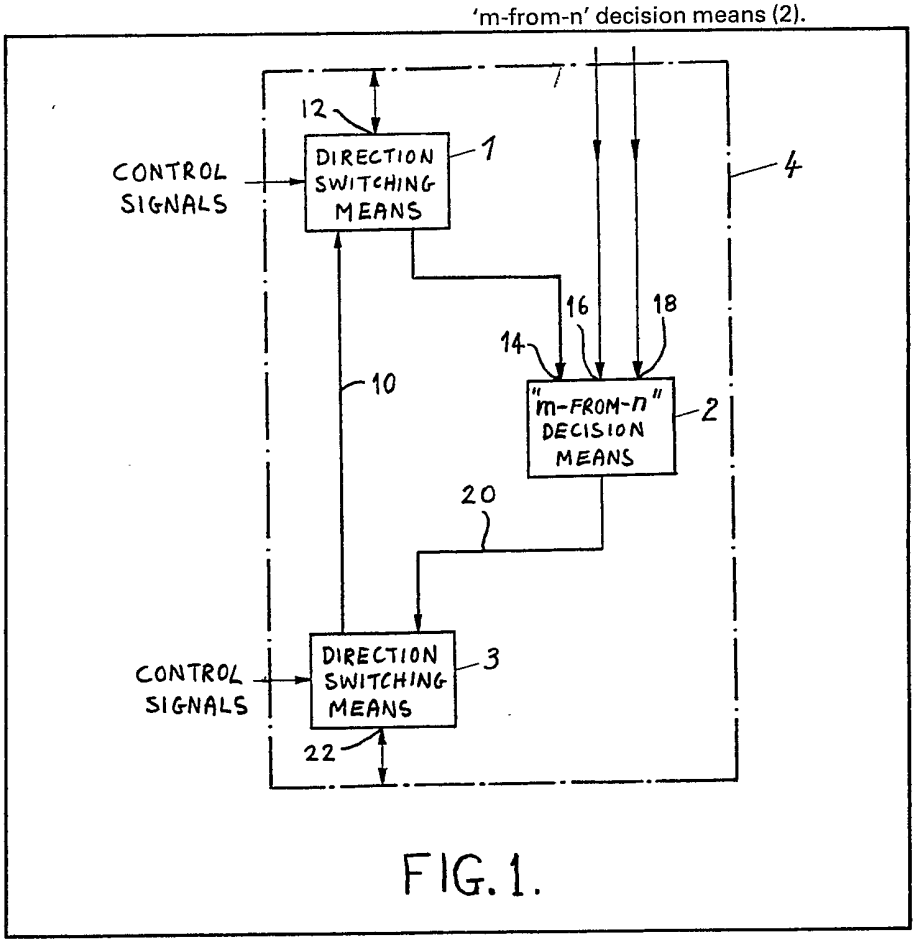

FIG. 1.

GB 2 095 877 A

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

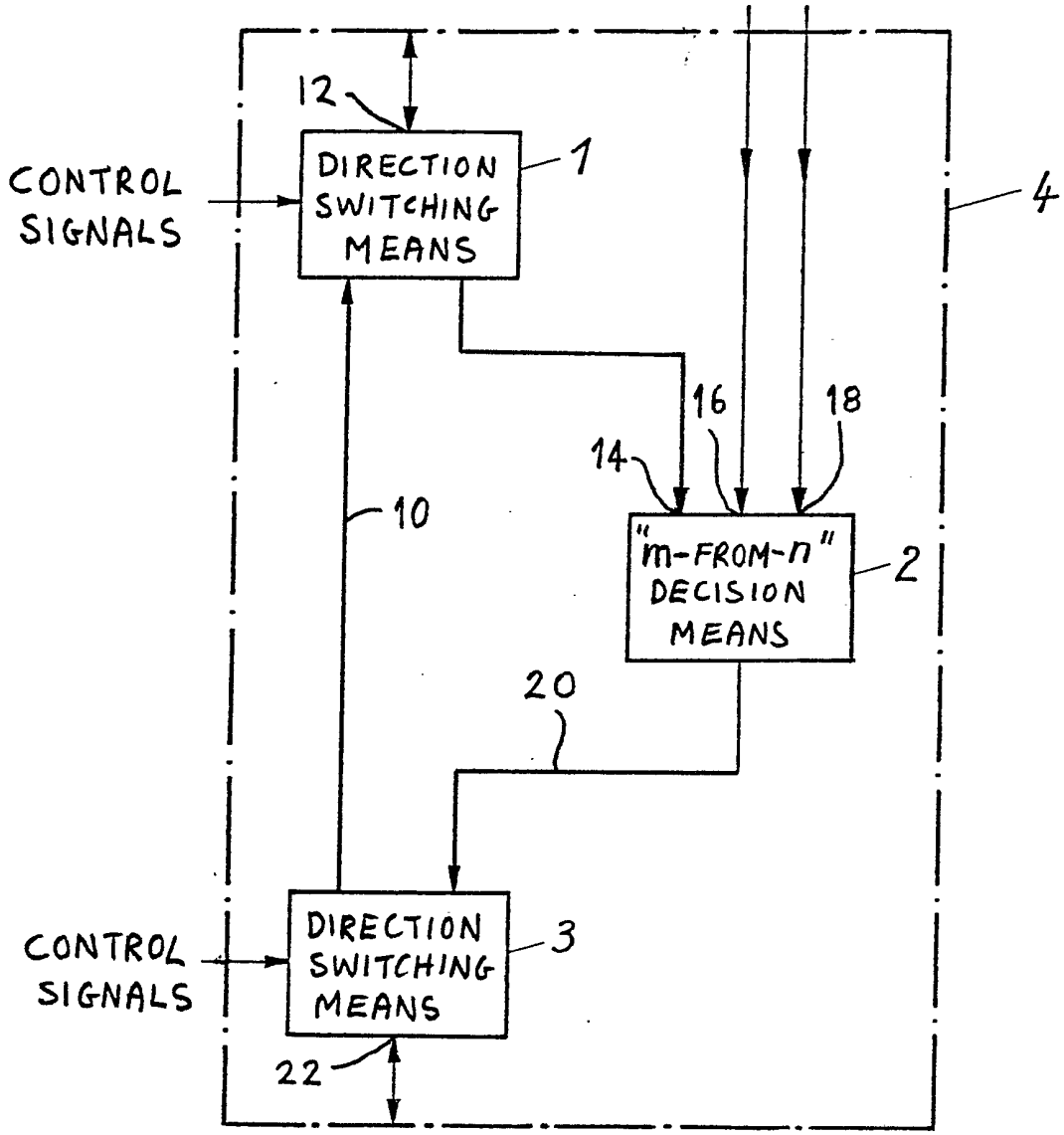
12
CONTROL SIGNALS
DIRECTION SWITCHING MEANS
1
4
16
18
14
10
"m-FROM-n" DECISION MEANS
2
20
CONTROL SIGNALS
DIRECTION SWITCHING MEANS
3
22

FIG. 1.

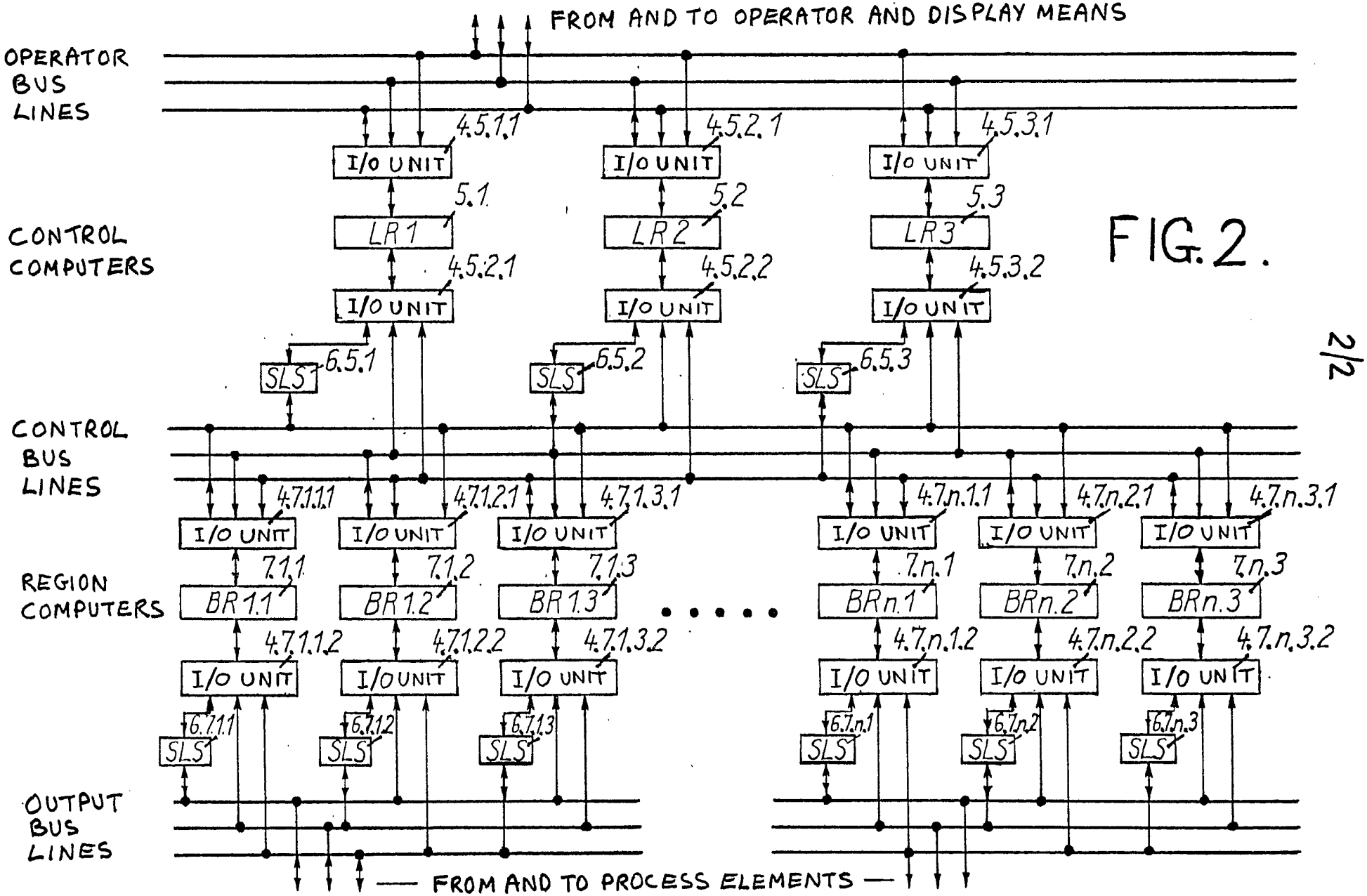
FROM AND TO OPERATOR AND DISPLAY MEANS
OPERATOR BUS LINES
CONTROL COMPUTERS
CONTROL BUS LINES
REGION COMPUTERS
OUTPUT BUS LINES
FROM AND TO PROCESS ELEMENTS
I/O UNIT
LR 1
LR 2
LR 3
SLS
BR 1.1
BR 1.2
BR 1.3
BRn.1
BRn.2
BRn.3
4.5.1.1
4.5.2.1
4.5.3.1
5.1
5.2
5.3
4.5.2.1
4.5.2.2
4.5.3.2
6.5.1
6.5.2
6.5.3
4.7.1.1.1
4.7.1.2.1
4.7.1.3.1
4.7.n.1.1
4.7.n.2.1
4.7.n.3.1
7.1.1
7.1.2
7.1.3
7.n.1
7.n.2
7.n.3
4.7.1.1.2
4.7.1.2.2
4.7.1.3.2
4.7.n.1.2
4.7.n.2.2
4.7.n.3.2
6.7.1.1
6.7.1.2
6.7.1.3
6.7.n.1
6.7.n.2
6.7.n.3

FIG. 2.

2/2

SPECIFICATION

Hierarchical data processing systems

This invention relates to hierarchical data processing systems that can be used, for example, for process automation.

A circuit arrangement is known (Published German Patent Application No. DE-A-2 108 496) wherein three computers operate in parallel. The three computers operate on a monitoring and output means which operates on the principle of majority decision and which, in the event of a fault, isolates or cuts out the defective computer. A computer is deemed to be suffering from a fault if the bit error rate at an output exceeds a given value. For the purpose of monitoring a testing circuit and comparison devices included in the arrangement, intentionally false data is produced by the computer at certain intervals of time. A circuit arrangement of this kind suffers from the disadvantage that, with a hierarchial design, errors on the bus lines are not detected.

A multi-computer system is also known (Published German Patent Application No. DE-B-2 725 922), for controlling line-connected communication equipment, wherein all computers process the same data asynchronously, and wherein the result data are compared together for testing for errors only at the end of a computing cycle. Data is supplied to the individual computers in a time-shifted manner, in order to ensure the asynchronous mode of operation. Output data of the individual computers is checked by means of a comparison and connecting-through device. The comparison operation is only carried out when the majority of the computers have arrived at a result. This operation is performed by a logic circuit which is not of a redundant design, so that errors which may occur within the logic circuit is not detected.

Another disadvantage with both these designs is that there are very high requirements in regard to reliability in respect of the monitoring and output devices, and the transmission of data downstream of the monitoring and output devices is in a single-channel mode.

According to the present invention there is provided a hierarchical data processing system comprising a plurality of computer units including at least one control computer and a plurality of region computers, wherein each computer unit has an input/output unit arranged at an input thereof, each input/output unit comprising an 'm-from-n' decision means and first and second direction switching means, and wherein a unidirectinal output of the second direction switching means is connected to a unidirectional input of the first switching means, control signals of a subordinate and/or a first primary computer are applied to control inputs of the first and the second direction switching means and upon movement in the data direction from the primary to the subordinate computer a bidirectional input/output of the first direction switching means is connected to a bidirectional bus line of the first primary computer and a unidirectional output of the first direction switching means is connected to a first input of the 'm-from-n' decision means, to further inputs of which are applied bidirectional bus lines of further primary computers, and an output of the 'm-from-n' decision means is connected to a unidirectional input of the second direction switching means, a bidirectional input/output of which is connected to a bidirectional bus line of a subordinate computer, and, upon movement in the data direction from the subordinate to the primary computer the bidirectional input/output of the first direction switching means is connected to the bidirectional bus line of a first subordinate computer and the unidirectional output of the first direction switching means is connected to the first input of the 'm-from-n' decision means, to the further inputs of which are applied bidirectional bus lines of further subordinate computers, and the output of the 'm-from-n' decision means is connected to the unidirectional input of the second direction switching means, the bidirectional input/output of which is connected to the bidirectional bus line of a primary computer.

A preferred embodiment of the invention described in detail below provides a circuit arrangement that will tolerate simple and multiple errors in different 'm-from-n' computer structures in one level or plane and multiple errors in different levels or planes in a hierarchical data processing system, and wherein multiple errors which are not tolerated can be detected. The transmission of data between the individual levels or planes is incorporated in the majority decision. The circuit arrangement can be used in fields which impose high requirements in regard to reliability and security.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the acompanying drawings, in which:

Figure 1 is a block diagram of an input/output unit for individual computers of a hierarchical data processing system embodying the invention; and

Figure 2 is a block diagram of the system, which comprises three computers per unit.

Figure 2 of the drawings shows an automation installation which is of a hierarchical construction. Associated with region, zone or area computers (BR) 7.1.1, ... 7.m.3 is a closed or terminated region, zone or area of a technological installation, e.g. for process control, while a control, main or pilot computer unit or arrangement comprising individual computers (LR) 5.1, ... 5.3 gives control instructions which are processed in detailed form in the computers 7.1.1, ... 7.n.3 to form control signals for individual technological units of equipment. In the opposite direction, data passes from the technological units of equipment (feedback signals) to the region computers and is there taken into consideration in further program performance and generally transmitted in condensed form to the control computers 5.1, ... 5.3. In this respect, it is possible for individual items of data from the process to be fed directly to the computers 5.1, ... 5.3, bypassing the computers 7.1.1, ... 7.n.3.

In the embodiment illustrated, each computer is provided in triplicate, in order to enhance reliability and availability. Each set of three associated computers operate on the same algorithms, while versions

of the program may be processed differently and also in a time-shifted manner. Bidirectional bus lines are provided to effect connections between the individual computer levels or planes. Communication between the three computer units of a level or plane may also be effected by way of the bus lines, which comprise address, control and data lines. When there is a very high level of data density on the bus lines, the communication between the computer units of a level or plane may also be effected by way of separate connections which are connected by way of input/output channels. Any matching of the three computers of a unit to each other that may be required is effected by way of the bus lines or by way of separate lines which are not shown in Figure 2 for the sake of simplicity.

In a different arrangement from that shown in Figure 2, it is also possible to provide more than one control computer unit, such units then also operating on the illustrated control and operator bus lines, while bus line control means (SLS) 6.5.1, ... 6.7.n.3 or the computers themselves must coordinate all the data communication between all computers connected to the bus line in question. The operator bus lines provide within the hierachy the connection between the data processing units and operator and display means or units which comprise, for example, displays, keyboards and the like and provide for communication with the operating personnel. From the lower level or plane of the hierachy, the connection to the process elements is by way of the illustrated output bus lines, each technological region or area having associated therewith a triple output bus line system which operates independently of each other and by way of which process control signals are outputted by the computers 7.1.1, ... 7.n.3 and process feedback signals are received.

The connection between the bus lines and the individual computers is made by way of input/output (I/O) units 4.5.1.1, ... 4.7.n.3.2, the constructional principle of which is shown in Figure 1. Each I/O unit 4 comprises first and second direction switching means 1 and 3 and an 'm-from-n' decision means 2. In the I/O units 4, which are described in more detail below, input signals for the respective computers in question are formed by majority decision from the data of the three associated bus lines.

Use of a modular majority ensures that a failure only has an effect on a narrowly restricted area and thus a defectively produced signal is cut out, on the receiving computer level or plane. That is to say, simple and multiple errors in different 'm-from-n' computer structures in one plane and multiple errors in different planes are tolerated.

Multiple errors which are not tolerated can be detected. Good error location is ensured by the interposition of the 'm-from-n' decision means. In addition, re-matching of a computer after a repair has been effected can be achieved by way of the 'm-from-n' decision means and the bus lines.

Processing of the programs can be effected asynchronously in a computer plane, while the comparison operation is performed synchronously. In the basic block diagram shown in Figure 1, in order to provide for separation into unidirectional connections, both the bidirectional connection to the computers and also that to the bus lines which connect all input/output units 4.5.1.1, ... 4.7.n.3.2, are taken by way of the controlled directional switching means 1,3.

On the assumption that no false data is produced at the outputs of the 'm-from-n' decision means 2 which are connected directly to the three bus lines, if in accordance with the program no input of data is required by way of the redundant bus lines, the first direction switching means 1 can be omitted.

The I/O unit 4 shown in Figure 1 will now be described in more detail. A unidirectional output of the second direction switching means 3 is connected by a line 10 to a unidirectional input of the first direction switching means 1, and control signals of a subordinate and/or a primary computer are applied as shown to control inputs of the first and second direction switching means 1 and 3. In passing in the data direction from the primary to the subordinate or secondary computer, a bidirectional input/output 12 of the first direction switching means 1 is connected to the bidirectional bus line of a first primary computer and a unidirectional output of the first direction switching means 1 is connected to a first input 14 of the 'm-from-n' decision means 2, the bidirectional bus lines of further primary computers being applied to further inputs 16, 18 of the decision means. The output of the 'm-from-n' decision means 2 is connected by a line 20 to a unidirectional input of the second direction switching means 3, a bidirectional input/output 22 of which is connected to the bidirectional bus line of a subordinate or secondary computer. In following the data direction from the secondary computer to the primary computer, the bidirectional input/output 12 of the first direction switching means 1 is connected to the bidirectional bus line of the first subordinate computer. The unidirectional output of the first direction switching means 1 is connected to the first input 14 of the 'm-from-n' decision means 2, the bidirectional bus lines of the further subordinate computers being applied to the further inputs 16, 18 of the decision means. The output of the 'm-from-n' decision means 2 is connected to the unidirectional input/output 22 of which is connected to the bidirectional bus line of a primary computer.

The 'm-from-n' decision means 2 may comprise a read only memory, a multiplexer or programmable logic fields.

CLAIMS

1. A hierachical data processing system comprising a plurality of computer units including at least one control computer and a plurality of region computers, wherein each computer unit has an input/output unit arranged at an input thereof, each input/output unit comprising an 'm-from-n' decision means and first and second direction switching means, and wherein a unidirectional output of the second direction switching means is connected to a unidirectional input of the first switching means, control signals of a subordinate and/or a first

primary computer are applied to control inputs of the first and second direction switching means and upon movement in the data direction from the primary to the subordinate computer a bidirectional input/output of the first direction switching means is connected to a bidirectional bus line of the first primary computer and a unidirectional output of the first direction switching means is connected to a first input of the 'm-from-n' decision means, to further inputs of which are applied bidirectional bus lines of further primary computers, and an output of the 'm-from-n' decision means is connected to a unidirectional input of the second direction switching means, a bidirectional input/output of which is connected to a bidirectional bus line of a subordinate computer, and, upon movement in the data direction from the subordinate to the primary computer the bidirectional input/output of the first direction switching means is connected to the bidirectional bus line of a first subordinate computer and the unidirectional output of the first direction switching means is connected to the first input of the 'm-from-n' decison means, to the further inputs of which are applied bidirectional bus lines of further subordinate computers, and the output of the 'm-from-n' decision means is connected to the unidirectional input of the second direction switching means, the bidirection input/output of which is connected to the bidirectional bus line of a primary computer.

2. A system according to claim 1, wherein each 'm-from-n' decision means comprises a read only memory.

3. A system according to claim 1, wherein each 'm-from-n' decision means comprises a multiplexer.

4. A system according to claim 1, wherein each 'm-from-n' decision means comprises programmable logic fields.

5. A hierarchical data processing system substantially as herein described with reference to the accompanying drawings.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1982.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.