

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 November 2007 (08.11.2007)

PCT

(10) International Publication Number
WO 2007/127491 A2

(51) International Patent Classification: **Not classified**

(21) International Application Number:
PCT/US2007/010703

(22) International Filing Date: 30 April 2007 (30.04.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/398,167 5 April 2006 (05.04.2006) US
11/398,168 5 April 2006 (05.04.2006) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 11/398,167 (CON)
Filed on 5 April 2006 (05.04.2006)

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, ZA, ZM, ZW.

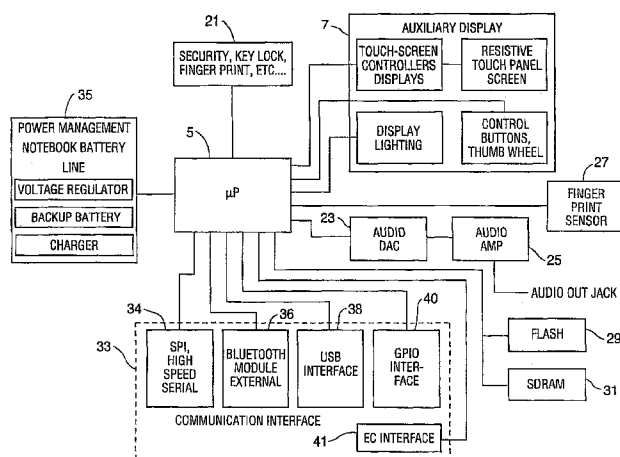
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- without international search report and to be republished upon receipt of that report
- the filing date of the international application is within two months from the date of expiration of the priority period

[Continued on next page]

(54) Title: DATA DISPLAY FROM AUXILIARY DISPLAY SUBSYSTEM



(57) **Abstract:** In some embodiments, a notebook including a main display, a main graphics subsystem, and an auxiliary display subsystem, but typically not an auxiliary display, wherein the notebook is configured to display on the main display one or both of data from the auxiliary display subsystem (or a scaled or otherwise processed version of such data), and data from the main graphics subsystem. Preferably, the notebook is configured to display a scaled version of data from the auxiliary display subsystem on part of the main display's screen. Other embodiments are timing controllers and other circuitry for use in such a notebook and methods for displaying data from such a notebook's auxiliary display subsystem on all or part of the main display's screen. The notebook can include a timing control subsystem for asserting to the main display one or both of display data from the auxiliary display subsystem (or a processed version thereof) and display data from the main graphics subsystem. The timing control subsystem can include a scaler for receiving raw auxiliary display data and a multiplexer having inputs for receiving the output of the scaler and display data from the main graphics subsystem.

WO 2007/127491 A2



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DATA DISPLAY FROM AUXILIARY DISPLAY SUBSYSTEM

5 Cross-reference to Related Application

This application is related to the U.S. Patent Application entitled "Method and System for Communication Between a Secondary Processor and an Auxiliary Display Subsystem of a Notebook" by Aleksandr Frid, assigned to the assignee of the present application and filed on the same day as the present application.

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Field

The writing pertains to methods and systems (e.g., notebook computers) for displaying data asserted by an auxiliary display subsystem of a notebook. In some
15 embodiments, the invention is a notebook (having a main display, a graphics chipset or other main graphics subsystem, and an auxiliary display subsystem) configured to display (on the main display) data from the auxiliary display subsystem or data from the main graphics subsystem. Broadly, this writing discloses methods and systems for displaying data from auxiliary display subsystem of a notebook on a main display of the notebook.

20

Background

The expression "notebook" herein denotes a notebook computer, tablet PC, PDA (personal digital assistant), smart cellular phone (e.g., one capable of playing and displaying multimedia content), or other portable computer or computing system
25 having a central processing unit ("CPU").

The expression "auxiliary display subsystem" herein denotes a subsystem of a notebook that is configured to receive data (and typically cache the received data) from at least one other element of the notebook and to perform (while the notebook is in a standby state or other low-power state) at least one function that at least one other
30 element of the notebook (external to the auxiliary display subsystem) could perform if the notebook were in a fully-powered normal operating mode. Examples of such functions include displaying cached video, still picture, or other image data (received from an element of the notebook external to the auxiliary display subsystem) or a

processed version of such cached data on an auxiliary display, or causing such cached data or a processed version thereof to be displayed on all or part of the screen of the notebook's main display; playing back cached audio data (received from an element of the notebook external to the auxiliary display subsystem) or a processed version of such cached data; displaying system information (e.g., information regarding charge level of a battery of the notebook, or information regarding the notebook's state) on an auxiliary display or causing such system information to be displayed on all or part of the screen of the notebook's main display; and answering incoming telephone calls.

The expression "auxiliary display" herein denotes a display of the auxiliary display subsystem which is distinct from the main display of the notebook in which the auxiliary display subsystem is included. Some embodiments of an auxiliary display subsystem do not include an auxiliary display, and instead are coupled and configured to cause the display of data on all or part of the screen of the main display of the notebook including the auxiliary display subsystem (e.g., while the notebook is in a standby state or other low-power state).

The expression "secondary processor" of a notebook (having a central processing unit) shall be used herein to denote any processor of the notebook other than the notebook's CPU. Examples of secondary processors of conventional notebook computers are embedded controllers (e.g., embedded controllers that perform keyboard controller functions as well as other functions).

The acronym "SMB" herein denotes the conventional, two-wire bus known as the "System Management Bus." The most recent version of the SMB is described in the System Management Bus (SMB) Specification, Version 2.0, published on August 3, 2000, and available at <http://www.smbus.org/specs>.

The expression that a notebook is in a "low-power state" herein denotes that the notebook is operating in a state in which it consumes less power than if it were in a fully-powered, normal operating mode. Examples of low-power states are hibernation and standby states. Typically, a notebook has been booted up (and its central processing unit runs operating system software) when operating in a fully-powered normal operating state, but a notebook must perform a booting operation in order to undergo a transition from a low-power state to a fully-powered normal operating state.

It has been proposed that a notebook include an auxiliary display subsystem for caching data received from other elements of the notebook and displaying the cached data on an auxiliary display.

For example, US Patent Application 2004/0225901 (published on November 11, 2004) discloses an auxiliary display system for use with a main computer (a personal computer or other computing device). The auxiliary display subsystem includes an auxiliary display, a memory, an auxiliary processor, and input devices, is operable while the main computer is in a standby state (e.g., to record voicemail, receive an incoming phone call, or play music), and is said to be capable of waking up the main computer while the main computer is in a standby state. The auxiliary display system can execute applications alone (without the main computer) or "in concert" with the main computer's "main processor." In some implementations, the main computer has a main monitor, and the auxiliary display system is apparently configured to direct "display messages" to the auxiliary display or to forward them for display on the main monitor.

US Patent Application 2004/0222978 (published on November 11, 2004) discloses a control and communications panel for use with a main computer. The control and communications panel can include an auxiliary display, an auxiliary processor, and controls, and can be operable (e.g., to perform telephone or other communication functions) while elements of the main computer are powered down.

US Patent Application 2004/0224638 (published November 11, 2004) discloses a notebook with a built-in docking station for receiving a detachable media player having an auxiliary display and at least one data port (e.g., a USB port) for receiving image, audio, or other data from the notebook or sending data to the notebook. US Application 2004/0224638 suggests generally that communication between the media player and notebook could be one way or two way, and could implement a master/slave, server/client, peer to peer, or other protocol.

US Patent Application 2005/0076088 (published on April 7, 2005) teaches a notebook (or other computer system) having a main display and a detachable module (having a processor, memory, auxiliary display, and input devices such as a fingerprint reader) mounted on the back of the notebook's main display. The detachable module can communicate with the notebook's main processor via a processor bus or communications link (e.g., to wake up the main processor). The detachable module can also perform functions such as displaying email, accessing contact and calendar information, and playing music files (apparently by accessing data previously cached, so as to be accessible by the detachable module, at a time when the notebook was fully

powered up and booted up) when the notebook is in a "quiescent low power mode" without the need to boot up the notebook and load its operating system.

Summary

5 In a class of embodiments, the invention is a notebook including a display (to be referred to herein sometimes as a "main" display), a main graphics subsystem (e.g., graphics chipset), and an auxiliary display subsystem, but not an auxiliary display. In some embodiments, the notebook is configured to display auxiliary display data on a portion (e.g., a relatively small window) of the main display's screen. In typical
10 embodiments, the notebook is configured to be operable (e.g., while in a standby state or other low-power state) to display auxiliary display data on all or part of the main display's screen, or (e.g., while in a fully powered state) to display data from the main graphics subsystem on the main display's screen. In some embodiments, the notebook is configured to display auxiliary display data, and display data from the main graphics
15 subsystem, on different parts of the main display's screen.

 Herein, the phrase "auxiliary display data" denotes raw auxiliary display data generated by an auxiliary display subsystem of a notebook, or a scaled or otherwise processed version of such raw auxiliary display data.

 In typical embodiments, the notebook includes a timing control subsystem (e.g.,
20 a timing controller) configured to assert to the main display (with proper timing) either display data from the main graphics subsystem or auxiliary display data. For example, the timing control subsystem can be coupled and configured to receive raw display data from the auxiliary display subsystem ("raw auxiliary display data") and display data from the main graphics subsystem ("main display data"), to generate auxiliary display
25 data from the raw auxiliary display data (e.g., by scaling the raw auxiliary display data), and to assert either the auxiliary display data (e.g., scaled data), raw auxiliary display data, or main display data to the main display with timing for display on all or a selected portion of the main display's screen (e.g., for display of the auxiliary display data on a selected region of the main display's screen). In some implementations, the
30 timing control subsystem is configured to combine (i.e., multiplex) the auxiliary display data with at least some of the main display data and to assert the combined data to the main display (e.g., for display of the auxiliary display data in a small region of the main display's screen and main display data on another region of the screen). In a class of embodiments, the raw auxiliary display data are asserted to the timing control

subsystem over a first link (e.g., an LVDS link), and the main display data are asserted to the timing control subsystem over a second link of the same type as the first link.

The timing control subsystem can include a scaler coupled to receive raw auxiliary display data and a multiplexer having an input coupled to receive the output
5 of the scaler, a second input coupled to receive main display data, and an output coupled to the main display. The multiplexer is configured to assert at its output either the data received at its first input or the data received at its second input. Optionally, the multiplexer is also operable to combine (i.e., multiplex) the auxiliary display data received at its first input with at least some of the main display data received at its
10 second input and to assert the combined data at its output (e.g., for display of the auxiliary display data in a small region of the main display's screen and main display data on another region of the screen).

In a class of preferred embodiments, the main display is an LCD array whose liquid crystal cells are backlit by an array of illumination elements (e.g., LEDs) that are
15 selectively and individually powerable. In other preferred embodiments, the main display has an array of pixels (light-emitting elements) that are selectively and individually powerable, or an array of pixels of which rows and columns are selectively and individually powerable.

In preferred embodiments, the notebook is configured to display auxiliary
20 display data on the main display while in a standby state or other low-power state. In these embodiments, the main display preferably has an array of pixels (light-emitting elements) that are selectively and individually powerable while the notebook is in a low-power state (or an array of pixels of which rows and columns are selectively and individually powerable while the notebook is in a low-power state), and the main
25 display is controlled (in a low-power state of the notebook) to power only pixels needed to display the auxiliary display data (or only rows and columns that include pixels needed to display the auxiliary display data).

Other aspects of the invention are circuitry (e.g., circuits useful as subsystems of notebooks, or timing controllers) for implementing any embodiment of the inventive
30 notebook, and methods for displaying data from an auxiliary display subsystem of a notebook on all or part of the screen of a main display of the notebook.

Brief Description of the Drawings

Fig. 1 is a block diagram of an embodiment of a notebook which includes an auxiliary display subsystem (personal media display system or "PMD" 3) coupled to an embedded controller (EC/KBC 11) of the notebook. EC/KBC 11 functions as a keyboard controller of the notebook. PMD 3 is also coupled by a USB (universal serial bus) to PC chipset 9 of the notebook.

Fig. 2 is a block diagram of a typical implementation of PMD 3 of Fig. 1.

Fig. 3 is a block diagram of an embodiment of the inventive notebook which includes an auxiliary display subsystem (PMD 103), a main graphics subsystem (graphics chipset 15), and a timing controller (108) configured to assert display data from microprocessor 5 of PMD 103 (or a scaled or otherwise processed version of such data) and/or from chipset 15 to main display 107 with timing for display on all or a selected portion of main display 107's screen.

Fig. 4 is a block diagram of a subsystem of the notebook Fig. 3, including elements of an implementation of timing controller 108.

Fig. 5 is a simplified side cross-sectional view of a main display (LCD panel 207) that can be included in an embodiment of the inventive notebook, showing elements of the Fig. 4 subsystem coupled thereto.

Fig. 6 is a front view of the screen (210) of main display 207 of Fig. 5, showing some pixels 211 thereof.

Detailed Description of Preferred Embodiments

In some embodiments of the invention, a conventional System Management Bus (SMB) is used as the underlying transport layer for communications between an auxiliary display subsystem and a secondary processor of a notebook. The bus protocols implemented by some embodiments of the invention for communication over an SMB between an auxiliary display subsystem and a secondary processor are compliant with the above-cited System Management Bus (SMB) Specification, Version 2.0. Notation used herein for SMB protocol description is consistent with that employed in the cited System Management Bus (SMB) Specification, Version 2.0.

Fig. 1 is a block diagram of notebook computer ("notebook") 1 which includes conventional PC chipset 9 (including a CPU which runs notebook 1's operating system software when notebook 1 has been booted up into its fully-powered normal operating mode), graphics chipset 15, main display 17, keyboard 13, and embedded controller (EC/KBC 11), connected as shown. EC/KBC 11 is of a conventional type which

functions as a keyboard controller. As shown, EC/KBC 11 is coupled to chipset 9 by a conventional low pin count ("LPC") bus, but in alternative implementations is coupled to chipset 9 by other means (e.g., by a conventional ISA bus or other bus). EC/KBC 11 is also coupled to keyboard 13 (e.g., by a conventional 26-pin cable) and typically also
5 to other elements (not shown in Fig. 1) of notebook 1.

Notebook 1 also includes an auxiliary display subsystem (personal media display system 3, to be referred to as "PMD" 3), which includes microprocessor 5 ("auxiliary processor" 5), auxiliary display 7 (coupled to and driven by microprocessor 5), and typically also other elements (to be described below). Microprocessor 5 is
10 coupled by an SMB to embedded controller (EC/KBC) 11 for communication with EC/KBC 11 when EC/KBC 11 is conventionally configured to operate as an SMB host. Microprocessor 5 is coupled by a conventional USB (universal serial bus) to PC chipset 9 for communication with PC chipset 9. Typically, microprocessor 5 communicates with EC/KBC 11 over the SMB when chipset 9 is in a low-power state (e.g., a standby
15 or hibernation state) or when chipset 9 is fully awake (and in a state in which it consumes full power), and microprocessor 5 communicates with chipset 9 over the USB when chipset 9 is fully awake (and in a state in which it consumes full power).

Notebook 1 typically includes elements (not shown in Fig. 1) in addition to those shown in Fig. 1. For example, it can include a smart battery (coupled to EC/KBC
20 11 by an SMB) and a smart battery charger (also coupled to EC/KBC 11 by an SMB).

PMD 3 typically also includes other elements (not shown in Fig. 1). For example, PMD 3 typically includes input devices (e.g., control buttons and a biometric sensor) and a memory. PMD 3 is typically configured to cache data received from other elements of notebook 1 as a result of communication over the USB between
25 microprocessor 5 and PC chipset 9. PMD 3 is typically configured to display such cached data (in the case that the cached data are video or other image data) on auxiliary display 7 and to play back the cached data (in the case that the cached data are audio data) on loudspeakers (not shown) of notebook 1. PMD 3 is typically also configured to display (on auxiliary display 7) system status data received by microprocessor 5 from
30 EC/KBC 11 over the SMB.

Examples of system status data that can be received by PMD 3 (e.g., for display on auxiliary display 7) from the non-PMD portion of notebook 1 (e.g., from EC/KBC 11 as described below) include indications that notebook 1 is on, off, shutting down, or powering up, indications that notebook 1 is in a standby, suspended, or hibernation

state, indications that a battery of notebook 1 is charging or discharging, indications of the charge level of a battery of notebook 1, low battery alarms, indications that communication with the non-PMD portion of notebook 1 is in progress, notifications that the non-PMD portion of notebook 1 has received new email, and current time and date updates.

PMD 3 can also be configured to perform, while PC chipset 9 is in a standby or other low-power state, other functions (e.g., answering incoming telephone calls) that other elements of notebook 1 could perform if notebook 1 were in a fully-powered, normal operating state. When PC chipset 9 is in a low-power state, other major power-consuming elements of notebook 1 (e.g., main display 17) are typically off or in a standby or other low-power state so that notebook 1 as a whole is in a low-power state. Preferably, microprocessor 5 and other elements of PMD 3 are implemented to consume less power (preferably, much less power) than consumed by the elements of notebook 1 other than PMD 3 in a fully-powered, normal operating state. Thus, a user can employ PMD 3 to conserve power while performing useful functions of notebook 1 (while notebook 1 is in a low-power state), without the need to cause notebook 1's CPU (implemented by PC chipset 9) to boot up (which would typically consume significant time).

Functions that can be performed by various embodiments of PMD 3 include cached music file playing (with optional equalization, sample rate conversion, or other audio post processing), display of cached picture slide shows (e.g., on auxiliary display 7), display of world clock, time, and date information, stop watch functionality, display of contact lists, email, reminder memos, timed memos, task lists, battery and other information regarding notebook 1 and users thereof (e.g., user name and information, system information, manufacturer, serial number and model number, OEM support, technical contact information, and logos), password/screen lock support functions, system functions (e.g., placing notebook in an on, off, hibernation, standby, or suspend state), and lid-closed notebook system and application control functions.

Fig. 2 is a block diagram of a typical implementation of PMD 3 of Fig. 1. In the Fig. 2 implementation, microprocessor 5 is a dual core, ARM-based microprocessor implemented to consume low power (e.g., to operate for 50 hours on power drawn from an AA battery), auxiliary display 7 includes touch-screen controller, a resistive touch panel screen, display lighting, and control buttons and a thumb wheel, connected as shown. Typically, when notebook 1 has the size and physical form of a conventional

notebook computer (and thus includes a keyboard section and a cover attached by hinges to the keyboard section, with the main display installed to be visible from the cover's front surface), PMD 3 is installed in the notebook computer's cover with the touch panel screen, control buttons, and thumb wheel of auxiliary display 7 accessible
5 from the cover's back surface (so as to be accessible when the cover's front surface is folded against the keyboard section to protect the main display).

In the Fig. 2 implementation, PMD 3 includes communication interface subsystem 33 (coupled to microprocessor 5), which can include high speed serial interface 34, Bluetooth module 36, USB interface 38 (configured to be coupled by USB
10 conductors to PC chipset 9), GPIO interface 40, and EC interface 41 (configured to be coupled by SMB conductors to EC/KBC 11), and other interface circuitry (e.g., RF, 802.11, Ethernet, and/or IR interface circuitry). In the Fig. 2 implementation, microprocessor 5 includes an internal boot block ROM (not separately shown), and PMD 3 includes NOR/NAND flash memory 29 and SRAM/SDRAM 31, security input
15 device 21 (e.g., a key lock), audio DAC 23, and fingerprint sensor 27, all coupled to microprocessor 5. Audio amplifier 25 is coupled to the output of DAC 23 for amplifying the analog audio that is output from DAC 23, and amplifier 25 can drive speakers which are external to PMD 3 (e.g., headphones plugged into a connector of PMD 3).

20 Fingerprint sensor 27 is used to authenticate users of PMD 3, using user identity data cached in memory (e.g., memory 29 or 31) of PMD 3. When typically programmed, PMD 3 can be placed in a locked state in which it can be unlocked by an authorized user only after PMD 3 successfully authenticates the user (even while notebook 1 is in a standby state or other low-power state, and without waking up
25 notebook 1) including by comparing user biometric data (e.g., a fingerprint) with cached biometric data.

In the Fig. 2 implementation, PMD 3 also includes analog power management circuitry 35 coupled to microprocessor 5. Circuitry 35 includes at least one voltage regulator (e.g., voltage regulators for regulating each of a 2.9 Volt digital supply
30 voltage, a 2.9 Volt analog supply voltage, a peripheral supply voltage in the range 1.7 to 3.3 Volts, an RTC supply voltage in the range 1 Volt to 2.5 Volts, and a 3.26 Volt USB transceiver voltage), a battery charger, a backup battery, and a DC-to-DC converter for providing a 3.2 or 3.4 V output in response to an input voltage in the range from 1.0 Volt to 3.3 Volts.

PMD 3 is typically configured to cache (e.g., in memory 29 and/or memory 31) data received from other elements of notebook 1 as a result of communication over the USB between microprocessor 5 and PC chipset 9. PMD 3 is typically configured to display such cached data (in the case that the cached data are video or other image data) on auxiliary display 7 and to play back the cached data (in the case that the cached data are audio data) on loudspeakers (not shown) of notebook 1. PMD 3 is typically also configured to display (on auxiliary display 7) system status data received by microprocessor 5 from EC/KBC 11 over the SMB. Microprocessor 5 (and other elements of PMD 3) can also be configured to implement digital rights management (e.g., to decrypt content received from elements of notebook 1 external to PMD 3, and to store, in read-only memory, unique identification data for digital rights management algorithms).

PMD 3 is typically also configured to perform one or more of the following functions:

provide low power, instant access to music and multimedia content cached in memory (e.g., memory 29 and/or memory 31) of PMD 3 and other information (e.g., critical information) cached in memory of PMD 3 (e.g., frequently used information transferred from other elements of notebook 1 and cached in PMD 3 before notebook 1 enters a standby or other low-power state);

allow a user to control notebook 1 with the cover of main display 17 closed (e.g., by waking up notebook 1 and controlling notebook 1 by actuating controls on or associated with auxiliary display 7, while main display 17 is covered and thus protected and unavailable); and

provide other functionality such as generating alarms (e.g., for elapsed time or scheduled events, or low battery alarms indicating that notebook 1's battery is nearly discharged), implementing user authentication (or other security functions) preliminary to booting of notebook 1's CPU, collecting and monitoring system diagnostics data (e.g., data indicating whether notebook 1 is shutting down, powering up, whether notebook 1 is in an on, off, standby, suspended, or hibernation state, whether notebook 1's battery is charging/discharging, and the charge level of notebook 1's battery), and communicating with notebook 1's operating system software regarding system power management policies.

Microprocessor 5 is preferably programmed with firmware for executing appropriate functions and with software for executing functions including the

following: boot block (e.g., for initializing microprocessor 5's CPU and PMD 3's flash memory 29 and other memory, authenticating a firmware boot loader in PMD 3's flash memory 29, and loading and executing a firmware boot loader), boot loader support (stored in PMD 3's flash memory 29, for authenticating firmware and device drivers and executing firmware), firmware kernel, file system, graphic tool kit, and drivers (e.g., USB, SMB, I2S, display controller, touch screen, and JTAG debugger support).

Several elements of the Fig. 2 implementation of PMD 3 (e.g., microprocessor 5 and circuitry 23, 25, and 35) can be and preferably are integrated in a single chip.

Any device on an SMB has a unique 7-bit address. In a conventional notebook architecture, the embedded controller which functions as keyboard controller (e.g., EC/KBC 11 of Fig. 1) is conventionally assigned SMB host device address 0001_000b.

In a class of implementations of Fig. 1, microprocessor 5 is assigned SMB device address 1000_101b as a default address for receiving messages over the SMB, and embedded controller (EC/KBC) 11 is assigned SMB host device address 0001_000b for receiving messages over the SMB. Preferably, notebook 1 is implemented so that if another device with the address 1000_101b is connected to the same SMB segment as is microprocessor 5, the default address for microprocessor 5 can be reprogrammed in firmware.

Typical SMB messages sent from microprocessor 5 (an SMB device acting as bus master) to EC/KBC 11 (an SMB host controller acting as bus slave) include data requests and action requests of any of the types described below.

In some embodiments, microprocessor 5 (an SMB device acting as bus master) sends messages to EC/KBC 11 (an SMB host controller acting as bus slave) in accordance with the SMB host notify protocol described in the above-cited SMB specification. In accordance with this protocol, the SMB device master can send to the SMB host controller (functioning as an SMB slave) 16-bit messages (each preceded by two 8-bit words that indicate the target and sending device addresses, with transmission of each 8-bit word followed by an "acknowledge" bit) in the following format:

1	7	1	1	7	1	1	8	1	8	1	1
S	Target Address	Wr	A	Sending Device Address		A	Data Byte Low	A	Data Byte High	A	P
	SMB Host Address	0	0	PMD Address	0	0	Command	0	Sub-Command	0	

In the previous paragraph, "S" denotes the conventional SMB "start condition" which the transmitter of the message (the SMB device master) must assert on the SMB to indicate the start of transmission of a message comprising a number of 8-bit packets separated by "acknowledge" bits, "Wr" denotes a command bit (whose bit value is 0 during transmission in accordance with the host notify protocol), "A" denotes an acknowledge bit (whose value is 0 for an ACK and 1 for a NACK), "P" denotes the conventional SMB "stop condition" which the message transmitter asserts on the SMB to indicate the end of transmission of a message, and the two 8-bit words "Data Byte Low" and "Data Byte High" are the body of the message. The 8-bit sending device address indicates to the message recipient (the SMB host controller slave) the origin of the message.

Depending on the command field value (the above-indicated 8-bit word "Data Byte Low"), all messages from microprocessor 5 to EC/KBC 11 can be divided into two categories: data requests and action requests.

In some embodiments, data requests (asserted from microprocessor 5 to EC/KBC 11) have the format indicated in Tables 1 and 2 below. Table 1 indicates the format of each data request's command field value (the above-indicated 8-bit word "Data Byte Low"), and Table 2 indicates the format of each data request's sub-command field value (the above-indicated 8-bit word "Data Byte High") and bits 3:0 of the data request's command field.

Table 1. Data Request Commands

Command Field Bit(s)	Description
7:5	Requestor Tag 000b – Invalid Others – Assigned by microprocessor 5 (no context for EC/KBC 11)
4	Message Type 0b – Data Request
3:0	Command Code 0h – EC Capabilities 1h – System Status 2h – Battery Information Others – Reserved

Table 2. Data Request Sub-Commands

Command Field	Sub-	Description
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Bits 3:0	Command Field Bit(s)	
0h	7:0	Reserved (00h)
1h	7:0	Reserved (00h)
2h	7:4	Battery Slot Tag 0h – Battery Slot 0 1h – Battery Slot 1 2h – Battery Slot 2 3h – Battery Slot 3 Others – Reserved
	3:0	Battery Information 0h – Battery Slot Status and Capacity Gauge 1h – Battery Voltage 2h – Battery Remaining Time to Empty 3h – Battery Charging/Discharging Rate 4h – Battery Remaining Capacity 5h – Battery Last Full Charge Capacity 6h – Battery Design Capacity 7h-Bh – Reserved Ch – Battery Manufacturer Name Dh – Battery Model Eh – Battery Type Fh – Reserved

In accordance with some embodiments, action requests (asserted from microprocessor 5 to EC/KBC 11) have the format indicated in Tables 3 and 4 below.

- 5 Table 3 indicates the format of each action request's command field value (the above-indicated 8-bit word "Data Byte Low"), and Table 4 indicates the format of each action request's sub-command field value (the above-indicated 8-bit word "Data Byte High") and bits 3:0 of the action request's command field.

Table 3. Action Request Commands

Command Field Bit(s)	Description
7:5	Requestor Tag 000b – Invalid Others – Assigned by microprocessor 5 (no context for EC/KBC 11)
4	Message Type 1b – Action Request
3:0	Command Code 0h – EC/KBC GPIO Control 1h – System Sleep State control 2h – Generate System Wake Event

	3h – Generate System Run Time Event Others – Reserved
--	--

Table 4. Action Request Sub-Commands

Command Field Bits 3:0	Sub- Command Field Bit(s)	Description
0h	7:6	Reserved (00b)
	5:4	Requested GPIO state 00b – Output Low 01b – Output High 1Xb – Input
	3:0	EC/KBC GPIO number (mapping of this number to EC/KBC 11's physical GPIO is preferably done by EC/KBC firmware) 00h-0Fh – GPIO0-GPIO15
1h	7:0	Requested System Sleep State 00h – Invalid 01h – ACPI S1 state (Standby) 02h – ACPI S2 State 03h – ACPI S3 State (Suspend to RAM) 04h – ACPI S4 State (Suspend to Disk, Hibernation) 05h – ACPI S5 State (System is Off) 06h – User defined state (emulate power/sleep button event) Others – Reserved
2h	7:0	PMD Wake Event ID reported by EC/KBC 11 to PC chipset 9 of notebook 1 00h-FFh – ID0-ID255
3h	7:0	PMD Run Time Event ID reported by EC/KBC 11 to PC chipset 9 of notebook 1 00h-FFh – ID0-ID255

In Tables 3 and 4, "GPIO" denotes "general purpose input/output." Action requests having the values indicated in Tables 3 and 4 in their command and sub-command fields can be asserted over the SMB to EC/KBC 11 to cause EC/KBC 11 to assert values (indicated by the messages) on specific GPIO pins of EC/KBC 11 (indicated by the messages) to control other elements of the notebook. The GPIO connections (to the elements of the notebook to be controlled) could be of a type present in a conventional notebook, but they are controlled in some embodiments of the present invention by action requests asserted from PMD 3 over an SMB (or another serial bus, in alternative embodiments) to EC/KBC 11 (or another embedded controller). For example (in one embodiment), microprocessor 5 of PMD 3 could assert action request messages over the SMB of Fig. 1 (or Fig. 3) to EC/KBC 11 to

cause EC/KBC 11 to assert control bits (indicated by the messages) on specific GPIO lines (also indicated by the messages) to an audio amplifier of the notebook, where such amplifier (not shown in the Figures) is coupled in a conventional manner to EC/KBC 11 by such GPIO lines.

5 In variations on the notebook of Fig. 1, action requests of the described type could be asserted over an SMB to a keyboard controller ("KBC") in a keyboard ("KB"), or similar action requests could be asserted over another two-wire serial bus to a KBC in a KB, from a microprocessor of an auxiliary display subsystem to control the KBC. The KBC could also be coupled by another two-wire serial bus to an embedded
10 controller (EC) so that either the EC or the microprocessor of the auxiliary display subsystem could control the KBC over the two-wire serial bus (thereby eliminating the need for a 26-wire cable or other bulky cable between the KBC, external to the KB but possibly internal to an EC, and the KB).

We next describe messages sent over the SMB from EC/KBC 11 (an SMB host
15 controller acting as bus master) to microprocessor 5 (an SMB device acting as bus slave). In some embodiments, the SMB write block protocol with the following format is used for all messages sent over the SMB from EC/KBC 11 (acting as bus master) to microprocessor 5. In accordance with this protocol, the SMB host controller master can send to microprocessor 5 (functioning as an SMB slave) $N \times 8$ -bit messages (where N is
20 an integer), each preceded by three 8-bit words that indicate microprocessor 5's address, a data report command, and a message byte count (indicative of the value of N), with transmission of each 8-bit word followed by an "acknowledge" bit) in the following format:

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command	A	Byte Count	A	Data Byte 1	A	...
	PMD Address	0	0	Data Report Command	0	$N (2-32)$	0	Sub-Command	0	

8	1	8	1		8	1	8	1	1
Data Byte 2	A	Data Byte 3	A	...	Data Byte N	A	PEC ¹	A	P
Report Status	0	Report Data	0		Report Data	0		0	

In the previous paragraph, "S" denotes the conventional SMB "start condition" which the transmitter of the message (the SMB host controller acting as bus master) must assert on the SMB to indicate the start of transmission of a message comprising a number of 8-bit packets separated by "acknowledge" bits, "Wr" denotes a command bit
 5 (whose bit value is 0 during transmission in accordance with the write block protocol), "A" denotes an acknowledge bit (whose value is 0 for an ACK and 1 for a NACK), "PEC" is a Packet Error Code, "P" denotes the conventional SMB "stop condition" which the message transmitter asserts on the SMB to indicate the end of transmission of a message, and the N 8-bit words "Data Byte" are the body of the message. The 7-bit
 10 slave address is the address of microprocessor 5. The Packet Error Code (PEC) byte is an optional CRC-8 error checking byte, and if included, it is appended after the last Data Byte of the message body and its usage is consistent with the PEC support bit included in an EC Capabilities Report (see Table 8 below).

Messages having the above-described format that are sent over the SMB from
 15 EC/KBC 11 (acting as bus master) to microprocessor 5 (acting as bus slave) are Data Report messages (each comprising N bytes that follow three initial address, command, and message byte count bytes), with the first byte of each N-byte message being a sub-command (i.e., the sub-command field of the Data Report Message), and the second
 20 byte of each N-byte message being a Report Status byte. A non-zero value of the Report Status byte indicates report failure. If the Report Status byte has a zero value, the report data transferred in the subsequent bytes of the message provide system information according to the command and sub-command fields.

The command byte transmitted following the address byte is sometimes denoted herein as the Command field of the Data Report Message. The content of the Command
 25 and Sub-Command fields of Data Report Messages from EC/KBC 11 is summarized in Table 5 and Table 6 below.

Table 5. Data Report Commands

Command Field Bit(s)	Description
7:5	Requestor Tag 000b – No requestor (message initiated by EC/KBC 11 itself) Others – Same as in the PMD data request which triggered the report (used internally by microprocessor 5 to properly route the report)
4	Message Type 0b – Data Report

3:0	Command Code 0h – EC Capabilities 1h – System Status 2h – Battery Information Others – Reserved
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Table 6. Data Report Sub-Commands

Command Field Bits 3:0	Sub-Command Field Bit(s)	Description
0h	7:0	Reserved (00h)
1h	7:0	Reserved (00h)
2h	7:4	Battery Slot Tag 0h – Battery Slot 0 1h – Battery Slot 1 2h – Battery Slot 2 3h – Battery Slot 3 Others – Reserved
	4:0	Battery Information 0h – Battery Slot Status and Capacity Gauge 1h – Battery Voltage 2h – Battery Remaining Time to Empty 3h – Battery Charging/Discharging Rate 4h – Battery Remaining Capacity 5h – Battery Last Full Charge Capacity 6h – Battery Design Capacity 7h-Bh – Reserved Ch – Battery Manufacturer Name Dh – Battery Model Eh – Battery Type Fh – Reserved

- 5 The Command and Sub-Command fields for each Data Report message from EC/KBC 11 are the same as the respective fields in the above-described data requests from microprocessor 5 with one exception: a “no requestor” tag can be specified if a Data Report is initiated by EC/KBC 11 itself (and is not a response to a data request from microprocessor 5).

- 10 Table 7 specifies values of the Report Status byte (the above-described second byte) of each N-byte Data Report message, and allowable Byte Count values that correspond to each value of the Report Status byte.

Table 7. Data Report Status and Byte Count

Report Status	Byte Count	Description
00h	3-32	Report Successful. Following the Report Status byte, at least one data byte is, and as many as 30 data bytes are, returned according to the command and subcommand fields
01h	2	Report Failed: attempt to access unsupported battery slot, or access to empty slot. A Battery Slot Status report must be returned successfully even for an empty slot. The "battery present flag" should be cleared in this case.
02h	2	Report Failed: unknown data
0FFh	2	Report Failed: any other reason than described above
Others	2	Reserved

No data is reported by failed report (no data bytes follow a Report Status byte having a non-zero value). Data fields for all successful Data Reports from EC/KBC 11 are defined below (the requestor tag for all report examples below is set to 001b).

- 5 Table 8 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of an "EC Capabilities" Data Report message (indicated in Tables 1 and 5 above).

Table 8. EC Capabilities Data Report

SMB Protocol Byte	Value	Note
Command Byte	20h	
Byte Count	08h	
Data Byte 1 (Sub-Command)	00h	
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Version Number (10h = version 1.0)	Indicates the specification version with which EC/KBC 11 is compliant (the major version is specified in the high nibble, the minor version in the low nibble)
Data Byte 4	GPIO allocation	Number of GPIO pins of EC/KBC 11 that are allocated for PMD control (up to 16)
Data Byte 5	Battery System Configuration	See Table 9
Data Byte 6	Supported System Sleep States	See Table 10
Data Byte 7	Reserved (00h)	

Data Byte 8	Reserved (00h)	
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Table 9. Battery System Configuration

Battery System Configuration Bit(s)	Description
7:5	Reserved (000b)
4	PEC Support bit 0b – EC/KBC messages to microprocessor 5 do not use a protocol with PEC 1b – EC/KBC messages to microprocessor 5 use a protocol with PEC
3:0	Number Battery Slots (maximum number of batteries in the system) 0h – Invalid 1h – One Battery Slot 0 2h – Two Battery Slots 1 and 2 3h – Three Battery Slots 0, 1 and 2 4h – Four Battery Slots 0, 1, 2 and 3 Others – Reserved

Table 10. System Sleep States Support

System Sleep State Support Bit(s)	Description
7	Reserved (0b)
6	User defined state (emulate power/sleep button event)
5	ACPI S5 state (System Is Off)
4	ACPI S4 state (Suspend to Disk, Hibernation)
3	ACPI S3 state (Suspend to RAM)
2	ACPI S2 state
1	ACPI S1 state (Standby) 0b – Sleep state is not supported 1b – Sleep state is supported
0	Reserved (0b)

Table 11 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "System Status" Data Report message (indicated in Tables 1 and 5 above).

5 Table 11. System Status Report

SMB Protocol Byte	Value	Note
Command Byte	21h	
Byte Count	08h	
Data Byte 1 (Sub-Command)	00h	
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	System State Bits 7-0	See Table 12
Data Byte 4	System State Bits 15-8	See Table 12
Data Byte 5	GPIO State Bits 7-0	Each bit 15-0 returns the state of the respective GPIO pin, GPIO15-GPIO0. Non supported GPIOs should be reported as "0."
Data Byte 6	GPIO State Bits 15-8	
Data Byte 7	Reserved (00h)	
Data Byte 8	Reserved (00h)	

Table 12. System State Flags

System State Bit(s)	Description
15 14 13 12	Battery in Slot 3 Present Battery in Slot 2 Present Battery in Slot 1 Present Battery in Slot 0 Present 0b – Battery is not present in the respective Slot 1b – Battery is present in the respective Slot
11:6	Reserved (000000b)
5	LID State 0b – LID closed 1b – LID open
4	AC Present 0b – No AC (Battery Power) 1b – AC Present
3:0	System Power State 0h – ACPI S0 state (System is On) 1h – ACPI S1 state (Standby) 2h – ACPI S2 State 3h – ACPI S3 State (Suspend to RAM) 4h – ACPI S4 State (Suspend to Disk, Hibernation) 5h – ACPI S5 State (System is Off) Others – Reserved

10 Table 13 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report

message (indicated in Tables 1 and 5 above) of the "Slot Status and Capacity Gauge" type (indicated in Table 6 above).

Table 13. Battery Information (Slot Status and Capacity Gauge) Report

SMB Protocol Byte	Value	Note
Command Byte	22h	
Byte Count	04h	
Data Byte 1 (Sub-Command)	X0h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Battery Slot Status	See Table 14
Data Byte 4	Battery Capacity Gauge	Battery's relative remaining capacity in %

5

Table 14. Battery Slot Status

Status Bit(s)	Description
7:5	Reserved (000b)
4	Discharging Alarm 0b – No alarm 1b – Alarm is set
3	Charging Alarm 0b – No alarm 1b – Alarm is set
2:1	Charging state 00b – Battery is idle (self-discharging) 01b – Battery is being charged 10b – Battery is being discharged (powering the system) 11b – Reserved
0	Present State 0b – Battery is not present in the respective slot 1b – Battery is present in the respective slot

10 Table 15 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Voltage" type (indicated in Table 6 above).

Table 15. Battery Voltage Report

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	04h	
Data Byte 1 (Sub-Command)	X1h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1

		X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Present Voltage Bits 7-0	Battery's present voltage (16-bit unsigned value, in [mV])
Data Byte 4	Present Voltage Bits 15-8	

- Table 16 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Remaining Time to Empty" type (indicated in Table 6 above).

Table 16. Battery Remaining Time to Empty Report

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	04h	
Data Byte 1 (Sub-Command)	X2h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Time to Empty Bits 7-0	Estimated remaining time to empty for discharging battery at present rate (in [min]) Report 0FFFFh if battery is not discharging
Data Byte 4	Time to Empty Bits 15-8	

- Table 17 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Charging/Discharging Rate" type (indicated in Table 6 above).

Table 17. Battery Charging/Discharging Rate Report

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	06h	
Data Byte 1 (Sub-Command)	X3h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Rate Bits 7-0	Battery's charging/discharging rate (24-bit unsigned value in specified <i>Rate Units</i> ; direction is reported in Slot Status).
Data Byte 4	Rate Bits 15-8	
Data Byte 5	Rate Bits 23-16	
Data Byte 6	<i>Rate Units</i>	00h = [mW] 01h = [mA]

		02h = [10mW]
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- Table 18 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Remaining Capacity" type (indicated in Table 6 above).

Table 18. Battery Remaining Capacity

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	06h	
Data Byte 1 (Sub-Command)	X4h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Capacity Bits 7-0	Battery's remaining capacity (24-bit unsigned value in specified <i>Capacity Units</i>)
Data Byte 4	Capacity Bits 15-8	
Data Byte 5	Capacity Bits 23-16	
Data Byte 6	<i>Capacity Units</i>	00h = [mWh] 01h = [mAh] 02h = [10mWh]

- Table 19 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Last Full Charge Capacity" type (indicated in Table 6 above).

Table 19. Battery Last Full Charge Capacity

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	06h	
Data Byte 1 (Sub-Command)	X5h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Capacity Bits 7-0	Battery's capacity when fully charged last time (24-bit unsigned value in specified <i>Capacity Units</i>)
Data Byte 4	Capacity Bits 15-8	
Data Byte 5	Capacity Bits 23-16	
Data Byte 6	<i>Capacity Units</i>	00h = [mWh] 01h = [mAh] 02h = [10mWh]

Table 20 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Design Capacity" type (indicated in Table 6 above).

5

Table 20. Battery Design Capacity

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	06h	
Data Byte 1 (Sub-Command)	X6h	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3	Capacity Bits 7-0	Battery's design (24-bit unsigned value in specified <i>Capacity Units</i>)
Data Byte 4	Capacity Bits 15-8	
Data Byte 5	Capacity Bits 23-16	
Data Byte 6	<i>Capacity Units</i>	00h = [mWh] 01h = [mAh] 02h = [10mWh]

Table 21 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Manufacturer" type (indicated in Table 6 above).

10

Table 21. Battery Manufacturer Report

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	N = 03h-20h	
Data Byte 1 (Sub-Command)	XCh	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3 – Data Byte N	ASCII string	Manufacturer name is up to 30 characters (may not be null-terminated)

15

Table 22 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Model" type (indicated in Table 6 above).

Table 22. Battery Model Report

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	N = 03h-20h	
Data Byte 1 (Sub-Command)	XDh	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3 – Data Byte N	ASCII string	Battery model is up to 30 characters (may not be null-terminated)

Table 23 specifies value for the Command and Sub-command fields, Byte Count and Report Status bytes, and data bytes of a "Battery Information" Data Report message (indicated in Tables 1 and 5 above) of the "Battery Type" type (indicated in Table 6 above).

Table 23. Battery Type Report

SMB Protocol Byte	Description	Note
Command Byte	22h	
Byte Count	N = 03h-20h	
Data Byte 1 (Sub-Command)	XEh	X = 0h for Battery in Slot 0 X = 1h for Battery in Slot 1 X = 2h for Battery in Slot 2 X = 3h for Battery in Slot 3
Data Byte 2 (Report Status)	00h	Successful
Data Byte 3 – Data Byte N	ASCII string	Battery type (commonly battery chemistry) is up to 30 characters (may not be null-terminated).

In some embodiments, EC/KBC 11 is configured to follow the following behavioral rules for communication with microprocessor 5 over the SMB:

- After Power On Reset, EC/KBC 11 is ready to accept PMD request messages over the SMB and respond to them as soon as possible with the following time-out limits:
 - After an EC Capabilities Request is received, the responsive EC Capabilities Report is sent over the SMB within 25 ms,
 - After a System Status Request is received, the responsive System Status Report is sent over the SMB within 25 ms,
 - After any Battery Information Request is received, the respective Data Report is sent over the SMB within 50 ms, and

- Action Requests are executed immediately upon receipt.
- After Power On Reset, EC/KBC 11 does not initiate any report messages (although it may send report messages in response to requests from microprocessor 5) until a first System Status Report is successfully sent in response to request therefore from microprocessor 5.
- After the first System Status Report has been sent, EC/KBC 11 will initiate subsequent System Status Reports by itself whenever any status information changes (e.g., if a battery is connected or removed, or system sleep state changes, etc.). In some implementations, there is an exception to this rule: in the case that GPIO state is changed by EC/KBC 11 in response to a GPIO control action request from microprocessor 5, EC/KBC 11 may not generate a System Status Report.
- EC/KBC 11 is configured to handle the case that a new Data Request is received from microprocessor 5 before EC/KBC 11 has sent one or more previously requested Data Reports in response to one or more previous Data Requests. In some implementations, EC/KBC 11 responds with one Data Report to all duplicated Data Requests (with the same command and sub-commands fields).

Notebook 100 of Fig. 3 is an embodiment of the inventive notebook which includes an auxiliary display subsystem (PMD 103) coupled by an SMB or I2C bus to an embedded controller (EC/KBC 11) of notebook 100. All elements of Fig. 3 that correspond to identical elements of above-described Fig. 1 are numbered identically in Figs. 1 and 3, and the description thereof will not be repeated with reference to Fig. 3.

Notebook 100 differs from notebook 1 in that PMD 103 of notebook 100 does not include its own auxiliary display. PMD 103 generates display data of the same type that are displayed on auxiliary display 7 of notebook 1, but sends the display data to timing controller 108 (following optional processing) with proper timing for display on all or part of the screen of main display 107. Main display 107 of notebook 100 can be identical to main display 17 of notebook 1, but is coupled to receive display data from timing controller 108 rather than display data directly from graphics chipset 15. Alternatively, main display 107 is replaced by a main display that includes timing controller 108 and an array of pixels (backlit liquid crystal cells or other light-emitting

elements), and timing controller 108 asserts display data to the pixels (or column drivers or other pixel driving circuitry) of the main display.

Timing controller 108 is configured to be operable in a mode in which it generates display data from raw display data asserted thereto by microprocessor 105 (e.g., by scaling the raw display data) and asserts the scaled data with timing for display on the screen of display 107 (e.g., in a small region of the screen of display 107), and also to be operable to assert display data from graphics chipset 15 for display on the screen of display 107. Optionally, timing controller 108 is configured to be operable in a mode in which it combines (multiplexes) display data from microprocessor 105 (or a scaled version of such data) with display data from graphics chipset 15 (e.g., so that data from microprocessor 105 or a scaled version thereof can be displayed in a small region of display 107's screen, while display data from graphics chipset 15 is displayed on the rest of display 107's screen).

Preferably, display 107 is an LCD of a type whose pixels (individual backlit liquid crystal cells) can be independently lit (e.g., independently backlit by independently controllable LEDs or other light sources) or a display of another type whose pixels can be independently powered and lit (e.g., independently backlit by independently controllable LEDs or other light sources). In such preferred embodiments, microprocessor 105 generates display data and asserts the display data (e.g., as 8-bit display data over a parallel link, or as serial data over an LVDS, or "low voltage differential signaling," serial link) for display in only a small region of the screen of display 107, and timing controller 108 asserts the display data (or a scaled version thereof) to the screen of display 107 with appropriate timing for display in the appropriate small region of display 107's screen. Microprocessor 105 is preferably configured to power only the pixels of display 107's screen in the region in which the display data from PMD 103 are to be displayed, thereby conserving power (e.g., when notebook 100 is in a sleep or other low-power state).

In the case that microprocessor 105 of PMD 103 is coupled by an SMB to EC/KBC 11, microprocessor 105 can be identical to microprocessor 5 of Fig. 1. In this case, messages are preferably sent between microprocessor 105 and EC/KBC 11 in the format described above with reference to Tables 1-23. In the case that microprocessor 105 of PMD 103 is coupled by an I2C bus to EC/KBC 11, messages of the same type described above with reference to Tables 1-23 can be sent between microprocessor 105

and EC/KBC 11 in an appropriate format that will be apparent to those of ordinary skill in the art in view of the description herein.

In the implementation shown in Fig. 4, timing controller 108 includes scaling circuit ("scaler") 58 and multiplexer 59, connected as shown. Scaler 58 is coupled and
5 configured to generate display data by scaling raw display data asserted thereto (as serial data over an LVDS link, or over another link) from microprocessor 105, and to assert the display data over an LVDS link (or other link) to multiplexer 59. In some
embodiments, scaler 58 is operable (under control of microprocessor 105) in at least
10 two modes: a mode in which it downscales the raw display data both horizontally and vertically; and a mode in which it passes through the raw display data without scaling it. Multiplexer 59 has an input coupled to receive the display data output from scaler
58, a second input coupled to receive display data asserted by graphics chipset 15 over an LVDS link (or other link) between chipset 15 and multiplexer 59, and an output
coupled to main display 107 by an LVDS link (or other link). Multiplexer 59 can be
15 controlled to assert the data it receives from scaler 58 to main display 107 with timing for display in a region (e.g., determined by control bits or other signals from microprocessor 105) of display 107's screen. For example, when no display data are
asserted from graphics chipset 15 to multiplexer 59 (e.g., when notebook elements including PC chipset 9 and graphics chipset 15 are in a standby state or other low-
20 power state), multiplexer 59 can assert the data it receives from scaler 58 to main display 107, with timing for display in a small region of display 107's screen (e.g., with no display of data on the rest of display 107's screen). Multiplexer 59 can be controlled
(e.g., while the notebook is in a fully powered state) to assert the data it receives from graphics chipset 15 (rather than the data it receives from scaler 58) to main display 107
25 with timing for display on display 107's screen.

In some embodiments, multiplexer 59 can be controlled to generate combined data by multiplexing the data received at its inputs, and to assert the combined data to
main display 107 with timing such that when the combined data are displayed on main
display 107, display data from microprocessor 105 (or a scaled version thereof) are
30 displayed in a region (e.g., a small region) of display 107's screen, and display data from graphics chipset 15 are displayed on the rest of display 107's screen.

In alternative embodiments, scaler 58 is omitted and timing controller 108 includes a multiplexer (e.g. multiplexer 59) that can be controlled to assert raw
auxiliary display data it receives from microprocessor 105 (or another element of an

auxiliary display subsystem) to main display 107 for display on display 107's screen. Preferably, such multiplexer can also be controlled (e.g., while the notebook is in a fully powered state) to assert data it receives from graphics chipset 15 (rather than data it receives from the auxiliary display subsystem) to main display 107 with timing for display on display 107's screen.

Main display 107 can be implemented as shown in Figs. 5 and 6 as an LCD panel 207 (to be referred to herein as main display 207). Main display 207 includes an array 201 of LCD cells and an array 202 of LEDs for illuminating the LCD cells of array 201. Each LED of array 202 underlies an LCD cell (or a small number of adjacent LCD cells) of array 201 and is capable of backlighting the LCD cell or cells that it underlies. Array 202 is mounted on printed circuit board (PCB) 203. PCB 203 implements a circuit for independently powering the individual LEDs of array 207. This circuit is controlled by control signals asserted thereto from microprocessor 105. In typical operation in which microprocessor 105 controls scaler 58 and multiplexer 59 to cause the display of scaled data from microprocessor 105 in a region of display 107's screen (i.e., a small region determined by a backlit subset of the LCD cells of array 201), microprocessor 105 asserts control signals to PCB 203 to cause only those LEDs of array 207 that underlie the relevant subset of the LCD cells of array 201 to be powered.

Thus, microprocessor 105 can control the consumption of power by main display 207 to prevent consumption of power by those pixels that are not needed to display scaled data from microprocessor 105 in a region (e.g., a small region) of display 107's screen. With reference to Fig. 6, microprocessor 105 may assert display data to timing controller 108, and control the timing controller 108 to cause the display of scaled version of this data on a region of screen 210 (of display 207) determined by N rows of M columns of the pixels 211 of display 207 (where display 207 has many more than N rows of pixels 211 and many more than M columns of pixels 211). Each pixel 211 is determined by an LCD cell of array 201. Preferably, only those LEDs of array 207 that underlie the relevant subset of LCD cells of array 201 are powered (to backlight those LCD cells) while the scaled data are displayed in the N pixel × M pixel region on display 207's screen.

In other embodiments of the inventive notebook, a main display (e.g., main display 107 of Fig. 4) includes an array of LCD cells and an array of independently controllable light sources (other than LEDs) for backlighting either selected subsets of

the LCD cells or all of the LCD cells of the LCD cell array, and an element of the notebook's auxiliary display subsystem (e.g., microprocessor 105 of Fig. 4) can control the consumption of power by the main display to prevent consumption of power by pixels of the main display that are not needed to display data generated by the auxiliary display subsystem (or a processed version of such data). For example, the auxiliary display subsystem that includes microprocessor 105 of Fig. 4 may prevent consumption of power by pixels of such an implementation of main display 107 that are not needed to display (in a small region of display 107's screen) a scaled version of data generated by the auxiliary display subsystem.

10 In other embodiments of the inventive notebook, a main display (e.g., main display 107 of Fig. 4) is of another type whose pixels can be independently powered and lit (e.g., independently backlit by independently controllable LEDs or other light sources), and an element of the notebook's auxiliary display subsystem (e.g., microprocessor 105 of Fig. 4) can control the consumption of power by main display 15 107 to prevent consumption of power by those pixels of the main display that are not needed to display data generated by the auxiliary display subsystem (or a processed version of such data).

In a class of implementations of the Fig. 4 circuitry, microprocessor 105 (or another element of the auxiliary display subsystem that includes microprocessor 105) 20 generates display data and asserts the display data as serial data over an LVDS serial link for display (or processing followed by display) on the main display of a notebook. In other embodiments, an auxiliary display subsystem generates display data and asserts the display data (e.g., as 8-bit display data, or N-bit display data where N is not equal to 8, over a parallel link, or as serial data over a serial link other than an LVDS 25 link) for display on the main display of a notebook (e.g., in only a small region of the screen of the main display).

In a class of embodiments of the inventive notebook, an auxiliary display subsystem (e.g., microprocessor 105 or another element of the auxiliary display subsystem that includes microprocessor 105) and a main display of the notebook are 30 configured to power selected pixels of the main display in a region of the main display's screen in which data from the auxiliary display subsystem (or a scaled version of such data) are to be displayed, thereby conserving power (e.g., when the notebook is in a sleep or other low-power state).

Another aspect of the invention is a method for displaying auxiliary display data from an auxiliary display subsystem of a notebook on a main display of the notebook, said main display having a screen. The method includes the steps of:

- (a) asserting raw auxiliary display data to a subsystem of the notebook;
- 5 (b) scaling the raw auxiliary display data in said subsystem to generate auxiliary display data; and
- (c) asserting the auxiliary display data to the main display with timing for display on a portion of the screen.

Step (b) can include the step downscaling the raw auxiliary display data to generate the auxiliary display data. All or some of steps (a), (b), and (c) can be performed while the notebook is in a low-power state.

In embodiments in which step (c) includes the steps of asserting the auxiliary display data to a multiplexer and controlling the multiplexer to pass through the auxiliary display data to the main display, the method can also include the steps of: (d) asserting main display data, from a main graphics subsystem of the notebook, to the multiplexer; and (e) controlling the multiplexer to pass through at least some said main display data to the main display. All or some of steps (a), (b), and (c) can be performed while the notebook is in a low-power state, and steps (d) and (e) can be performed while the notebook is in a fully powered state.

As a broad overview, this writing discloses in some embodiments, a notebook including a main display, a main graphics subsystem, and an auxiliary display subsystem, but typically not an auxiliary display, wherein the notebook is configured to display on the main display one or both of data from the auxiliary display subsystem (or a scaled or otherwise processed version of such data), and data from the main graphics subsystem. Preferably, the notebook is configured to display a scaled version of data from the auxiliary display subsystem on part of the main display's screen. Other embodiments are timing controllers and other circuitry for use in such a notebook and methods for displaying data from such a notebook's auxiliary display subsystem on all or part of the main display's screen. The notebook can include a timing control subsystem for asserting to the main display one or both of display data from the auxiliary display subsystem (or a processed version thereof) and display data from the main graphics subsystem. The timing control subsystem can include a scaler for receiving raw auxiliary display data and a multiplexer having inputs for receiving the output of the scaler and display data from the main graphics subsystem.

It should be understood that while some embodiments of the present invention are illustrated and described herein, the invention is defined by the claims and is not to be limited to the specific embodiments described and shown.

CLAIMS

What is claimed is:

1. A notebook, including:
 - 5 a main display having a screen;
 - a timing control subsystem;
 - a main graphics subsystem, coupled and configured to assert main display data to the timing control subsystem; and
 - an auxiliary display subsystem, coupled and configured to assert raw auxiliary display data to the timing control subsystem,
 - 10 wherein the timing control subsystem is operable to assert the main display data to the main display with timing for display on the screen and is operable to assert, in response to the raw auxiliary display data, auxiliary display data to the main display with timing for display on at least a portion of the screen.
- 15 2. The notebook of claim 1, wherein the timing control subsystem includes a scaler coupled to receive the raw auxiliary display data and configured to downscale the raw auxiliary display data to generate the auxiliary display data.
- 20 3. The notebook of claim 2, wherein the timing control subsystem is operable to assert the main display data to the main display with timing for display on at least a first region of the screen, and is also operable to assert the auxiliary display data to the main display with timing for display on a region of the screen that is substantially smaller than the first region.
- 25 4. The notebook of claim 1, wherein the timing control subsystem includes:
 - a scaler coupled to receive the raw auxiliary display data and configured to downscale the raw auxiliary display data to generate the auxiliary display data; and
 - a multiplexer having at least one input coupled to receive the auxiliary display data,
 - 30 data, at least one other input coupled to receive the main display data, and at least one output coupled to the main display.

5. The notebook of claim 4, wherein the multiplexer is operable to assert combined data at the at least one output, wherein the combined data include at least some of the auxiliary display data and at least some of the main display data.

5 6. The notebook of claim 5, wherein the multiplexer is operable to assert the combined data to the main display with timing for display of the auxiliary display data of said combined data on a region of the screen and display of the main display data of said combined data on another region of the screen.

10 7. The notebook of claim 1, wherein the timing control subsystem includes:
a multiplexer having at least one input coupled to receive one of the raw auxiliary display data and the auxiliary display data, at least one other input coupled to receive the main display data, and at least one output coupled to the main display.

15 8. The notebook of claim 1, wherein the timing control subsystem is configured to downscale the raw auxiliary display data to generate the auxiliary display data, and the timing control subsystem is operable to assert the auxiliary display data to the main display with timing for display on a portion of the screen.

20 9. The notebook of claim 1, wherein the auxiliary display data are identical to the raw auxiliary display data.

10. A notebook operable in any one of a fully powered state and at least one low-power state, said notebook including:

25 a main display;
a timing control subsystem coupled to the main display;
a main graphics subsystem, coupled and configured to assert main display data to the timing control subsystem; and
an auxiliary display subsystem, coupled and configured to assert raw auxiliary
30 display data to the timing control subsystem,

wherein the timing control subsystem is configured to be operable when the raw auxiliary display data are asserted thereto and the notebook is in at least one said low-power state, to assert auxiliary display data to the main display with timing for display on said main display.

11. The notebook of claim 10, wherein the timing control subsystem includes a scaler coupled to receive the raw auxiliary display data and configured to downscale the raw auxiliary display data to generate the auxiliary display data.

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12. The notebook of claim 11, wherein the main display has a screen, the timing control subsystem is operable to assert the main display data to the main display with timing for display on at least a first region of the screen, and the timing control subsystem is also operable to assert the auxiliary display data to the main display with timing for display on a region of the screen that is substantially smaller than the first region.

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13. The notebook of claim 10, wherein the timing control subsystem includes: a scaler coupled to receive the raw auxiliary display data and configured to downscale the raw auxiliary display data to generate the auxiliary display data; and a multiplexer having at least one input coupled to receive the auxiliary display data, at least one other input coupled to receive the main display data, and at least one output coupled to the main display.

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14. The notebook of claim 13, wherein the multiplexer is operable to assert combined data at the at least one output, wherein the combined data include at least some of the auxiliary display data and at least some of the main display data.

20

15. The notebook of claim 10, wherein the timing control subsystem includes: a multiplexer having at least one input coupled to receive one of the raw auxiliary display data and the auxiliary display data, at least one other input coupled to receive the main display data, and at least one output coupled to the main display.

25

16. The notebook of claim 10, wherein the main display has a screen, the timing control subsystem is configured to downscale the raw auxiliary display data to generate the auxiliary display data, and the timing control subsystem is operable to assert the auxiliary display data to the main display with timing for display on a portion of the screen.

30

17. The notebook of claim 10, wherein the auxiliary display data are identical to the raw auxiliary display data.

18. A timing control system configured for use in a notebook having a main display, a main graphics subsystem which generates main display data, and an auxiliary display subsystem which generates raw auxiliary display data, said timing control system including:

at least one input configured to be coupled to receive the raw auxiliary display data;

at least one other input configured to be coupled to receive the main display data;

at least one output configured to be coupled to the main display; and circuitry, coupled between each said input and each said output and configured to be operable to assert the main display data to the at least one output with timing for display on a screen of the main display, and to be operable to assert auxiliary display data at said at least one output in response to the raw auxiliary display data with timing for display on at least a portion of the screen.

19. The system of claim 18, wherein said circuitry includes a scaler coupled to the at least one input, said scaler configured to downscale the raw auxiliary display data to generate the auxiliary display data.

20. The system of claim 18, wherein said circuitry includes:

a scaler coupled to the at least one input, said scaler configured to downscale the raw auxiliary display data to generate the auxiliary display data; and

a multiplexer having at least one input coupled to receive the auxiliary display data, and at least one other input coupled to receive the main display data.

21. The system of claim 20, wherein the multiplexer is coupled and configured to be operable to assert combined data at the at least one output, said combined data including at least some of the auxiliary display data and at least some of the main display data.

22. The system of claim 18, wherein said circuitry includes:

a multiplexer having at least one input coupled to receive one of the raw auxiliary display data and the auxiliary display data, and at least one other input coupled to receive the main display data.

5 23. The system of claim 18, wherein said circuitry is configured to downscale the raw auxiliary display data to generate the auxiliary display data, and to assert the auxiliary display data to the at least one output with timing for display on a portion of the screen of the main display.

10 24. The system of claim 18, wherein the auxiliary display data are identical to the raw auxiliary display data.

 25. A method for displaying auxiliary display data from an auxiliary display subsystem of a notebook on a main display of the notebook, said main display having a
15 screen, said method including the steps of:

- (a) asserting raw auxiliary display data to a subsystem of the notebook;
- (b) scaling the raw auxiliary display data in said subsystem to generate auxiliary display data; and
- (c) asserting the auxiliary display data to the main display with timing for
20 display on a portion of the screen.

 26. The method of claim 25, wherein step (b) includes the step of downscaling the raw auxiliary display data to generate the auxiliary display data.

25 27. The method of claim 25, wherein step (c) includes the steps of:
asserting the auxiliary display data to a multiplexer; and
controlling the multiplexer to pass through the auxiliary display data to the main display.

30 28. The method of claim 25, also including the steps of:
(d) asserting main display data, from a main graphics subsystem of the notebook, to the multiplexer; and
(e) controlling the multiplexer to pass through at least some said main display data to the main display.

29. The method of claim 28, wherein step (c) is performed while the notebook is in a low-power state, and steps (d) and (e) are performed while the notebook is in a fully powered state.

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30. The method of claim 29, wherein steps (a), (b), and (c) are performed while the notebook is in the low-power state.

31. The method of claim 25, wherein at least step (c) is performed while the notebook is in a low-power state.

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32. The method of claim 25, wherein steps (a), (b), and (c) are performed while the notebook is in a low-power state.

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1/3

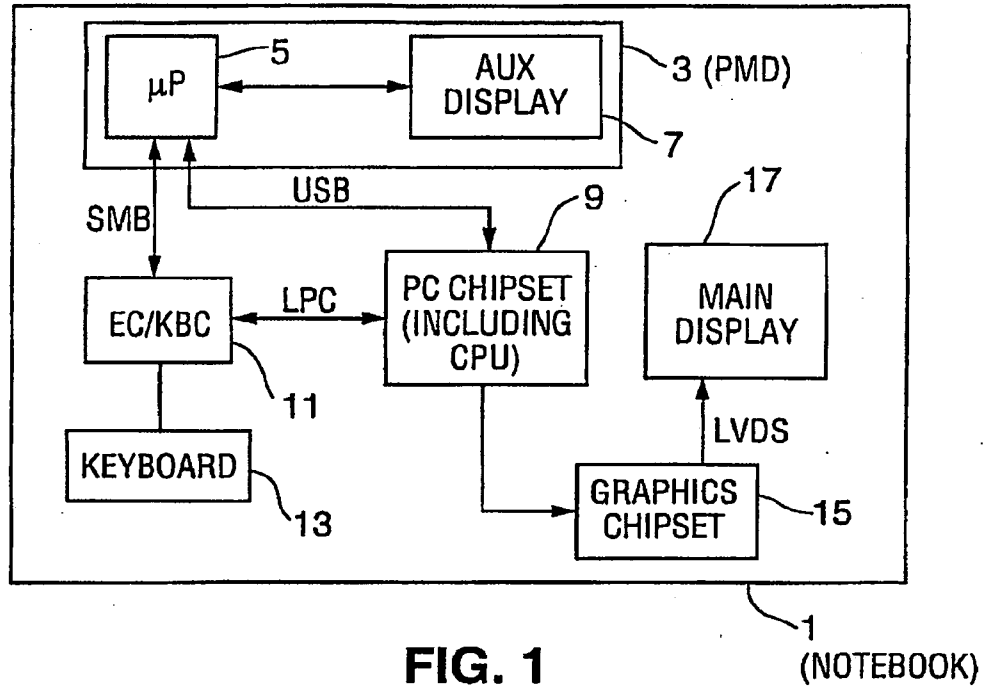


FIG. 1

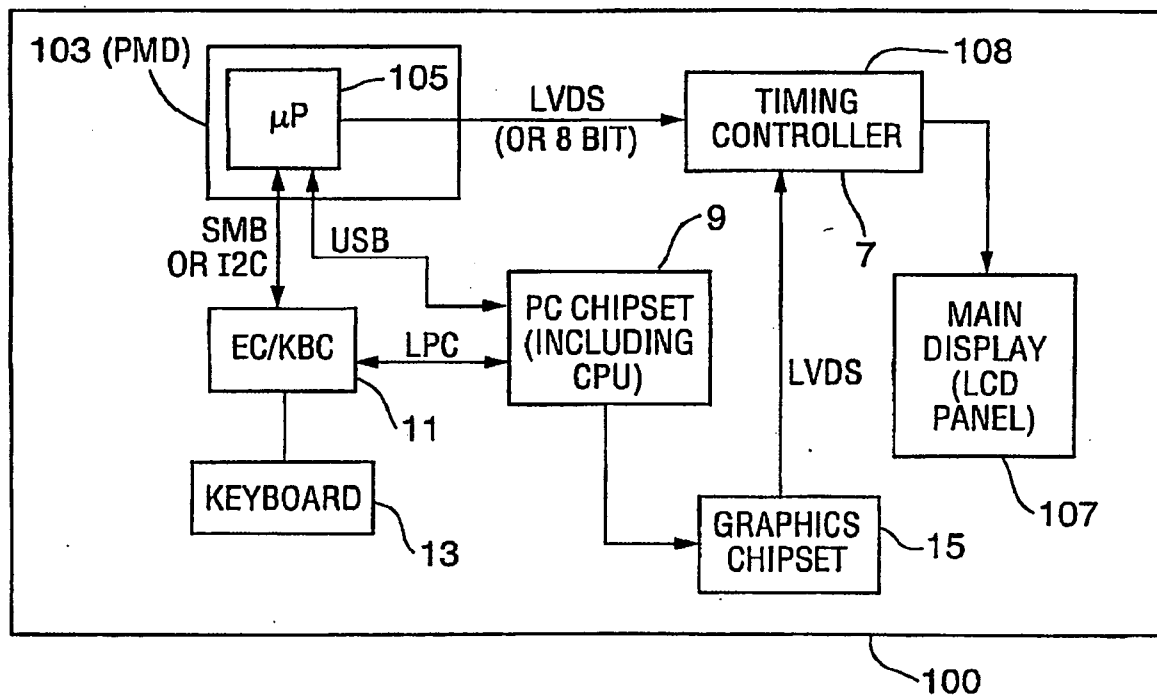


FIG. 3

2/3

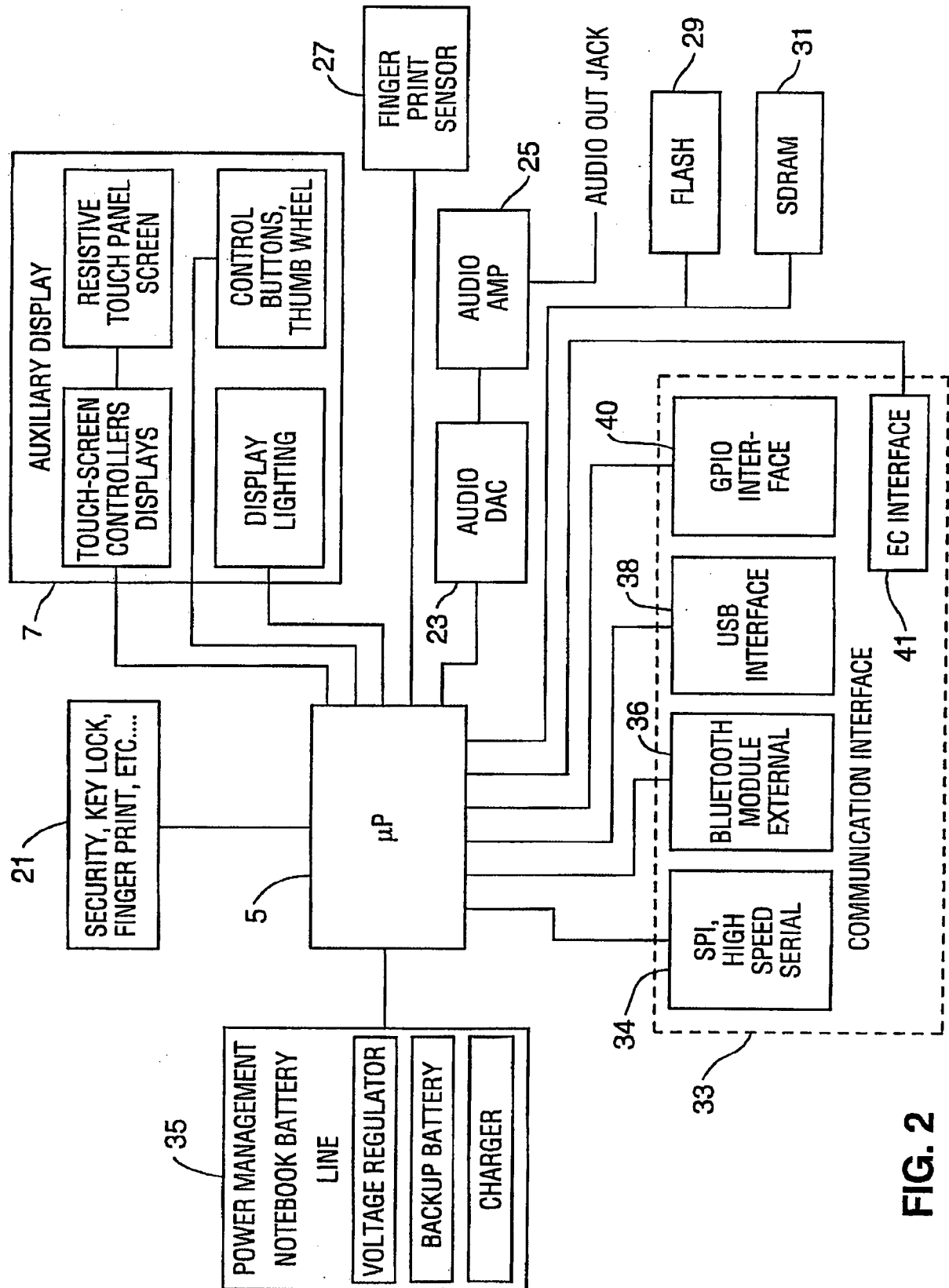
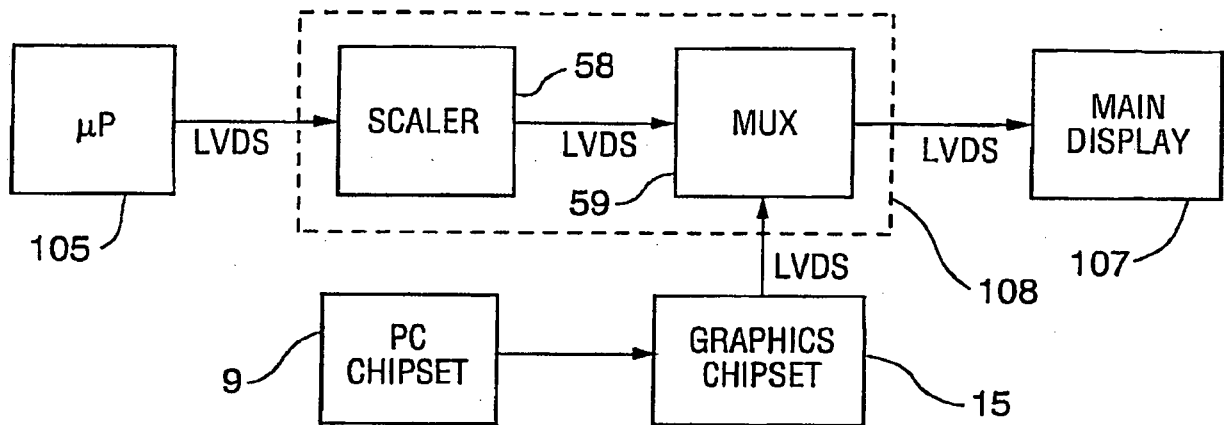
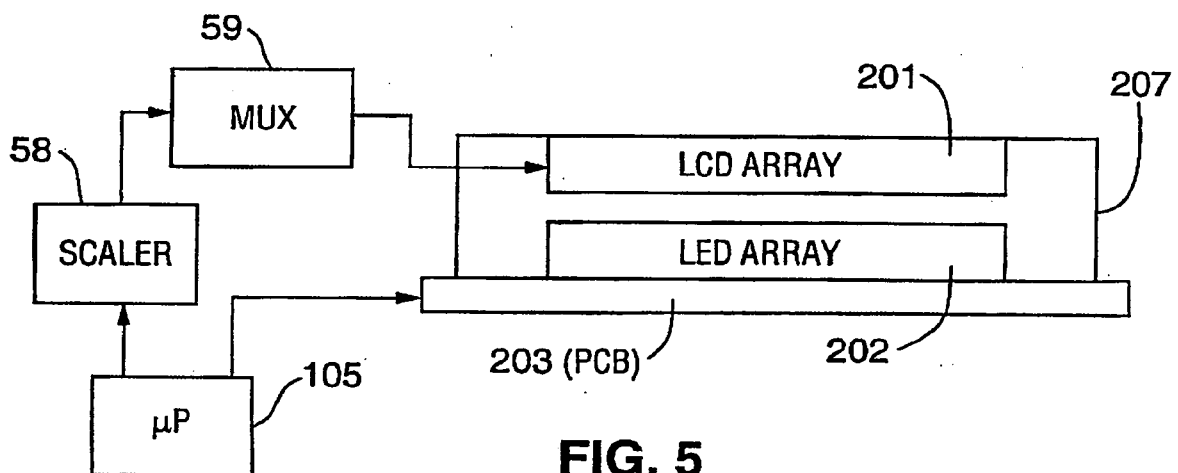
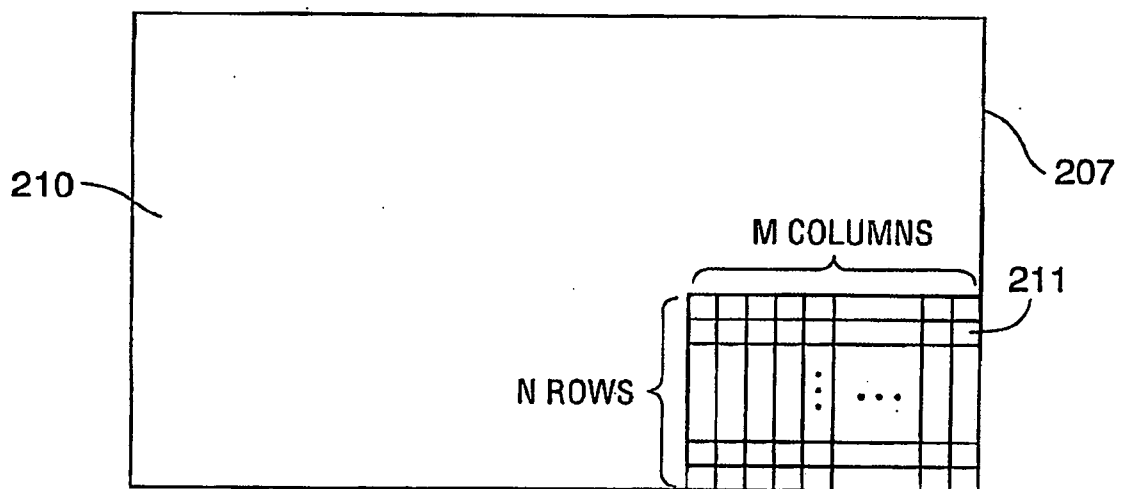


FIG. 2

3/3

**FIG. 4****FIG. 5****FIG. 6**