

(51) International Patent Classification:
H03F 1/30 (2006.01)(21) International Application Number:
PCT/EP2017/069333(22) International Filing Date:
31 July 2017 (31.07.2017)

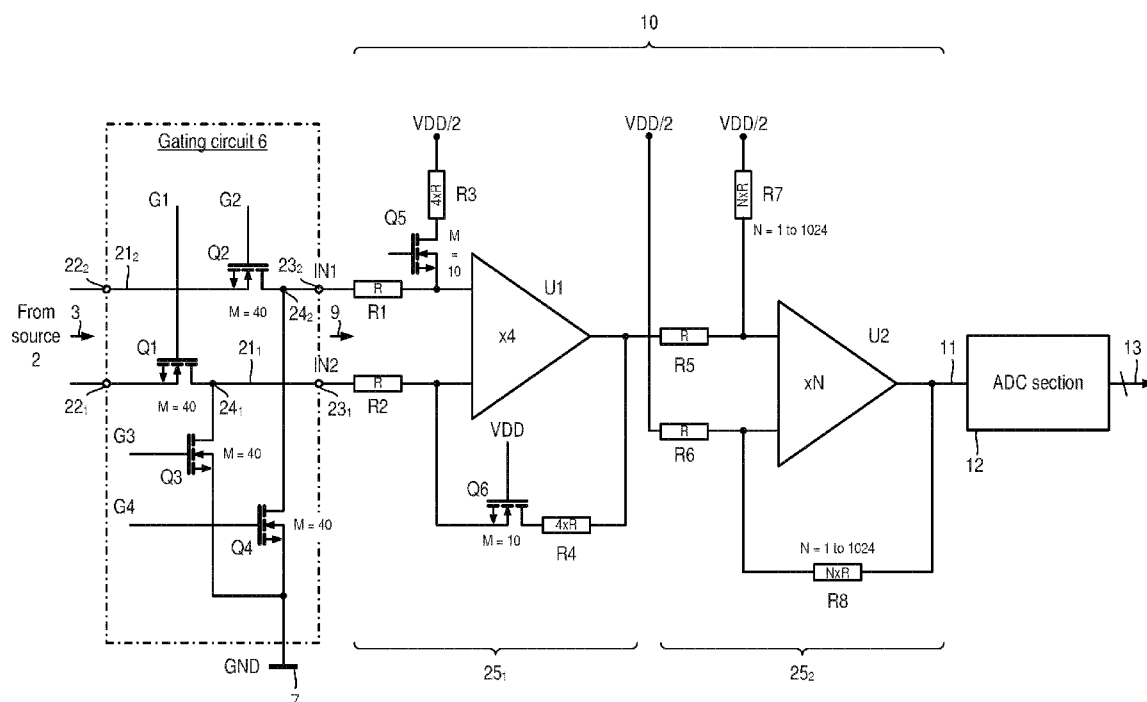
(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(54) Title: OFFSET CANCELLATION



(57) **Abstract:** Apparatus for performing offset cancellation is disclosed. The apparatus comprises a gating circuit (6) for receiving an analogue signal (3) from a source (2) and providing a gated analogue signal (9) to an analogue circuit (10), a gating controller (7; 14; Fig. 1) and a digital processor (14; Fig. 1) for receiving a digital signal (13) converted from an analogue output (11) from the analogue circuit (10). The gating circuit comprises at least one path (2), each path respectively comprising, an input terminal (22), an output terminal (23), a node (24) interposed between the input and output terminals, a first transistor (Q1) having a channel arranged between the input terminal and the node, and a second transistor (Q3) having channel arranged between the node and a fixed reference, such as ground (GND). The gating controller is configured, in a first time window (1A), to switch the first transistor so that the input terminal and the output terminal are decoupled and to switch the second transistor so that the node is coupled to the fixed reference. The gating controller

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

is configured, in a second, different time window (1B), to switch the second transistor so that the node and the fixed reference are decoupled and to switch the first transistor so that the input terminal is coupled to the input terminal. The digital processor is configured, in the first time window, to take a first measurement of the digital signal, and, in the second, different time window, to take a second measurement of the digital signal. The digital processor configured to subtract the first measurement from the second measurement.

Offset cancellation

Field of the Invention

The present invention relates to offset cancellation.

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Background

Non-zero offset cancellation non-zero offset correction (which may be referred to simply as “offset correction”, and which may be also called “offset cancellation”, “offset compensation” or “self-calibration”), may be used in a wide variety of applications.

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Examples of offset cancellation circuits can be found in US 2012/196555 A1, US 8 258 864 B, US 2012/200351 A1, US 2004/137853 A1, US 2009/261881 A1, US 2007/188219 A1, US 2007/139242 A1, US 2004/266381 A1, US 2002/175731 A1, US 5 812 023 A, US 6 141 169 A, US 4 841 252 A1, and US 5 648 738 A.

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Richard Palmer: “DC Parameters: Input Offset Voltage (V_{IO})”, Texas Instruments (RTM) Application report SLOA059 (2001) shows (in Figure 14) an autocalibration circuit for adjusting for removing input offset voltage. A CMOS op amp digitally trims input offset voltage using an ADC, a successive approximation register (SAR) and a
20 DAC. During start-up, two switches A which couple two inputs to the respective inputs of op amp are open, a switch B which couples the inputs of the op amp are closed, thereby shorting the inputs of the op amp, and connecting the output to the ADC. The input offset voltage of the amplifier appears at the output and is converted to a digital signal, then stored on the SAR. The DAC output current is fed into the null line of the
25 op amp, reducing the input offset voltage.

Summary

According to a first aspect of the present invention there is provided apparatus for performing offset cancellation. The apparatus comprises a gating circuit for receiving an analogue signal from a source and providing a gated analogue signal to an analogue circuit (such as a gain amplifier), a gating controller, and a digital processor for receiving a digital signal converted from an analogue output from the analogue circuit. The gating circuit comprises at least one path, each path respectively comprising, an input terminal, an output terminal, a node interposed between the input and output terminals, a first transistor having a channel arranged between the input terminal and the node, and a second transistor having channel arranged between the node and a fixed reference, such as ground. The gating controller is configured, in a first time window, to switch the first transistor so that the input terminal and the output terminal are decoupled and to switch the second transistor so that the node is coupled to the fixed reference. The gating controller is configured, in a second, different time window, to switch the second transistor so that the node and the fixed reference are decoupled and to switch the first transistor so that the input terminal is coupled to the input terminal. The digital processor is configured, in the first time window, to take a first measurement of the digital signal, and, in the second, different time window, to take a second measurement of the digital signal. The digital processor configured to subtract the first measurement from the second measurement.

Rather than using an approach employing feedback, this can provide more accurate offset cancellation and, moreover, can be easier to incorporate into existing analogue circuit systems.

The gating circuit may comprise two paths including first and second paths. Thus, the gating circuit may be configured to receive a differential input and output a differential output. The fixed reference may be ground.

According to a second aspect of the present invention there is provided apparatus for performing offset cancellation. The apparatus comprises a gating circuit for receiving an analogue signal from a source and providing a gated analogue signal to an analogue circuit, a gating controller, and a digital processor for receiving a digital signal converted from an analogue output from the analogue circuit. The gating circuit comprises first and second paths, each path respectively comprising an input terminal, an output terminal, a node interposed between the input and output terminals and a

first transistor having a channel arranged between the input terminal and the node. The gating circuit further comprises a second transistor having channel arranged between the nodes in the first and second paths. The gating controller is configured, in a first time window, to switch the first transistor so that the input terminal and the
5 output terminal are decoupled and to switch the second transistor so that the nodes are coupled, and, in a second, different time window, to switch the second transistor so that the nodes are decoupled and to switch the first transistor so that the input terminal is coupled to the input terminal. The digital processor is configured, in the first time window, to take a first measurement of the digital signal, and, in the second, different
10 time window, to take a second measurement of the digital signal, the digital processor configured to subtract the first measurement from the second measurement.

The analogue circuit may be a gain amplifier. The gain amplifier may be a programmable gain amplifier.

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The transistors may take the form of MOSFETs. The MOSFETs may include n-channel and/or p-channel MOSFETS. The MOSFETs may be enhancement-mode MOSFETs.

The digital processor may be a digital signal processor. The digital processor may be
20 provided by a microcontroller or system-on-a-chip.

According to a third aspect of the present invention there is system comprising the apparatus according to the first aspect or the second aspect of the present invention, an analogue circuit having at least one input terminal and at least one output terminal,
25 and an analogue-to-digital converter section. The output terminal(s) of the output circuit are connected to the input terminal(s) of the analogue circuit so as to provide the gated analogue signal, the output terminal(s) of the analogue circuit are connected to the analogue-to-digital converter section, and the analogue-to-digital converter section is arranged to provide the digital signal to the digital processor.

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The system may further comprise a signal source coupled to the gating circuit. The signal source may be a battery.

According to a fourth aspect of the present invention there is provided a vehicle or
35 plant comprising the system according to the third aspect.

The vehicle or plant may be a motor vehicle. The motor vehicle may be a motorcycle, an automobile (sometimes referred to as a “car”), a minibus, a bus, a truck or lorry. The motor vehicle may be powered by an internal combustion engine and/or one or more electric motors.

Brief Description of the Drawings

Certain embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic block diagram of a measurement system which includes auto
5 offset cancellation;

Figure 2 is a schematic circuit diagram of a switching circuit and switching circuit controller, an analogue circuit, and an analogue-to-digital converter section;

Figure 3 is a timing diagram for auto offset cancellation;

Figure 4 is a flow diagram of a method performed by a switching circuit controller;

10 Figure 5 is a flow diagram of a method performed by a digital processor; and

Figure 6 is a schematic circuit diagram of an alternative switching circuit.

Detailed Description of Certain Embodiments

Referring to Figure 1, a measurement system 1 and a signal source 2 is shown.

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The measurement system 1 samples an analogue input signal 3 (which may be single-ended or differential) from the source 2, such as a battery. The measurement system 1 is able to perform non-zero offset correction. A non-zero offset arises when a nominally zero input signal results in a non-zero output signal.

20

The measurement system 1 includes a gating device 5 (herein referred to as a “gating section” or “gating module”) which includes a gating circuit 6 provided with a fixed reference 7, such as ground, and a gating controller 8. The gating device 5 receives the analogue signal 3 from the source 2 and provides a gated analogue signal 9 to an
25 analogue circuit 10. The analogue circuit 10 may be for example, an amplifier, such as a fixed or programmable gain amplifier, or a comparator, and may include one, two or more stages. The analogue circuit 10 provides an output analogue signal 11 to an analogue-to-digital section 12 which digitises the signal 11 and which, optionally, may carry out analogue or digital filtering. The analogue-to-digital section 11 outputs a
30 digital signal 13 to a digital processor 14. The digital processor 14 may take the form of a digital signal processor (DSP) or other suitable form of digital processor, such as a microcontroller, system-on-a chip, or field-programmable gate array.

As will be explained in more detail later, the digital processor 14 can measure the digital
35 signal 13 at different times and process values taken at different times. A first measurement 13A is made in a first time window 15A (Figure 3) during which the input

signal 3 is decoupled from the analogue circuit 10 and provided instead a nominally zero input signal. A second measurement 13B is made in a second time window 15_B (Figure 3) during which the input signal 3 is coupled to the analogue circuit 10.

5 The digital processor 14 includes memory 15 for storing the first measurement 13_A, *i.e.* a digital value of a measured non-zero offset value (herein referred to as the “measured offset signal”), and a subtraction module 16 which subtracts the measured offset signal 13_A from the second measurement 13B (herein referred to as the “measured input signal”) to provide a third signal 13_C, *i.e.* a compensated measured signal. Single values
10 may be used, e.g. by taking an instantaneous value or averaging several values.

The gating section 5 may provide a timing signal 17, e.g. a copy of a transistor enable signal, to the digital processor 14 to enable the digital processor 14 to identify the end of the first time window 15_A (Figure 3) and, thus, the start of the second time window 15_B
15 (Figure 3). Conversely, the digital processor 14 may provide control signal(s) 18 to the gating section 5 to control operation of the gating circuit 5. Thus, the gating controller 8 may be provided by the digital processor 14 and a gating controller in the gating section 5 need not be provided.

20 Referring to Figure 2, the gating circuit 6 and the analogue circuit 10 in the form of a two-stage, programmable gain amplifier, are shown.

The gating circuit 6 includes first and second paths 21₁, 21₂ each having a respective input terminal 22₁, 22₂, a respective output terminal 23₁, 23₂ and a respective
25 intermediate node 24₁, 24₂ lying on the path 21₁, 21₂ between the input terminal 22₁, 22₂ and output terminal 23₁, 23₂.

Each path 21₁, 21₂ includes a respective first transistor Q1, Q2 in the form of an n-channel, enhancement-type MOSFET in which the channel forms part of the path 21₁,
30 21₂. The first transistor Q1, Q2 is used to selectively couple and decouple the input terminal 22₁, 22₂ to the output terminal 23₁, 23₂.

A respective second transistor Q3, Q4 in the form of an n-channel, enhancement-type MOSFET is connected between the intermediate node 24₁, 24₂ and the fixed reference
35 7, in this case ground. Each second transistor Q3, Q4 is used to selectively couple and decouple to the output terminal 23₁, 23₂ to the fixed reference.

Gates G1, G2, G3, G4 of the transistors Q1, Q2, Q3, Q4 are controlled by the controller 8. The first transistors Q1, Q2 are controlled as a set, that is, have same state ON or OFF, and are switched at the same time. Likewise, the second transistors Q3, Q4 are controlled as a set. However, operating of the first transistors Q1, Q2 and second transistors Q3, Q4 are complementary, that is, when the first transistors Q1, Q2 are ON, the second transistors Q3, Q4 are OFF and *vice versa*.

The output terminals 22₁, 22₂ are coupled to the inputs of a first operation amplifier U1 via first and second resistors R1, R2 of the first stage 25₁ of the programmable gain amplifier.

The first stage 25₁ of the programmable gain amplifier includes the first operational amplifier U1, fifth and sixth transistors Q5, Q6 and third and fourth resistors R3, R4. The first input of the first operational amplifier U1 is connected to half the supply voltage 0.5VDD via the fifth transistor Q5 and the third resistor R3. The second input of the operational amplifier U1 is connected to the output of the operational amplifier U1 via the sixth transistor Q6 and the fourth resistor R4. In this case, $R_1 = R_2 = R$ and $R_3 = R_4 = 4.R$.

The output of the operational amplifier U1 and the supply voltage 0.5VDD are coupled to the inputs of a second operation amplifier U2 via fifth and sixth R5, R6 of the second stage 25₂ of the programmable gain amplifier.

The second stage 25₂ of the programmable gain amplifier includes seventh and eighth resistors R7, R8. The first input of the second operational amplifier U1 is connected to half the supply voltage 0.5VDD via the seventh resistor R7. The second input of the operational amplifier U2 is connected to the output of the operational amplifier U2 via the eight resistor R8. The resistance values of the seventh and eighth resistors R7, R8 can be programmed and can take a value N.R where N is a positive, non-zero integer which lies in the range from 1 to 1024.

The output of the operational amplifier U2 is supplied to the ADC section 12.

Figure 2 shows an arrangement employing differential input. However, offset correction circuit employing a single path may be used for a single-ended input.

Referring also to Figures 3, 4, and 5, operation of the measurement system 1, in particular the gating section 5 and the digital processor 14, to perform offset cancellation will now be described.

5

The measurement system 1 may become active, for example, by power being applied by the gating section 5 and/or the digital processor 14 waking from a dormant state.

10

The gating controller 8 (or if gating control is provided by the digital processor 14, the digital processor 14), turns OFF the first transistors Q1, Q2 and turns ON the second transistors Q3, Q4 (steps S4.1 & S4.2). Turning OFF the first transistors Q1, Q2 and turning ON the second transistors Q3, Q4 may occur at the same time. Alternatively, the first transistors Q1, Q2 may be switched OFF before the second transistors Q3, Q4 are switched ON. The gating controller 8 (or the digital processor 14) then waits for a time t_1 which defines a first time window 15_A (step S4.3).

15

During this time window 15_A, the digital processor 14 measures and stores a measured offset signal 13_A (step S5.1). The measurement takes place after a delay Δt after the start of the first time window 15_A, $\Delta t \ll t_1$, where t_1 is the duration of the first time window 15_A. The digital processor 14 then waits a period $t_3 \ll (t_4 - \Delta t)$ until the second time window 15_B (step S5.2).

20

The gating controller 8 (or digital processor 14), turns OFF the second transistors Q3, Q4 and turns ON the first transistors Q1, Q2 (steps S4.4 & S4.5) and then waits time t_2 (step S4.6).

25

During the second time window 15_B, the digital processor 14 measures the input signal 13_B (step S5.3), subtracts the measured offset signal 13_A from the input signal 13_B (step S5.4) and outputs (e.g. stores) the corrected signal 13_C (step S5.5). The digital processor 14 then waits a period t_5 (step S5.6) until Δt after the start of the next period.

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Performing offset cancellation in digital domain can help to provide much greater sensitivity, not just in the range of milli- or micro-volts, but of the order of nano-volts.

For example, for a battery and/or other applications, an offset voltage error after cancellation may be of the order 100 nV for a voltage measurement range of +/- 75 mV.

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Thus, a voltage resolution of 250nV may be needed thus requiring an ADC resolution of 22 bits. For a smaller ratio of offset voltage to measurement range or measurement resolution, a greater ADC resolution may be needed. Conversely, for a larger ratio of offset voltage to measurement range or measurement resolution, a smaller ADC resolution may be needed.

Alternative gating circuit 6'

Figure 6 shows an alternative gating circuit 6' which can be used instead of the gating circuit 6 shown in Figure 2.

10

Referring to Figures 2 and 6, the alternative gating circuit 6' is the same as the gating circuit 6 shown in Figure 2, except that instead of two second transistors Q3, Q4, a single transistor Q7 is used, arranged so that it selectively couples and decouples the nodes 24₁, 24₂. Thus, fewer transistors can be used.

15

In this arrangement, however, the outputs 23₁, 23₂ may float which can lead to an error at the amplifier output due to common mode shift of the amplifier inputs. Thus, in cases where accurate offset cancellation is required, an additional transistor Q8 may be used to couple the nodes 24₁, 24₂ to a fixed reference, for example ground.

20

Modifications

It will be appreciated that various modifications may be made to the embodiments hereinbefore described. Such modifications may involve equivalent and other features which are already known in the design, manufacture and use of amplifier circuits, analogue-to-digital converters and digital processors and component parts thereof and which may be used instead of or in addition to features already described herein. Features of one embodiment may be replaced or supplemented by features of another embodiment.

Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel features or any novel combination of features disclosed herein either explicitly or implicitly or any generalization thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features

and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

Claims

1. Apparatus for performing offset cancellation, the apparatus comprising:
a gating circuit (6) for receiving an analogue signal (3) from a source (2) and
5 providing a gated analogue signal (9) to an analogue circuit (10);
a gating controller (7; 14); and
a digital processor (14) for receiving a digital signal (13) converted from an
analogue output (11) from the analogue circuit (10);
wherein the gating circuit comprises:
10 at least one path (21_i), each path respectively comprising:
an input terminal (22_i);
an output terminal (23_i);
a node (24_i) interposed between the input and output terminals;
a first transistor (Q1) having a channel arranged between the input terminal
15 and the node; and
a second transistor (Q3) having channel arranged between the node and a
fixed reference;
wherein the gating controller configured:
in a first time window:
20 to switch the first transistor so that the input terminal and the output terminal
are decoupled and to switch the second transistor so that the node is coupled to
the fixed reference; and
in a second, different time window:
to switch the second transistor so that the node and the fixed reference are
25 decoupled and to switch the first transistor so that the input terminal is coupled
to the input terminal.
wherein the digital processor is configured:
in the first time window:
to take a first measurement of the digital signal; and
30 in the second, different time window:
to take a second measurement of the digital signal;
the digital processor configured to subtract the first measurement from the second
measurement.
- 35 2. The apparatus of claim 1, wherein the gating circuit comprises two paths
including first and second paths.

3. The apparatus of claim 1 or 2, wherein the fixed reference is ground.
4. Apparatus for performing offset cancellation, the apparatus comprising:
- 5 a gating circuit (6') for receiving an analogue signal (3) from a source (2) and providing a gated analogue signal (9) to an analogue circuit (10);
- a gating controller (7; 14); and
- a digital processor (14) for receiving a digital signal converted from an analogue output from the analogue circuit (10);
- 10 wherein the gating circuit comprises:
- first and second paths, each path respectively comprising:
- an input terminal (22_i);
- an output terminal (23_i);
- a node (24_i) interposed between the input and output terminals; and
- 15 a first transistor (Q1) having a channel arranged between the input terminal and the node;
- wherein the gating circuit further comprises:
- a second transistor having channel arranged between the nodes in the first and second paths;
- 20 wherein the gating controller configured:
- in a first time window:
- to switch the first transistor so that the input terminal and the output terminal are decoupled and to switch the second transistor so that the nodes are coupled, and
- 25 in a second, different time window:
- to switch the second transistor so that the nodes are decoupled and to switch the first transistor so that the input terminal is coupled to the input terminal.
- wherein the digital processor configured:
- in the first time window:
- 30 to take a first measurement of the digital signal; and
- in the second, different time window:
- to take a second measurement of the digital signal;
- the digital processor configured to subtract the first measurement from the second measurement.
- 35

5. The apparatus of any one of claims 1 to 4, wherein the analogue circuit (10) is a gain amplifier.
6. The apparatus of claim 5, wherein the gain amplifier is a programmable gain amplifier.
7. The apparatus of any one of claims 1 to 5, wherein the digital processor (15) is a digital signal processor.
- 10 8. A system comprising:
the apparatus according to any one of claims 1 to 6;
an analogue circuit (10) having at least one input terminal and at least one output terminal; and
an analogue-to-digital converter section (12);
15 wherein the output terminal(s) of the output circuit are connected to the input terminal(s) of the analogue circuit (10) so as to provide the gated analogue signal (9), the output terminal(s) of the analogue circuit are connected to the analogue-to-digital converter section (12), and the analogue-to-digital converter section (12) is arranged to provide the digital signal to the digital processor (14).
- 20 9. A system of claim 8, further comprising:
a signal source (2) coupled to the gating circuit (6).
10. A system of claim 9, wherein the signal source (2) is battery.

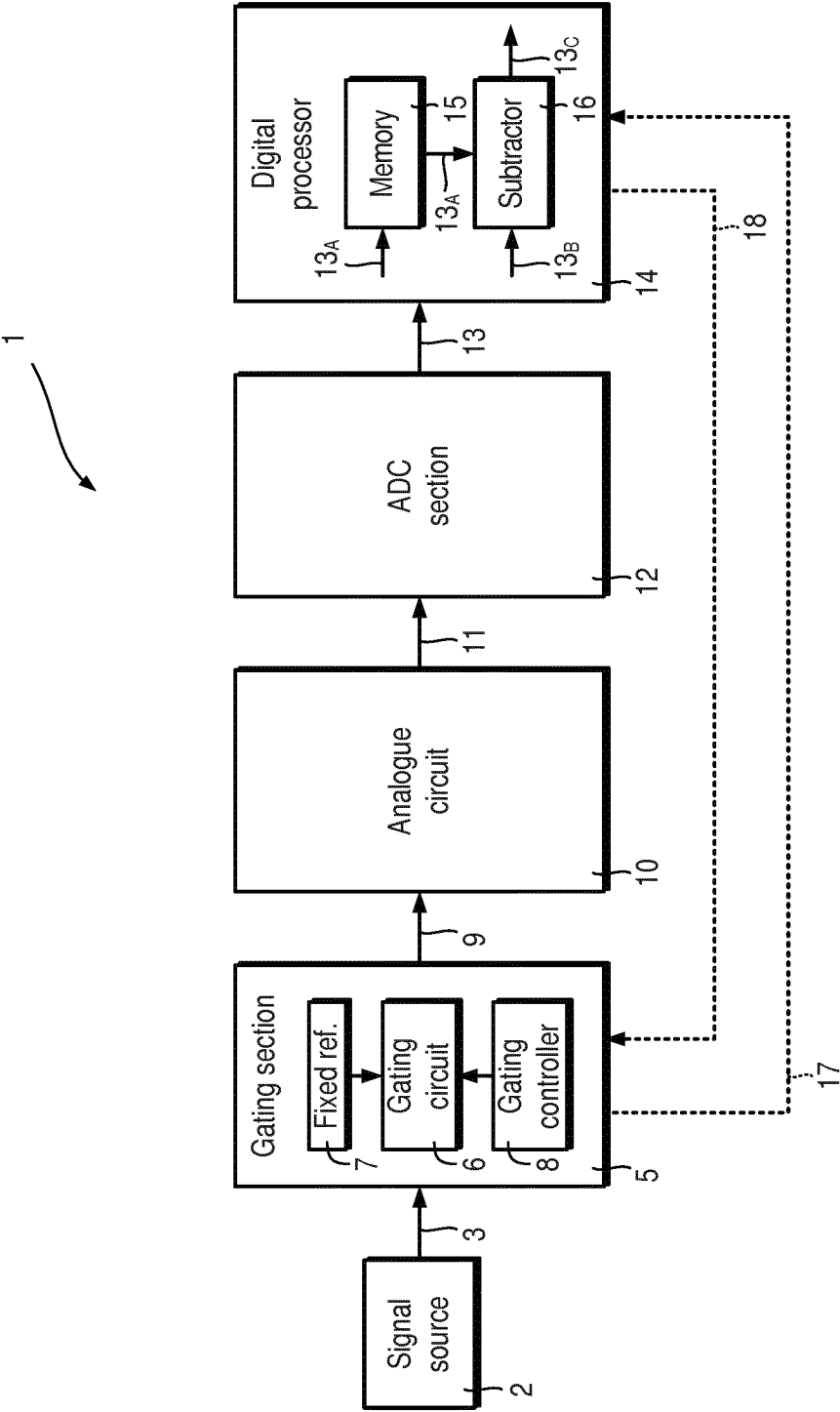


Fig. 1

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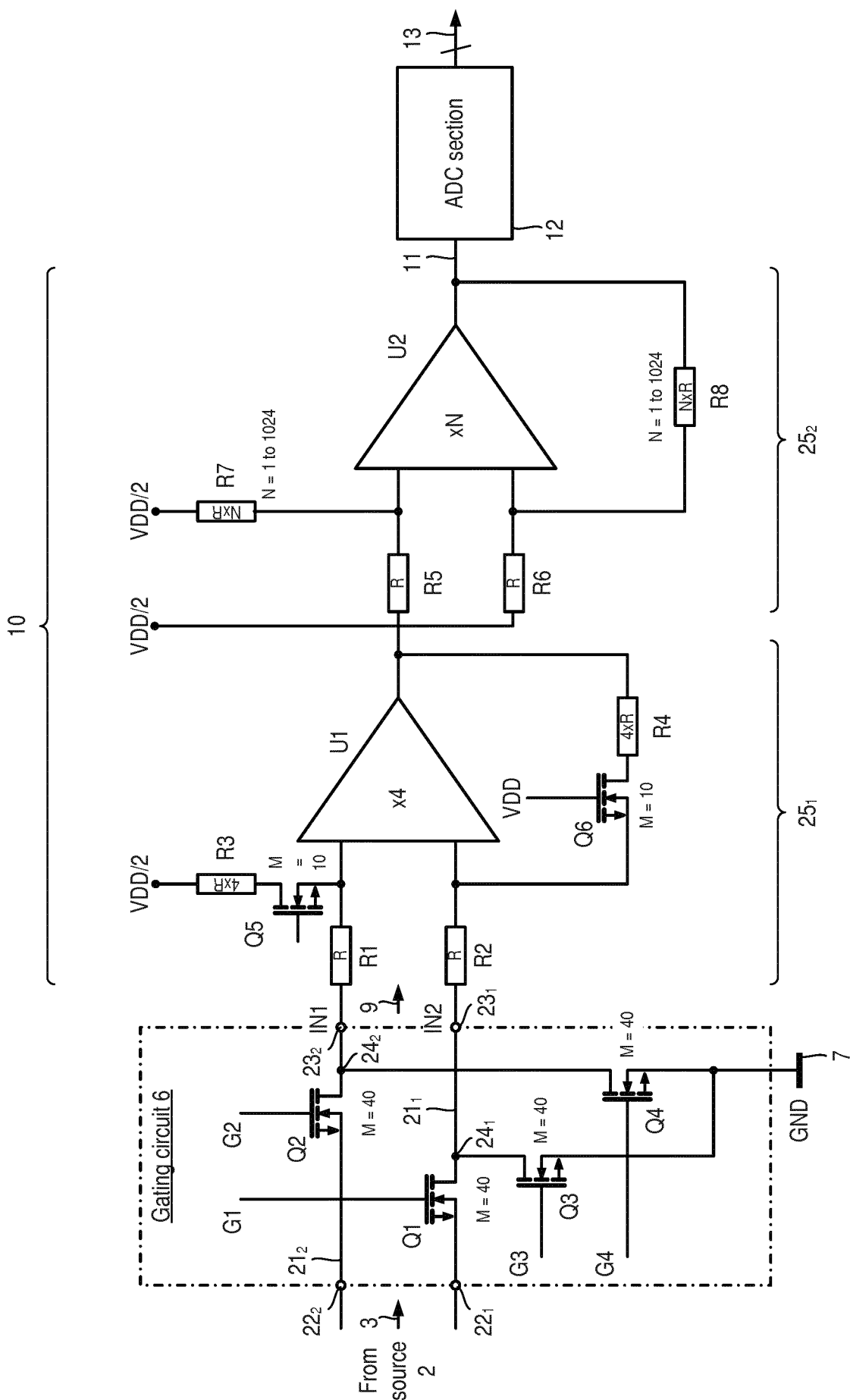


Fig. 2

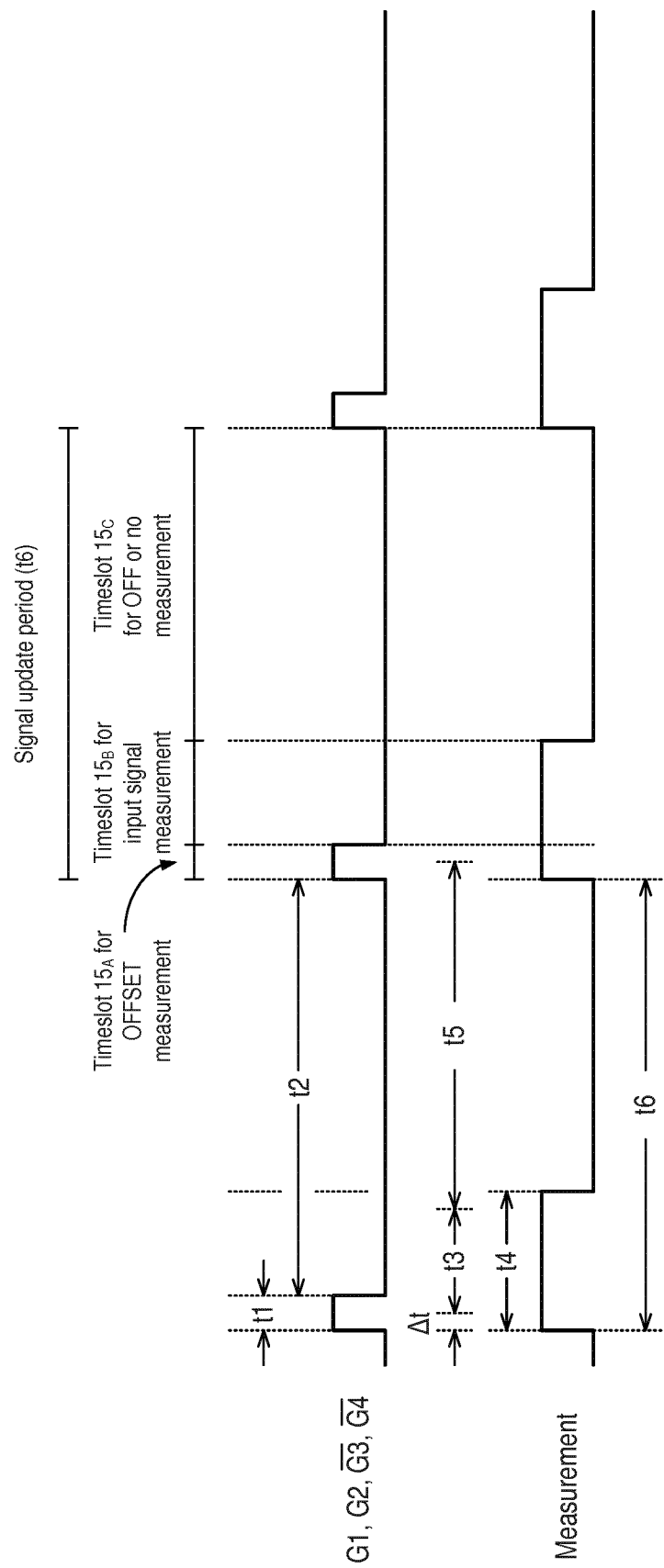


Fig. 3

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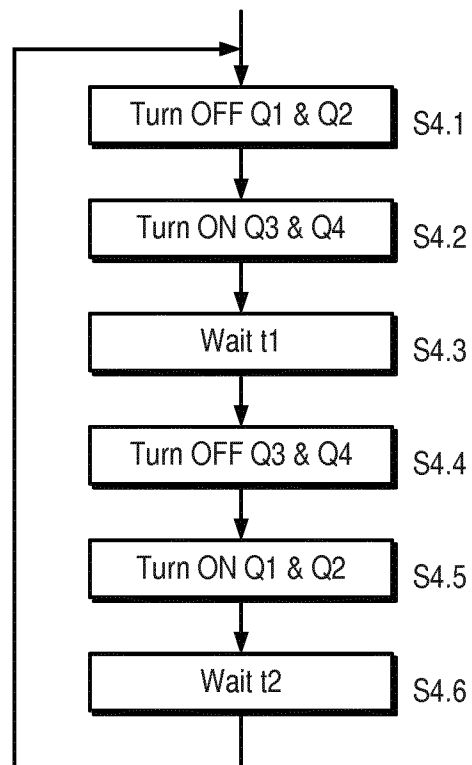


Fig. 4

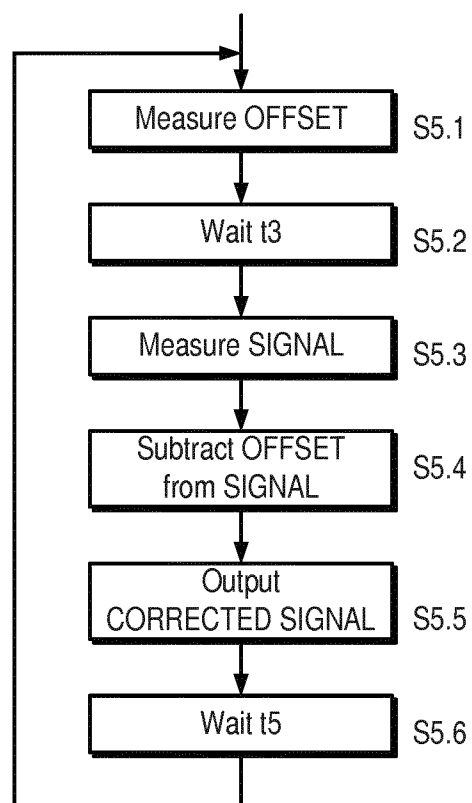


Fig. 5

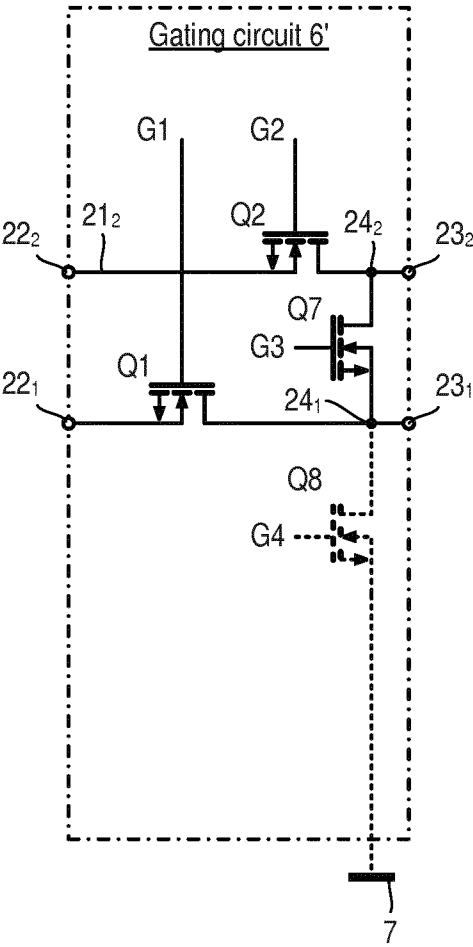


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/069333

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 721 547 A (LONGO LORENZO L [US]) 24 February 1998 (1998-02-24) column 3, line 63 - column 4, line 4; figure 1 column 4, line 50 - column 5, line 66 -----	1-10
X	US 2009/206854 A1 (BERNARDON DEREK [AT] ET AL) 20 August 2009 (2009-08-20) paragraph [0036] - paragraph [0052]; figures 1, 2 -----	1-10



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/069333

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