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(71) Applicant: VLSI TECHNOLOGY, INC. [US/US]; 1109 McKay Drive, San Jose, CA 95131 (US).

(72) Inventors: GANAPOL, David, L.; 110 Lucia Lane, Scotts Valley, CA 95066 (US). MARCUSE, Arno, G.; 4580 West Ivanhoe Street, Chandler, AZ 85226 (US).

(74) Agent: HICKMAN, Paul, L.; P.O. Box 61059, Palo Alto, CA 94306 (US).

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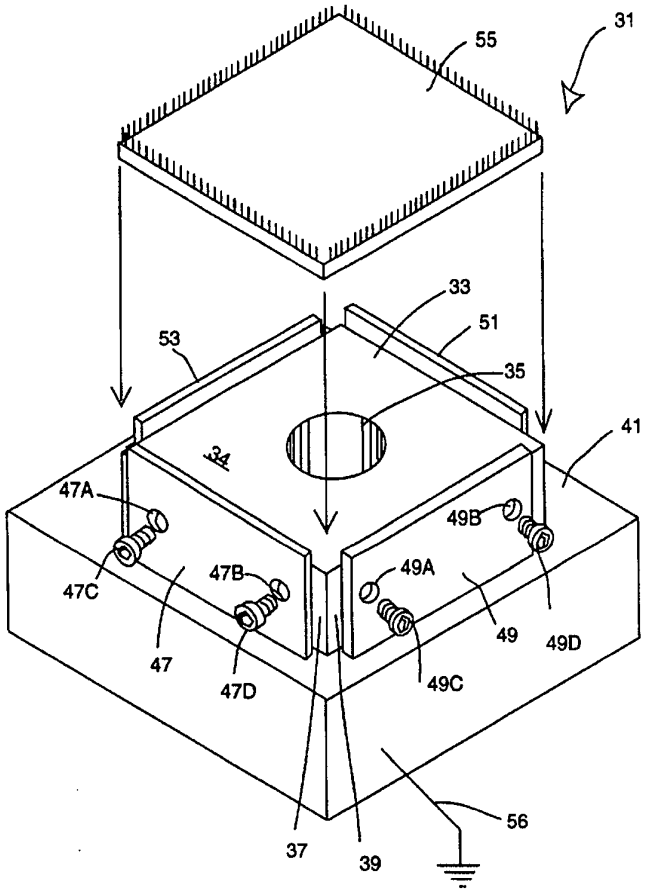
(54) Title: INTEGRATED CIRCUIT TEST JIG

(57) Abstract

Test jig apparatus for testing an integrated circuit chip that suppresses build-up and subsequent discharge of electrical charge on the test jig apparatus or on the chip. The test jig apparatus includes a base (33) of selected material having a top surface (34) of the same general shape and dimensions as the chip to be tested. Preferably, the entire top surface of the base is electrically grounded. The base has two or more side surfaces (37, 39) with side surface planes that are approximately perpendicular to a plane defining the top surface of the base. Each side surface accepts a side plate (47, 49, 51, 53), made of a selected material such as ULTIM, than can be attached to or removed from the base. The side plane material resists electrical charge buildup and subsequent discharge so that the chip being tested is not subjected to electrical discharge from this source. In another embodiment, the side plates are replaced by plates (67, 69) mounted on the top surface of the base.



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INTEGRATED CIRCUIT TEST JIG

Technical Field

This invention relates to integrated circuit chip testing, and more particularly to a test jig apparatus for holding and aligning the integrated circuit chip.

Background Art

After an integrated circuit (IC) is fabricated, the IC may be tested to determine whether the IC is functional and whether it operates within product specifications. A test jig apparatus is typically provided to receive and align the IC for testing purposes. The IC leads can be pressed against test pads connected to a circuit tester, using a workpress that reciprocatingly urges the IC leads and the test pads together.

As the workpress moves back and forth, an electrostatic charge can develop within the test jig apparatus. If this electric charge flows through the IC by electrostatic discharge (ESD), the resulting current can physically damage the IC held by the test jig apparatus. For example, ESD from accumulated charged on an IC test jig workpress can discharge several microcoulombs (equivalent to more than 10^{13} free electrons) on an adjacent IC chip, thus destroying or disabling the chip. The problem of ESD appears to worsen for operation at higher temperatures, e.g. $T \geq 125°C$.

Figure 1 illustrates operation of test jig apparatus 11 from the prior art. The test jig apparatus 11 is of a one-piece construction, including a base 13 with a central aperture 15 (optional) therein, the base 13 having a substantially rectangular top surface 14 with approximately the same shape and planar dimensions as an IC chip 21 to be tested. The test jig apparatus 11 also has four side flanges 17A, 17B, 17C and 17D rigidly extending from the base 13 to form a "cup" to receive and hold the IC chip 21 for testing. The base 13 and four side flanges 17A, 17B, 17C and 17D together form a one-piece construction and are made of a non-electrically conductive material such as VESPULE. An IC chip 21 is received by this "cup" and is further aligned so that the IC leads 23 mate with test pads (not shown) connected to electronic equipment (not shown) that will be used to test the IC chip.

Because the material from which the base and side flanges is made is electrically non-conductive, static charge that accumulates on test jig 11 may discharge through the IC chip being tested in the test jig apparatus. This can damage or destroy the IC chip.

Furthermore, accumulated electrical charge on the test jig apparatus 11 may destroy or damage the test jig apparatus itself, requiring that the entire test jig apparatus be replaced.

What is needed is a test jig apparatus that: (1) can operate reliably over a long term at temperatures exceeding 125°C; (2) allows replacement of damaged portions of the test jig apparatus without requiring replacement of the entire test jig apparatus; and (3) resists electric charge build-up and subsequent electrostatic discharge during operation of the apparatus.

DISCLOSURE OF THE INVENTION

These needs are met by apparatus that provides a body of electrically conducting material and four removable non-conductive side plates which cooperate with the base to receive an IC chip for testing. The conductive base drains electrostatic charges from the jig apparatus, and the side plates hold the IC and its leads in position for testing. If, over time, the side plates wear or become defective, they can be replaced without removing the entire test jig apparatus.

The combination of the electrically conductive base material and the removable plates provides a configuration that has an improved lifetime (estimated to be 50,000 chip testing sequences or more), sharply reduced test jig apparatus cost, and reduced likelihood of build-up of electrostatic charge.

These and other advantages of the present invention will become apparent to those skilled in the art upon a reading of the following specification of the invention and a study of the several figures of the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a test jig apparatus from the prior art;

Figures 2 and 3 are perspective views of a test jig apparatus constructed according to the present invention, without and with the ESD-resistive side plates attached; and

Figure 4 is a perspective view of another embodiment of the present invention.

BEST MODE FOR INDUSTRIAL APPLICATION

Figure 1 illustrates prior art test jig apparatus which was discussed in the Background Art, above.

Figure 2 illustrates an embodiment 31 of a test jig apparatus of the present invention. An electrically grounded base 33 of electrically conductive material, such as aluminum or steel, is provided to hold an IC chip on its top surface 34. The top surface 34 preferably has approximately the same shape and dimensions as the IC chip that will be received by that surface for alignment and testing. Optionally, the block 33 may have an aperture 35 therein to facilitate placement of the IC chip on, and removal of the IC chip from, the top surface 34, e.g. by extending a pin through the aperture 35 to engage an IC. The base 33 is preferably a rectangular parallelepiped having four side surfaces, such as 37 and 39, that are oriented approximately perpendicularly to the top surface 34 of the base 33. Each side surface preferably has two or more threaded bores, such as threaded bores 37A and 37B, 39A and 39B. Optionally, the base 33 may be coupled to another larger block 41 of material that is also electrically conductive, for stability or weight or electrical grounding or some other test-related reason.

Figure 3 illustrates the test jig apparatus of 31 of Figure 2 with side plates 47, 49, 51 and 53 attached to the base 33. Each of the side plates 47, 49, 51 and 53 extends above the top surface 34 of the base so that these plates, in combination with the top surface 34, form a "cup" to receive and hold an IC chip 55 to be tested. As illustrated in Figure 3, the side plates have apertures (e.g. apertures 47A, 47B, 49A, and 49B) which align with the threaded bores 37A, 37B, 39A, and 39B, respectively of the base 33. Each of the apertures 47A, 47B, 49A and 49B receives a screw or other attachment means 47C, 47D, 49C and 49D, respectively, that attaches the side plate 47 or 49, as the case may be, to the corresponding side surface of the base 33. Similar apertures and screws or attachments means (not shown) are provided for the side plates 51 and 53, for the same purpose.

The side plates 47, 49, 51 and 53 are preferably made of a selected material, such as ULTIM, that resists charge buildup and subsequent ESD. An electric charge that would otherwise accumulate on the base 33 can be conducted through the base 33 to ground by a line 56 or other discharge means. The material for the side plates 47, 49, 51 and 53 is electrically non-conductive so that the IC chip leads and the circuit testing pads are not shorted together if these leads or pads make contact with a side plate. Operated in this manner, the embodiment 31 resists the accumulation of electrical charge. Thus, the test jig

apparatus shown in Figure 3 is subjected to reduced ESD damage and may be used for an estimated 50,000 or more IC chip processings. The base 33 should last a much longer time. Further, when one or more of the side plates 47, 49, 51, and 53 no longer functions as required, that side plate may be replaced with a new or reconditioned side plate without replacing the entire test jig apparatus.

Figure 4 illustrates a second embodiment 61 of the invention, in which a grounded base 63 of electrically conducting material has two or more side plates 67 and 69 attached to a top surface 64 of the base adjacent to each other. The side plates 67 and 69 are made of an ESD-resistant material, such as ULTIM, and are attached to the top surface 64 of the base 63 by screws or other attachment means 67C, 67D, 69C, 69D as shown. Optionally, the base 63 has an aperture 65 therein to facilitate placement of the IC chip 71 in, or removal of the chip from, the test jig 61, as described previously.

A test jig, constructed according to the invention, can operate at temperatues T = 125 - 150°C. The electrical conductivity of the material used for the base 33 may decrease slightly with increasing temperature, but any accumulated electrical charge can still be safely conducted to ground. The material, such as ULTIM, from which the side plates in Figure 3 or the side plates in Figure 4 are made, has been tested and found to perform well at these operating temperatures.

Although the preceding discussion has assumed that the entire base (33 in Figures 2 and 3, 63 in Figure 4) is electrically conductive, it is sufficient if merely a portion of the top surface of this base be electrically conductive, such that it provides an electrical path to safely discharge the electrical charge that may accumulate on the base or its top surface.

While this invention has been described in terms of several preferred embodiments, it is contemplated that alterations, modifications and permutations thereof will become apparent to those skilled in the art upon a reading of the specification and study of the drawings. It is therefore intended that the following appended claims include all such alterations, modifications and permutations as fall within the true spirit and scope of the present invention.

IN THE CLAIMS

1. Test and alignment jig apparatus for an integrated circuit chip, the apparatus comprising:

a base (33) of selected material, having a top surface (34) with a defining top surface plane having a shape and dimensions that are approximately the same as the shape and dimensions of an integrated circuit chip to be tested, and having at least two substantially planar side surfaces (37,39) with defining side surface planes that are approximately perpendicular to the defining top surface plane, where at least a portion of the top surface of the base is electrically conductive; and

at least two plates (47, 49) of a selected electrically non-conductive material, each plate extending above the top surface of the base and being attached to one of the plurality of side surfaces, where the plurality of plates plus the top surface of the base define a test area that receives an integrated circuit chip thereon.

2. The apparatus of claim 1, wherein said selected non-conductive material resists electrostatic discharge.

3. The apparatus of claim 2, where the selected non-conductive material comprises ULTIM.

4. The apparatus of claim 1, wherein said electrically conductive portion of said top surface of said base is electrically grounded.

5. The apparatus of claim 1, wherein substantially all of said base is electrically conductive.

6. The apparatus of claim 1, wherein said base has an aperture (35) opening on said top surface.

7. Test and alignment jig apparatus for an integrated circuit chip, the apparatus comprising:

a base (33) having a top surface (34), where at least a portion of the top surface of the base is electrically conductive; and

a plurality of non-conductive plates (47, 49, 51, 53), each plate being coupled to said base and extending above the top surface of the base, the plates being positioned proximate to each other to define a test area on the top surface of the base that receives an integrated circuit chip thereon.

8. The apparatus of claim 7, wherein said non-conductive plates resist electrostatic discharge.

9. The apparatus of claim 8, wherein said non-conductive plates are made of a material comprising ULTIM.

10. The apparatus of claim 7, wherein said electrically conductive portion of said top surface of said base is electrically grounded.

11. The apparatus of claim 7, wherein substantially all of said base is electrically conductive.

12. A method for testing an integrated circuit chip, the method comprising the steps of:

providing a base (33) of a selected material having a top surface (64), where at least a portion of the top surface of the base is electrically conductive;

attaching to the base, proximate the top surface thereof, at least two plates (47, 49) of electrically non-conductive material, each plate extending above the top surface of the base, where the plates and the top surface of the base define a test area that receives an integrated circuit chip;

positioning an integrated circuit chip (55) in the test area; and

performing at least one electrical test on the chip while the chip is positioned in the test area.

13. The method of claim 12, further comprising the step of electrically grounding said electrically conductive portion of said top surface of said base.

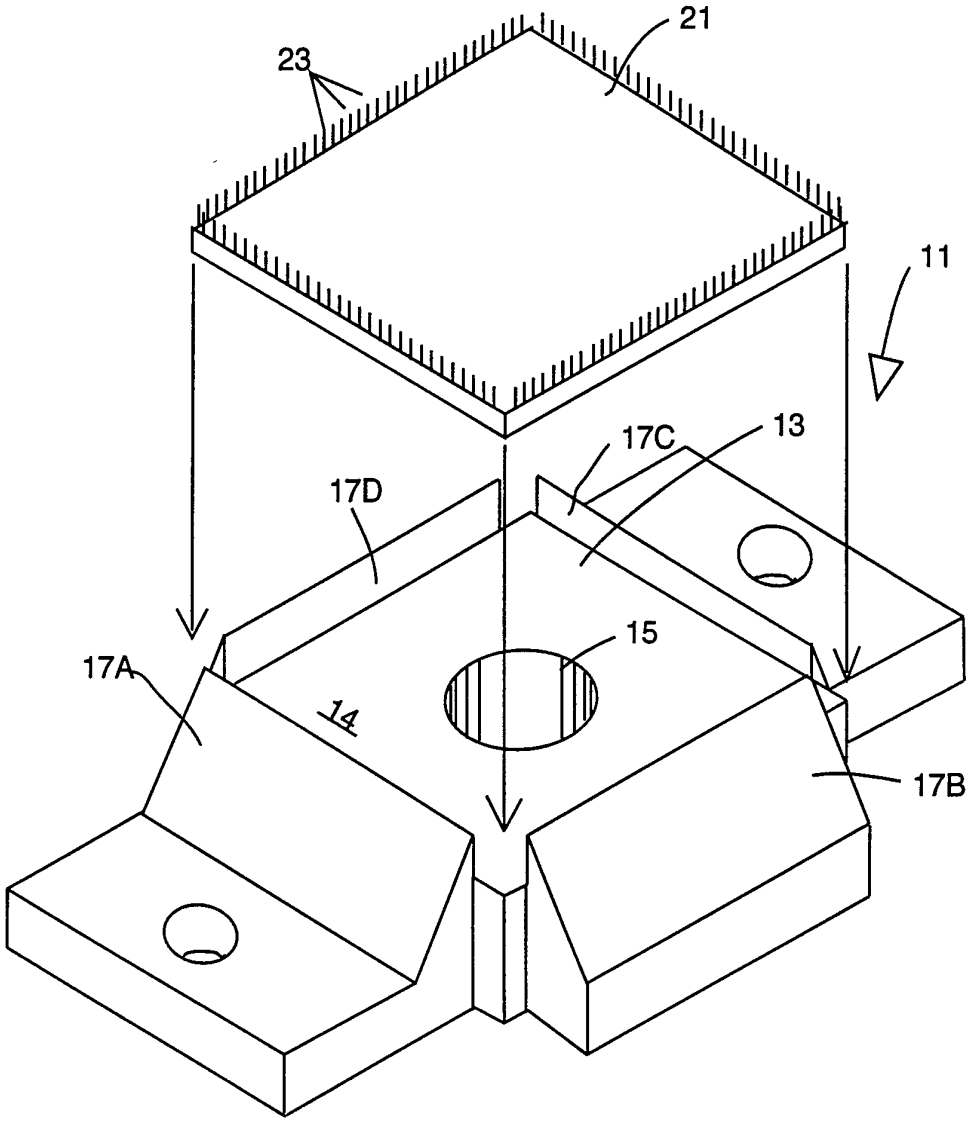

Fig. 1 (Prior Art)

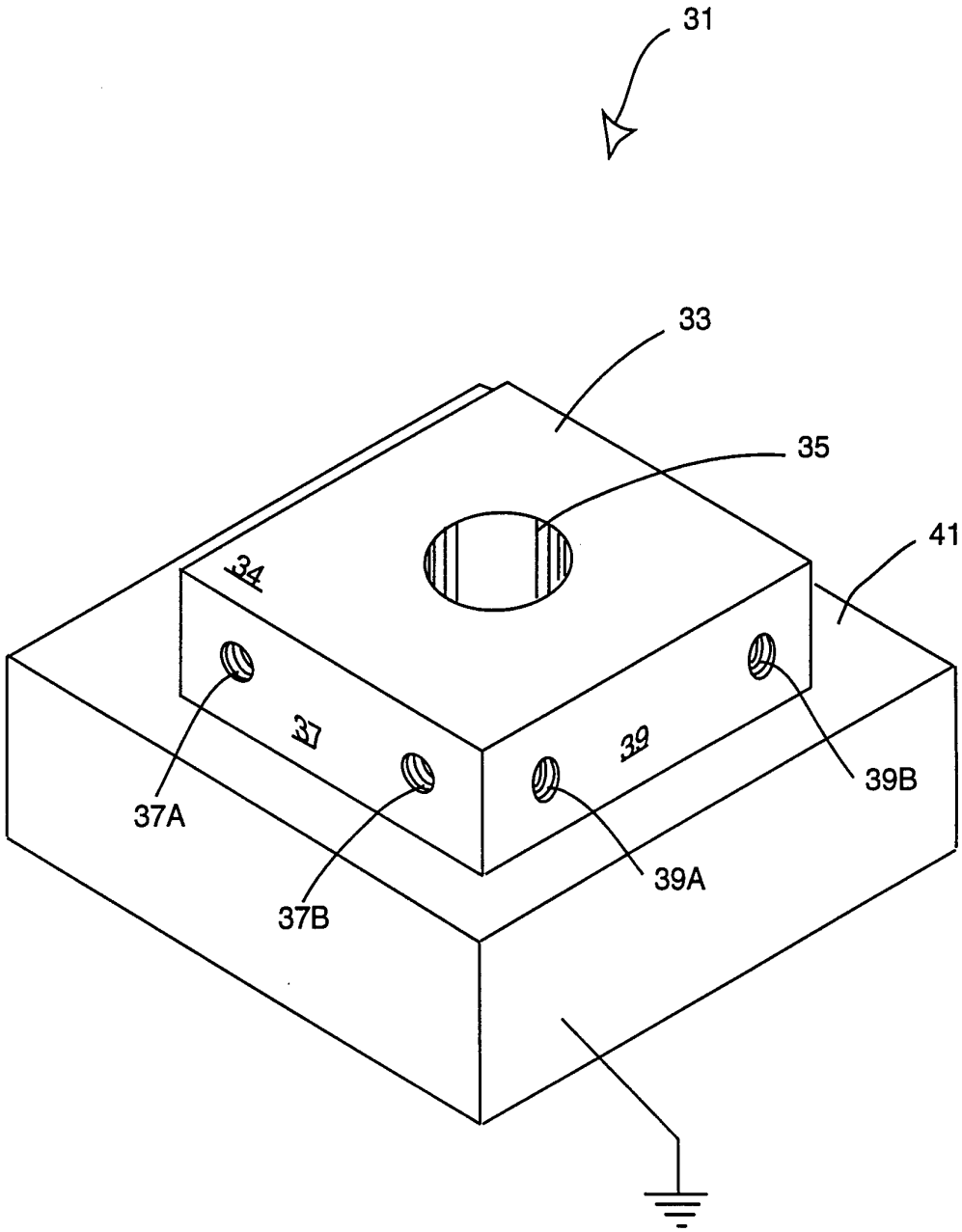

Fig. 2

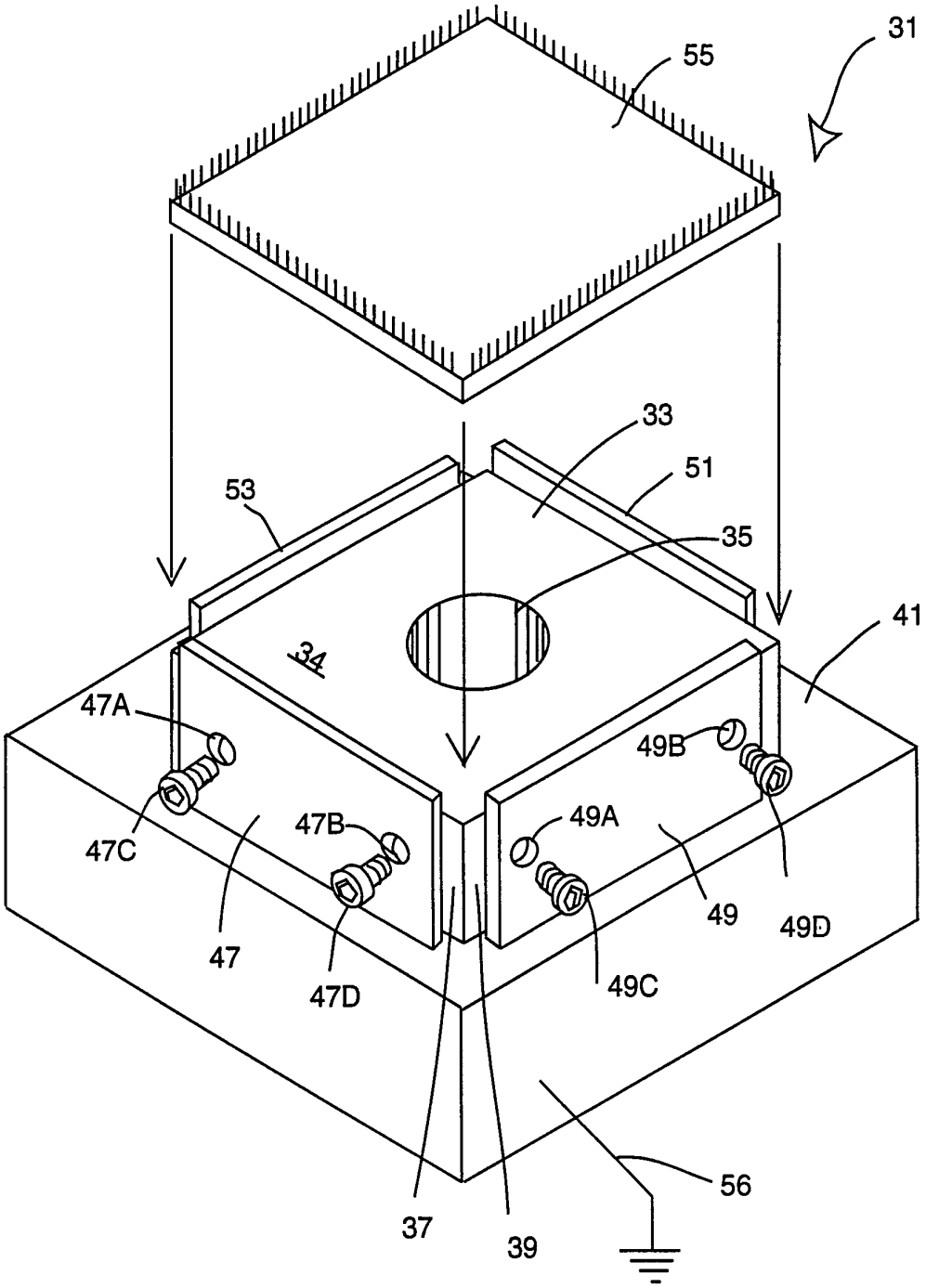
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Fig. 3

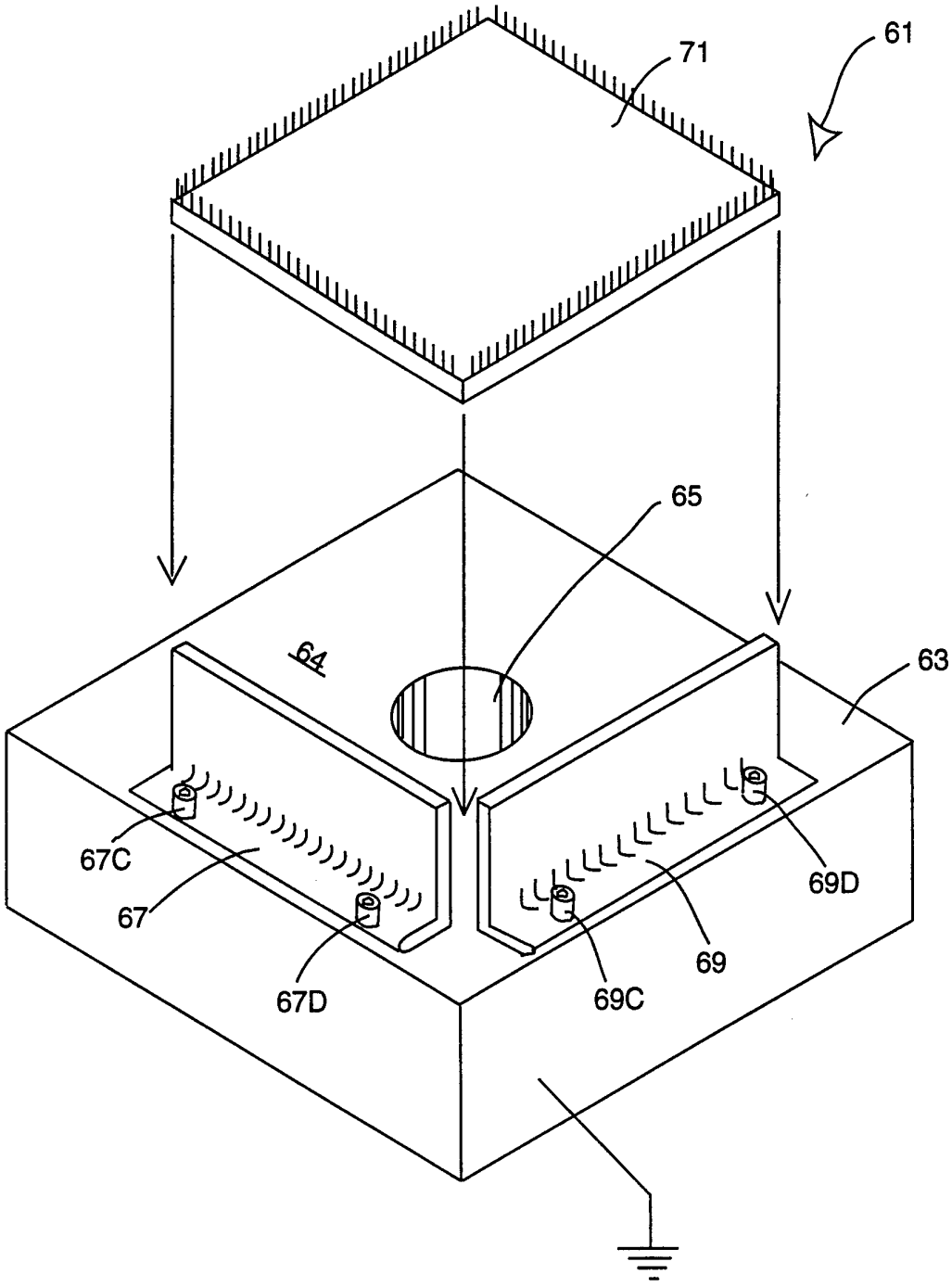

Fig. 4

INTERNATIONAL SEARCH REPORT

Internatio. Application No
PCT/US 93/12273

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G01R1/04 H05F3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G01R H05K H05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	ELECTRONICS TEST, vol.11, no.4, March 1990, SAN FRANCISCO US pages 50 - 52 J.ROBLEE 'Mechanical Challenges of IC Handler Contactor Designs' see page 50, left column, paragraph 1; figure 1 see page 51, paragraph 3 -last paragraph ---	1,7,12
Y	US,A,5 143 450 (N.R.SMITH ET AL.) 1 September 1992 see abstract; figures 3,4 see column 5, line 20 - line 23 see column 9, line 2 - line 6 ---	1,7,12
A	US,A,5 124 637 (M.W.FRISBIE) 23 June 1992 see abstract; figures 1-3 see column 2, line 62 - line 68 --- -/--	1,7,12

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 156 649 (P.M.COMPTON ET AL.) 20 October 1992 see abstract; figures 1,2,5 see column 5, line 53 - line 56	1,7,12
X	EP,A,0 458 448 (TEKTRONIX) 27 November 1991 see abstract; figures 1,2,7	1,7,12
X	EP,A,0 305 951 (EVERETT/CHARLES CONTACT PROD.) 8 March 1989 see abstract; figure 34	7,12

INTERNATIONAL SEARCH REPORT

Information on patent family members

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US-A-5124637	23-06-92	NONE		
US-A-5156649	20-10-92	NONE		
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