



- (51) **International Patent Classification:**
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)
- (21) **International Application Number:**
PCT/US2013/054641
- (22) **International Filing Date:**
13 August 2013 (13.08.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
13/584,016 13 August 2012 (13.08.2012) US
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- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))

(54) **Title:** MOS TRANSISTORS HAVING REDUCED LEAKAGE WELL-SUBSTRATE JUNCTIONS

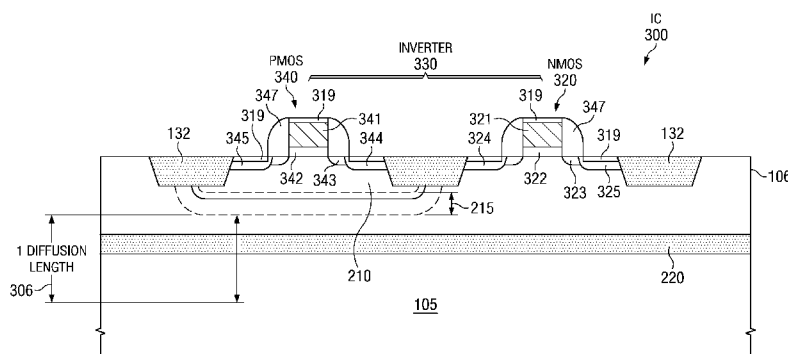


FIG. 3

(57) **Abstract:** A Metal-Oxide Semiconductor (MOS) transistor (340) includes a substrate (105) having a topside semiconductor surface (106) doped with a first dopant type having a baseline doping level. A well (210) is formed in the semiconductor surface (106) doped with a second doping type. The well forms a well-substrate junction having a well depletion region (215). A retrograde doped region (220) is below the well-substrate junction doped with the first dopant type having a peak first dopant concentration of between 5 - 100 times above the baseline doping level at a location of the peak first dopant concentration, wherein with zero bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is below the bottom of the well depletion region. A gate structure (341, 342) is on the well. Source (344) and drain regions (345) are on opposing sides of the gate structure.

MOS TRANSISTORS HAVING REDUCED LEAKAGE WELL-SUBSTRATE JUNCTIONS

[0001] This relates to semiconductor devices including integrated circuits having pn junctions, including doping arrangements for reducing pn junction leakage.

BACKGROUND

[0002] Leakage current has become a significant contributor to standby power dissipation of Complementary Metal-Oxide Semiconductor (CMOS) integrated circuits (ICs), and is commonly measured at the transistor level by the transistor parameter off-state current (I_{off}). I_{off} is the drain current when the applied gate voltage is zero, with some applied drain-to-source voltage (V_{dd}).

[0003] I_{off} is influenced by the device's threshold voltage (V_t), channel physical dimensions, channel/surface doping profile, drain/source junction depth, gate dielectric thickness, and V_{dd} . I_{off} in long-channel devices is known to be dominated by reverse-bias leakage from the drain-well junctions and the well-substrate junctions. Short-channel transistors typically require lower power supply levels to reduce their internal electric fields and power consumption. Use of lower power supply levels forces a reduction in the V_t , which can cause a substantial increase in I_{off} . Accordingly, IC standby power can be reduced if reverse bias well-substrate leakage can be reduced.

SUMMARY

[0004] Disclosed embodiments include methods for forming Metal-Oxide Semiconductor (MOS) transistors and ICs therefrom including at least one high energy implant for enhancing (increasing) the substrate doping below the bottom of the depletion region of the well-substrate junction (well depletion region) to add a retrograde doped region within one diffusion length of the bottom of this depletion region. The increased substrate doping level significantly reduces junction leakage by reducing the minority carrier doping level below the well depletion region.

[0005] In the case of an nwell in a p-substrate, it has been found one or more high energy boron implants between the bottom of the nwell depletion region and one diffusion length below

beyond reduces the nwell to the surrounding p-type substrate junction leakage. Alternatively, if the substrate material is n-type, and the well is a pwell, one or more n-type implants (P, As, or Sb) can be positioned below the pwell to reduce pwell to the surrounding n-type substrate junction leakage.

[0006] Disclosed retrograde doped regions are positioned in an appropriate depth range so that they are deep enough to not significantly alter electrical characteristics of devices within the well including the threshold voltages (V_t) of MOS devices in the well, the well-substrate breakdown voltage and well-substrate capacitance. This positioning is also close enough (within 1 diffusion length) to significantly increase the doping level in the substrate doping near the bottom of the well-substrate junction to reduce the minority carrier doping level therein to reduce the well-substrate junction leakage.

[0007] Disclosed retrograde doped regions below the well-substrate junction generally have a peak dopant concentration of 5 to 100 times above the baseline doping level provided by the surrounding substrate at the location (i.e. depth) of the peak dopant concentration. For example, for a p-substrate having a boron doping level of $1 \times 10^{15} \text{ cm}^{-3}$, the retrograde doped regions below the well-substrate junction provide a peak boron concentration of from $5 \times 10^{15} \text{ cm}^{-3}$ to $1 \times 10^{17} \text{ cm}^{-3}$. In addition, with zero bias across the well-substrate junction at least 90% of a total (integrated) dose of the retrograde doped region is below the bottom of the well depletion region. As implanted, typically > 95% (e.g., > 99%) of the high energy implant dose(s) are below a bottom of the well depletion region, while in the completed IC the percentage may drop to at least 90% due to post-implant diffusion.

[0008] One disclosed embodiment is a MOS transistor including a substrate having a semiconductor surface doped with a first dopant type having a baseline doping level. A well is formed in the semiconductor surface doped with a second doping type. The well forms a well-substrate junction having a well depletion region. A retrograde doped region is below the well-substrate junction doped with the first dopant type having a peak first dopant concentration of between 5 to 100 times above the baseline doping level at a location of the peak first dopant concentration, wherein with zero bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is below the bottom of the well depletion region. A gate structure on the well. Source and drain regions are on opposing sides of the gate structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a flow chart that shows steps in an example method including at least one high energy implant for forming a MOS transistor including a well-substrate junction having a retrograde doped region below the well depletion region for reducing leakage, according to an example embodiment.

[0011] FIG 2A illustrates two example high energy implant conditions which form a retrograde doped region that increases the p-type doping in the substrate below the nwell shown, while FIG. 2B illustrates the doping profile of a disclosed retrograde doped region formed using three separate high energy implant conditions to increase the p-substrate doping below the nwell. The baseline conditions are shown as "baseline p-substrate doping", where there is no addition of any disclosed high energy implant.

[0012] FIG. 3 is a simplified cross sectional depiction of an IC showing a CMOS inverter in a topside semiconductor surface of a substrate, where the PMOS transistor is in an nwell having a retrograde doped region below the nwell to provide a disclosed reduced leakage well-substrate diode, according to an example embodiment.

[0013] FIG. 4 provides data showing the log of nwell reverse leakage current (I) as a function of inverse temperature ($1/kT$) with and without example leakage reduction high energy implants described above relative to FIG. 2A. A 5 to 8 times reduction in junction leakage for a disclosed nwell diode is shown as compared to a baseline nwell diode that did not include any disclosed high energy implant.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0014] FIG. 1 is a flow chart that shows steps in an example method 100 including at least one high energy implant for enhancing (increasing) the substrate doping below the well-substrate junction's depletion region to add a retrograde doped region below the junction for forming a MOS transistors having a reduced leakage well-substrate junction, according to an example embodiment. The well-substrate junction leakage is reduced by increasing the substrate surface doping between the bottom of well depletion region and 1 diffusion length out from the well depletion region, thus reducing the minority carrier doping level, without significantly altering electrical characteristics of devices within the well, including the V_t and junction capacitance of

MOS devices within the well. A typical value for a diffusion length for a well-substrate junction may be from 5 to 20 μm .

[0015] Step 101 comprises forming a well doped with a second doping type in a semiconductor surface doped with a first dopant type having a baseline doping level, wherein the well forms a well-substrate junction. The well can be an n-well, and the semiconductor surface a p- surface, such as a bulk p- substrate, or a p-epi layer on a p⁺ substrate. The well can be a p-well and the semiconductor surface an n- surface, such as a bulk n-substrate, or a n-epi layer on a n⁺ substrate. Well formation can comprise conventional well formation using at least one ion implant followed by an anneal/ drive. The substrate can comprise silicon, silicon-germanium, or other substrate material that provides a semiconductor surface.

[0016] Step 102 comprises ion implantation with a first dopant type (same type as the semiconductor substrate surface) at a dose and energy to form a retrograde doped region below the well depletion region of the well-substrate junction, having a peak first dopant concentration of 5 to 100 times the baseline doping level at a location of the peak first dopant concentration. The implant energies are selected so that after ion implantation, with zero bias across the well-substrate junction, at least 90% of a total dose of the retrograde doped region is below the bottom of the well depletion region, and in one embodiment at least 80% of the implanted dose is also within two (2) μm from the bottom of the well depletion region.

[0017] FIG. 2A described below shows example dopant profiles as well as the baseline doping profile provided by the semiconductor substrate surface. In one embodiment the implantation is a blanket ion implantation, so that no added mask levels are needed. In another embodiment, a set of one or more implants may be masked to apply the resulting leakage reduction to selected wells while masking the high energy implants to maintain high substrate resistivity in other wells and regions (e.g., under integrated inductors).

[0018] In the case of a nwell in p-substrate surface, the first dopant type is generally boron, and the implant dose is generally between $2 \times 10^{12} \text{ cm}^{-2}$ and $3 \times 10^{13} \text{ cm}^{-2}$, and the energy is generally from 400 keV to 1.8 MeV, but can be at a higher energy provided the dose remains within one diffusion length of the bottom of the well depletion region. The ion implantation can include at least two different implants having different implant energies, such as the three separate implants described below relative to FIG. 2B.

[0019] Step 103 comprises forming a gate structure on the well including a gate electrode on a gate dielectric. Step 104 comprises forming source and drain regions on opposing sides of the gate structure. Although not described relative to method 100, disclosed methods generally include conventional CMOS processing including forming isolation (e.g., shallow trench isolation), lightly doped drains, spacers, various channel implants, multi-level metallization, and passivation processing.

[0020] FIG. 2A illustrates simulations of two example high energy implant conditions which form a retrograde doped region that significantly increases the p-type doping in the substrate below the nwell-substrate depletion region 215. The example implant conditions are shown as a $^{11}\text{B}^+$ dose of $4 \times 10^{12} \text{ cm}^{-2}$ at 750 keV, and a $^{11}\text{B}^+$ dose of $1 \times 10^{13} \text{ cm}^{-2}$ at 750 keV.

[0021] The baseline condition is shown as "baseline p-substrate doping", where there is no addition of a disclosed high energy implant. The baseline p-substrate doping profile shown is not constant as a function of depth due to the addition of an optional blanket boron implant for improving the nwell-to-nwell isolation. The position of peak doping for each of the boron high energy implant is set by the implant energy (and stopping power of the substrate) such that implanted profile encroaches minimally into the nwell 210 and nwell-substrate depletion region 215. The retrograde doped region 220 is below the nwell-substrate depletion region 215 and has a peak dopant concentration about 1.5 μm s from the surface of the device (about $1 \times 10^{17} \text{ cm}^{-3}$ for the $4 \times 10^{12} \text{ cm}^{-2}$ dose and about $3 \times 10^{17} \text{ cm}^{-3}$ for the $1 \times 10^{13} \text{ cm}^{-2}$ dose) which is more than an order of magnitude above the baseline p-substrate doping level at the depth of the peak dopant concentration which is about $4 \times 10^{15} \text{ cm}^{-3}$ at 1.5 μm s from the surface. Substantially all of the retrograde doped region 220 can be seen to be positioned between a bottom of the well depletion region 215 and 2 microns from the bottom of well depletion region 215.

[0022] The implant dose can be set to reduce the leakage within the constraints a) ability to adequately anneal out implant damage from the high energy implants to the crystal and b) to prevent an increase of the depletion region electric field caused by encroachment of dopant from the high energy implant into the well depletion region. Multiple (additive) high energy implants may be used with different dose and energy combinations, such as described below relative to FIG. 2B to achieve increased leakage suppression given other design constraints (e.g., well breakdown voltage, well capacitance, deep substrate resistivity).

[0023] Disclosed retrograde doped regions may be contrasted with conventional deep implants used for CMOS latchup suppression and well-to-well isolation. Disclosed retrograde doped regions involve a different design objective and subsequent well design and doping profile for achieving reduced leakage, being suppression of minority carriers within a diffusion length of the well depletion region to reduce junction leakage. Implanted profiles for leakage reduction are at a lower concentration as compared to buried layers and doped regions suited for well-to-well leakage reduction. FIG. 2B illustrates the doping profile of a disclosed retrograde doped region formed using three separate high energy implant conditions to increase the p-substrate doping below an nwell. As in FIG. 2A, the baseline condition is shown as "baseline p-substrate doping", where there is no addition of any disclose high energy implant.

[0024] FIG. 3 is a simplified cross sectional depiction of an IC 300 showing a CMOS inverter 330 in a topside semiconductor surface 106 of a substrate 105, where the PMOS transistor 340 is in an nwell 210 having a retrograde doped region 220 between the bottom of the nwell-substrate depletion region 215 and the one diffusion length 306 shown to provide a disclosed reduced leakage well-substrate diode, according to an example embodiment. The CMOS inverter 330 comprises an NMOS transistor 320 and PMOS transistor 340 (coupling between NMOS transistor 320 and PMOS transistor 340 not shown). Substrate 105 can be a p-substrate or a p-epi layer on a p⁺ substrate. Dielectric isolation is shown as trench isolation 132.

[0025] Although the topside semiconductor surface 106 is described in FIG. 3 as being p-type, in another embodiment the topside semiconductor surface 106 can be n-type, the well a pwell, and the MOS transistor having a disclosed reduced leakage well-substrate diode can be an n-channel MOS transistor. Moreover, although not shown, IC 300 generally includes a large number of MOS transistors and other circuit elements, such as capacitors, resistors, capacitors, diodes, etc. In addition, although not shown, IC 300 includes functional circuitry, which is circuitry that realizes and carries out desired functionality of IC 300, such as that of a digital IC (e.g., digital signal processor) or analog IC (e.g., amplifier or power converter). The capability of functional circuitry provided by IC 300 may vary, for example ranging from a simple device to a complex device. The specific functionality contained within functional circuitry is not of importance to disclosed embodiments.

[0026] Although only one nwell 210 is shown, disclosed ICs generally includes a plurality of nwells 210. Retrograde doped region 220 is shown as blanket doped region. However, in other embodiments, the retrograde doped region 220 can be a patterned region, so that a portion of the plurality of nwells or other regions on the IC do not include the retrograde doped region 220, such as for integrated inductors.

[0027] PMOS transistor 340 comprises gate electrode 341, gate dielectric 342, sidewall spacer 347, lightly doped drains 343, source 344, and drain 345, with a silicide layer 319 on the source 344, drain 345, and gate electrode 341 for the case the gate electrode 341 comprises polysilicon. NMOS transistor 320 comprises gate electrode 321, gate dielectric 322, sidewall spacer 347, lightly doped drains 323, source 324 and drain 325, with a silicide layer 319 on the source 324, drain 325 and gate electrode 321 for the case the gate electrode 321 comprises polysilicon.

EXAMPLES

[0028] Disclosed embodiments are further illustrated by the following specific examples, which should not be construed as limiting the scope or content of this disclosure in any way.

[0029] Technology computer-aided design (TCAD) simulations were performed to simulate nwell diodes with disclosed additional high energy implants which position dopants in the semiconductor surface below the bottom of the nwell depletion region to demonstrate a reduction in reverse leakage current as compared to controls (identified as "baseline") not including any disclosed high energy implant. FIG. 4 provides data showing the log of nwell reverse leakage current (I) as a function of inverse temperature ($1/kT$) with and without example leakage reduction high energy implants described above relative to FIG. 2A. The bias conditions used was the rated V_{dd} of the nwell + 10%; in this case, 3.6V (reverse bias). A 5 to 8x reduction in junction leakage for a disclosed nwell diode is shown as compared to a baseline nwell diode that did not include any disclosed high energy implant.

[0030] Advantages of the disclosed embodiments include no need for additional masks and associated additional cost. Blanket high energy implants can be added to existing process flows without measurably altering other device properties. As evidenced in FIG. 4, standby leakage can be reduced by up to an order of magnitude, which can reduce IC standby power for disclosed ICs.

[0031] The disclosed embodiments can be integrated into a variety of assembly flows to form a variety of different semiconductor integrated circuit (IC) devices and related products. The assembly can comprise single semiconductor die or multiple semiconductor die, such as PoP configurations comprising a plurality of stacked semiconductor die. A variety of package substrates may be used. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, CMOS, BiCMOS and MEMS.

[0032] Those skilled in the art to which this disclosure relates will appreciate that many other embodiments and variations of embodiments are possible within the scope of the claimed invention, and further additions, deletions, substitutions and modifications may be made to the described embodiments without departing from the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A Metal-Oxide Semiconductor (MOS) transistor, comprising:
 - a substrate having a semiconductor surface doped with a first dopant type having a baseline doping level,
 - a well formed in the semiconductor surface doped with a second doping type, the well forming a well-substrate junction having a well depletion region;
 - a retrograde doped region below the well-substrate junction doped with the first dopant type having a peak first dopant concentration of between 5 to 100 times above the baseline doping level at a location of the peak first dopant concentration, wherein with zero bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is below a bottom of the well depletion region;
 - a gate structure on the well, and
 - source and drain regions on opposing sides of the gate structure.
2. The MOS transistor of claim 1, wherein the well is an n-well, and the semiconductor surface is a p- surface.
3. The MOS transistor of claim 1, wherein the well is a p-well and the semiconductor surface is an n- surface.
4. The MOS transistor of claim 1, wherein the retrograde doped region includes at least two peaks including the peak first dopant concentration and another peak.
5. The MOS transistor of claim 1, wherein with 3 volt reverse bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is between the bottom of the well depletion region and one diffusion length below the bottom of the well depletion region.

6. An integrated circuit (IC), comprising:
 - a substrate having a semiconductor surface doped with a first dopant type having a baseline doping level,
 - a plurality of wells formed in the semiconductor surface doped with a second doping type each forming a well-substrate junction having a well depletion region;
 - a plurality of p-channel or n-channel Metal-Oxide Semiconductor (MOS) transistor formed in the plurality of wells including:
 - a gate structure on the plurality of wells;
 - source and drain regions on opposing sides of the gate structure, and
 - a retrograde doped region below the well-substrate junction doped with the first dopant type having a peak first dopant concentration of between 5 to 100 times above the baseline doping level at a location of the peak first dopant concentration, wherein with zero bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is below a bottom of the well depletion region.
7. The IC of claim 6, wherein the IC is a complementary MOS (CMOS) IC including the plurality of p-channel MOS transistors formed in the plurality of wells, further comprising a plurality of n-channel MOS transistors formed in the semiconductor surface.
8. The IC of claim 6, wherein the plurality of wells are n-wells, and wherein the plurality of p-channel or n-channel MOS transistors are the p-channel MOS transistors.
9. The IC of claim 6, wherein the plurality of wells are p-wells and wherein the plurality of p-channel or n-channel MOS transistors are the n-channel MOS transistors.
10. The IC of claim 6, wherein the retrograde doped region is a blanket doped region.
11. The IC of claim 8, wherein the retrograde doped region is a patterned region, and wherein a portion of the plurality of n-wells do not include the retrograde doped region.

12. The IC of claim 6, wherein with 3 volt reverse bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is between the bottom of the well depletion region and one diffusion length below the bottom of the well depletion region.

13. A method of forming a Metal-Oxide Semiconductor (MOS) transistor, comprising:
forming a well doped with a second doping type in a semiconductor surface doped with a first dopant type having a baseline doping level, the well forming a well-substrate junction having a well depletion region;

ion implantation with the first dopant type at a dose and energy to form a retrograde doped region below the well-substrate junction having a peak first dopant concentration of between 5 to 100 times above the baseline doping level at a location of the peak first dopant concentration, wherein with zero bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is below a bottom of the well depletion region;

forming a gate structure on the well, and

forming source and drain regions on opposing sides of the gate structure.

14. The method of claim 13, wherein with 3 volt reverse bias across the well-substrate junction at least 90% of a total dose of the retrograde doped region is between the bottom of the well depletion region and one diffusion length below the bottom of the well depletion region.

15. The method of claim 13, wherein the first dopant type is boron, the well is an n-well, the semiconductor surface is a p- surface, and the dose is $2 \times 10^{12} \text{ cm}^{-2}$ to $3 \times 10^{13} \text{ cm}^{-2}$ and wherein the energy is from 400 keV to 1.8 MeV.

16. The method of claim 13, wherein the energy includes at least two different energies.

17. The method of claim 13, wherein the well comprises a plurality of nwells and the method comprises a method of forming a complementary MOS (CMOS) integrated circuit (IC)

comprising a plurality of p-channel MOS transistors outside the plurality of nwells and a plurality of p-channel MOS transistor formed in the plurality of nwells.

18. The method of claim 17, wherein the retrograde doped region is a blanket doped region.

19. The method of claim 17, wherein the retrograde doped region is a patterned region, and wherein a portion of the plurality of nwells do not include the retrograde doped region.

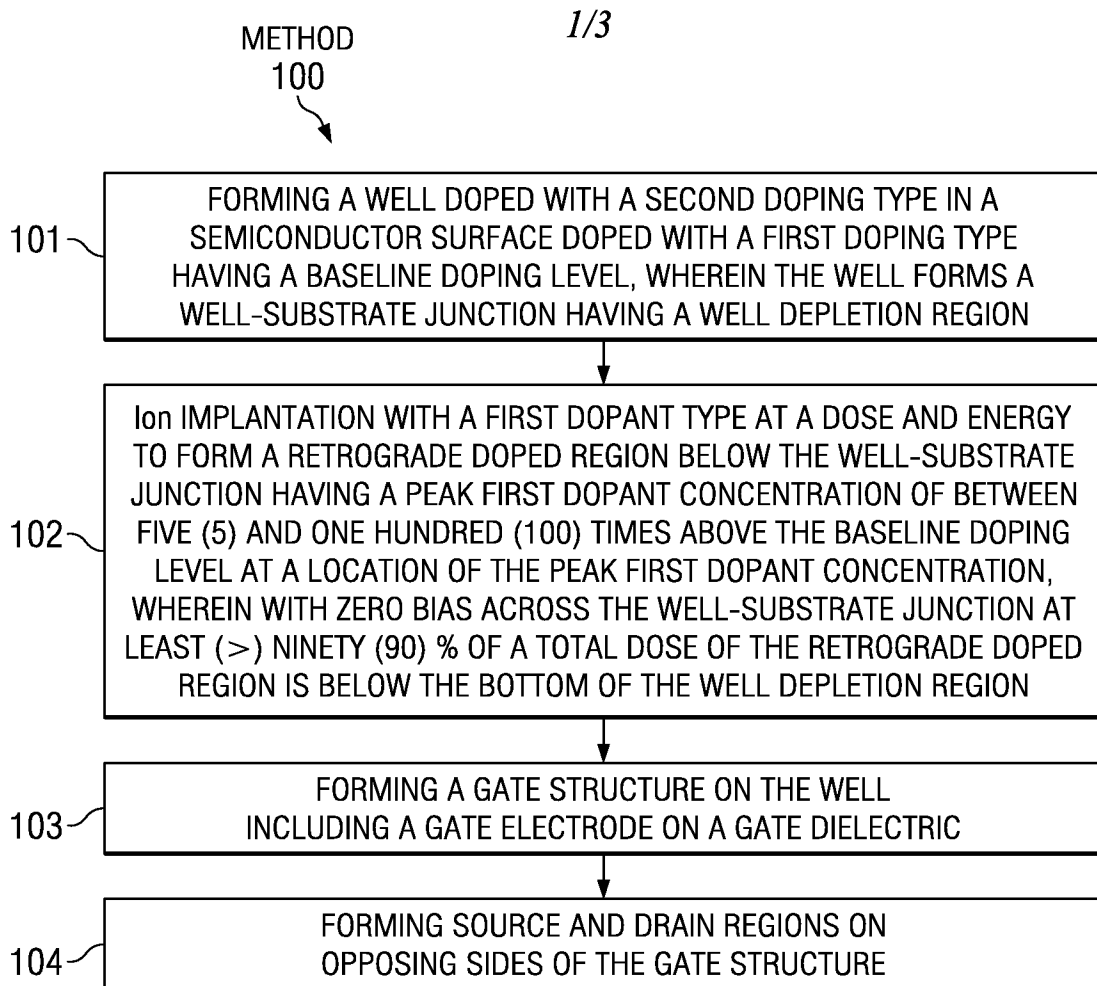


FIG. 1

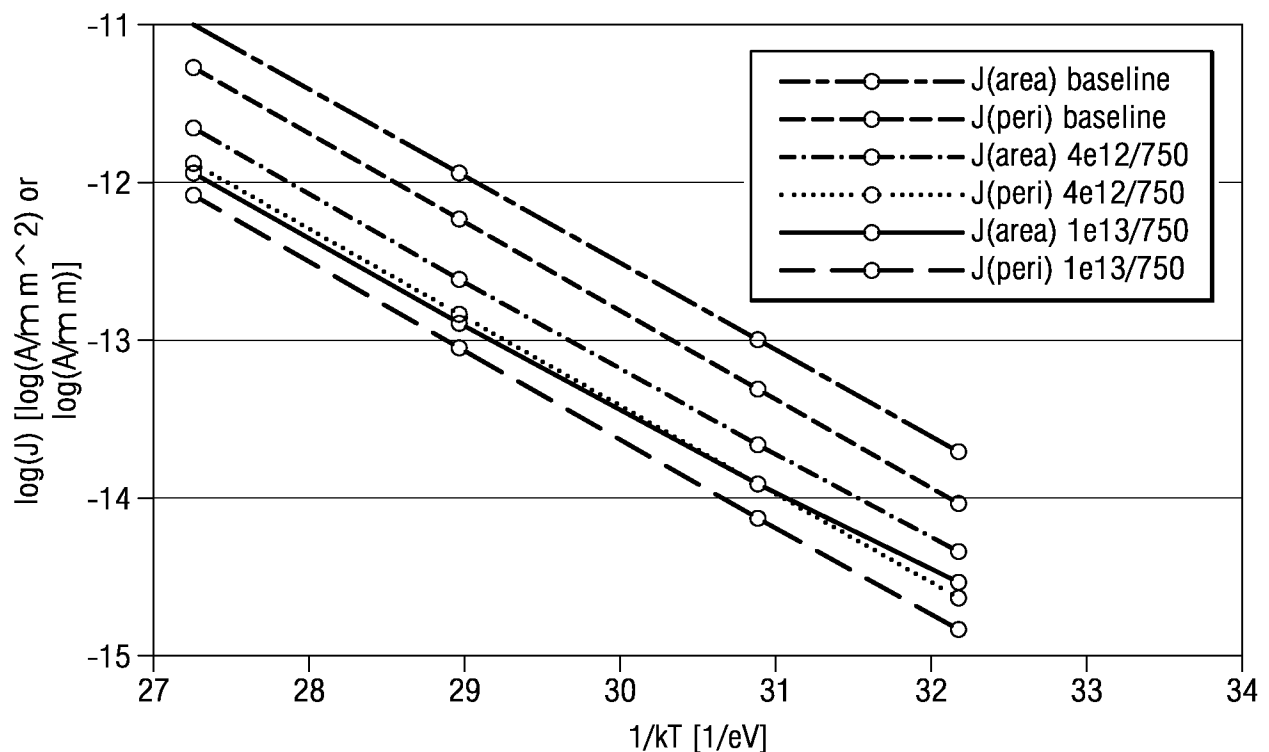


FIG. 4

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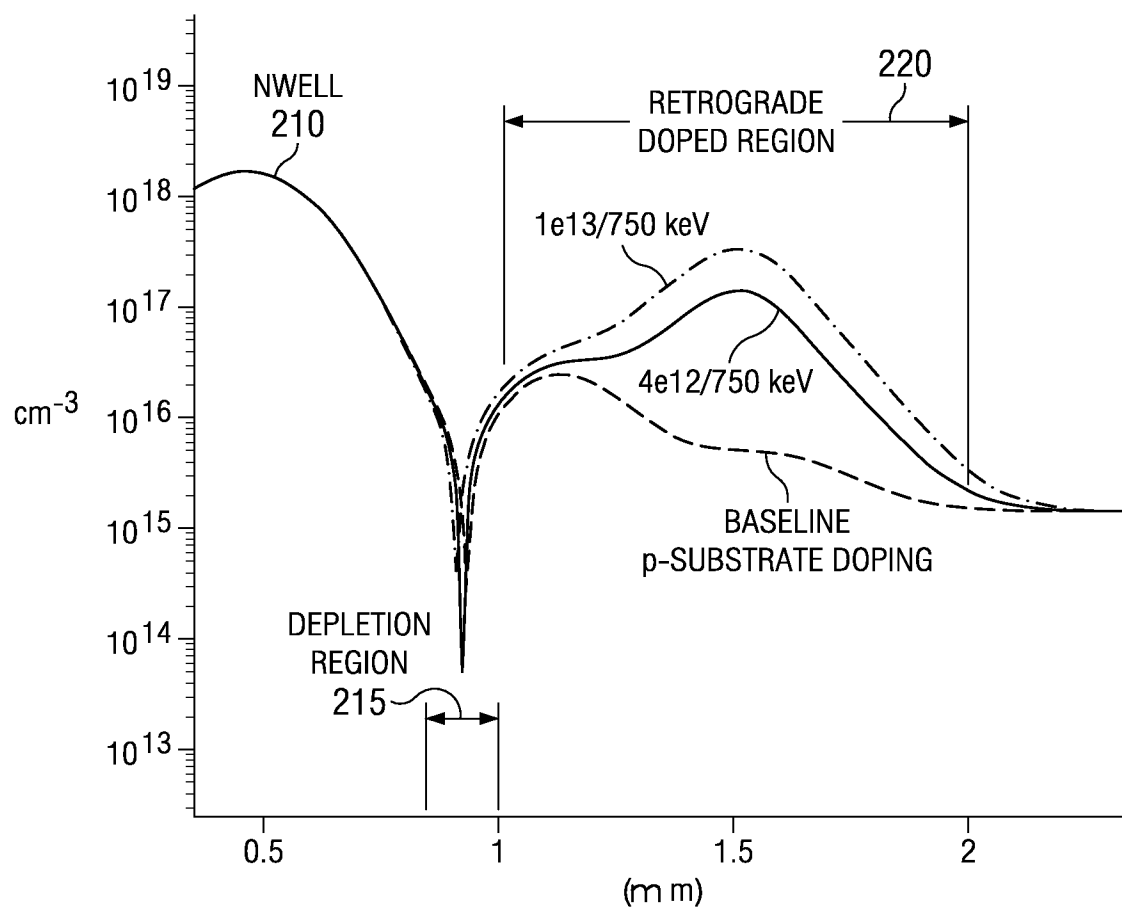


FIG. 2A

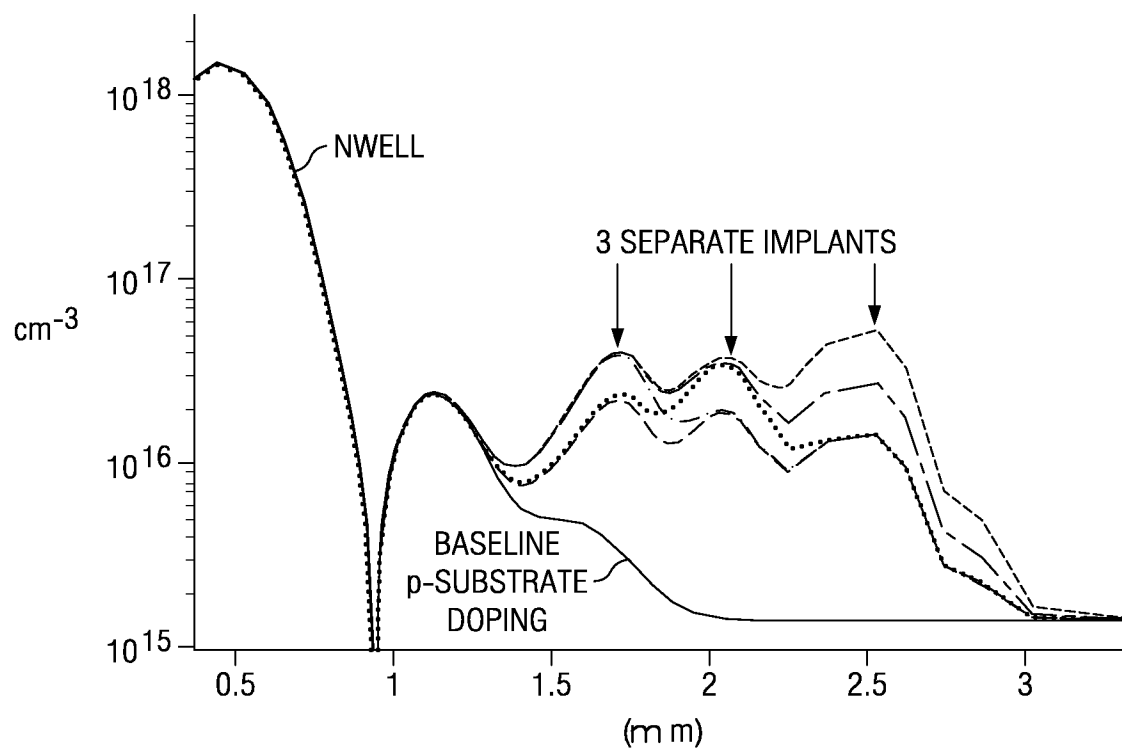


FIG. 2B

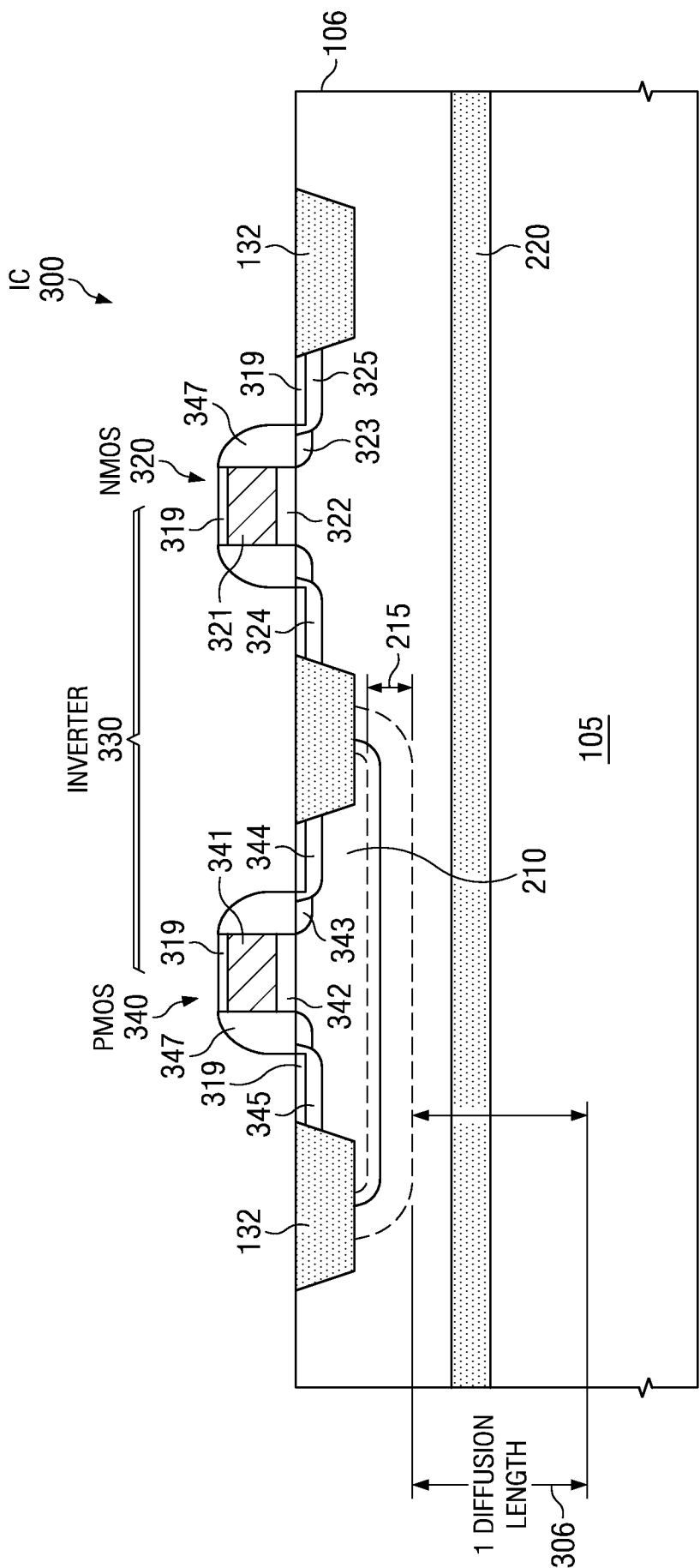


FIG. 3

A. CLASSIFICATION OF SUBJECT MATTER**H01L 29/78(2006.01)i, H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 27/06; H01L 21/336; H01L 31/12; H01L 31/062; H01L 29/788

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: well, retrograde, MOS, leakage, current, depletion

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2001-0059613 A (SK HYNIX INC.) 06 July 2001 See abstract, pages 2-3, claim 1 and figures 10-11.	1-19
A	US 2004-0126947 A1 (YONG-SUN SOHN) 01 July 2004 See paragraphs [0014], [0028]-[0029], [0061]-[0064], [0073] and figures 6-7.	1-19
A	KR 10-1999-0017331 A (SAMSUNG ELECTRONICS CO., LTD.) 15 March 1999 See abstract, pages 2-3, claim 1 and figures 2-3.	1-19
A	KR 10-2003-0057877 A (SK HYNIX INC.) 07 July 2003 See abstract, pages 2-3, claims 1, 3-5 and figures 1a-2.	1-19
A	US 6310366 B1 (HOWARD E. RHODES et al.) 30 October 2001 See column 5, line 53 - column 6, line 6, column 6, line 36 - column 8, line 17 and figures 5-6.	1-19



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

22 November 2013 (22.11.2013)

Date of mailing of the international search report

22 November 2013 (22.11.2013)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/054641

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