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(54) **Title**: POLAR REGIONS FOR ELECTROSTATIC DE-CHUCKING WITH LIFT PINS

(57) **Abstract**: An apparatus for electrostatic chucking and dechucking of a semiconductor wafer includes an electrostatic chuck with a number of zones. Each zone includes one or more polar regions around a lift pin that contacts a bottom surface of the semiconductor wafer. The apparatus also includes one or more controllers that control the lift pins and one or more controllers that control the polar regions. The controller for the lift pins receives data from one or more sensors and uses the data to adjust the upward force of the lift pins. Likewise, the controller for the polar regions receives data from the sensors and uses the data to adjust the voltage in the polar regions.

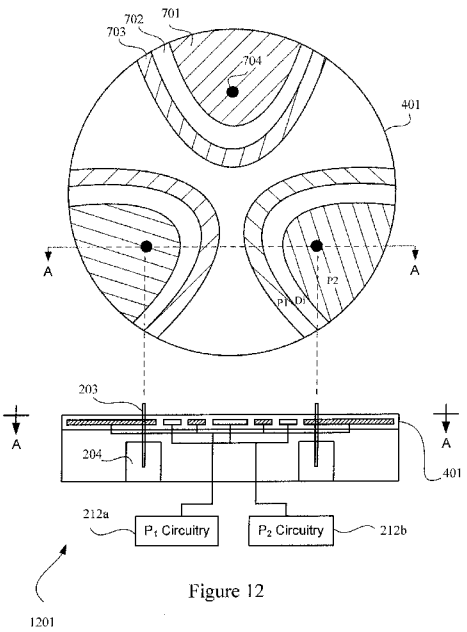


Figure 12

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Polar Regions for Electrostatic De-chucking With Lift Pins

by Inventor: Fangli J. Hao

BACKGROUND

[0001] The designs for many semiconductor processing facilities involve a process chamber where a semiconductor wafer is processed (e.g., etched or subjected to deposition) by a plasma. The designs often include an electrostatic chuck (or ESC) to clamp the semiconductor wafer during such processing, through the use of an electrical pole pattern in the electrostatic chuck. The design of the electrical pole pattern can have an effect on the uniformity of the clamping.

[0002] Once the processing is complete, the semiconductor wafer is separated or de-chucked from the electrostatic chuck so that it can be removed from the process chamber. However, residual electrostatic charge might remain, making efficient separation difficult. Here again, the design of the electrical pole pattern can have an effect on the efficiency of such separation.

[0003] To address the problem of residual electrostatic charge and to assist with process automation, among other things, some designs for semiconductor processing facilities include lift pins that raise the semiconductor wafer off the electrostatic chuck into a position where the semiconductor wafer can be retrieved with a robotic arm. Of course, if the force generated by such lift pins is not monitored and controlled, the lift pins can damage or even break the semiconductor wafer. In this regard, co-owned U.S. Patent No. 6,646,857 describes, among other things, a group of lift pins that are connected in a yoke arrangement and that are coupled to a feedback loop.

SUMMARY

[0004] In an example embodiment, an apparatus for electrostatic chucking and dechucking of a semiconductor wafer includes an electrostatic chuck with a number of zones. Each zone includes one or more polar regions around a lift pin that contacts a bottom surface of the semiconductor wafer. The apparatus also includes one or more controllers that control the lift pins and one or more controllers that control the polar region. In an example embodiment, the controller for the lift pins receives data from one or more sensors and uses the data to adjust the upward force of the lift pins. Likewise, in an example embodiment, the controller for the polar regions receives data from the sensors and uses the data to adjust the voltage in the polar regions.

[0005] In another example embodiment, an automated method for processing semiconductor wafers is performed by a process controller. The process controller begins by placing a semiconductor wafer on an electrostatic chuck in a process chamber. The electrostatic chuck includes a number of zones and each zone includes one or more polar regions around a lift pin moved by pneumatic pressure. The process controller then clamps the semiconductor wafer to the electrostatic chuck by applying a voltage to the one or more polar regions. The process controller processes the semiconductor and terminates the processing operation. And the process controller applies another voltage to one or more polar regions of one or more zones to initiate dechucking. The process controller then begins lifting the semiconductor wafer off the electrostatic chuck with the lift pins. The process controller uses a sensor to measure the electrostatic force between the semiconductor and the electrostatic chuck and adjusts the upward force to avoid damage to the semiconductor wafer.

[0006] In another example embodiment, an apparatus for processing a semiconductor wafer includes a process chamber with a top electrode coupled to an RF power source and an electrostatic chuck coupled to an RF power source. The electrostatic chuck includes a number of zones and each zone includes one or more polar regions around a lift pin that contacts a bottom surface of the semiconductor wafer.

[0007] The advantages of the present invention will become apparent from the following detailed description, which taken in conjunction with the accompanying drawings, illustrates by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a schematic diagram showing a system for processing a semiconductor wafer in a process chamber, in accordance with an example embodiment.

[0009] Figure 2 is a schematic diagram showing a system for electrostatic chucking and dechucking, in accordance with an example embodiment.

[0010] Figure 3A is a schematic diagram showing a pneumatic lift pin with a pneumatic sensor, in accordance with an example embodiment.

[0011] Figure 3B is a schematic diagram showing a pneumatic lift pin with a piezoelectric sensor, in accordance with an example embodiment.

[0012] Figure 4A is a diagram showing a perspective view of a pneumatic cylinder, in accordance with an example embodiment.

[0013] Figure 4B is a diagram showing a cross-section view of a pneumatic cylinder, in accordance with an example embodiment.

[0014] Figure 5 is a diagram showing a group of lift pins and a sensor pin, in accordance with an alternative example embodiment.

[0015] Figure 6 is a diagram showing a group of lift pins capable of being connected to a single pneumatic cylinder, in accordance with an example embodiment.

[0016] Figure 7 is a schematic diagram showing a system of multiple zones of patterned polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0017] Figure 8 is a schematic diagram showing a system with a sensor pin and multiple zones of patterned polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0018] Figure 9 is a schematic diagram showing a system with an alternative pattern for polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0019] Figure 10 is a schematic diagram showing a system with another alternative pattern for polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0020] Figure 11A is a schematic diagram showing a system for creating two polar regions, in accordance with an example embodiment.

[0021] Figure 11B is a schematic diagram showing a system for creating two polar regions using circuitry in a dielectric layer, in accordance with an example embodiment.

[0022] Figure 12 is a schematic diagram showing a cross-sectional view of a system with multiple zones of patterned polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0023] Figure 13 is a schematic diagram showing the electrical circuitry for a system with multiple zones of patterned polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0024] Figure 14 is a schematic diagram showing alternative electrical circuitry for a system with multiple zones of patterned polar regions centered on a bore for a lift pin, in accordance with an example embodiment.

[0025] Figure 15 is a flowchart diagram showing a process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor pin, in accordance with an example embodiment.

[0026] Figure 16 is a flowchart diagram showing another process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor pin, in accordance with an example embodiment.

[0027] Figure 17 is a flowchart diagram showing a process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor associated one-to-one with a lift pin, in accordance with an example embodiment.

[0028] Figure 18 is a flowchart diagram showing another process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor associated one-to-one with a lift pin, in accordance with an example embodiment.

DETAILED DESCRIPTION

[0029] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the example embodiments. However, it will be apparent to one skilled in the art that the example embodiments may be practiced without some of these specific details. In other instances, implementation details and process operations have not been described in detail, if already well known.

[0030] Figure 1 is a schematic diagram showing a system for processing a semiconductor wafer in a process chamber, in accordance with an example embodiment. As depicted in that figure, a system 100 includes a process chamber 102 that is used for processing semiconductor wafers, e.g., through etching or deposition operations. Process chamber 102 includes an electrostatic chuck 104a which is designed to clamp or grip a semiconductor wafer 106. The process chamber 102 includes a top electrode 114 which is designed to receive processing gases that are distributed into the plasma region 112 during processing.

[0031] The plasma region 112 is defined between the surface of the top electrode 114 and the surface of the semiconductor wafer 106. The top electrode 114 is connected to a match box 116a and to an RF (radio frequency) power source 118a. The electrostatic chuck 104 is connected to a match box 116b and an RF power source 118b. The process chamber 102 is provided with outlets 120 which pump out excess gases from within the process chamber 102 during processing. When in operation, the RF power supply 118a biases the top electrode 114 and operates at frequencies of approximately 27 MHz, in some embodiments. The RF power source 118a is primarily responsible for generating most of the plasma density within the plasma region 112, while the RF power source 118b is primarily responsible for generating a bias

voltage within the plasma region 112. The RF power source 118b generally operates at lower frequencies of approximately 2 MHz.

[0032] It will be appreciated that the system shows a process chamber for a capacitively-coupled plasma. However, the inventions described below will work with other process chambers, including, for example, a process chamber for a transformer-coupled plasma (TCP), which might not have a top electrode. That is to say, Figure 1 is intended to be illustrative, rather than limiting.

[0033] Figure 2 is a schematic diagram showing a system for electrostatic chucking and dechucking, in accordance with an example embodiment. As depicted in this figure, a process chamber 102 includes an electrostatic chuck 104 for gripping or clamping a semiconductor wafer 106. It will be appreciated that in an alternative embodiment, semiconductor wafer 106 might be some other substrate suitable for processing in the process chamber 102. In turn, electrostatic chuck 104 includes bores (or passages) for three lift pins 203a, 203b, and 203c, each of which is connected to a corresponding pneumatic cylinder 204a, 204b, or 204c. Each of these pneumatic cylinders is associated with a corresponding sensor, 205a, 205b, or 205c. It will be appreciated that when in operation, the lift pins 203a, 203b, and 203c exert an upward force against the bottom surface of the semiconductor wafer 106.

[0034] A pneumatic controller 207 controls each of the pneumatic cylinders 204a, 204b, and 204c. In an example embodiment, the pneumatic controller 207 includes a separate control module for each cylinder, as is depicted in Figure 2. However, in an alternative example embodiment, the pneumatic controller 207 might not be so modularized. Also as depicted in this figure, sensors 205a, 205b, and 205c provide data to the sensor feedback module 210. It will be appreciated that this data relates to the electrostatic force (e.g., residual or post-processing) between the electrostatic chuck 104 and the semiconductor wafer 106. In turn, sensor feedback module 210 transmits data based on this data to the activation state logic 208, which might employ a threshold circuit 209, in an example embodiment. So for example, if the data transmitted by a specific sensor indicates an electrostatic force greater than a specific threshold, the activation state logic 208 might use the received data to cause the pneumatic controller 207 to cease further upward movement of a specific lift pin, in that example embodiment.

[0035] As also depicted in Figure 2, sensor feedback module 210 transmits data based on the sensor data to electrical-pole circuit controller 211, which in turn controls polar regions 212 (P1/P2) in electrostatic chuck 104. As will be explained in greater detail below, polar regions 212 might be arranged in specific patterns to facilitate uniform chucking and dechucking of the

semiconductor wafer 106. Also, as explained in greater detail below, electrical-pole circuit controller 211 might use the received data to adjust one or more of the polar regions 212 (P1 and/or P2) so as to lessen the electrostatic force between the electrostatic chuck 104 and the semiconductor wafer 106 and thereby facilitate dechucking of the semiconductor wafer 106.

[0036] Figure 3A is a schematic diagram showing a pneumatic lift pin with a pneumatic sensor, in accordance with an example embodiment. As depicted in this figure, pneumatic cylinder 204 includes lift pin 203 and receives air through an input pipe 301. A pneumatic sensor 205 is connected to pneumatic cylinder 204 and measures the air pressure (e.g., in psi) inside the cylinder beneath the piston 302. Pneumatic sensor 205 is located beneath pneumatic cylinder 204. However, this location is merely illustrative. In alternative example embodiments, pneumatic sensor 205 might be on a side of pneumatic cylinder 204 or even connected to input pipe 301. It will be appreciated that the air pressure inside the cylinder 204 beneath the piston 302 (and also the air pressure inside the input pipe 301) will reflect the electrostatic force between the electrostatic chuck and the semiconductor wafer when the lift pin 203 is in contact with the semiconductor wafer. Also as depicted in this figure, the pneumatic sensor 205 transmits its measure of the air pressure to a sensor feedback module, which is not shown but was described in relation to Figure 2.

[0037] Figure 3B is a schematic diagram showing a pneumatic lift pin with a piezoelectric sensor, in accordance with an example embodiment. As depicted in this figure, pneumatic cylinder 204 includes lift pin 203 and receives air through an input pipe 301. A piezoelectric sensor 205 (e.g., a sensor constructed from a piezoelectric material) is connected to pneumatic cylinder 204 and measures the air pressure (e.g., in psi) inside the cylinder beneath the piston 302. Piezoelectric sensor 205 is located beneath pneumatic cylinder 204. However, this location is merely illustrative. In alternative example embodiments, piezoelectric sensor 205 might be on a side of pneumatic cylinder 204 or even connected to input pipe 301. It will be appreciated that the air pressure inside the cylinder 204 beneath the piston 302 (and also the air pressure inside the input pipe 301) will reflect the electrostatic force between the electrostatic chuck and the semiconductor wafer when the lift pin 203 is in contact with the semiconductor wafer. Also as depicted in this figure, the piezoelectric sensor 205 transmits its measure of the air pressure to a sensor feedback module, which is not shown but was described in relation to Figure 2.

[0038] The above examples of sensors are illustrative, rather than limiting. Thus, in alternative example embodiment, the sensor might be a strain gauge or other suitable substitute.

[0039] Figure 4A is a diagram showing a perspective view of a pneumatic cylinder, in accordance with an example embodiment. As depicted in this figure, pneumatic cylinder 204 is located below an electrostatic chuck 104 which includes a conductive layer 402 beneath an insulating or dielectric layer 401. A semiconductor wafer 106 is gripped by the electrostatic chuck 104. In an example embodiment, conductive layer 402 might be made of a metal such as aluminum or copper and the insulating or dielectric layer 401 might be made of a material such as alumina (aluminum oxide), quartz, or yttrium, or a ceramic material. However, in another alternative embodiment, other materials with similar properties might be employed.

[0040] Figure 4B is a diagram showing a cross-section view of a pneumatic cylinder, in accordance with an example embodiment. As depicted in this figure, a pneumatic cylinder 204 uses a compressed gas from an input tube 403 to raise lift pin 203 through a bore in an electrostatic chuck 104 so that the lift pin 203 comes into contact with a semiconductor wafer 106. As in Figure 4A, the electrostatic chuck 104 includes a conductive layer 402 beneath an insulating or dielectric layer 401. In an example embodiment, the gas might simply be air, although other suitable gases (e.g., inert gases) might be used in alternative example embodiments. Also, in an example embodiment, the lift pin 203 might be made of the same conductive material (e.g., aluminum) as the conductive layer 402.

[0041] Figure 5 is a diagram showing a group of lift pins and a sensor pin, in accordance with an alternative example embodiment. As depicted in this figure, the electrostatic chuck 104 includes a conductive layer 402 beneath an insulating or dielectric layer 401. Each of three lift pins 203a, 203b, and 203c pass through the electrostatic chuck 104 and connect to a corresponding lift assembly 403a, 403b, and 403c, respectively, which are connected to a pin lifter yoke (not shown), such as the one described in the following figure. In contrast to the pneumatic cylinders previously described, each of these lift assemblies is not associated with a corresponding sensor. Rather, a sensor pin 501, similar to the lift pin shown in Figure 3, measures the electrostatic force between the semiconductor wafer and the electrostatic chuck 104. Here again, the sensor pin 501 might be made of the same conductive material (e.g., aluminum) as conductive layer 402. And the sensor pin 501 might be associated with a sensor that is pneumatic, piezoelectric, a strain gauge, etc., in alternative example embodiments.

[0042] Figure 6 is a diagram showing a group of lift pins capable of being connected to a single pneumatic cylinder, in accordance with an example embodiment. As depicted in the figure, three lift pins 203a, 203b, and 203c are connected to corresponding lift assemblies 403a, 403b, and 403c, respectively. Each of these lift assemblies is connected to a pin lifter yoke 502,

which is lifted upward from spokes 503a and 503c (the third spoke is not shown) by a pneumatic cylinder that is not shown. Likewise, the electrostatic chuck through which the lift pins pass is not shown in this figure. It will be appreciated that the pin lifter yoke 502 shown in this figure might be used with the lift pins 203a, 203b, and 203c, shown in Figure 5, in an example embodiment.

[0043] Here it will be appreciated that a sensor pin can also be used with a lift pin that has its own pneumatic cylinder rather than being connected to a pin lifter yoke, in an alternative example embodiment. However, in that example embodiment, the lift pin's pneumatic cylinder would not have a corresponding sensor. The only sensor would be the sensor pin.

[0044] Figure 7 is a schematic diagram showing a system of multiple zones of patterned polar regions around a bore (or passage) for a lift pin, in accordance with an example embodiment. As used herein, the term "around a bore" means that the patterned polar region is located near, adjacent, all the way around, partially around, or centered thereon. However, "centering" does not mean an exact center, but instead, oriented about the center of the bore or passage of the lift pin. As depicted in this figure, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, each of which is centered on a bore for a lift pin. Thus, the zone centered on the bore 704a includes a polar region 701a with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702a from another polar region 703a with an opposite electrical polarity P1. Similarly, the zone around the bore 704b includes a polar region 701b with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702b from another polar region 703b with an opposite electrical polarity P1. And zone around the bore 704c includes a polar region 701c with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702c (Di) from another polar region 703c with an opposite electrical polarity P1. Here it will be appreciated that each polar region achieves its polarity (e.g., positive or negative) by operation of an applied voltage (e.g., direct current or DC). So for example, polar region 703a might include an embedded conductive layer (or electrode pattern) that receives an applied voltage (e.g., direct current or DC) through the P1 circuitry. And polar region 701a includes an embedded conductive layer (or electrode pattern) that receives an applied voltage (e.g., direct current or DC) through the P2 circuitry.

[0045] In an example embodiment, there might be an approximate equality of the total surface area of polar regions with P1 polarity and of the total surface area of polar regions with P2 polarity. During gripping or chucking of the semiconductor wafer, the same voltage might be applied to each of the total surface areas, to prevent warping. However, in alternative example

embodiments, the total surface area of polar regions with P1 polarity might differ from the total surface area of polar regions with P2 polarity and the voltage applied to each of these total surface areas might also differ.

[0046] In an alternative example embodiment, the electrostatic chuck might be unipolar, rather than bipolar. In such an embodiment, there would be no polar regions with polarity P2. So, for example, both polar regions 701a and 703a in a zone might be associated with P1, though still separated by a dielectric region 702a and still centered on or around a bore for a lift pin 704a in the insulating or dielectric layer 401.

[0047] Figure 8 is a schematic diagram showing a system with a sensor pin and multiple zones of patterned polar regions centered on or around a bore for a lift pin, in accordance with an example embodiment. For the most part, Figure 8 is identical to Figure 7. Thus, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, each of which is around a bore for a lift pin. Thus, the zone around the bore 704a includes a polar region 701a with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702a from another polar region 703a with an opposite electrical polarity P1. Similarly, the zone around the bore 704b includes a polar region 701b with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702b from another polar region 703b with an opposite electrical polarity P1. And the zone around the bore 704c includes a polar region 701c with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702c (Di) from another polar region 703c with an opposite electrical polarity P1.

[0048] Additionally, Figure 8 shows a bore 805 for a sensor pin, as described earlier. Thus, Figure 8 might be used in an example embodiment with the pin lifter yoke depicted in Figure 5B or in an example embodiment where a lift pin's pneumatic cylinder lacks a corresponding sensor.

[0049] Figure 9 is a schematic diagram showing a system with an alternative pattern for polar regions centered on or around a bore for a lift pin, in accordance with an example embodiment. As depicted in this figure, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, Zone 1, Zone 2, and Zone 3. Once again, each zone is around a bore for a lift pin. Thus, the zone around the bore 704 includes a polar region 701 with an electrical polarity (e.g., positive or negative) P1 separated by a dielectric region 702 from another polar region 703 with an opposite electrical polarity P2. In contrast to earlier example embodiments in which the polar regions were shaped as half-rings, the polar regions in this example embodiment are shaped as rings.

[0050] Figure 10 is a schematic diagram showing a system with another alternative pattern for polar regions around a bore for a lift pin, in accordance with an example embodiment. As depicted in this figure, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, each of which is around a bore for a lift pin. Thus, the zone around the bore 704 includes a polar region 701 with an electrical polarity (e.g., positive or negative) P1, which is separated by a dielectric region 702 from another polar region 703 with an opposite electrical polarity P2, which, in turn, is separated from another polar region 1002 with a polarity P1 by a dielectric region 1001. It will be appreciated that other geometric patterns might be substituted for the geometric patterns shown, e.g., in Figures 8-10. That is to say, the geometric patterns shown in those figures are intended to be illustrative, rather than limiting.

[0051] It will be appreciated that the figures described above, the dielectric layer 401 included three zones. In alternative example embodiments, there might be only two zones or there might be four, five, six or more zones. Generally, the number of zones is determined by the number of lift pins, although some embodiments might have fewer or more zones than lift pins.

[0052] Figure 11A is a schematic diagram showing a system for creating two polar regions, in accordance with an example embodiment. As depicted in this figure, a semiconductor wafer 106 is gripped by an insulating or dielectric layer 401 of an electrostatic chuck 104. Inside the insulating or dielectric layer 401 are two embedded conductive layers, 1101a and 1101b, which are sometimes referred to as "electrode patterns". See, e.g., co-owned U.S. Patent No. 7,525,787. These embedded layers might be made from a metal such as tungsten, although other suitable materials (including other metals such as copper) might be used in alternative example embodiments. In an example embodiment, the thickness A of the insulating or dielectric layer 401 might be in the range of approximately .02-.06 inch, and the thickness B of the embedded conductive layer 1101a or 1101b might be in the range of approximately of .0001-.0005 inch.

[0053] Also, as depicted in Figure 11A, each embedded layer is connected to corresponding circuitry for creating a polar region (e.g., positive or negative) that contributes to the electrostatic force between the semiconductor wafer and the electrostatic chuck. Thus, embedded conductive layer 1101a is connected to P1 (Pole 1) circuitry 212a and embedded conductive layer 1101b is connected to P2 (Pole 2) circuitry 212b. It will be appreciated that the diagram in Figure 11A has been truncated for purposes of illustration and emphasis, as indicated by the S-shaped line bisecting the electrostatic chuck 104 and the semiconductor wafer 106 on the left. If not truncated, the dielectric layer 401 would include additional embedded conductive layers.

[0054] Figure 11B is a schematic diagram showing a system for creating two polar regions using circuitry in a dielectric layer, in accordance with an example embodiment. As depicted in this figure, a semiconductor wafer 106 is gripped by an insulating or dielectric layer 401 of an electrostatic chuck 104. Inside the insulating or dielectric layer 401 are two embedded conductive layers, 1101a and 1101b. Also inside the insulating or dielectric layer 401 are two electrical connections 1102a and 1102b. Electrical connection 1102a connects (e.g., through a hole in dielectric layer 401) embedded conductive layer 1101a to P1 (Pole 1) circuitry 212a to create a polar region (e.g., positive or negative). Similarly, electrical connection 1102b connects (e.g., through a hole in dielectric layer 401) embedded conductive layer 1101b to P2 (Pole 2) circuitry 212b to create a polar region (e.g., positive or negative). Again it will be appreciated that the diagram in Figure 11B has been truncated for purposes of illustration and emphasis, as indicated by the S-shaped line bisecting the electrostatic chuck 104 and the semiconductor wafer 106 on the left. If not truncated, the dielectric layer 401 would include additional embedded conductive layers.

[0055] It will be appreciated that a dielectric layer with embedded conductive layers and electrical connections as in Figure 11B can be manufactured using existing microfabrication or micromanufacturing techniques.

[0056] Figure 12 is a schematic diagram showing a cross-sectional view of a system with multiple zones of patterned polar regions around a bore for a lift pin, in accordance with an example embodiment. As depicted in this figure, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, each of which is around a bore for a lift pin. Thus, the zone around the bore 704 includes a polar region 701 with an electrical polarity (e.g., positive or negative) P2 separated by a dielectric region 702 from another polar region 703 with an opposite electrical polarity P1.

[0057] The cross-sectional view 1201 includes the insulating or dielectric layer 401, along with its circuitry and two of the lift pins 203 that pass through the layer. Each of those lift pins has a corresponding pneumatic cylinder 204. As shown in the cross-sectional view 1201, the P1 circuitry 212a is connected to polar region 703 and the P2 circuitry 212b is connected to polar region 701. Here it will be recalled that each polar region includes an embedded conductive layer made of a material such as tungsten, which creates the region's polarity (positive or negative) when voltage (e.g., direct current or DC) is applied to the circuitry.

[0058] Figure 13 is a schematic diagram showing the electrical circuitry for a system with multiple zones of patterned polar regions around a bore for a lift pin, in accordance with an

example embodiment. As depicted in this figure, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, each of which is around a bore for a lift pin. The zone around the bore 704 includes a polar region 701 with an electrical polarity (e.g., positive or negative) P1, which is separated by a dielectric region 702 from another polar region 703 with an opposite electrical polarity P2, which, in turn, is separated from another polar region 1002 with a polarity P1 by a dielectric region 1001. Insulating or dielectric layer 401 also includes a bore for sensor pin 501.As shown in this figure, the P1 circuitry 212a is connected to polar regions 701 and 1001 and the P2 circuitry 212b is connected to polar region 703. Once again, it will be recalled that each polar region includes an embedded conductive layer made of a material such as tungsten, which creates the region's polarity (positive or negative) when voltage (e.g., direct current or DC) is applied to the circuitry.

[0059] Figure 14 is a schematic diagram showing alternative electrical circuitry for a system with multiple zones of patterned polar regions around a bore for a lift pin, in accordance with an example embodiment. As depicted in this figure, an insulating or dielectric layer 401 of an electrostatic chuck has three zones, each of which is around a bore for a lift pin. The zone around the bore 704 includes a polar region 701 with an electrical polarity (e.g., positive or negative) P1, which is separated by a dielectric region 702 from another polar region 703 with an opposite electrical polarity P2, which, in turn, is separated from another polar region 1002 with a polarity P1 by a dielectric region 1001.

[0060] As shown in this figure, the P1 circuitry in 212 (PIN-1) is connected to polar regions 701 and 1001 and the P2 circuitry in 212 is connected to polar region 703. Here it will be appreciated that each zone has its own P1-P2 circuitry, e.g., PIN-1, PIN-2, and PIN-3, respectively. This circuitry arrangement contrasts with the circuitry arrangement shown in Figure 13, where the P1 circuitry connected to all three zones, as did the P2 circuitry. Of course, in the latter circuitry arrangement, different voltages cannot be applied to the P1 regions in different zones. In the circuitry arrangement shown in Figure 14, different voltages can be applied to P1 in the first zone, P1 in the second zone, and P1 in the third zone, for example.

[0061] Figure 15 is a flowchart diagram showing a process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor pin, in accordance with an example embodiment. The process is described from the point of view of a process controller, which in an example embodiment, might include an application program executing on an x86-processor platform with a Linux or Windows operating system.

[0062] In operation 1501 of the process, the process controller places a semiconductor wafer on a process chamber's electrostatic chuck with multiple zones, each of which includes a pattern of polar regions around a lift pin, as described above. In operation 1502, the process controller clamps the semiconductor wafer to the electrostatic chuck by applying voltage (e.g., direct current or DC) to one or more of the polar regions in the zones. Then in operation 1503, the process controller processes the semiconductor wafer through generating a plasma and using the plasma to etch the substrate, deposit a material on the substrate, or perform some other semiconductor manufacturing operation.

[0063] The process controller terminates the processing in operation 1504. In operation 1505, the process controller begins lifting the semiconductor wafer off of the electrostatic chuck with the lift pins. The process controller then measures, with a sensor pin as described above, the electrostatic force between the semiconductor wafer and the electrostatic chuck, in operation 1506. In operation 1507, the process controller adjusts the upward force (e.g., pneumatic pressure) of the lift pins, based on the sensor pin's measurement.

[0064] Figure 16 is a flowchart diagram showing another process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor pin, in accordance with an example embodiment. In operation 1601 of the process, the process controller places a semiconductor wafer on a process chamber's electrostatic chuck with multiple zones, each of which includes a pattern of polar regions around a lifting pin. In operation 1602, the process controller clamps the semiconductor wafer to the electrostatic chuck by applying voltage (e.g., direct current or DC) to one or more of the polar regions in the zones. Then in operation 1603, the process controller processes the semiconductor wafer through generating a plasma and using the plasma to etch the substrate, deposit a material on the substrate, or perform some other semiconductor manufacturing operation.

[0065] The process controller terminates the processing and applies a voltage (e.g., direct current or DC) to the polar regions to initiate dechucking, in operation 1604. It will be appreciated that this application of voltage did not occur in the process shown in Figure 15. Such dechucking voltages are described in U.S. Patent No. 5,612,850. Then in operation 1605 of the process shown in Figure 16, the process controller begins lifting the semiconductor wafer off of the electrostatic chuck with the lift pins. The process controller measures, with a sensor pin as described above, the electrostatic force between the semiconductor wafer and the electrostatic chuck, in operation 1606. In operation 1607, the process controller adjusts the upward force

(e.g., pneumatic pressure) of lift pins and/or the dechucking voltage, based on the sensor pin's measurement.

[0066] Figure 17 is a flowchart diagram showing a process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor associated one-to-one with a lift pin, in accordance with an example embodiment. The process is described from the point of view of a process controller, which in an example embodiment, might include an application program executing on an x86-processor platform with a Linux or Windows operating system.

[0067] In operation 1701 of the process, the process controller places a semiconductor wafer on a process chamber's electrostatic chuck with multiple zones, each of which includes a pattern of polar regions around a lift pin, as described above. In operation 1702, the process controller clamps the semiconductor wafer to the electrostatic chuck by applying voltage (e.g., direct current or DC) to one or more of the polar regions in the zones. Then in operation 1703, the process controller processes the semiconductor wafer through generating a plasma and using the plasma to etch the substrate, deposit a material on the substrate, or perform some other semiconductor manufacturing operation.

[0068] The process controller terminates the processing in operation 1704. In operation 1705, the process controller begins lifting the semiconductor wafer off of the electrostatic chuck with the lift pins. The process controller then measures, with a sensor associated one-to-one with a lift pin as described above, the electrostatic force between the semiconductor wafer and the electrostatic chuck, in operation 1706. In operation 1707, the process controller adjusts the upward force (e.g., pneumatic pressure) of the lift pin, based on the sensor's measurement.

[0069] Figure 18 is a flowchart diagram showing another process for processing a semiconductor wafer in a process chamber with an electrostatic chuck with a sensor associated one-to-one with a lift pin, in accordance with an example embodiment. In operation 1801 of the process, the process controller places a semiconductor wafer on a process chamber's electrostatic chuck with multiple zones, each of which includes a pattern of polar regions around a lifting pin. In operation 1802, the process controller clamps the semiconductor wafer to the electrostatic chuck by applying voltage (e.g., direct current or DC) to one or more of the polar regions in the zones. Then in operation 1803, the process controller processes the semiconductor wafer through generating a plasma and using the plasma to etch the substrate, deposit a material on the substrate, or perform some other semiconductor manufacturing operation.

[0070] The process controller terminates the processing and applies a voltage (e.g., direct current or DC) to one or more the polar regions to initiate dechucking, in operation 1804. It will be appreciated that this application of voltage did not occur in the process shown in Figure 17. Then in operation 1805 of the process shown in Figure 18, the process controller begins lifting the semiconductor wafer off of the electrostatic chuck with the lift pins. The process controller measures, with a sensor associated one-to-one with a lift pin as described above, the electrostatic force between the semiconductor wafer and the electrostatic chuck, in operation 1806. In operation 1807, the process controller adjusts the dechucking voltage in a polar region, based on the sensor's measurement. Then in operation 1808, the process controller adjusts the upward force (e.g., pneumatic pressure) of the lift pin, based on the sensor's measurement.

[0071] It will be appreciated that the process described in Figure 18 uses both applied voltage (e.g., direct current or DC) and a sensor associated one-to-one with a lift pin to separate a semiconductor wafer from an electrostatic chuck. The application of the voltage can be varied from zone to zone, as can the upward force of the lift pin, to make "pinpoint" adjustments as to locations where electrostatic force might lead to damage to the semiconductor wafer by a lift pin.

[0072] In still another embodiment, the voltage applied (magnitude and time) to the one ore more polar regions can be based on predefined formula. The formula can defined based on the processing expected to occur one the wafer. For instance, if a particular type of etch recipe is expected, predefined expected dechucking voltages and durations can be applied. In one embodiment, by arranging the conductive patterns on the chuck (i.e., defining polar regions) it is possible to better target dechucking at the point of lifting.

[0073] With the above embodiments in mind, it should be understood that the invention may employ various computer-implemented operations involving data stored in computer systems. These operations are those requiring physical manipulation of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. Further, the manipulations performed are often referred to in terms, such as producing, identifying, determining, or comparing.

[0074] Any of the operations described herein that form part of the invention are useful machine operations. The invention also relates to a device or an apparatus for performing these operations. The apparatus may be specially constructed for the required purposes, such as the

carrier network discussed above, or it may be a general purpose computer selectively activated or configured by a computer program stored in the computer. In particular, various general purpose machines may be used with computer programs written in accordance with the teachings herein, or it may be more convenient to construct a more specialized apparatus to perform the required operations.

[0075] The invention can also be embodied as computer readable code on a computer readable medium. The computer readable medium is any data storage device that can store data, which can thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, DVDs, Flash, magnetic tapes, and other optical and non-optical data storage devices. The computer readable medium can also be distributed over a network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[0076] Although the foregoing example embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. For example, the electrostatic chuck might be tripolar (e.g., a polar region might be associated with a magnitude in addition to being positive or negative) rather than bipolar or unipolar, in an alternative example embodiment. Accordingly, the example embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

Claims

1. An apparatus for electrostatic chucking and dechucking, comprising:

an electrostatic chuck with a plurality of zones, wherein each zone includes one or more polar regions around a lift pin for contacting a bottom surface of a substrate;

one or more controllers that control the lift pins; and

one or more controllers that control the polar regions.

2. An apparatus as in claim 1, wherein the lift pin further comprises a pneumatic cylinder.

3. An apparatus as in claim 2, wherein each lift pin is associated with a separate sensor.

4. An apparatus as in claim 3, wherein the sensor provides feedback to the controller for the lift pin.

5. An apparatus as in claim 4, wherein one controller is connected to all lift pins.

6. An apparatus as in claim 4, wherein a separate controller is connected to each lift pin.

7. An apparatus as in claim 6, wherein the sensor provides feedback to the controller for the lift pin.

8. An apparatus as in claim 3, wherein one controller is connected to all the polar regions.

9. An apparatus as in claim 8, wherein the sensor provides feedback to the controller for the polar regions.

10. An apparatus as in claim 3, wherein a separate controller is connected to each polar region.

11. An apparatus as in claim 10, wherein the sensor provides feedback to each controller for each polar region.

12. An apparatus as in claim 1, further comprising a sensor pin.

13. An apparatus as in claim 12, wherein the sensor pin provides feedback to the controller for the lift pin.

14. An apparatus as in claim 13, wherein one controller is connected to all polar regions.

15. An apparatus as in claim 14, wherein the sensor pin provides feedback to the controller for the polar regions.

16. An apparatus as in claim 13, wherein a separate controller is connected to each polar region.

17. An apparatus as in claim 16, wherein the sensor pin provides feedback to each controller for each polar region.

18. An automated method for processing a substrate for manufacturing integrated circuits, comprising operations of:

placing the substrate on an electrostatic chuck in a process chamber, wherein the electrostatic chuck includes a plurality of zones and wherein each zone includes one or more polar regions around a lift pin moved by pneumatic pressure;

clamping the substrate to the electrostatic chuck by applying a voltage to the one or more polar regions;

processing the substrate;

terminating the processing operation;

applying another voltage to the one or more polar regions of the one or more zones to initiate dechucking;

causing one or more lift pins to come into contact with a bottom surface of the substrate; and

measuring, with a sensor, an electrostatic force between the substrate and the electrostatic chuck.

19. The method of claim 18, further comprising the operation of adjusting the pneumatic pressure of one or more lift pins.

20. The method of claim 18, further comprising the operation of adjusting the voltage of one or more polar regions in one or more zones.

21. The method of claim 18, wherein the operation of processing the substrate includes generating a plasma and using the plasma to etch the substrate, deposit a material on the substrate, or perform another semiconductor manufacturing operation.

22. A chamber for processing a semiconductor wafer, the chamber comprising:

an electrostatic chuck defined to support a substrate, the electrostatic chuck having a plurality of bores for receiving lift pins for engaging the substrate when present, the electrostatic chuck including a plurality of polar regions that are defined to at least partially surround each of the plurality of bores.

23. The chamber of claim 22, wherein each of the plurality of polar regions has a geometric pattern and a voltage supply coupled to the geometric pattern.

24. The chamber of claim 22, wherein each of the plurality of polar regions is coupled to a same voltage.

25. The chamber of claim 22, wherein each of the plurality of polar regions is coupled to a different voltage.

26. The chamber of claim 22, wherein each of the plurality of polar regions defines a zone, and each zone is coupled to a voltage supply.

27. The chamber of claim 22, wherein the electrostatic chuck includes,

a metallic base;

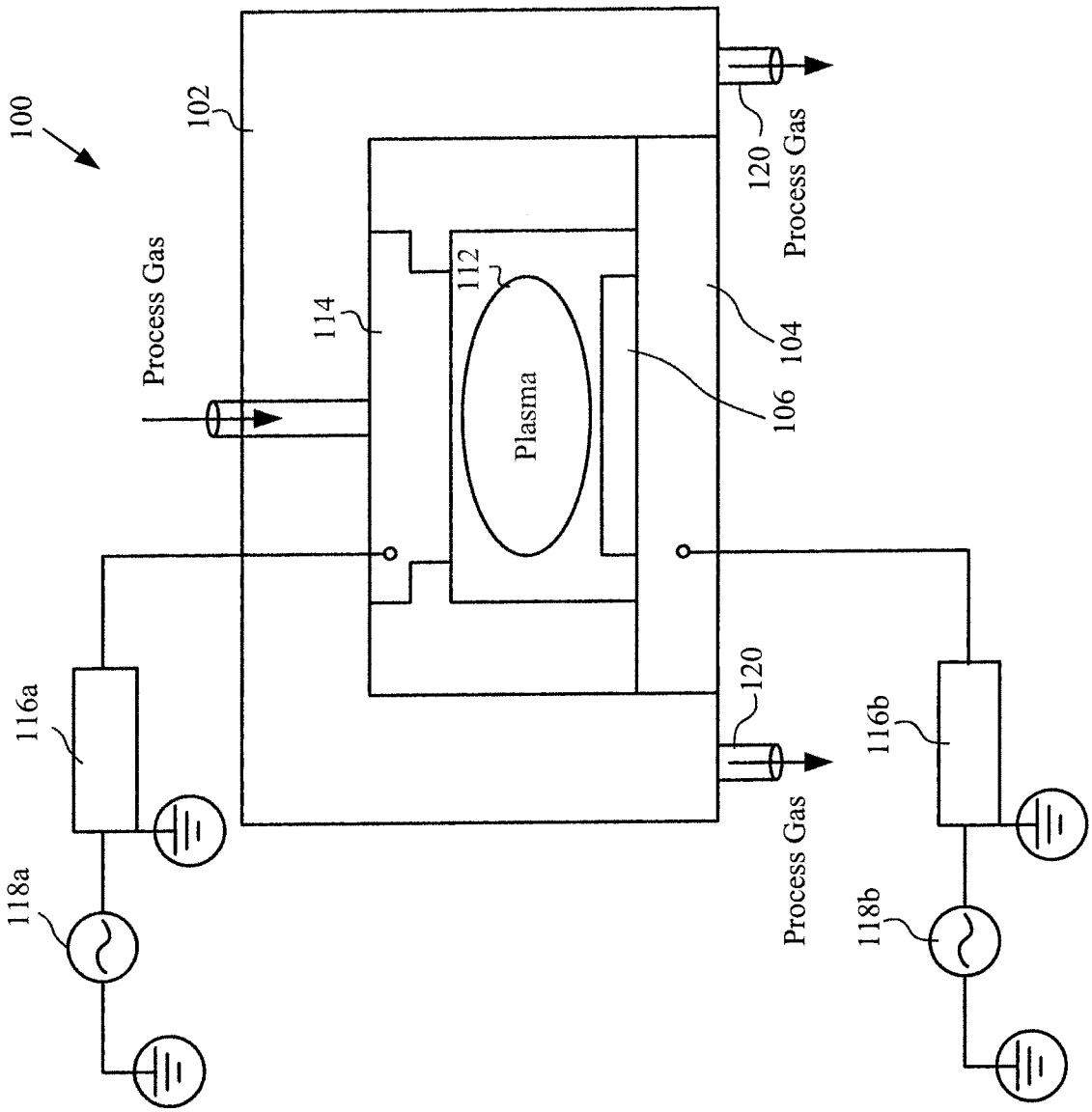
a dielectric layer disposed over the metallic base, the dielectric layer defining a surface for the support of the substrate;

the geometric patterns defined from a conductive metal disposed in the dielectric layer; and

circuitry for applying voltage to the conductive material, wherein the circuitry is disposed in the dielectric layer.

28. The chamber of claim 27, wherein the bores are defined through the metallic base and the dielectric layer.

Figure 1


100
102
Process Gas
114
112
Plasma
104
106
120
Process Gas
120
Process Gas
116a
116b
118a
118b

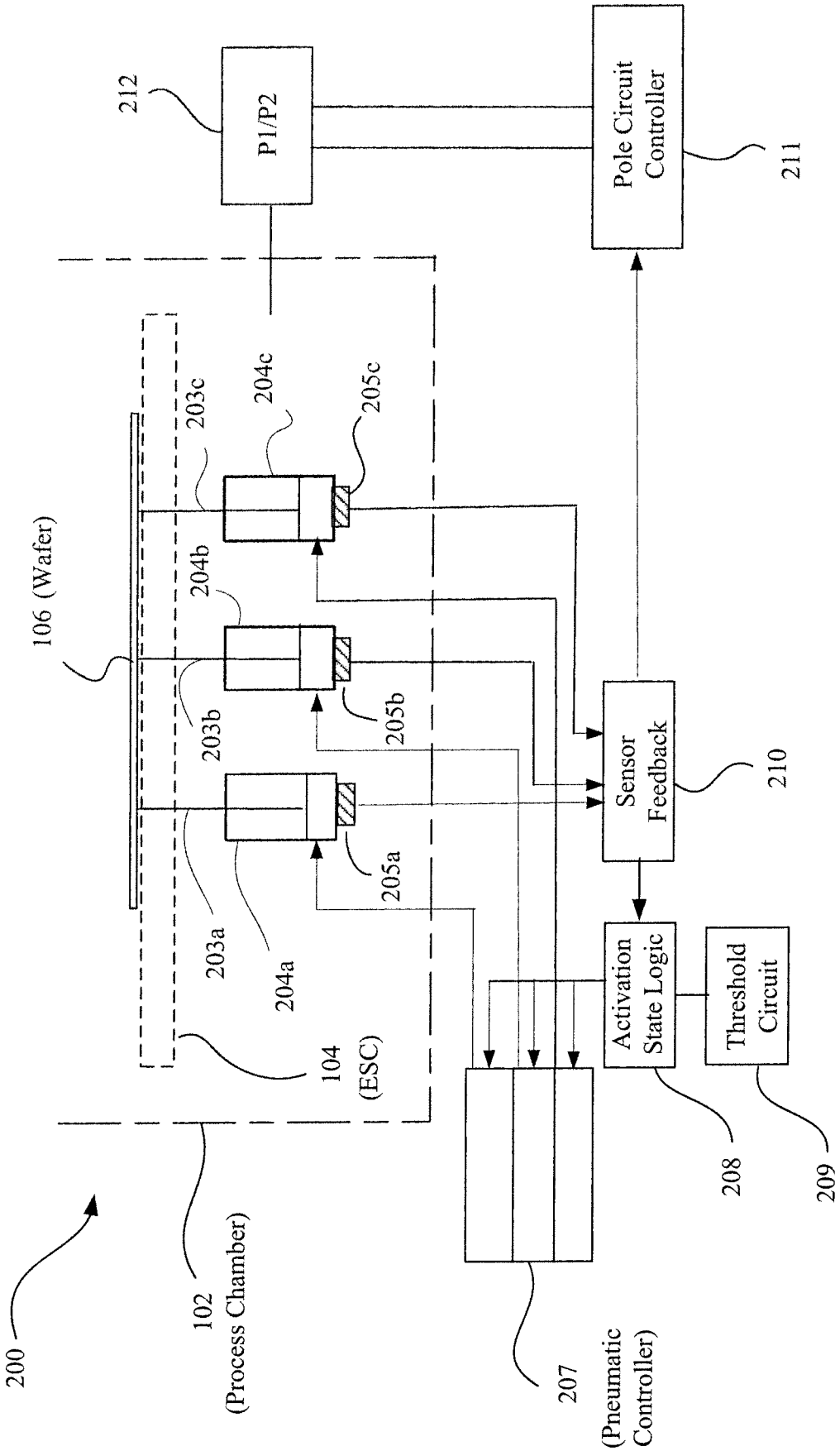

212
P1/P2
Pole Circuit Controller
211
106 (Wafer)
203c
204c
205c
204b
203b
205b
203a
204a
205a
104
(ESC)
Sensor Feedback
210
Activation State Logic
Threshold Circuit
208
209
200
102
(Process Chamber)
207
(Pneumatic Controller)

Figure 2

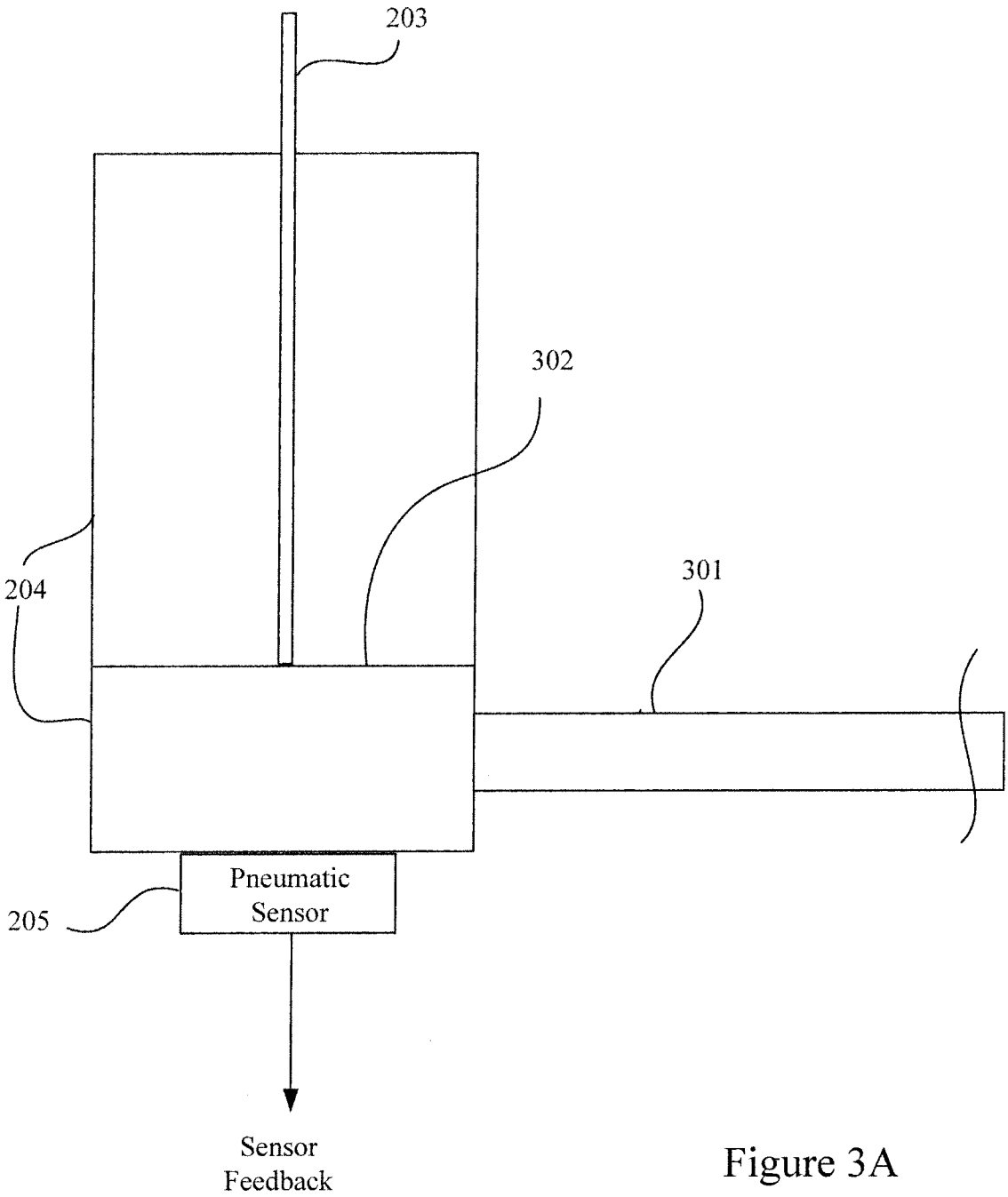


Figure 3A

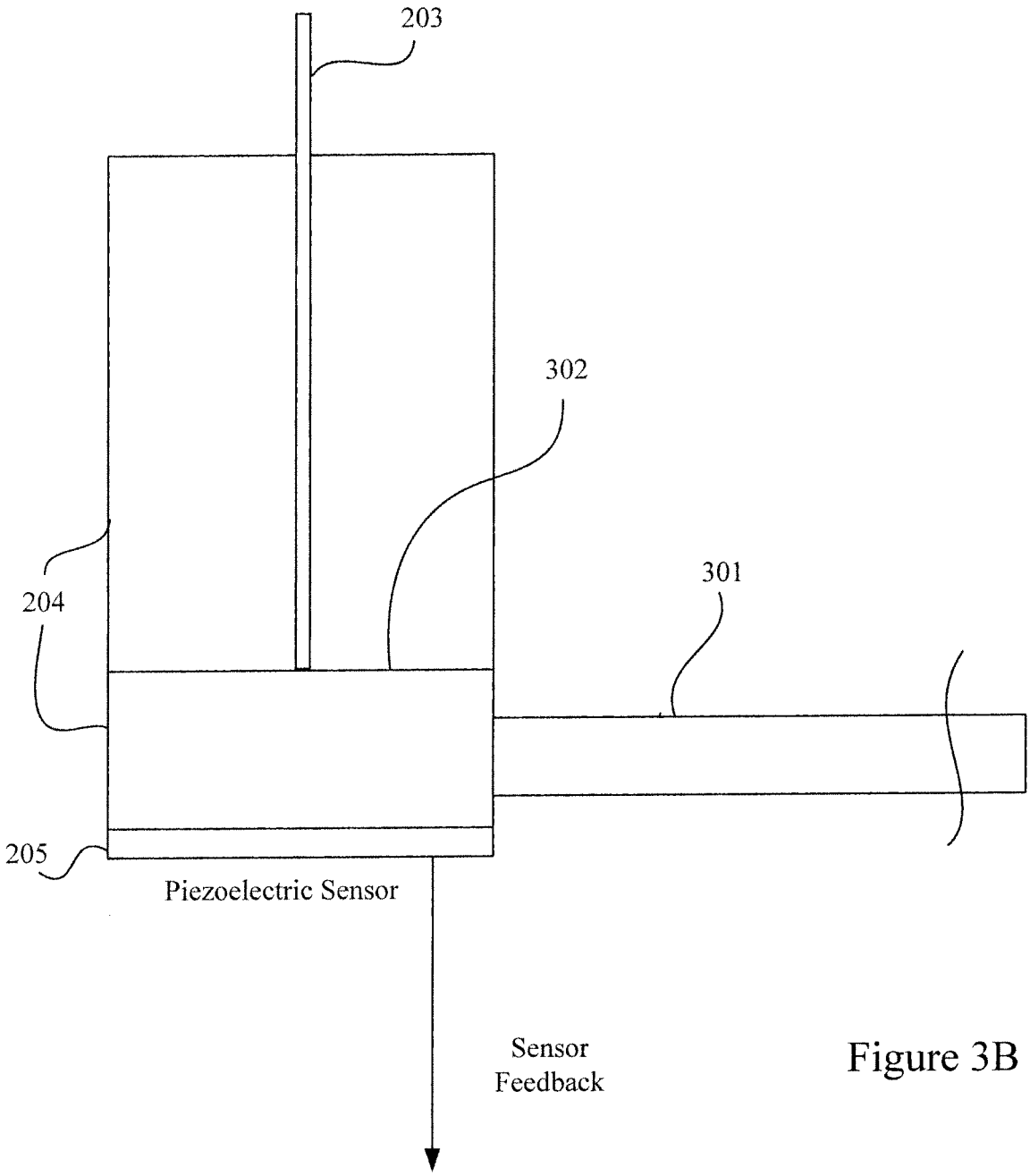


Figure 3B

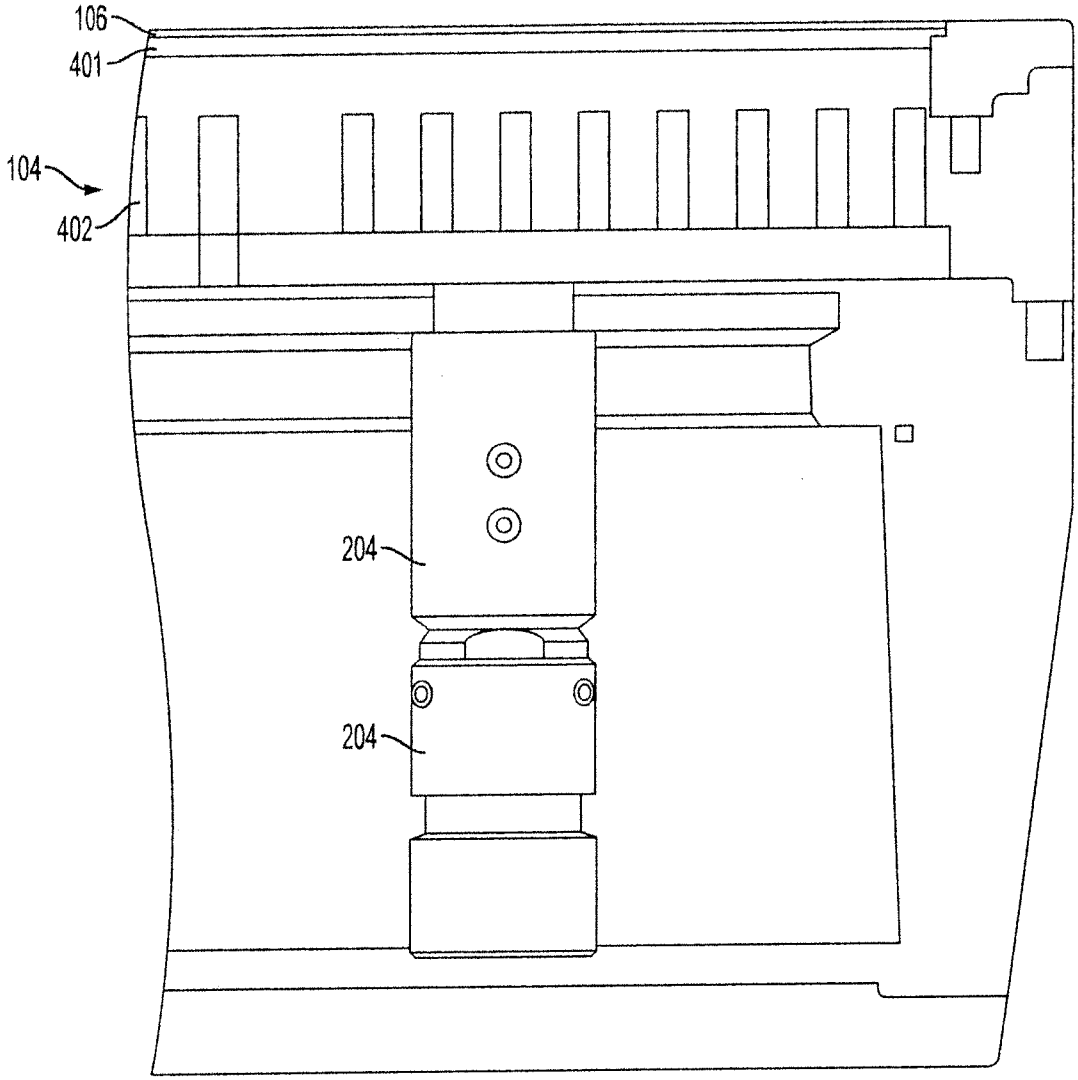


FIG. 4A

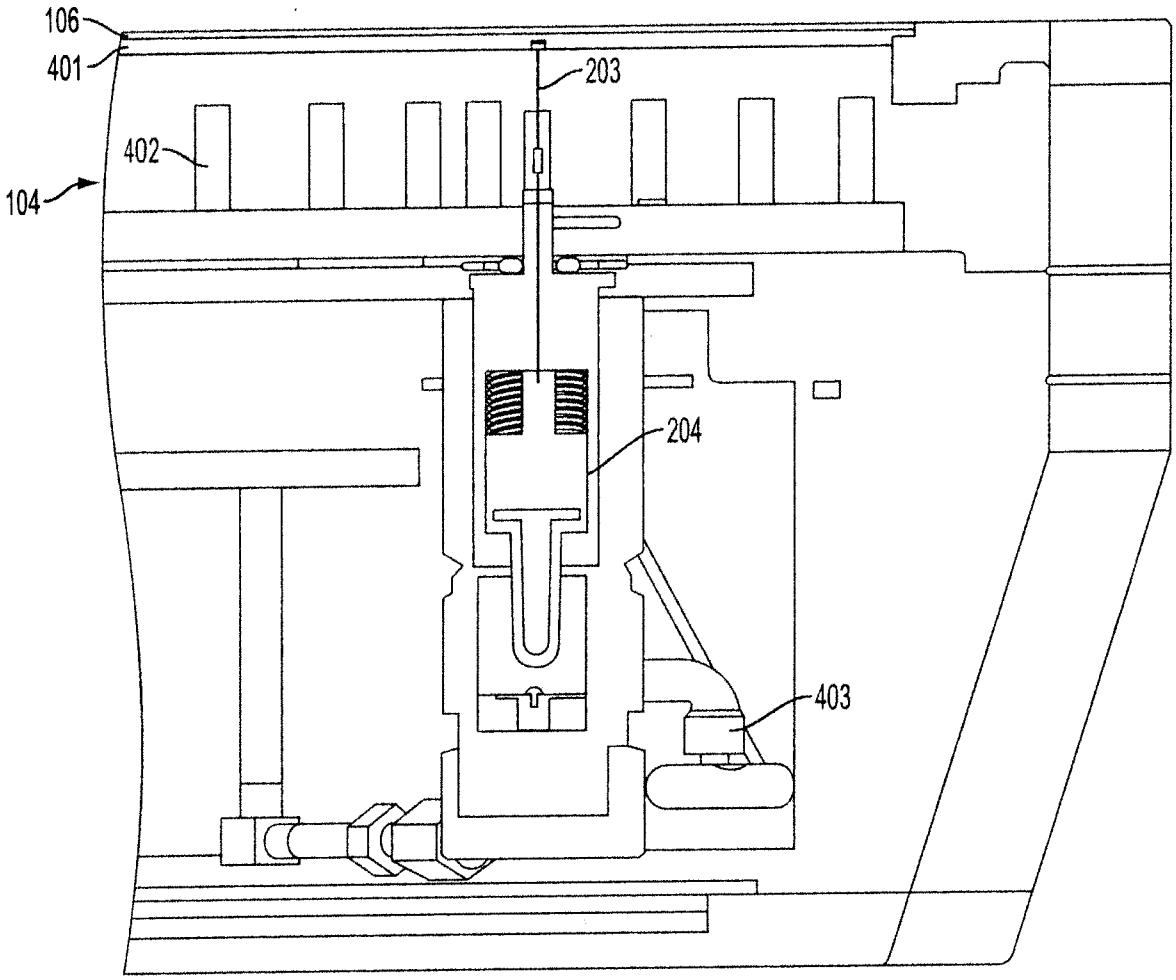


FIG. 4B

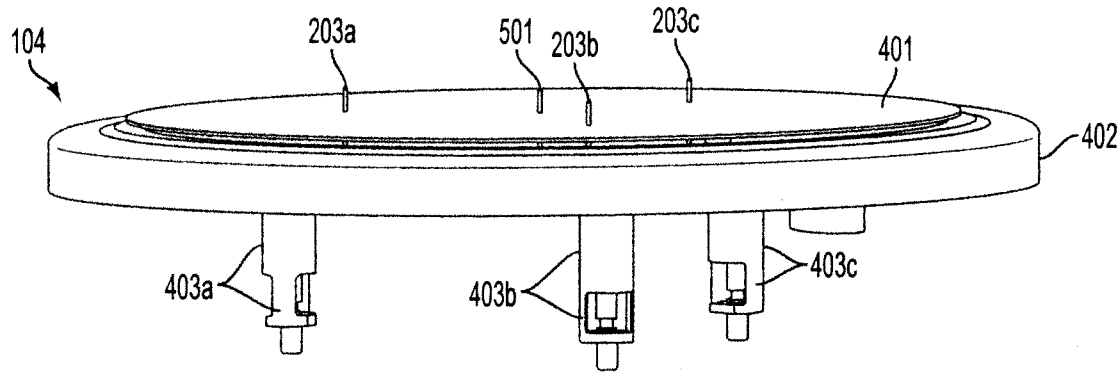


FIG. 5

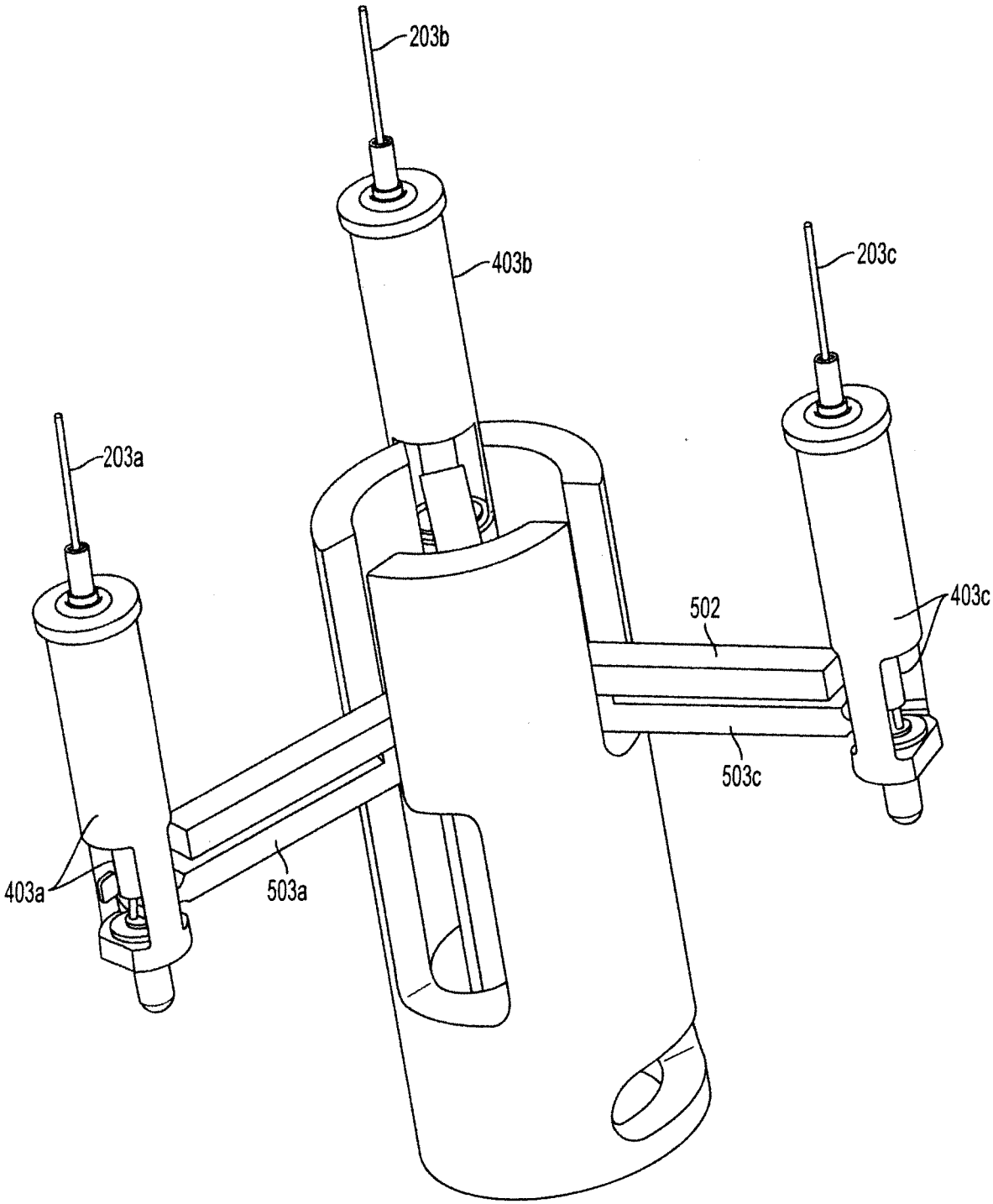


FIG. 6

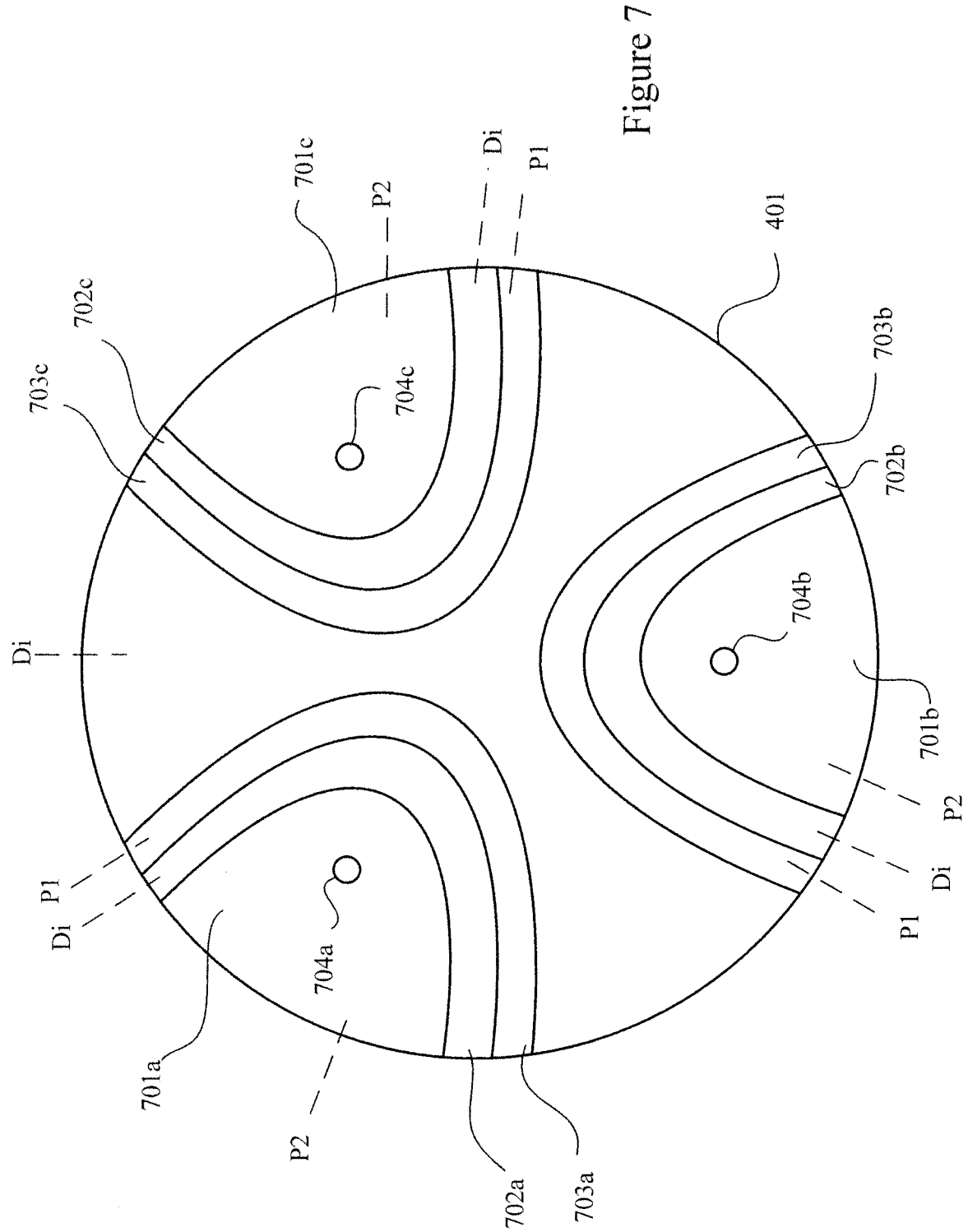

701c
P2
Di
P1
401
703c
702c
704c
703b
702b
Di
704b
701b
P1
Di
P2
Di
P1
704a
701a
P2
702a
703a

Figure 7

Figure 8

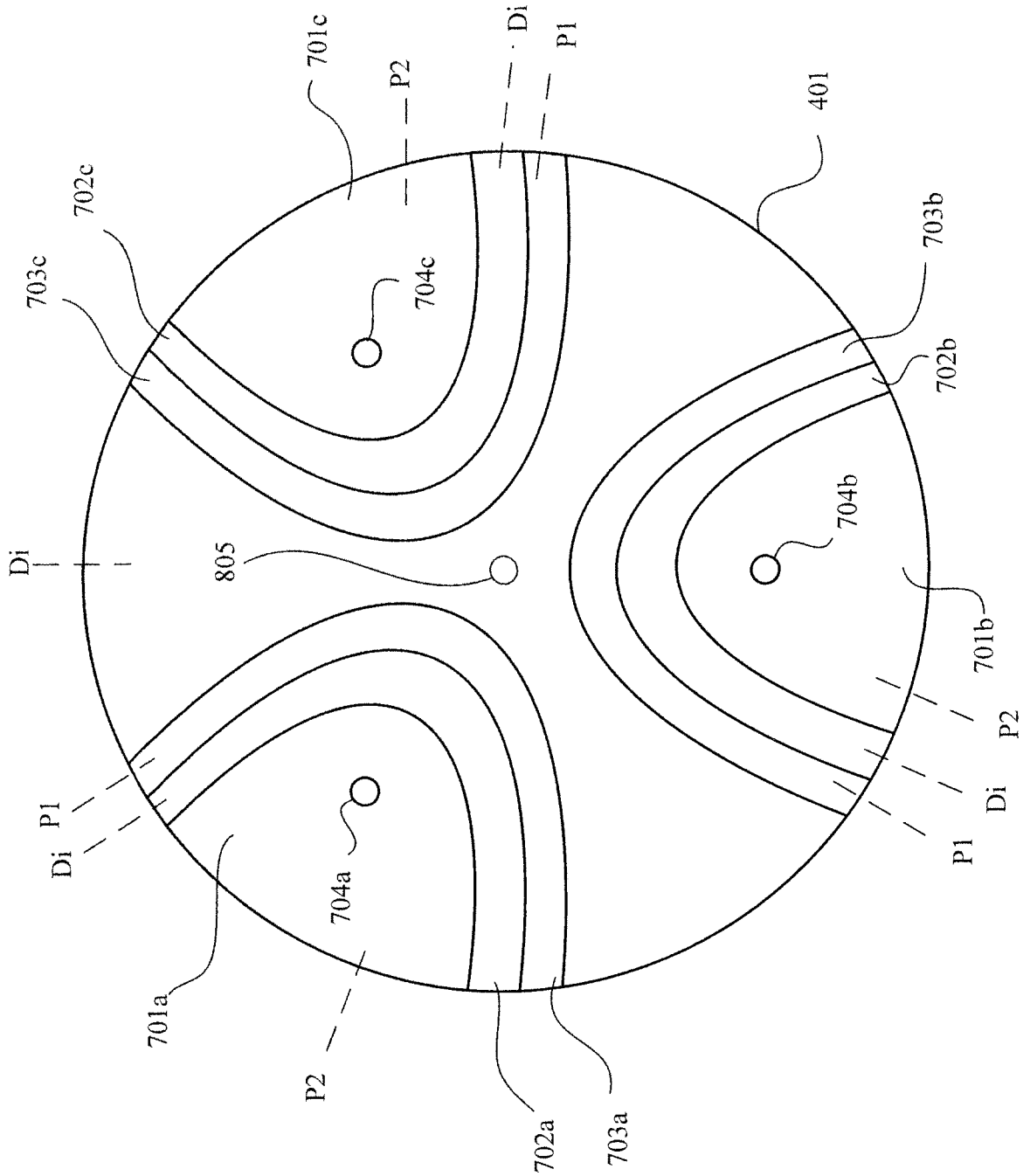
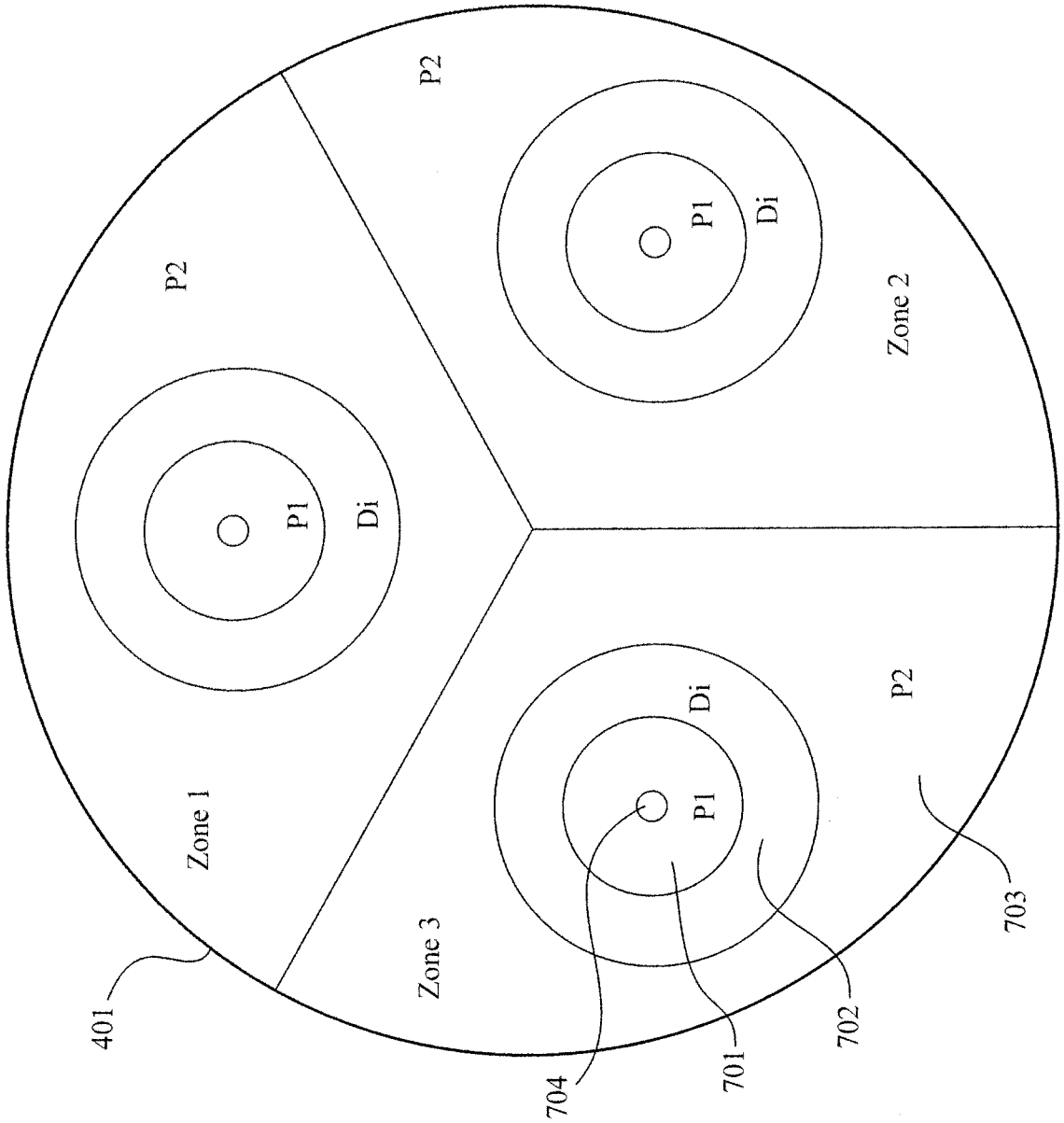

701c
P2
Di
P1
401
703c
702c
704c
703b
702b
Di
805
704b
701b
P1
Di
P2
Di
P1
704a
701a
P2
702a
703a

Figure 9



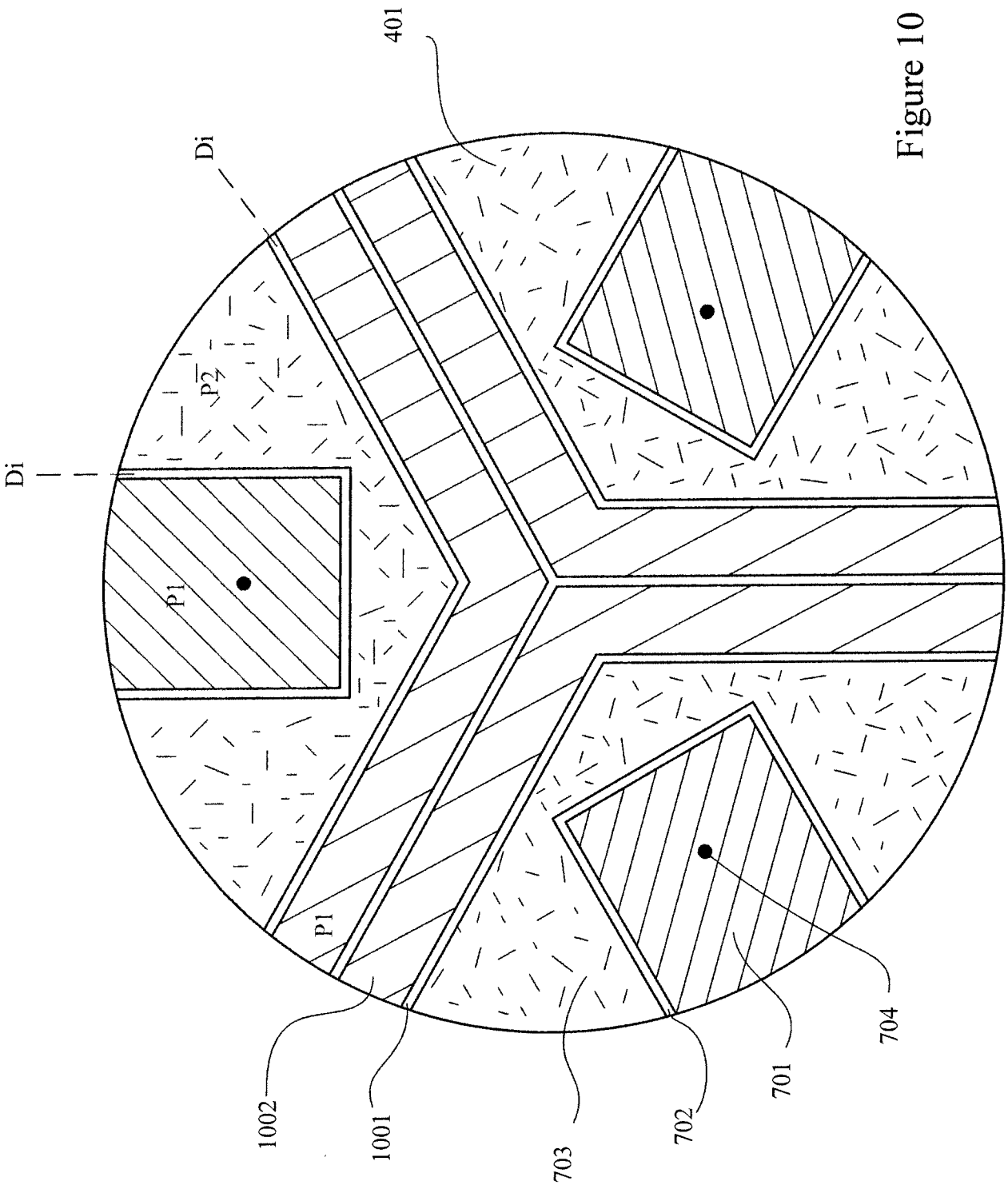


Figure 10

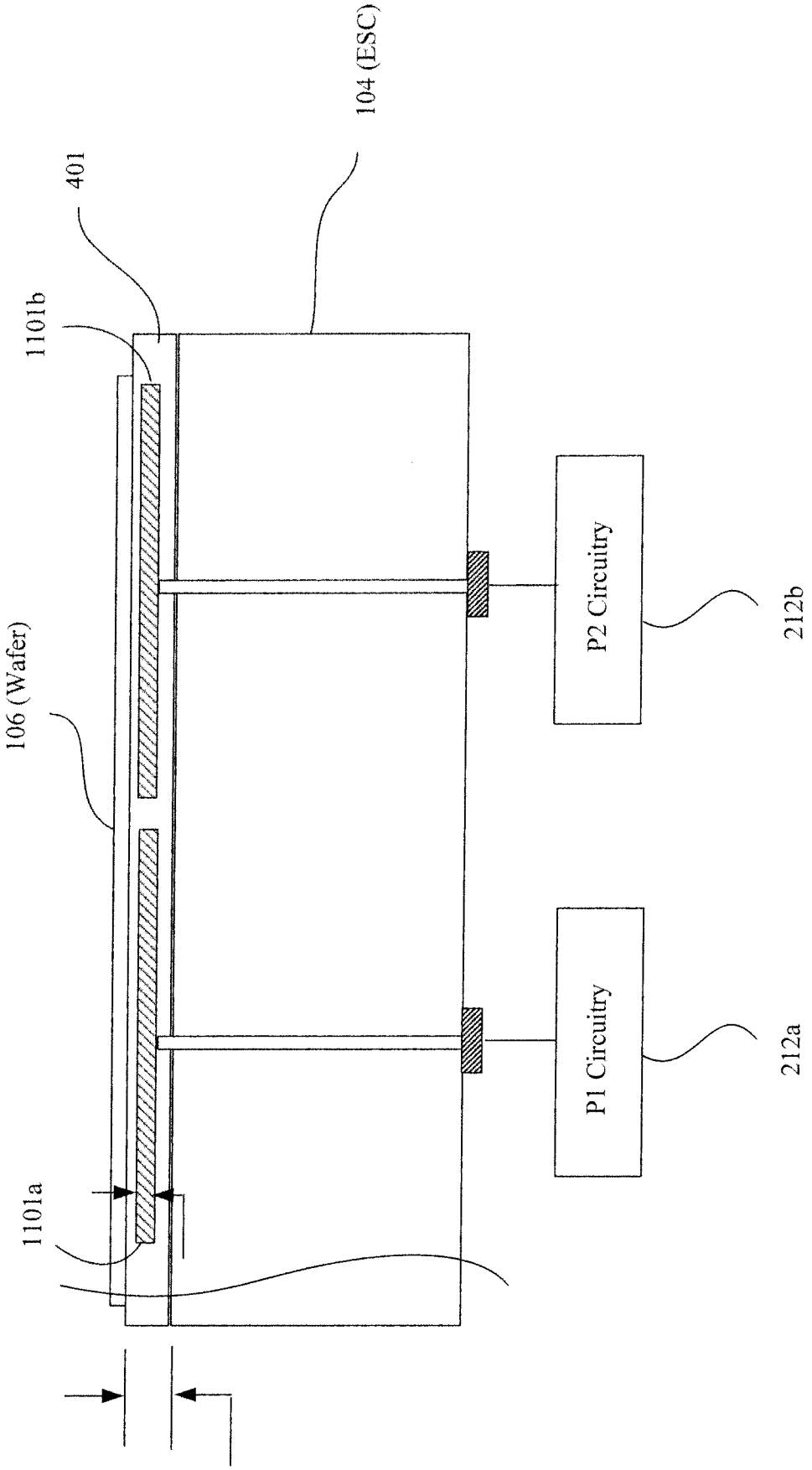

104 (ESC)
401
1101b
106 (Wafer)
P2 Circuitry
212b
P1 Circuitry
212a
1101a

Figure 11A

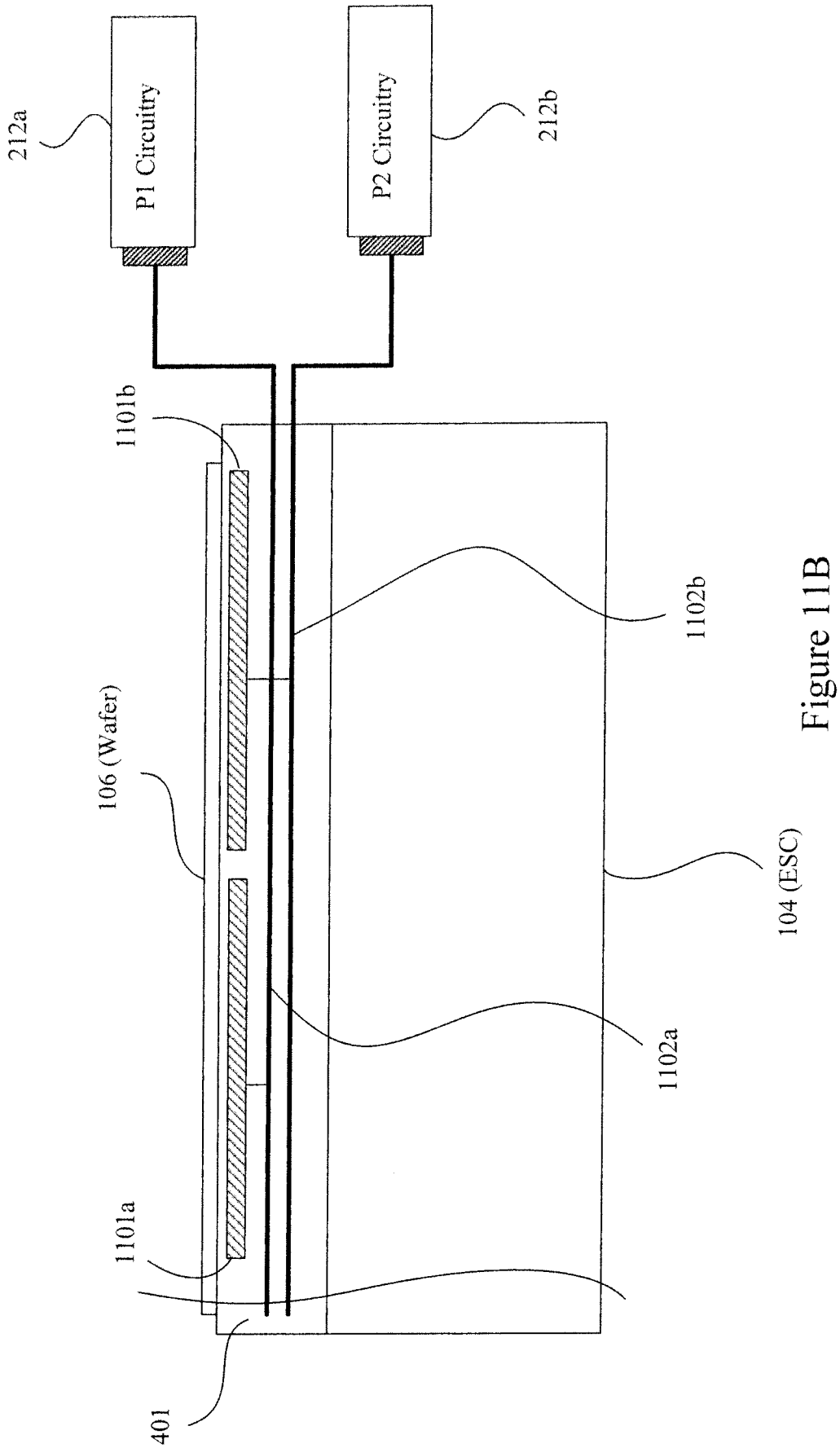

212a
P1 Circuitry
P2 Circuitry
212b
1101b
1102b
106 (Wafer)
104 (ESC)
1102a
1101a
401

Figure 11B

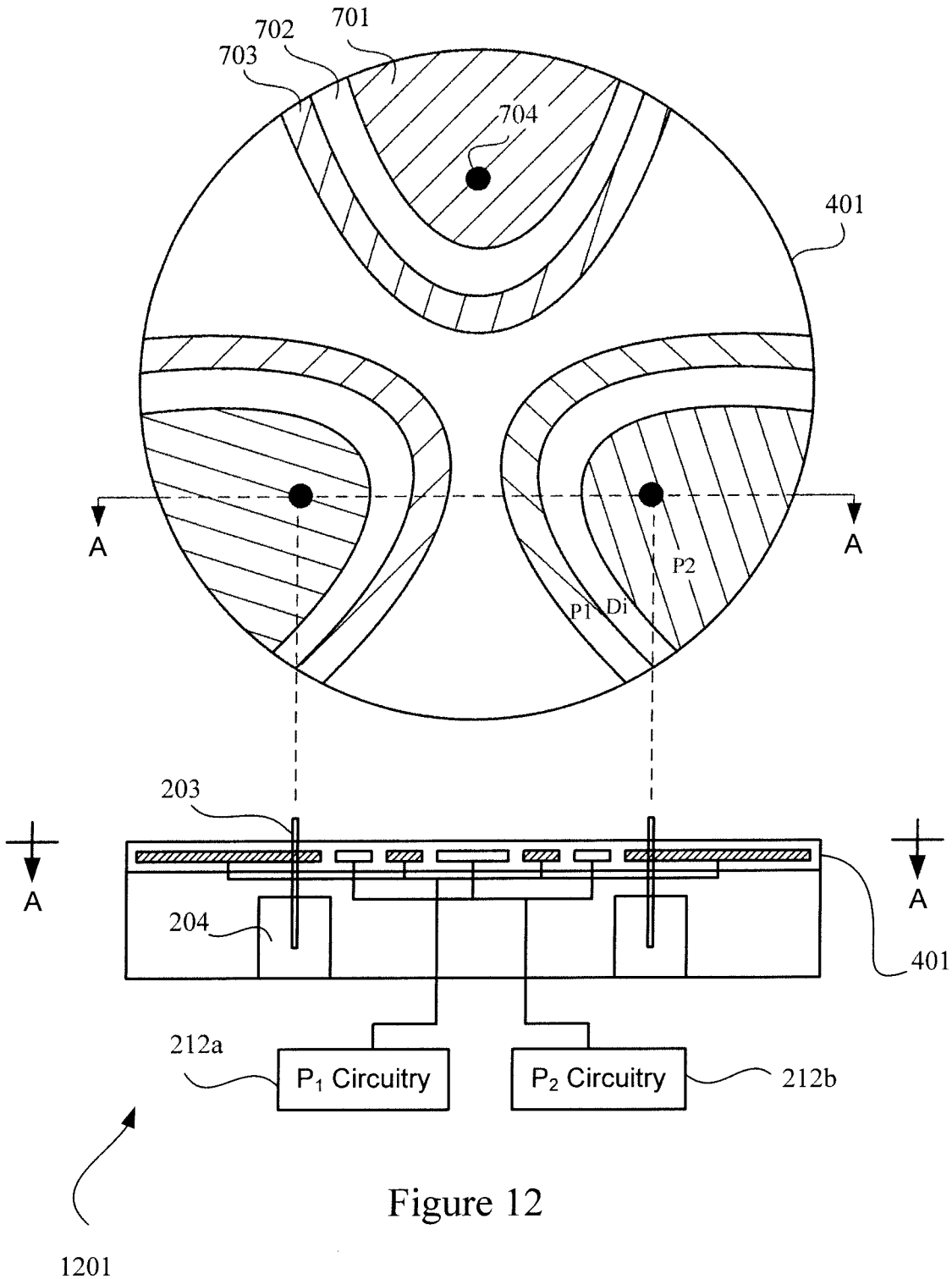

702
701
703
704
401
A
A
P2
P1
Di
203
A
A
204
401
212a
P1 Circuitry
P2 Circuitry
212b
1201

Figure 12

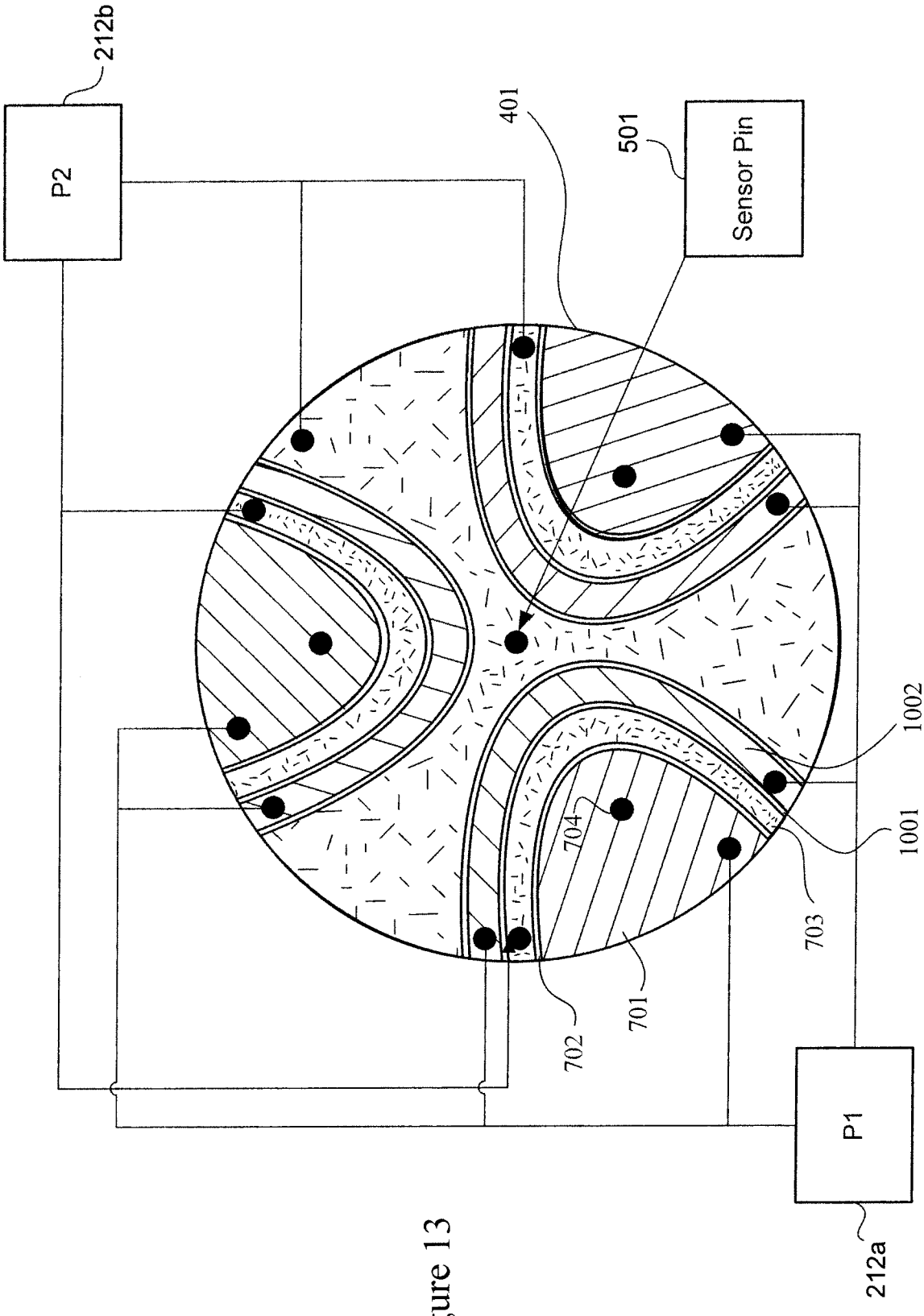
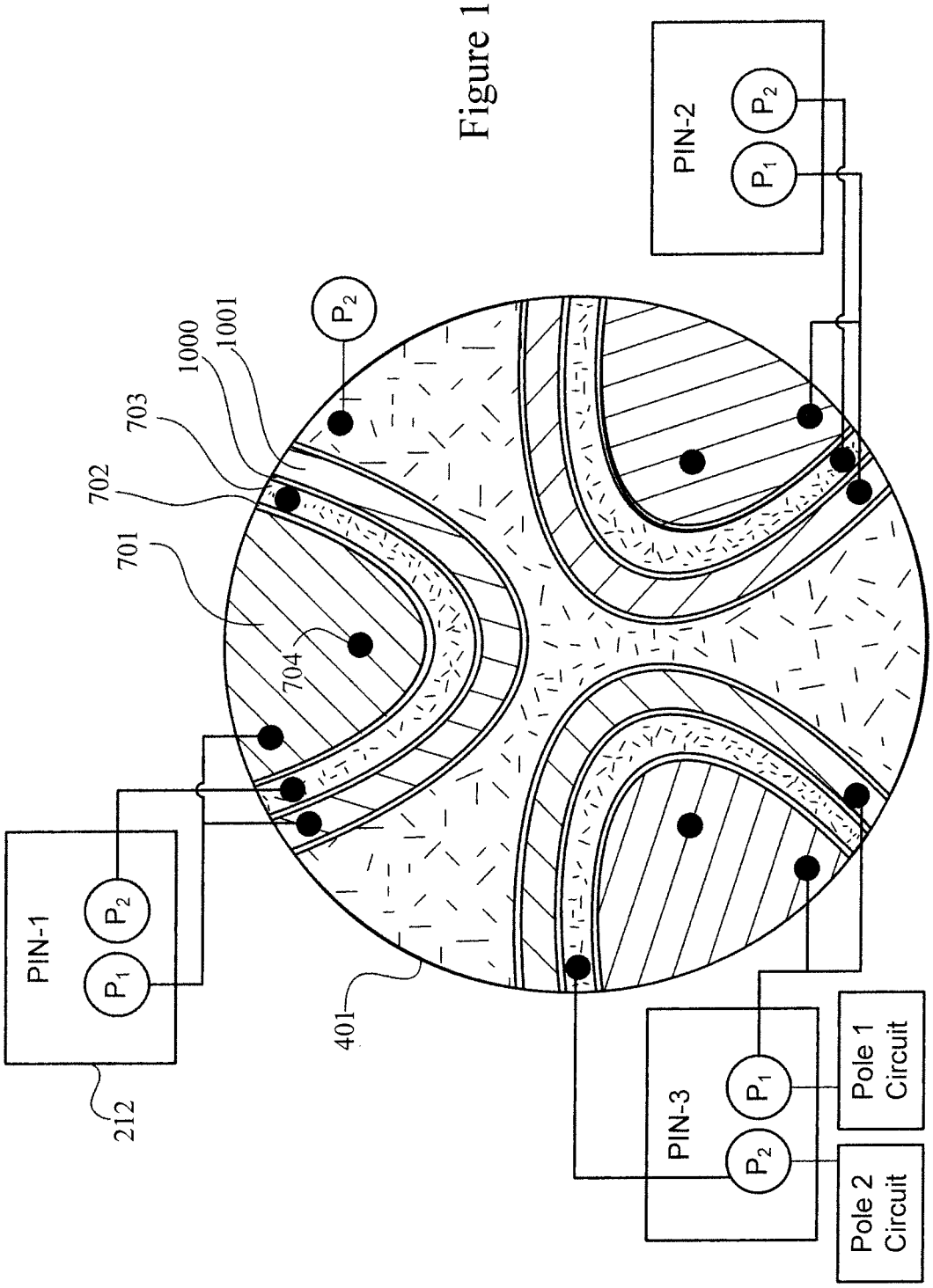


Figure 13

Figure 14


PIN-1
P1
P2
212
PIN-2
P1
P2
PIN-3
P1
P2
Pole 1 Circuit
Pole 2 Circuit
401
704
701
702
703
1000
1001
P2

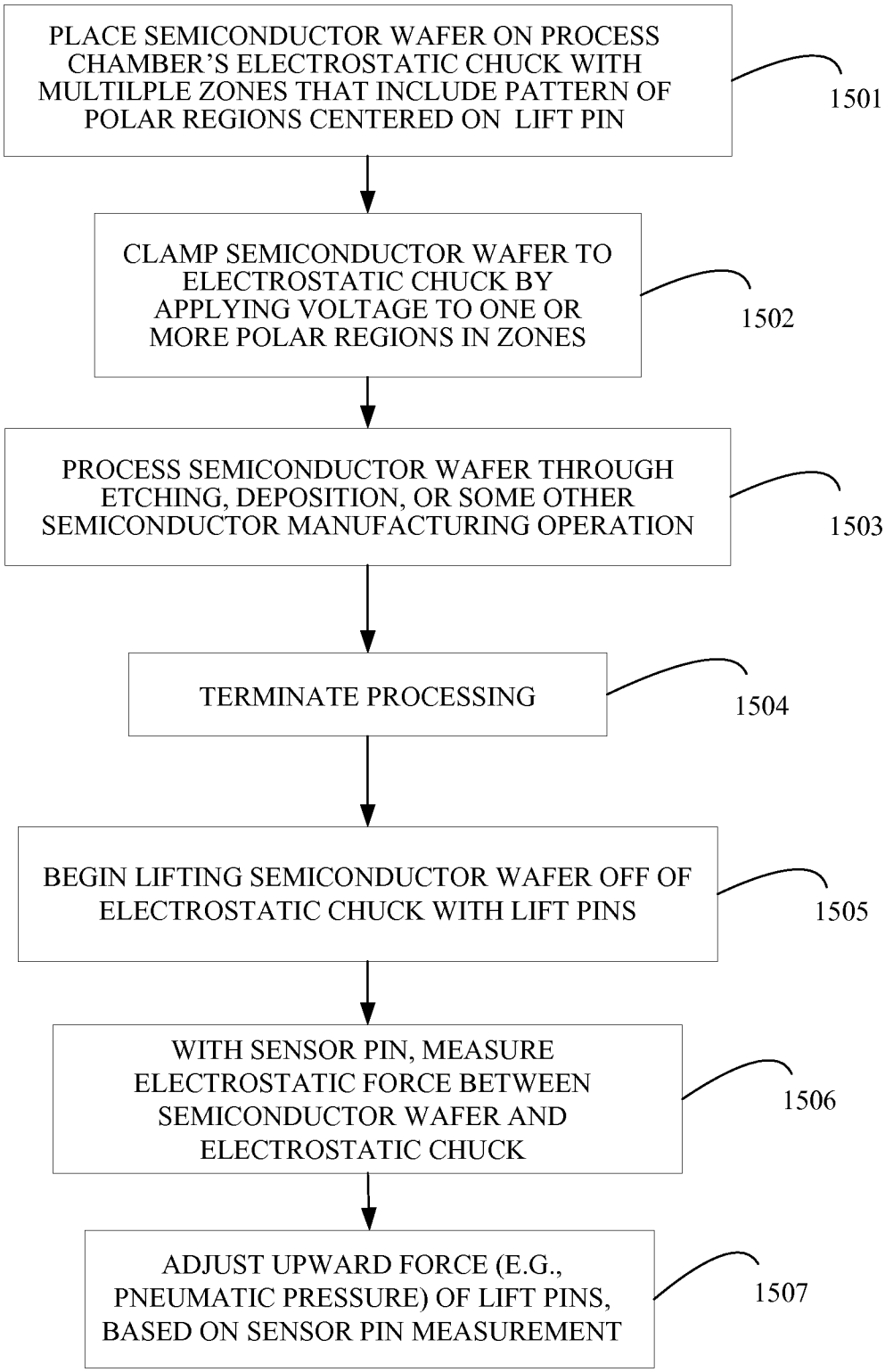

PLACE SEMICONDUCTOR WAFER ON PROCESS CHAMBER'S ELECTROSTATIC CHUCK WITH MULTILPLE ZONES THAT INCLUDE PATTERN OF POLAR REGIONS CENTERED ON LIFT PIN
1501
CLAMP SEMICONDUCTOR WAFER TO ELECTROSTATIC CHUCK BY APPLYING VOLTAGE TO ONE OR MORE POLAR REGIONS IN ZONES
1502
PROCESS SEMICONDUCTOR WAFER THROUGH ETCHING, DEPOSITION, OR SOME OTHER SEMICONDUCTOR MANUFACTURING OPERATION
1503
TERMINATE PROCESSING
1504
BEGIN LIFTING SEMICONDUCTOR WAFER OFF OF ELECTROSTATIC CHUCK WITH LIFT PINS
1505
WITH SENSOR PIN, MEASURE ELECTROSTATIC FORCE BETWEEN SEMICONDUCTOR WAFER AND ELECTROSTATIC CHUCK
1506
ADJUST UPWARD FORCE (E.G., PNEUMATIC PRESSURE) OF LIFT PINS, BASED ON SENSOR PIN MEASUREMENT
1507

Figure 15

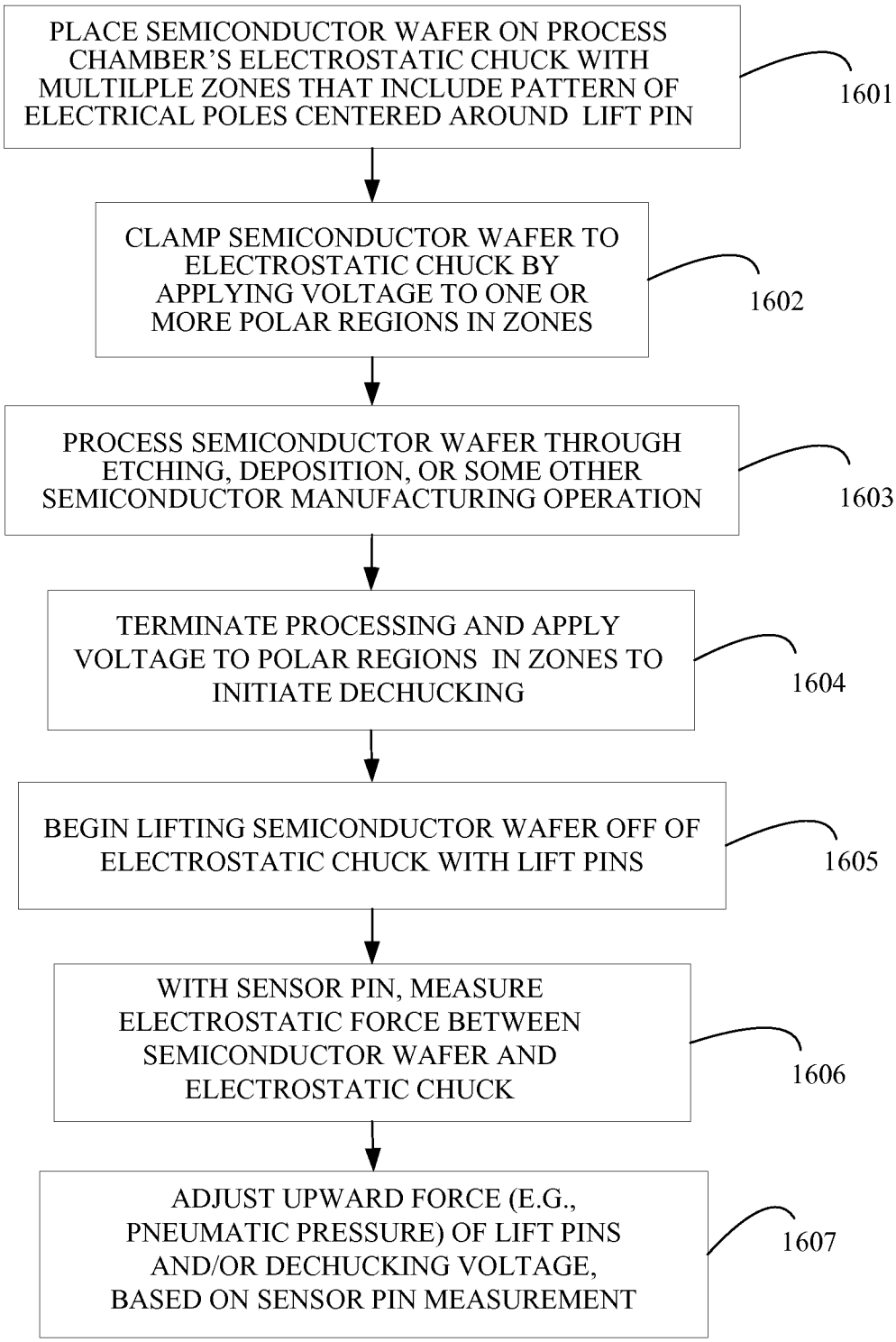

PLACE SEMICONDUCTOR WAFER ON PROCESS CHAMBER'S ELECTROSTATIC CHUCK WITH MULTILPLE ZONES THAT INCLUDE PATTERN OF ELECTRICAL POLES CENTERED AROUND LIFT PIN
1601
CLAMP SEMICONDUCTOR WAFER TO ELECTROSTATIC CHUCK BY APPLYING VOLTAGE TO ONE OR MORE POLAR REGIONS IN ZONES
1602
PROCESS SEMICONDUCTOR WAFER THROUGH ETCHING, DEPOSITION, OR SOME OTHER SEMICONDUCTOR MANUFACTURING OPERATION
1603
TERMINATE PROCESSING AND APPLY VOLTAGE TO POLAR REGIONS IN ZONES TO INITIATE DECHUCKING
1604
BEGIN LIFTING SEMICONDUCTOR WAFER OFF OF ELECTROSTATIC CHUCK WITH LIFT PINS
1605
WITH SENSOR PIN, MEASURE ELECTROSTATIC FORCE BETWEEN SEMICONDUCTOR WAFER AND ELECTROSTATIC CHUCK
1606
ADJUST UPWARD FORCE (E.G., PNEUMATIC PRESSURE) OF LIFT PINS AND/OR DECHUCKING VOLTAGE, BASED ON SENSOR PIN MEASUREMENT
1607

Figure 16

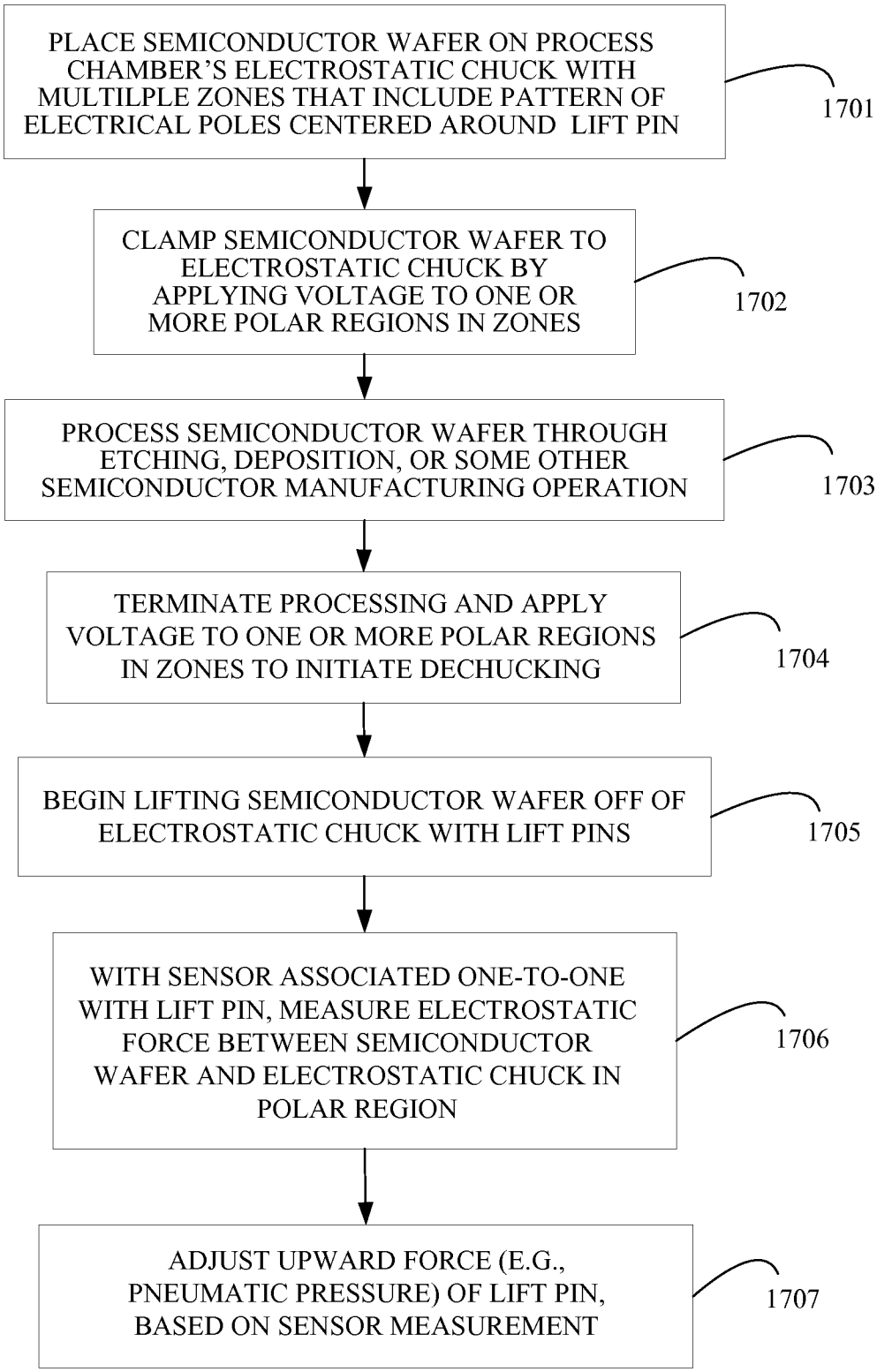

PLACE SEMICONDUCTOR WAFER ON PROCESS CHAMBER'S ELECTROSTATIC CHUCK WITH MULTILPLE ZONES THAT INCLUDE PATTERN OF ELECTRICAL POLES CENTERED AROUND LIFT PIN
1701
CLAMP SEMICONDUCTOR WAFER TO ELECTROSTATIC CHUCK BY APPLYING VOLTAGE TO ONE OR MORE POLAR REGIONS IN ZONES
1702
PROCESS SEMICONDUCTOR WAFER THROUGH ETCHING, DEPOSITION, OR SOME OTHER SEMICONDUCTOR MANUFACTURING OPERATION
1703
TERMINATE PROCESSING AND APPLY VOLTAGE TO ONE OR MORE POLAR REGIONS IN ZONES TO INITIATE DECHUCKING
1704
BEGIN LIFTING SEMICONDUCTOR WAFER OFF OF ELECTROSTATIC CHUCK WITH LIFT PINS
1705
WITH SENSOR ASSOCIATED ONE-TO-ONE WITH LIFT PIN, MEASURE ELECTROSTATIC FORCE BETWEEN SEMICONDUCTOR WAFER AND ELECTROSTATIC CHUCK IN POLAR REGION
1706
ADJUST UPWARD FORCE (E.G., PNEUMATIC PRESSURE) OF LIFT PIN, BASED ON SENSOR MEASUREMENT
1707

Figure 17

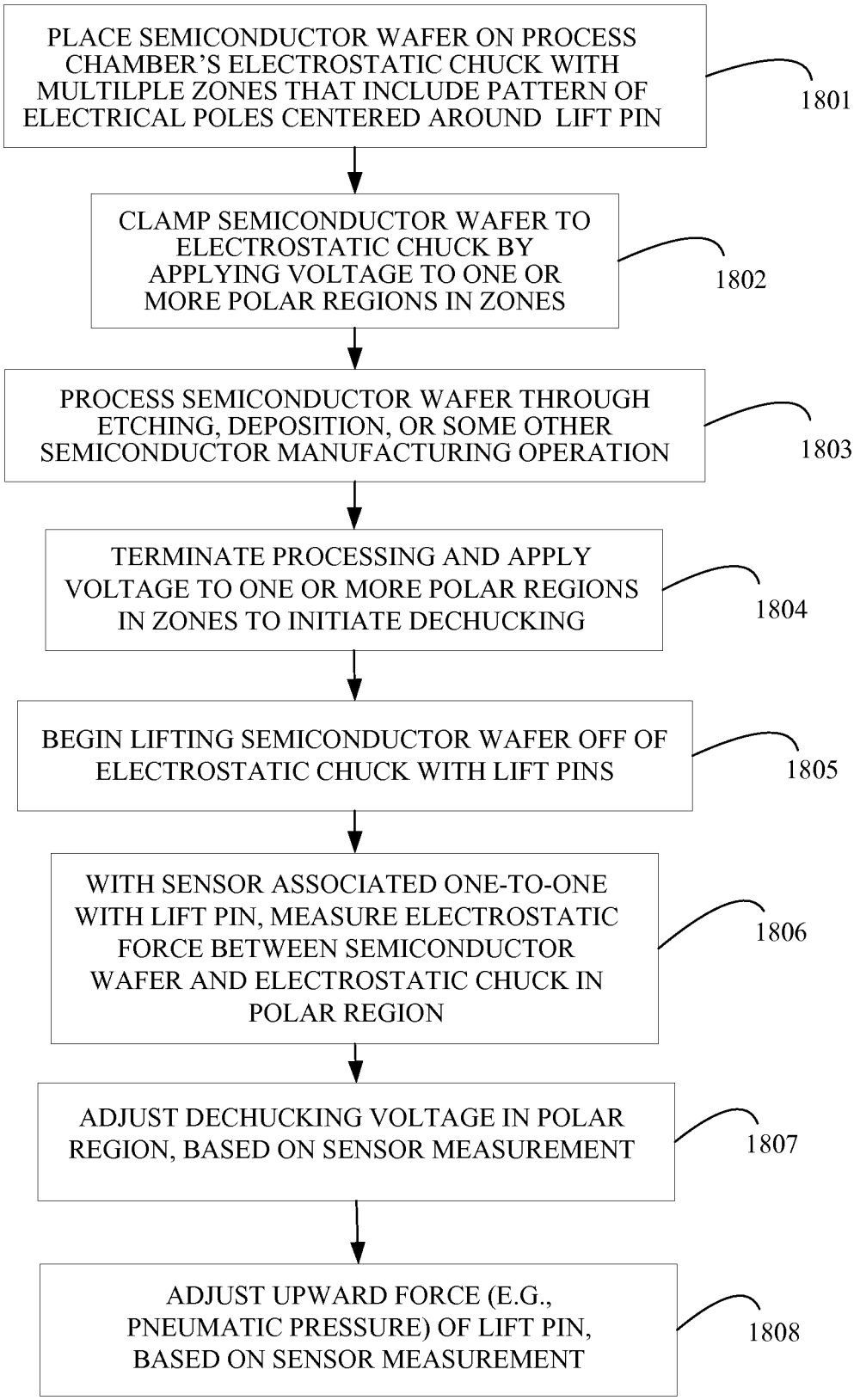

PLACE SEMICONDUCTOR WAFER ON PROCESS CHAMBER'S ELECTROSTATIC CHUCK WITH MULTILPLE ZONES THAT INCLUDE PATTERN OF ELECTRICAL POLES CENTERED AROUND LIFT PIN
1801
CLAMP SEMICONDUCTOR WAFER TO ELECTROSTATIC CHUCK BY APPLYING VOLTAGE TO ONE OR MORE POLAR REGIONS IN ZONES
1802
PROCESS SEMICONDUCTOR WAFER THROUGH ETCHING, DEPOSITION, OR SOME OTHER SEMICONDUCTOR MANUFACTURING OPERATION
1803
TERMINATE PROCESSING AND APPLY VOLTAGE TO ONE OR MORE POLAR REGIONS IN ZONES TO INITIATE DECHUCKING
1804
BEGIN LIFTING SEMICONDUCTOR WAFER OFF OF ELECTROSTATIC CHUCK WITH LIFT PINS
1805
WITH SENSOR ASSOCIATED ONE-TO-ONE WITH LIFT PIN, MEASURE ELECTROSTATIC FORCE BETWEEN SEMICONDUCTOR WAFER AND ELECTROSTATIC CHUCK IN POLAR REGION
1806
ADJUST DECHUCKING VOLTAGE IN POLAR REGION, BASED ON SENSOR MEASUREMENT
1807
ADJUST UPWARD FORCE (E.G., PNEUMATIC PRESSURE) OF LIFT PIN, BASED ON SENSOR MEASUREMENT
1808

Figure 18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/051825

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/687 (2011.01)
USPC - 361/234
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/67, 683, 687 (2011.01)
USPC - 361/234, 235; 438

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Patent, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,459,632 A (BIRANG et al) 17 October 1995 (17.10.1995) entire document	1-11, 22-28 ---------- 12-21
Y	US 6,215,640 B1 (HAUSMANN) 10 April 2001 (10.04.2001) entire document	12-21
Y	US 7,436,645 B2 (HOLLAND et al) 14 October 2008 (14.10.2008) entire document	18-21
A	US 2008/0220622 A1 (GOODMAN et al) 11 September 2008 (11.09.2008) entire document	1-28
A	US 5,557,215 A (SAEKI et al) 17 September 1996 (17.09.1996) entire document	1-28

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