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(71) Applicant *(for all designated States except US)*: **CAVENDISH KINETICS LIMITED** [GB/GB]; Home Farm, Heydon, Nr Royston, Hertfordshire, SG8 8PZ (GB).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **VAN KAMPEN, Robert** [NL/NL]; Prauwstraat 14, NL-5237 PL 'sHertogenbosch (NL). **SMITH, Charles, Gordon** [GB/GB]; 21 Kimberley Road, Cambridge CB4 1HG (GB). **KAZINSKI, Robert** [NL/NL]; Graafseweg 207, NL-5213 AE 'sHertogenbosch (NL).

(74) Agent: **Gill Jennings & Every Broadgate House**; Broadgate House, 7 Eldon Street, London, EC2M 7LH (GB).

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(54) Title: MICRO FUSE

(57) Abstract: A micro fuse for use in a semiconductor device. The micro fuse comprises an insulating substrate and an elongate metal fuse member, the fuse member being supported at either end on the substrate and including at least one fuse region suspended out of contact with the substrate and shaped such that, in use, a predetermined current can be applied to it to make it non-conducting. At least one barrier may be formed between the fuse region of the fuse member and the insulator. The fuse member may be formed from a readily oxidisable metal, such as Titanium, Tungsten, Tantalum, Copper or Aluminium. The fuse member may have two or more fuse regions, with a region between adjacent fuse regions being supported by a metal track. In this case, the fuse member may also be supported on the substrate via one or more inter layers.

MICRO FUSE

The present invention relates to a micro fuse, in particular a MEMS micro fuse, for use in semiconductor devices.

5 During the fabrication of semiconductor microprocessors and memory chips there is a need for one-time programmable non-volatile structures that are used to record which active devices on the chip have failed. The chips are designed to have spare devices which can be switched in to replace the failed devices. This built-in redundancy allows a higher chip yield per wafer. After test onboard non-volatile 10 memory devices are used to record which devices have failed and which ones are being used to replace them.

There are various non-volatile devices employed at the moment to record this data. These structures are sometimes referred to as repair fuse boxes. In some fabrication facilities the information is stored in electronically programmable 15 semiconductor devices such as EEPROM's and FLASH memory devices. These non-volatile devices need different semiconductor processes than that used to provide the random access memory (DRAM) or microprocessor devices on the rest of the chip, so are expensive to add. Instead of these active devices, often cheaper metal lines are used which can be blown using a focussed laser beam or a large current density 20 applied along their length. The laser technique can only be performed in the fabrication facility after test. It is a slow process involving test, followed by laser cutting in a separate tool, followed by test. The test identifies the failed elements and the fuses are blown to bring in new devices. After this the surface has to be passivated with a layer to prevent ions and water vapour causing damage to the chips 25 during dicing and packaging of the wafer.

The fuses which are blown using high current densities are hard to produce because the surrounding metal has to cover a large area to accommodate the large currents. This makes the cell size for these structures large. When the metal does blow it can redeposit on the insulator that the metal track sits on. Generally for metal 30 tracks on a substrate, the threshold for destroying the wires is controlled by the current density and is variable, depending on the detailed grain structure, and resistivity of the metal.

Other techniques employ an anti-fuse which consists of a very thin insulator placed between two metals. When a large electric field is placed across the insulator,

it breaks down creating a shorted path. The problem with this technology is that the shorted path can vary greatly in resistance from device to device. This is because the breakdown will be initiated at regions of high electric field which depend on the surface roughness.

5 The object of this patent is to provide one time programmable fusible link which can be electrically programmed, is faster to programme, has less collateral damage and can be produced with a higher yield.

According to the present invention there is provided a micro fuse for use in a semiconductor device, the micro fuse comprising:

10 an insulating substrate: and

an elongate metal fuse member, the fuse member being supported at either end on the substrate and including at least one fuse region suspended out of contact with the substrate and shaped such that, in use, a predetermined current can be applied to it to make it non-conducting.

15 At least one barrier may be formed between the fuse region of the fuse member and the insulator.

The fuse member may be formed from a readily oxidisable metal, such as Titanium, Tungsten, Tantalum, Copper or Aluminium.

The fuse member may have two or more fuse regions, with a region between 20 adjacent fuse regions being supported by a metal track. In this case, the fuse member may also be supported on the substrate via one or more inter layers.

Corresponding methods of manufacture of the fuse are also provided.

The invention involves fabricating a double-clamped cantilever structure which does not touch the substrate along its length. Because the wire does not touch the 25 substrate the heat loss is via thermal conduction along the wire length, rather than out through the substrate. The heat going in is related to the resistance in the free standing wire. The heat which leaves is also related to the resistance of the wire via the Wiedemann-Franz law, that relates the thermal conductivity to the electrical resistivity. The heat loss from the lattice vibrations or Phonons is small in comparison 30 to that lost by the conduction of the electrons. For micron sized or sub-micron sized wires, the heat loss from radiation is small. If we consider the scaling laws for the various heat loss mechanisms and compare this with the heat dumped into the wire of radius r and length L and resistivity R due to electronic heating by a current I, then:

for a small element dx the heat going in is given by I^2R, or $I^2 \rho dx / \pi r^2$

The heat loss from the ends of the wire is dominated by the thermal conductivity K_e of the electrons and so is proportional to the area of the wire πr^2 and the thermal gradient along the wire.

The heat lost due to radiation which goes as the surface area $2\pi r.dx.s_B T^4$,

5 where s_B is Stephan's constant. The heat input is $\frac{I^2\rho}{\pi r^2 R}$ and the radiation is $\frac{2s_B T^4}{r}$

The balance equation is then:

$$\frac{\partial}{\partial x}\left(\pi r^2 k \frac{\partial T}{\partial x}\right) + \frac{I^2 R\rho}{\pi r^2} - 2\pi s_B T^4 r = 0$$

Given that for metals at room temperature K_e is related to the resistivity by the Wiedemann Franz law:

10 $K_e = LT/\rho$, where L is the Lorenz constant ($L = (\pi^2/3)(k_B/e)^2$). K_B is the Boltzmann constant and e is the charge of an electron. We also need to calculate the above differential equation is a functional form for the temperature dependence of the resistivity.

Considering scaling of such a formula, assume that all fuse dimensions (radius,

15 length) are reduced by a scaling factor F. For a given temperature change dT in the fuse, we can see that the heat lost via thermal conduction does not change with the scaling factor, but the heat lost via thermal radiation is reduced by a factor F. Thus, as the fuse dimensions are scaled down, the heat lost via radiation will become negligible compared to the heat lost via thermal conduction. Ignoring the radiation term

20 in the balance equation, we can see that if all dimensions of the fuse are reduced by a factor F, then the current required to melt the fuse is reduced by a factor F as well.

Because of the simple thermal properties, the fuses can be designed to predictably fuse at a well defined voltage dropped along its length. This also results in a well defined temperature dependence along the wire length, with the central

25 portion being the hottest, this results in better control of the temperature at the centre of the wire. A consequence of this is that a very small region can be melted in a controllable fashion at the centre of the free standing double clamped cantilever. Because the melted region is small, there is a lower probability that the evaporated metal will short out the fused wire, or that the melted material will land somewhere else

30 on the chip and cause damage. When the central part of the double cantilever has

been melted away the two end parts remain free standing. This means that the broken fuse does not touch the surrounding insulator, which may have some evaporated metal on the surfaces. This helps in maintaining a well defined difference between the on and off resistance.

5 The threshold for blowing the device is given by the voltage dropped along the wire which is a product of the wire dimensions and the wire resistivity. As these values are well controlled the voltage for switching can be well predicted. To read the state of the wire, the current through the wire can be measured with a device to limit the voltage drop across the fuse. To blow the wire the current limiting device can be 10 removed, which results in a voltage being dropped across the wire that is greater than the threshold for melting. Because the wire is not connected to the substrate along its length it has a very small specific heat which allows it to reach melting temperatures in a very short time.

To ensure that no evaporated metal from the fuse causes a continuous 15 conducting path between the two blown ends of the wire, there may be provided a barrier between the melted portion and at least one end of the blown fuse where it touches the substrate.

The present invention, with its free-standing fuse member, has benefits in terms of its ability to be positioned about other active devices without causing damage 20 to them when fusing. We have shown that when the fuse member blows at over 3,000K the temperature under the centre of the fuse member does not raise by more than 60K. Furthermore, the fuse members are smaller than prior art arrangements, and therefore requires lower currents to fuse, resulting in less damage to adjacent components, reducing the spacing. This in turn helps reduce routing problems and 25 timing problems that occur with prior art fuses that, by their nature, needs to be located some way away from other memory areas. The low current fusing requirements also mean that the fuses do not need an extra power pad, reducing further the component count in a device employing the fuse.

Examples of the present invention will now be described with reference to the 30 accompanying drawings, in which:

Figures 1 to 3 show a first example microfuse according to the invention, including a method of manufacture thereof;

Figures 4 and 5 show a second example microfuse according to the invention during manufacture and after being blown;

Figures 6 to 8 show a further example of the present invention both during manufacture, prior to and after being blown;

Figure 9 shows a further example of the present invention employing an oxidizing metal;

5 Figure 10 shows another example of the present invention employing an in-plane design;

Figures 11a-f show a micro fuse according to the present invention at the various stages of its fabrication;

Figure 12 shows a micro fuse according to the present invention arranged in 10 an S-shape;

Figure 13 shows a micro fuse according to the present invention arranged in a U-shape; and

Figure 14 shows a micro fuse according to the present invention arranged in an L-shape.

15 Figure 1 shows a technique for fabricating an example MEMS micro fuse of the present invention. A substrate 1 is provided which may be an insulator on top of a silicon chip containing completed semiconductor devices, such as memory products or microcontrollers. A sacrificial layer 2 is provided a substrate and which can be removed using a gas plasma etch without removing other layers, such as substrate 20 1, appreciably during release. A metal conducting layer 3 is provided. This layer 3 is normally formed from the metal used in one of the metalisation layers of the underlying semiconductor devices in order to minimise manufacturing complexity. This layer 3 can be formed Aluminium, Aluminium Copper, Copper, Titanium Nitride, or Titanium, or Tungsten or Tantalum or Tantalum Nitride, for example. The sacrificial 25 layer 2 can be Silicon Nitride, sputtered amorphous silicon, or a different material which etches selectively compared to the metal of the fuse layer 3.

Figure 2 shows a diagram of the fuse after the sacrificial layer 2 has been etched.

As can be seen from figure 2, a central fuse region 7 is provided suspended 30 above the insulated substrate 1 and supported at either end from the substrate 1. As discussed above, the centre region 7 has dimensions which can be controlled to a high degree of accuracy, given the manufacturing techniques that are employed, such that the central fusing region can be destroyed by application of an appropriate control current in an extremely reliable and predictable way.

Figure 3 shows the fused wire after the appropriate electric field has been applied. From this it can be seen that the remainder of the layer 3 does not contact substrate 1.

Figure 4 shows a second example MEMS micro fuse according to the invention where an extra layer 4 has been added. This layer 4 can be an insulator or conductor. It is not removed when the sacrificial layer 3 is removed. It provides a line-of-sight barrier for any evaporated metal generated when layer 3 is fused, preventing it forming a continuous path from one end of the layer 3 to the other.

Figure 5 shows the device in figure 4 after the removal of the sacrificial layer during the etch and the subsequent blowing of the fuse region 7. It can be seen that the layer 4 acts as a barrier to break up the evaporated material 5 on the substrate which is generated during blowing of the fuse, and which prevents it shorting out the blown fuse.

It can be seen that, in this example, the sacrificial layer 3 has given the fuse a shape that means that even if layer 4 was removed with layer 5 the fuse shape is such that the region of the fuse close to the base acts as a barrier to prevent the metal evaporated at the region 7 of the metal layer 3 reaching the substrate 1, and this configuration may be employed in the invention.

In both the above examples it is possible to choose the fuse metal in layer 3 such that when it is heated so that it fuses the evaporated metal is chosen to be very reactive, so that it oxidizes as it evaporates. Metals such as Al, Ta, Ti, TiN or Cu would all oxidize if evaporated in air. This means that the residue after the fuse is blown becomes an insulator and so will not cause any problems with shorting.

Another example of the invention, shown in figures 6 to 8, has a vertical fuse portion to reduce the area it occupies on the chip. The fuse of this example can replace the standard via technology which connects metal tracks at different levels in the chip. The fabrication of such a vertical arrangement will now be described. In this construction layer 6 is a inter metal dielectric on the substrate 1. A hole 8 is opened in the interlayer dielectric 6 above track 9 which runs into the view shown. A sacrificial layer 2 is then put into the hole 8 and a polish is performed back to the dielectric layer 6. A small via hole is then opened up down through the sacrificial layer 2 to metal track layer 9. Then a metal layer 3 is deposited into the hole 8. The side wall coverage is reduced due to shadowing effects.

Figure 7 shows the structure of figure 6 after the sacrificial layer 2 has been removed.

Figure 8 shows the vertical fuse of figure 7 after melting. If, instead of the etched hole, an etched groove running along metal track 9 is produced, then track 9 can provide two fuses, one from each side. In this case, they can be separately blown by applying a potential difference between track 9 and the left hand side of layer 3,
5 while keeping the right hand side of layer 3 at the same voltage as track 9.

In order to get continuous coverage of metal up the side of the etched sacrificial layer 2, it is important that the side wall is not undercut or vertical. Alternatively Plasma enhanced CVD may be used with a metal such as TiN on the side walls of hole 8 before deposition of the top metal layer 3. This technique gives
10 better conformal coverage of vertical side walls.

In a fourth example, it is possible to make the fuse out of a metal layer 3 which oxidizes at high temperatures. The metal may be Ti, Ta, W, Cu or Al, for example. Then when a current is passed through the fuse region 7, it is heated up above a threshold temperature for oxidation in air. At elevated temperatures the metal begins
15 to be oxidized. By designing the metal layer 3 to be thin enough, the growth of a surface oxide on the top, bottom and sides is such that there is no longer any conductive material left. The advantage of this technique is that there is no evaporation of material which could provide a short between the two ends of the cantilever.

20 Figure 9 shows such an example with a fuse region 7 after it has been heated by applying a voltage across the metal length 3 while in air. The hottest portion (in the middle) has reached a temperature above a threshold temperature for oxidation (for example with TiN this is 350° C). This hot region then oxidizes turning the metal into an insulator.

25 Figure 10 shows an example of the present invention showing an in-plane design. This design has the advantage of eliminating the shorting of the two beam bases. The metal length 3 consists of two parallel beams connected together by a third beam that is considerably narrower than the other two beams. When this fuse blows the narrow connecting beam blows and the configuration of these beams
30 ensures that the evaporated metal cannot extend to the base of the wide beams. This, in turn, ensures that the blown fuse cannot accidentally be short circuited.

Figures 11a-f show a MEMS micro fuse according to the present invention in the various stages of its fabrication. Figure 11a shows a CMOS wafer that has been processed by a standard dual damascene process up to the last metal layer. This is
35 usually capped with a silicon nitride layer which will be used as the sacrificial layer

under the TiN fuse. The thickness of the layer may have to be adjusted to provide a suitable gap under the fuse. During the first masking process a TiN layer is deposited and etched into the desired pattern. The TiN layer that will form the fuse is left over the copper, because it can not be easily etched off the copper with good selectivity. The next stage of the process involves depositing and patterning a SiN sacrificial layer above the fuse, followed by a silicon dioxide layer. A second masking process then takes place to open holes in the oxide layer. This is shown in figure 11d and results in the fuse being ready to be released as shown in Figure 11a. This etch removes the SiN both bellow and above the fuse so that it is only in physical contact to the rest of the chip at each end. Finally a passivation layer 21 is deposited at low pressure to fill up the holes in the silicon dioxide Figure 11f. This etch removes the SiN both below and above the fuse so that it is only in physical contact to the rest of the chip at each end. Finally a passivation layer is deposited at low pressure to fill up the holes in the silicon dioxide Figure 11f. This ensures that the fuses are housed in a controlled atmosphere and at a low pressure. It also ensures that the wafer can be diced and packaged without damage to the free standing fuses. This ensures that when the fuses are blown the heat lost via convection of gas molecules is small in comparison to the heat lost via thermal conduction along the fuse. Finally, the there is a masking stage to open up the bond pads and deposit and pattern A1.

Upon passage of a current, the highest temperature is registered at the centre of the free-standing fuse element, which causes it to melt and break the contact. If the free-standing fuse element is insufficiently spaced from the overlying encapsulating layer, thermal expansion thereof occurs before melting and may cause sufficient in-plane deformation to cause it to buckle out-of-plane and consequently make contact with either the overlying encapsulating layer or the underlying substrate which, in use, renders the fuse inoperable. Therefore, the size of the cavity housing of the free-standing fuse may be increased accordingly to allow a certain degree of deformation before blowing thereof occurs. A greater spacing above and below the fuse element, after removal of the sacrificial layer, would permit some deformation before it blows. This increased spacing can be achieved by using thicker sacrificial layers sandwiching the fuse element during the fabrication stage as described hereinbefore.

It is important to control such thermal expansion stresses so that deformation of the fuse element is not sufficient to bring it undesirably into contact with contiguous layers, such as, any overlying passivation and/or encapsulation layers, or underlying

substrate layers. Having free-standing, shaped structures enables the control of in-plane and out-of-plane thermal deformations.

The elongate fuse of the present invention encompasses a variety of free-standing structures including 'S'-shaped fuses and 'U'-shaped fuses. Microfuse structures differing from the linear fuse structure described hereinbefore provide control over their thermo-mechanical behaviour. It has been determined that different fuse structures can resist out of plane deformation which may result in detrimental contact with layers of material above or below the structural layer forming it.

Figure 12 shows a schematic of a free-standing S-shaped fuse 10 clamped at via 11 and via 12. In this example, it has been determined that, in use, in-plane stresses induced on application of voltage of the order sufficient to blow the fuse element induce little or no out-of-plane deformation. The S-shaped fuse element melts along the centre link 13. This S-shaped design regulates the thermal chacteristics of the fuse when current flows through the fuse in use.

Referring to figure 13, in this embodiment the free-standing U-shaped fuse 14 clamped at via 15 and via 16 is arranged so that, when current is excessive, it melts along length 17 where the heat intensity is the greatest.

Referring to figure 14, in yet a further example, the fuse element 18 is clamped at via 19 and via 20, and is L shaped so that the fuse blows in the centre.

In all of the above examples it is possible to provide a micro fuse for semiconductor devices which can be fused in an extremely reliable fashion due to the highly controlled nature of the manufacture. It is also possible to provide a fuse member which does not contaminate its surrounding environment and hence produces a micro fuse which is more reliable, yet most cost effective, than currently known in micro fuses.

CLAIMS

1. A micro fuse for use in a semiconductor device, the micro fuse comprising:
an insulating substrate; and
an elongate metal fuse member, the fuse member being supported at either end on the substrate and including at least one fuse region suspended out of contact with the substrate and shaped such that, in use, a predetermined current can be applied to it to make it non-conducting.

2. A micro fuse according to claim 1, wherein at least one barrier is formed between the fuse region of the fuse member and the insulator.

3. A micro fuse according to claim 1 or 2, wherein the fuse member is formed from one or more of the group of Titanium, Tungsten, Tantalum, Copper or Aluminium.

4. A micro fuse according to any preceding claim, wherein the fuse member may have two or more fuse regions, with a region between adjacent fuse regions being supported by a metal track.

5. A micro fuse according to claim 4, wherein the fuse member is supported on the substrate via one or more inter layers.

6. A micro fuse according to any of the preceding claims, wherein said micro fuse is a MEMS micro fuse.

7. A micro fuse according to any proceeding claim, further comprising an encapsulating layer for encapsulating the region including the fuse member.

8. A micro fuse according to any preceding claim, wherein the micro fuse is arranged in an S-shape.

9. A micro fuse according to any of claims 1 to 7, wherein the micro fuse is arranged in a U-shape.

10. A micro fuse according to any of claims 1 to 7, wherein the micro fuse
5 is arranged in an L-shape.

11. A method of manufacturing a micro fuse for use in a semiconductor device, the method comprising the steps of:

applying a shape sacrificial layer to the surface of an insulating
10 substrate;

applying a metal layer to the surface of the insulating substrate and sacrificial layer; and

removing the sacrificial layer, wherein the sacrificial layer is shaped such that, when it is removed, the metal layer is shaped so as to provide a fuse region
15 suspended out of contact with the substrate, the fuse region being shaped so that, in use, a predetermined current can be applied to it to make it non-conductive.

12. A method according to claim 11, and further comprising the step of:

applying a barrier component to the surface of the substrate such that
20 any evaporated metal generated when the metal layer is fused cannot form a continuous path.

13. A method according to claim 11 or 12, wherein the metal layer provided by physical vapour deposition or chemical vapour deposition.

25

14. A method according to any of claims 11 to 13, wherein the metal layer is formed from one or more of the group of Titanium, Tungsten, Tantalum, Copper or Aluminium.

30 15. A method according to any of claims 11 to 14, and further comprising the step of adding an encapsulating layer over the micro fuse.

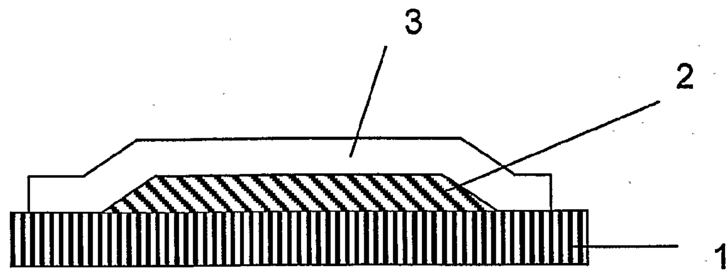

Figure 1

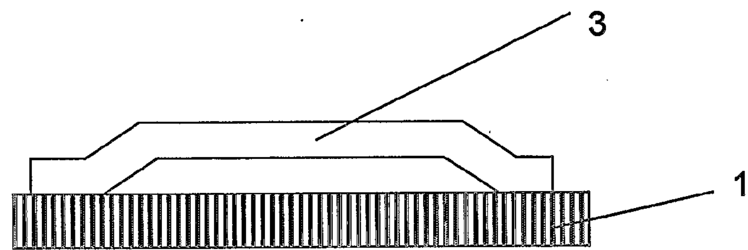

Figure 2

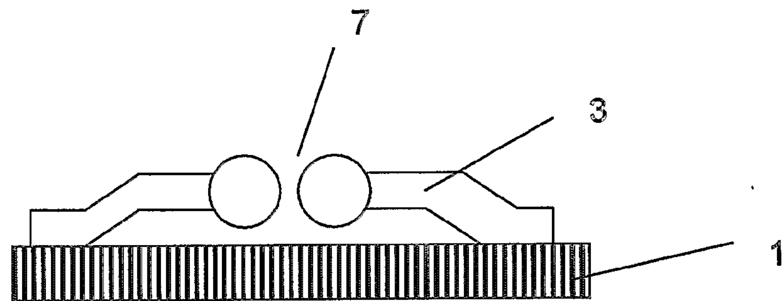

Figure 3

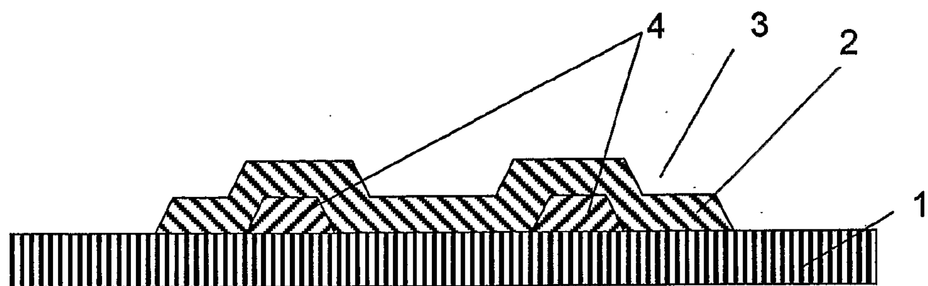

Figure 4

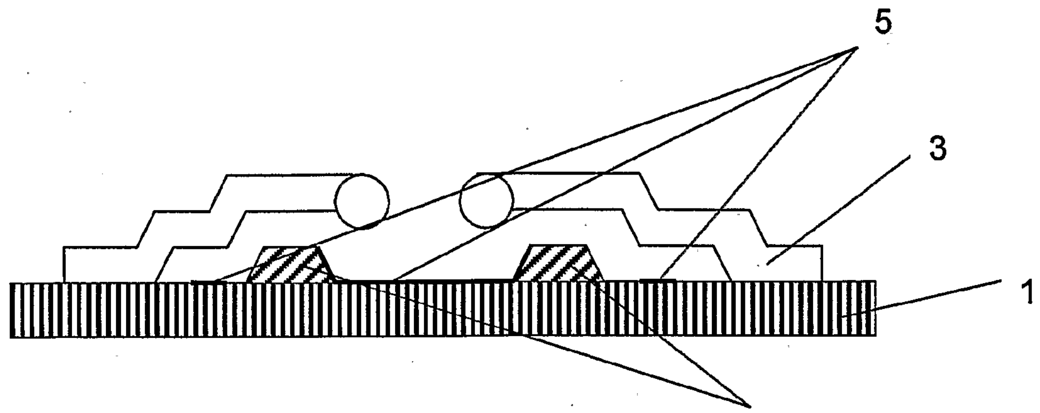

Figure 5

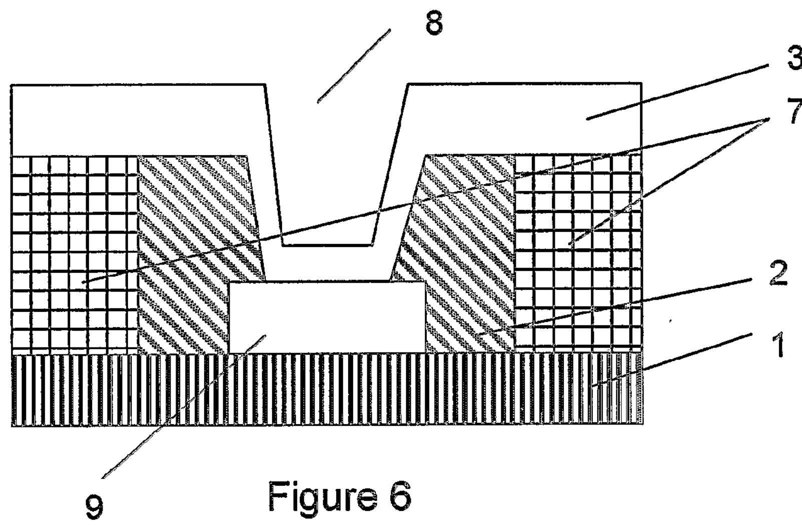

Figure 6

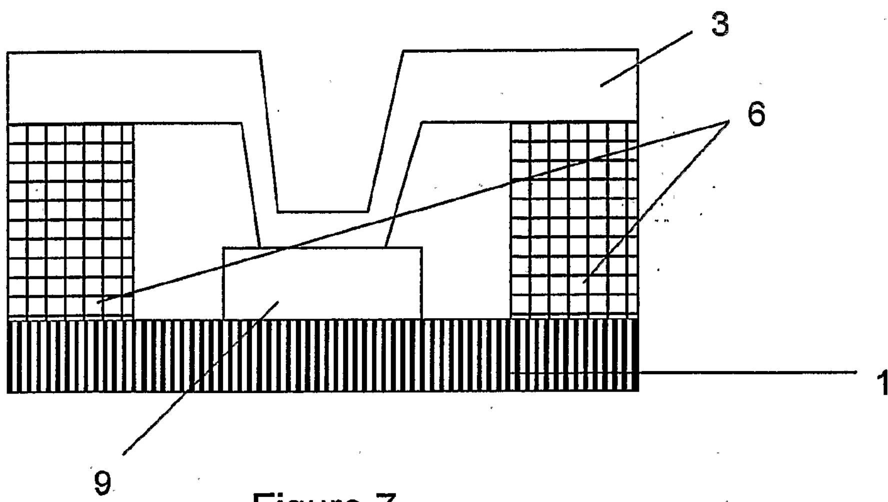

Figure 7

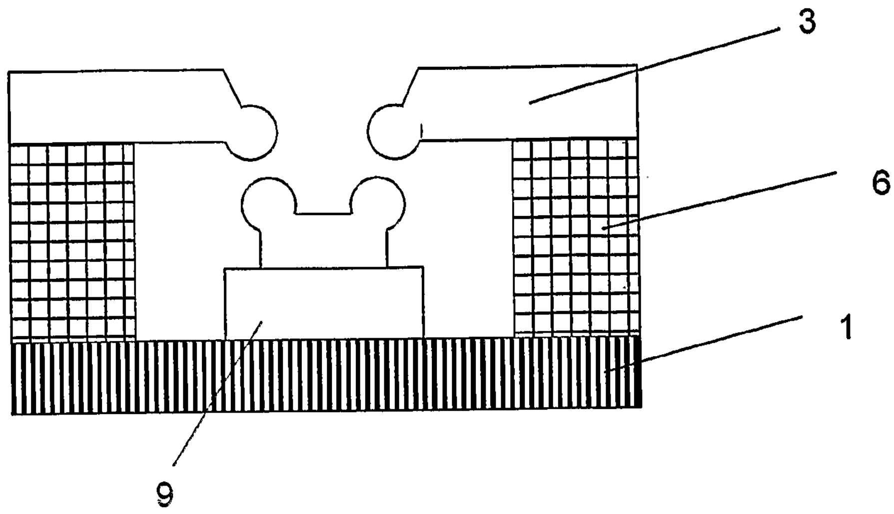

Figure 8

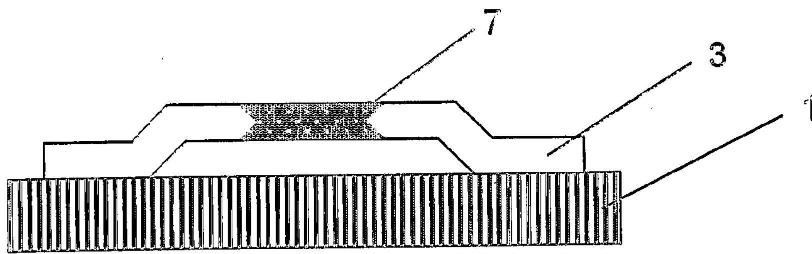

Figure 9

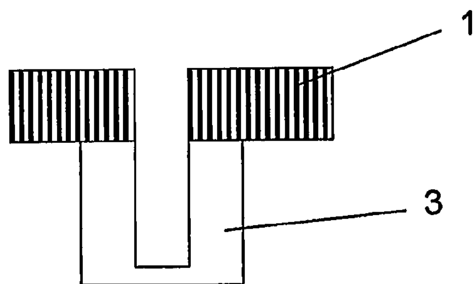

Figure 10

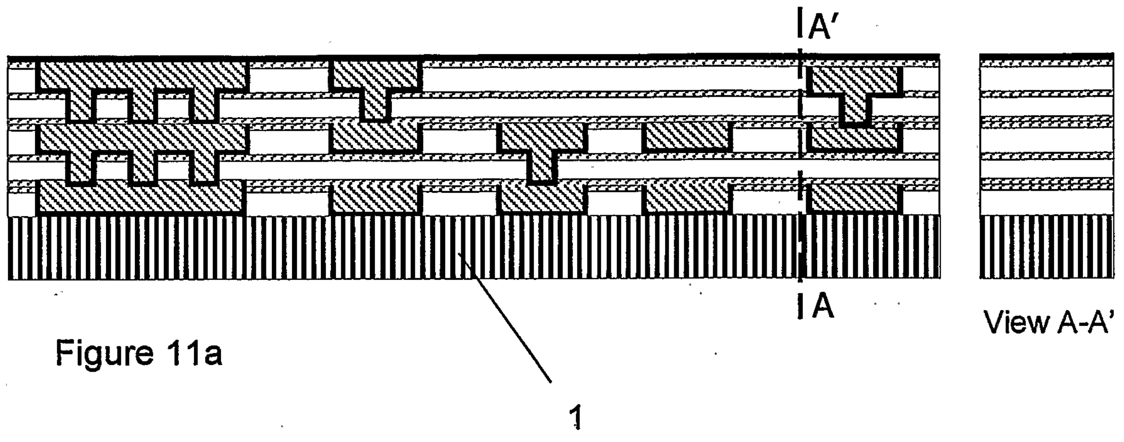

Figure 11a

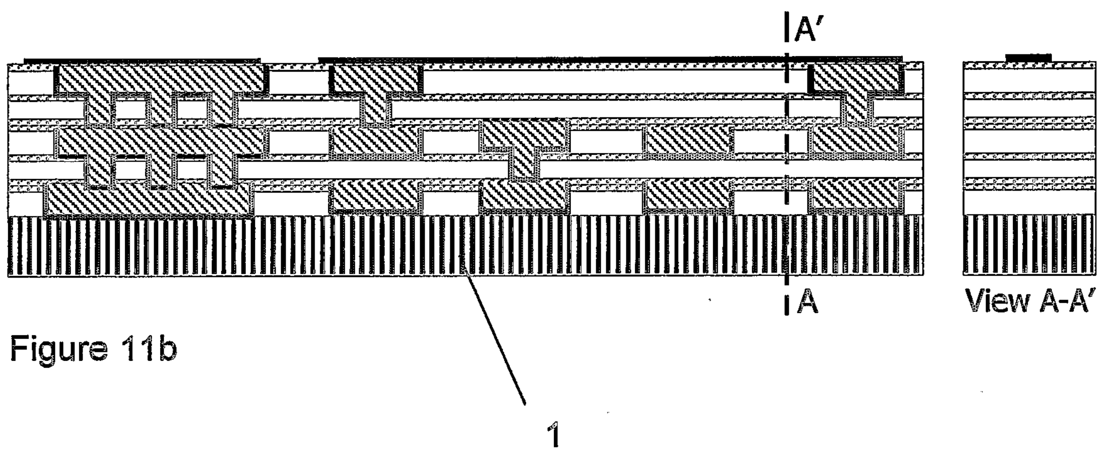

Figure 11b

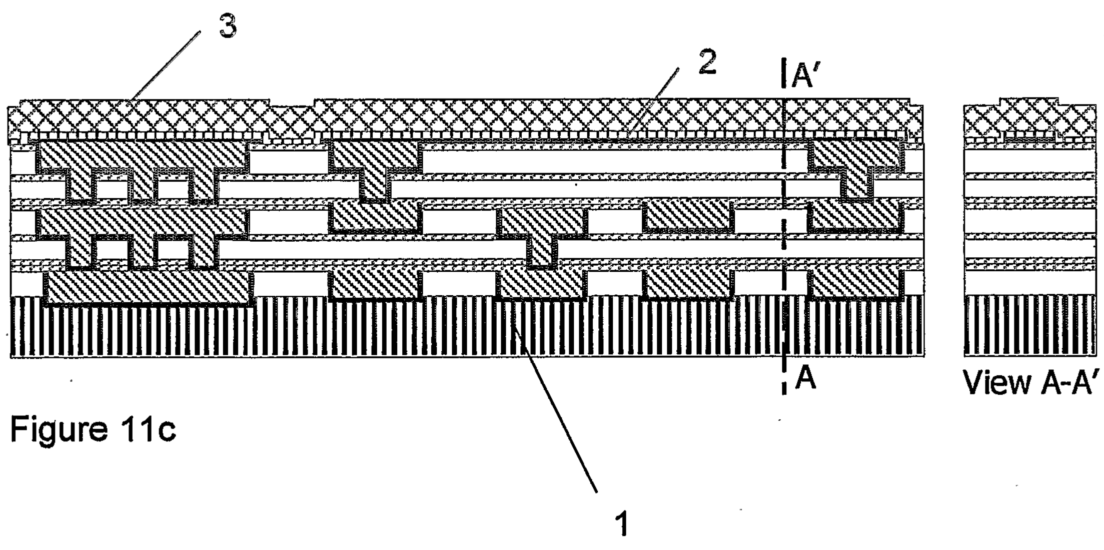

Figure 11c

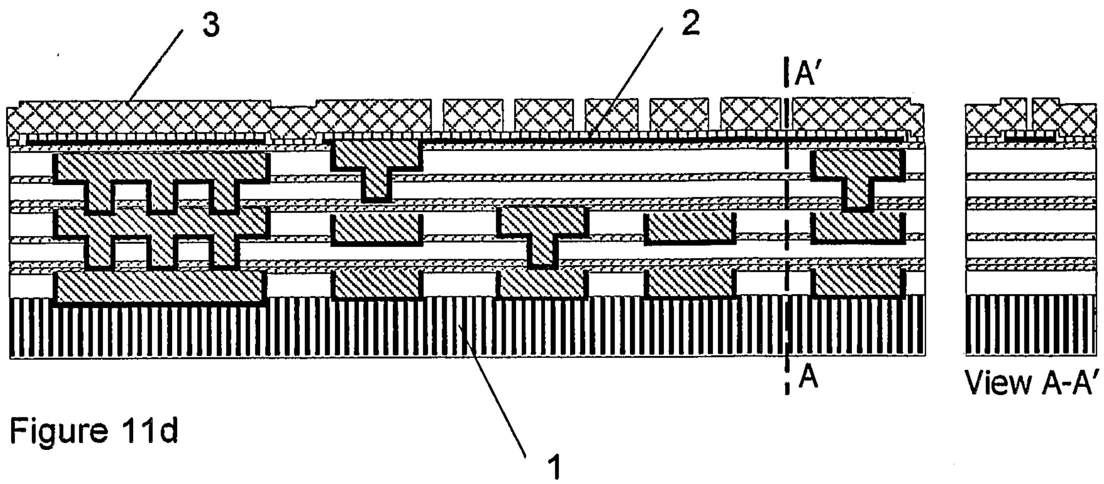

Figure 11d

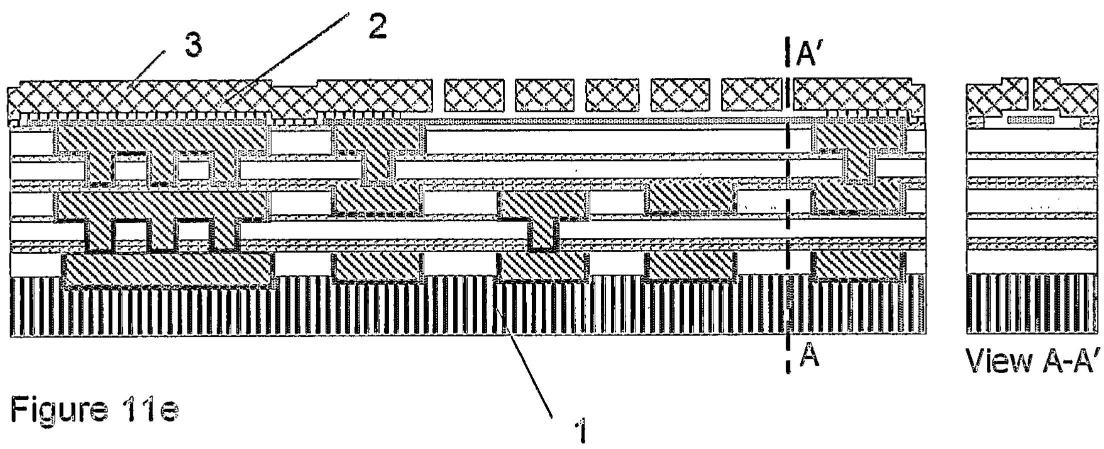

Figure 11e

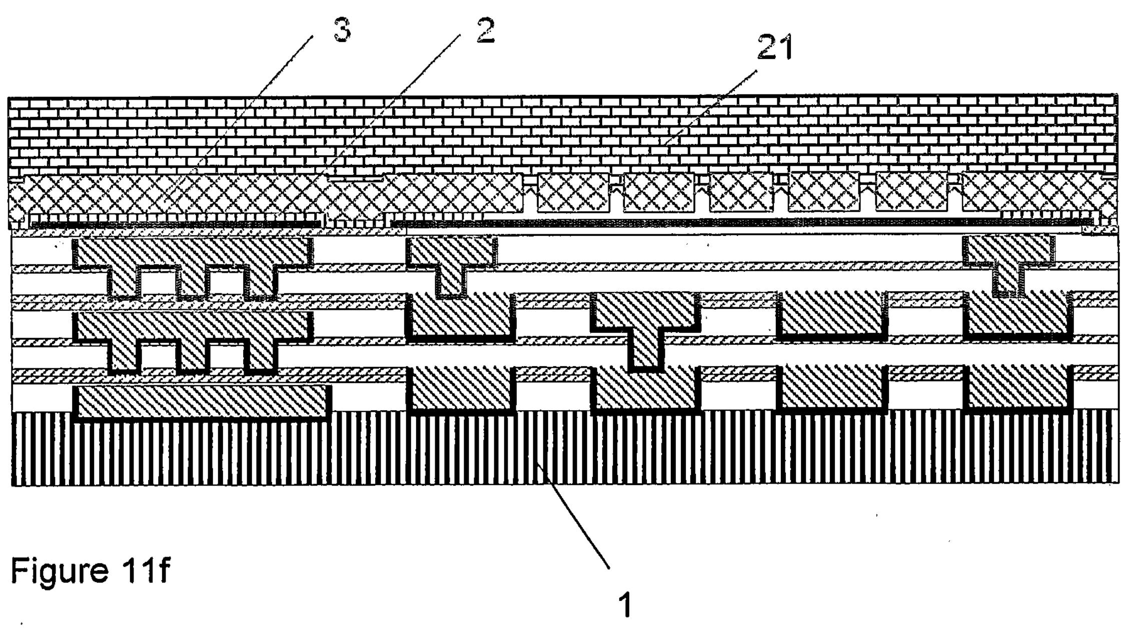

Figure 11f

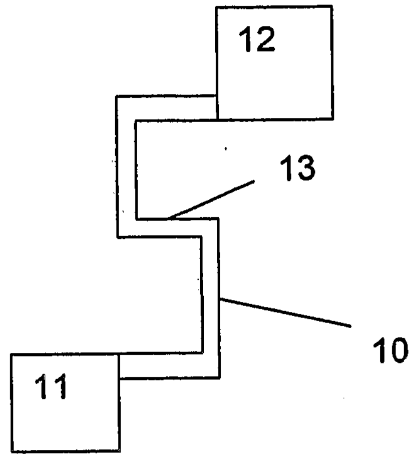

Figure 12

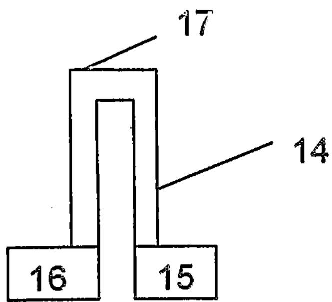

Figure 13

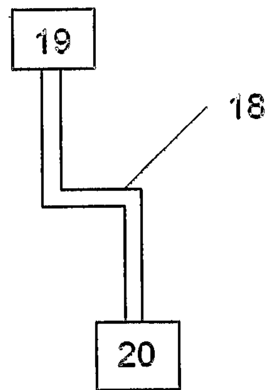

Figure 14