

[54] **MATSIDE WRESTLING SCOREBOARD**

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[58] Field of Search**340/323, 324 B, 324 S; 235/92 GA, 92 T, 92 EV; 273/1 E; 58/39.5, 145 D, 152 R**

[56] **References Cited**

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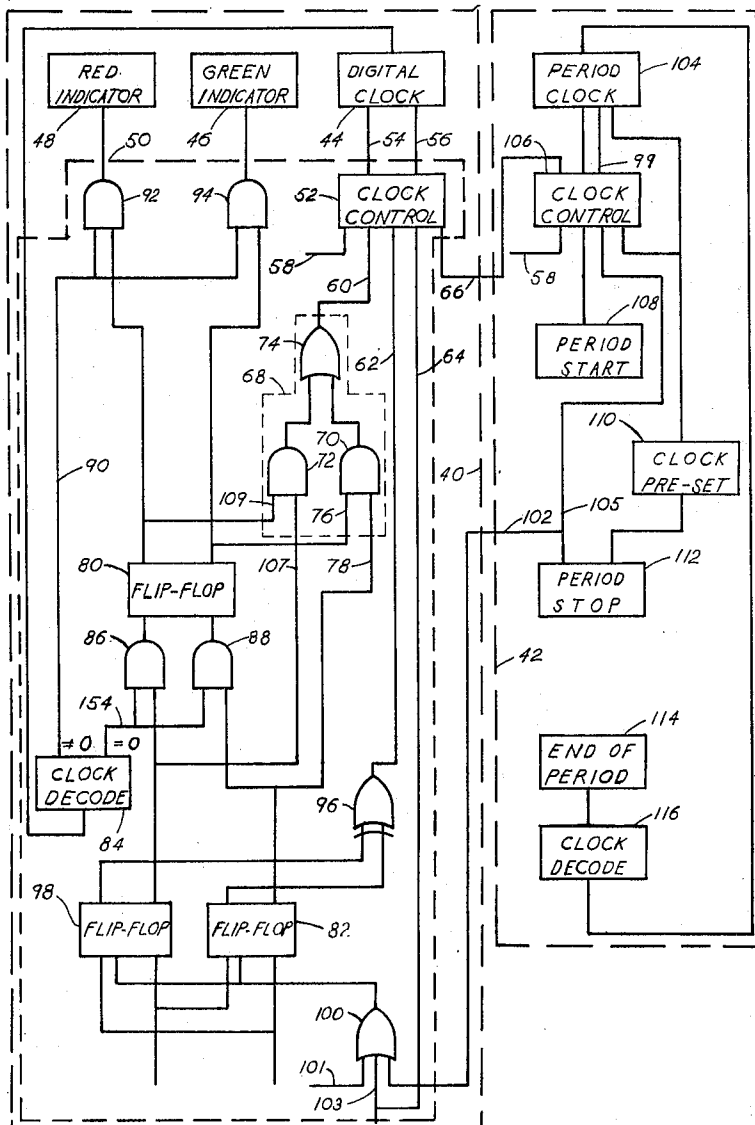
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[57] **ABSTRACT**

A Wrestling Scoreboard including an Advantage Time Display and Advantage Indicators which display net advantage time in digital form and indicate which one of two wrestlers has accrued the net advantage time. In a preferred embodiment, the scoreboard is packaged in a multi-sided casing which is portable to permit positioning of the scoreboard adjacent a wrestling mat and each side is provided with a Match Display, Period Indicators, Period Time Display, a Match Score Display, and a Team Score Display in addition to the Advantage Time Display and pair of Advantage Indicators.

13 Claims, 4 Drawing Figures



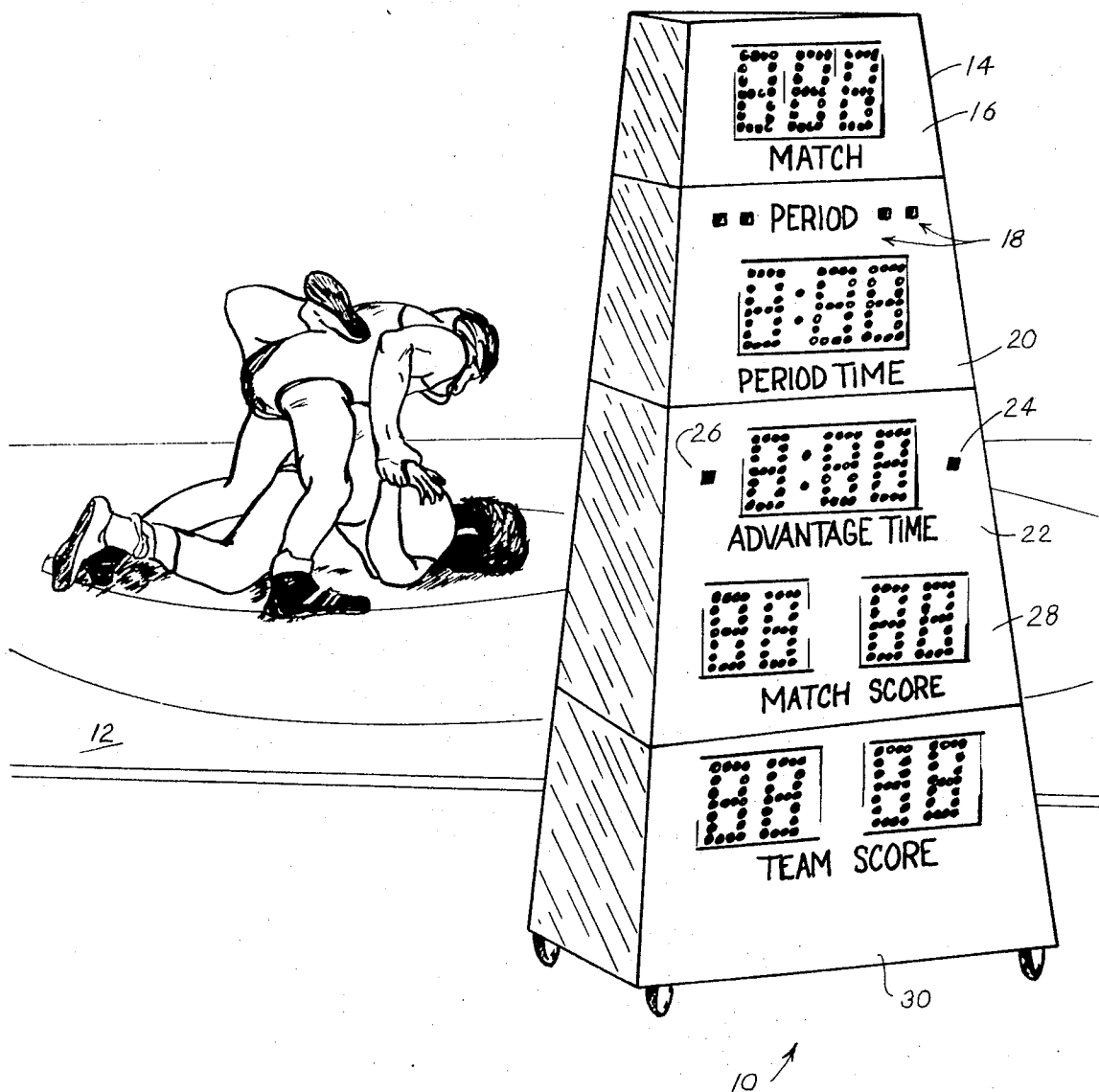
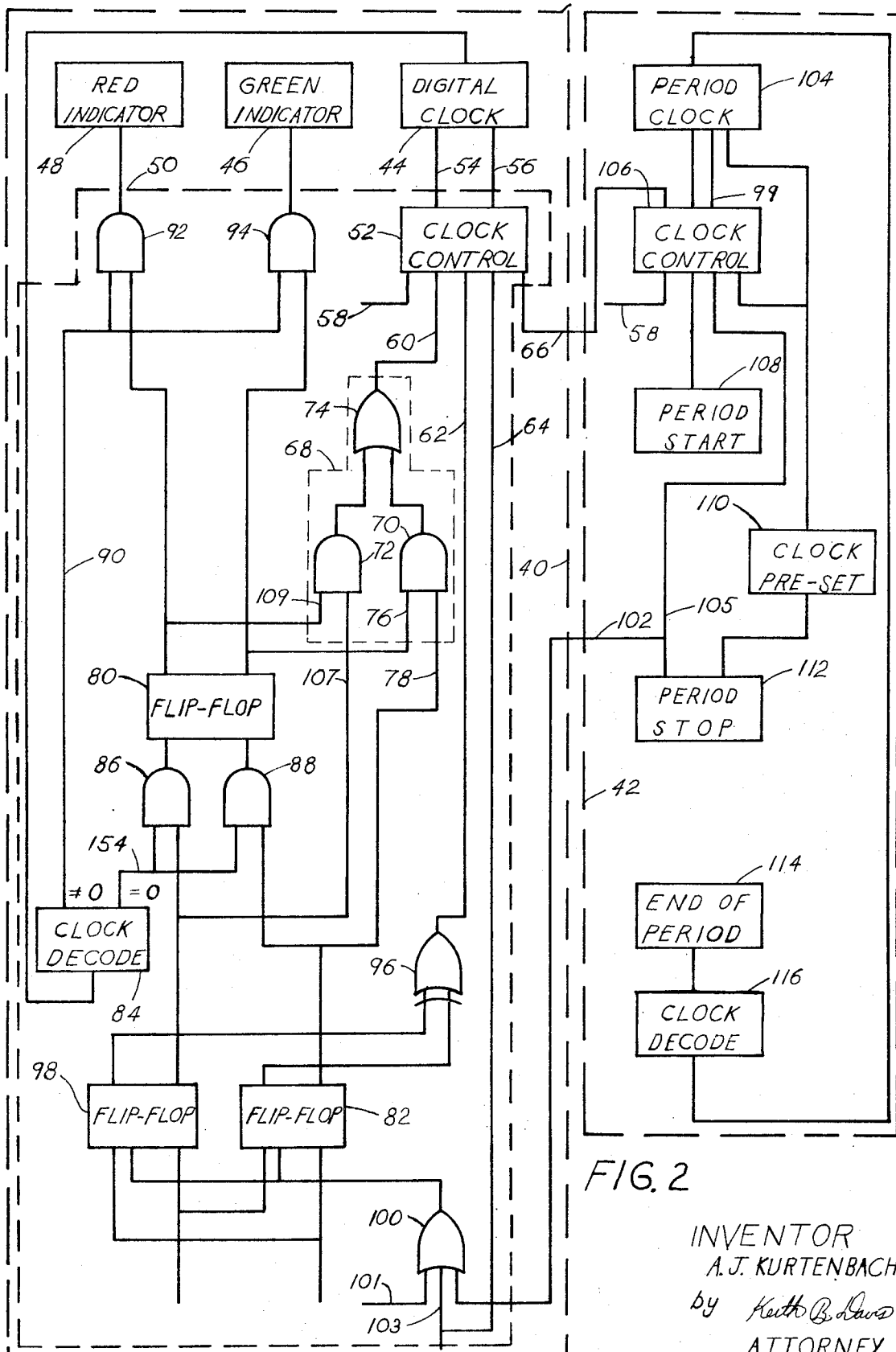
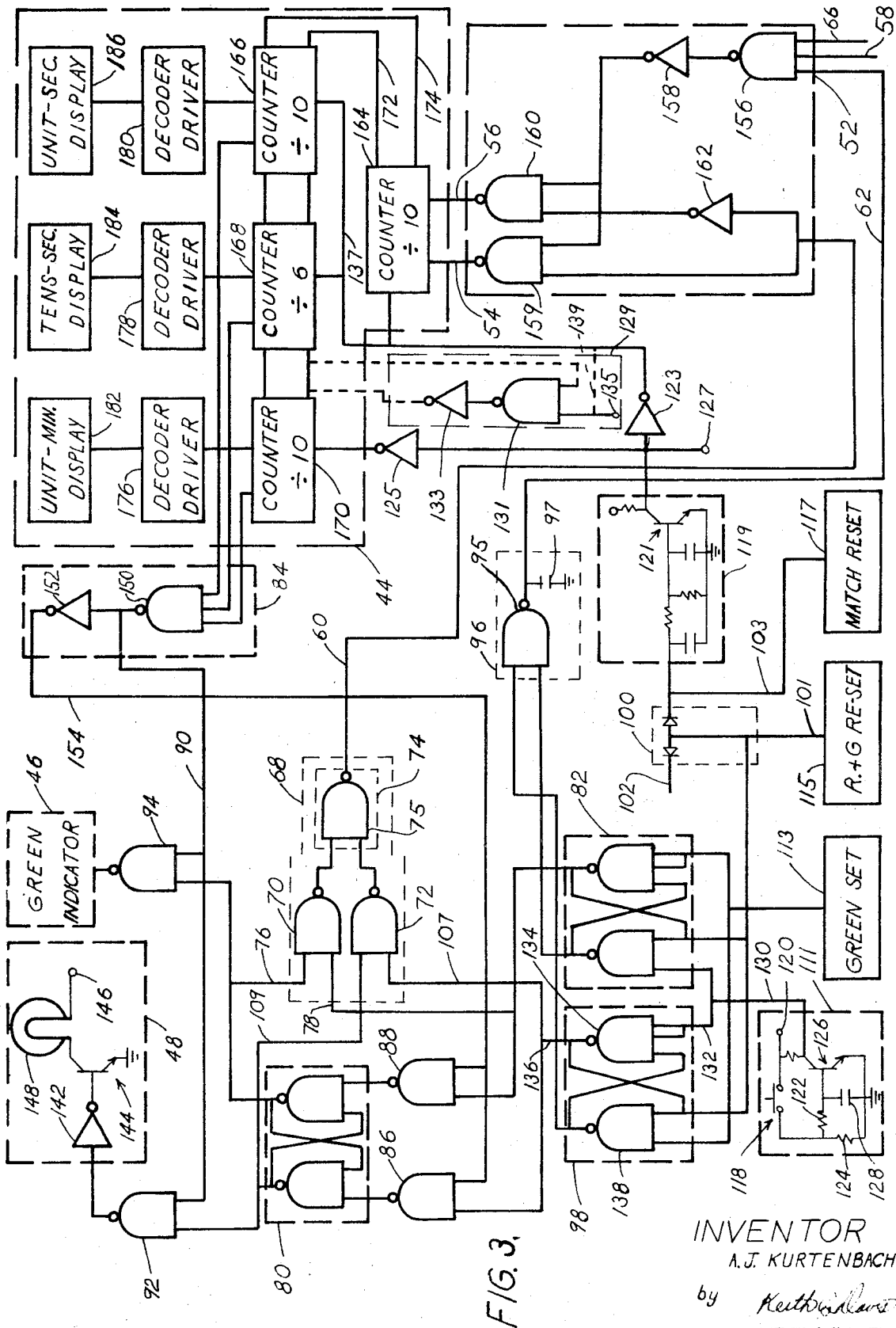


FIG. 1

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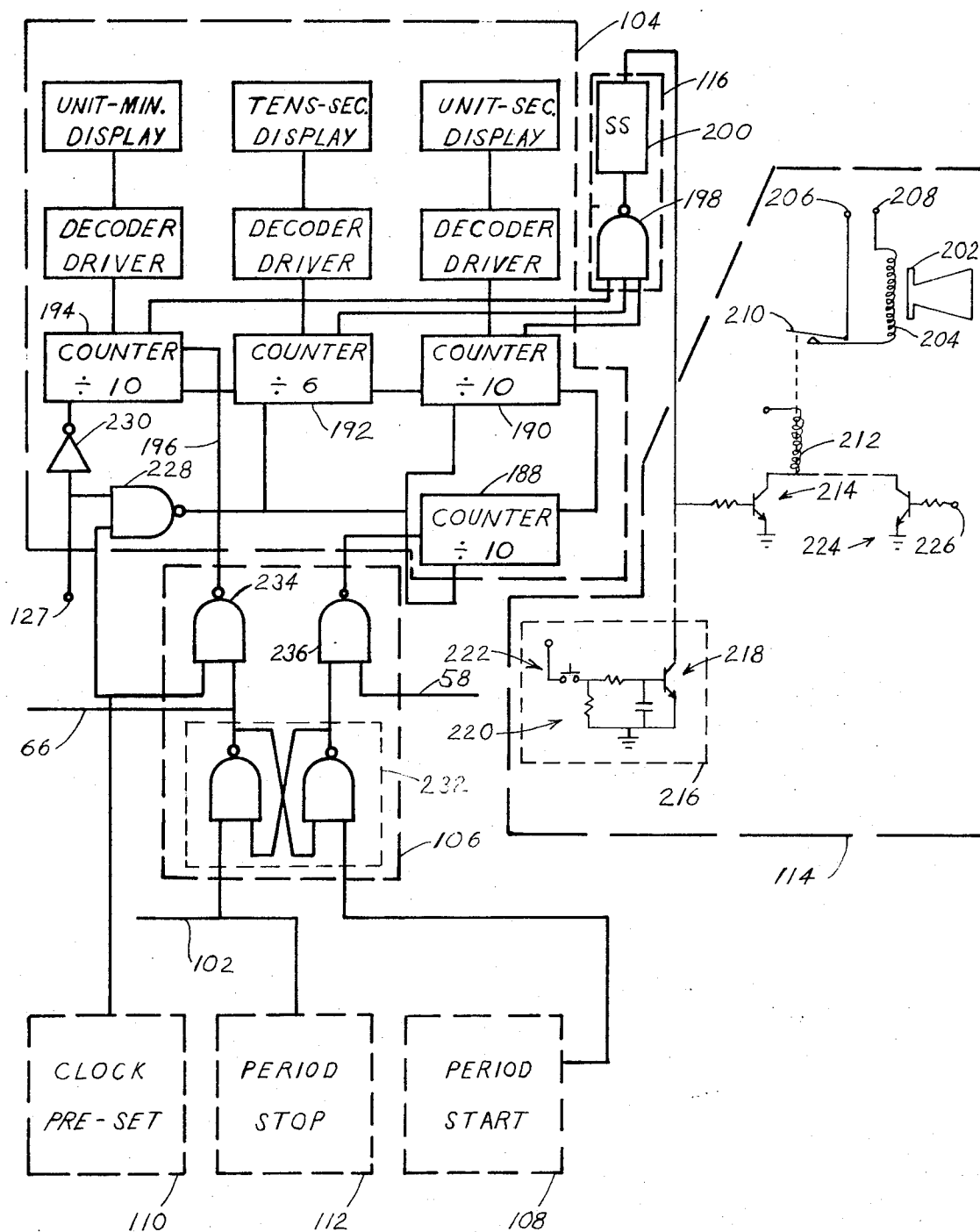


FIG. 4

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MATSIDE WRESTLING SCOREBOARD

BACKGROUND AND FIELD OF INVENTION

This invention relates in general to scoreboards and in particular to wrestling scoreboards which incorporate the feature of an advantage timer.

The sport of wrestling is literally thousands of years old. In the United States, it has enjoyed widespread popularity for many years at numerous levels, including the high school and college levels. Characteristic of the sport at all levels are the intense emotions induced in observers. As one would expect, the matches which generally generate the greatest excitement are close scoring. Frequently, such matches are decided by "riding" or "advantage" time points awarded immediately following the last period of the match, such points usually being awarded based on the net time in minutes which one of the wrestlers exercised and maintained restraining power over his opponent sufficient to control the opponent.

In many cases spectators are unable to determine whether a wrestler has in fact accrued, or can potentially earn, match deciding advantage time points. Frequently, a scorekeeper records advantage time by means of one or more hand stop watches. However in some instances, an attempt is made to provide the spectators with the advantage time information. For example, the Fair Play Scoreboard Co. of Des Moines, Ia. markets a wrestling scoreboard which includes two digital advantage time clocks. Each clock corresponds to one of the wrestlers. At the conclusion of the match, the separate advantage times are compared and appropriate points awarded to whichever, if either, wrestler has accrued a sufficient net advantage time. While such a scoreboard provides a generally satisfactory way of finally determining advantage time points, it obviously has the serious deficiency of requiring a spectator, often in a highly excited state, to mentally subtract one time from another. The problem is further compounded in those instances of a real need to know the net advantage time, towards the end of a match which could be decided by advantage time, if one of the advantage time clocks is running. Further, the Fair Play Scoreboard is designed for wall mounting which most often places the scoreboard out of the field of vision of an observer focusing on the wrestling mat. This presents the further disadvantage of forcing a spectator to take his eyes off the wrestlers in order to focus them on the scoreboard should he wish to compute the net advantage time.

Another device for indicating advantage time is marketed by the Aristo Import Co. Inc. of New York, N.Y. This Aristo timer consists of a modified clock mechanism of the rotatably driven shaft type. Instead of carrying the 12 conventional digits of the hours of the day, the clock dial begins with a zero in the 12 position and progresses with two sets of the numerals one through five in consecutive order, one set in the clockwise direction and the other in the counter-clockwise direction and concludes with a numeral six in its normal position. The mechanism for driving a minute and a second hand is drivable in both the clockwise and counter-clockwise directions. This arrangement provides a left and a right hand set of the numerals zero through six where the sets share the zero and six. The left and right hand sides of the dial are

color coded red and green and are individually backlighted. The two halves of the dial each correspond to one of the wrestlers and are selectively backlighted to indicate which of the wrestlers is currently earning advantage time. The Aristo Timer does not require the same mental calculations as the aforescribed dual-clock Fair Play Scoreboard. However, in addition to the problems inherent in any clock mechanism using rotatably driven pointers and a dial, such as inaccuracies of bent or misaligned pointers and errors from interpreting pointer position, the Aristo timer suffers from the further deficiency that determination as to which of the wrestlers has accrued net advantage time tends to be confusing. When the wrestler earning advantage time has accrued less time than his opponent, the spectator must keep in mind that the dial light indicates which wrestler is earning time and not which wrestler has accrued the most time. To ascertain this last information, the spectator must note either or both the direction of movement of the timer pointers or whether the minute pointer is in the lighted portion of the dial.

According to the present invention, the aforementioned disadvantages are eliminated. An advantage timer is provided which displays the net advantage time digitally and which indicates which of the wrestlers has accrued the display net advantage time. With the net advantage time thus displayed and an indication provided as to which of the two wrestlers has accrued the time, a spectator is fully apprised of the advantage time status with only a glance at the clock. Moreover, the invention is packageable in a multi-sided, portable, case. Packaged thusly, the scoreboard can be readily positioned at matside so that spectators can simultaneously encompass both the action on the mat and the scoreboard in their field of vision.

BRIEF DESCRIPTION OF THE INVENTION

Briefly, the present invention includes a digital clock for displaying advantage time and a pair of advantage indicators such as colored lights. The respective indicators correspond to one of a pair of wrestlers and when activated indicate that the wrestler corresponding thereto has accrued the most advantage time. Also included is a clock and indicator control. The clock and indicator control activate throughout a match the indicator corresponding to the wrestler having accrued the most advantage time and update the digital clock in favor of a wrestler earning advantage time. Updating the clock comprises incrementing and decrementing the clock whenever a wrestler earning advantage time has during the match accrued, respectively, more and less advantage time than his opponent.

In a preferred embodiment, the scoreboard is in the form of a multi-sided, portable, case. The advantage time clock is displayed from each side of the case, as are digital displays of the Period Time, Match, Match Score, and Team Score. The period time display comprises a timing device for visually displaying the time of a wrestling match period and means for starting and stopping the timing device. The period time display stopping means is also connected to stop the advantage time clock in synchronism with stopping of the period timer timing device during a period whenever the advantage time clock is running at the time a period is stopped.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a perspective view illustrating a portable wrestling scoreboard according to the present invention in situ at mat-side;

FIG. 2 is a basic logic diagram of an advantage timer and period timer of the present invention;

FIG. 3 is a partial schematic and partial detailed logic diagram of an advantage timer of FIG. 2;

FIG. 4 is a partial schematic and partial detailed logic diagram of a period timer of FIG. 2.

DETAILED DESCRIPTION

Referring now to FIG. 1, a preferred embodiment of the invention is shown to comprise a portable, three-sided wrestling scoreboard 10 adjacent a wrestling mat 12. Each side of the scoreboard 10 is shown to be a truncated triangle, one of which sides is designated 14. Each scoreboard side includes a match display 16, a grouping of four period indicators 18, a period time display 20, an advantage time display 22 and a pair of advantage indicators 24 and 26 located on opposite sides of the advantage time display 22. Also included are a match score display 28 and a team score display 30.

At this point in the description, it should be noted that the logic symbols used in the remaining figures of the drawings, and the definitions and conventions used in the descriptions thereof except as noted below, are standard graphic symbols and definitions for logic diagrams as set forth in MIL-STD-806B dated 26 Feb. 1962, copies of which may be obtained from the Dept. of Defense, Washington, D.C. 20525. A definition of the standards specifically applicable to FIG. 2 is that of a "basic" logic diagram which means a diagram in which the logic symbols depict logic relationships as simply and understandably as possible without necessarily corresponding literally to physical implementations. Specific examples of such depictions of logic relationships in preference to specific physical embodiments in FIG. 2 hereof are, for example, the noninverting logic, the OR gate 74 the exclusive OR gate 96, and the OR gate 100. The corresponding physical implementations, in a preferred embodiment, of these logic relationships are illustrated in and described with reference to FIGS. 3 and 4. Exceptions to the conventions of MIL-STD-806B are that logic flow is from bottom to top and that flip-flop outputs are referred to as "set" and "reset" outputs rather than as "1" and "0" outputs.

With reference to FIG. 2, a basic logic diagram of the combination of an advantage timer 40 and a period timer 42 according to the present invention is shown. Advantage timer 40 is shown to comprise a digital clock 44 and a pair of indicators shown as green indicator 46 and red indicator 48. Also included in advantage timer 40 is a clock and indicator control means 50. The control means 50 includes a clock control 52 which updates digital clock 44 by selectively placing signals on output "increment" lead 54 and "decrement" lead 56. As implied, the output leads 54 and 56 are designated as increment and decrement leads because of the control function which a signal on the leads exercises over updating of the digital clock. Updating of the clock is in accordance with the control signals received on clock control input leads 58, 60, 62, 64, and 66 and consists of periodically incrementing the clock when a wrestler

earning advantage time has during the match accrued more advantage time and, conversely, periodically decrementing the clock when the wrestler earning advantage time has accrued less advantage time than his opponent. The manner in which clock updating is carried out will become apparent upon consideration of the sources of control signals which are provided to clock control 52 and the clock control 52 input leads. Input lead 58 is from a source of clock pulses such as a crystal controlled oscillator. Input lead 60 indicates whether a wrestler earning advantage time has or has not accrued a net advantage time; input lead 62 indicates whether or not a wrestler is earning advantage time; input lead 64 is provided for clearing of the digital clock between the end of one and the start of the next match; and, input 66 is provided for synchronizing operation of the advantage timer 40 and period timer 42 clocks. For purposes of the present description, assume that lead 58 carries thereon a 10 Hz. frequency wave train of timing pulses wherein each pulse consists of one positive and one negative going phase. When an enabling signal is present on input 62, these timing pulses are gated to one or the other of clock control output leads 54 and 56 in accordance with the state of the increment/decrement (I/D) logic 68. The I/D logic 68 provides a signal on lead 60 of a first state, an increment state, whenever a wrestler earning advantage time has also accrued a net advantage time and provides a signal on lead 60 of a second decrement state at all other times. The I/D logic 68 consists of a pair of AND gates 70 and 72 and an OR gate 74 coupled to receive the outputs of these AND gates as its inputs and the output of which is the lead 60. The active state of AND 70 corresponds to green wrestler, both, earning advantage time and having accrued net advantage time, i.e. the increment state of I/D logic 68. Similarly, the active state of AND 72 corresponds to the increment state for red wrestler. The increment state of I/D logic 68 corresponds to both of ANDs 70 and 72 inactive. It is of no consequence that the I/D logic 68 is in a decrement state when neither wrestler is earning advantage time because passage of decrement timing pulses on decrement output lead 56 is dependent upon a signal on lead 62 representative that one of the wrestlers is earning advantage time.

From the foregoing it is apparent that two sets of conditions result in an increment state of I/D logic 68, i.e. the conditions for which AND 70 and AND 72 are active, and that one set of conditions results in a decrement state of I/D logic 68. This latter set is the conditions for which ANDs 70 and 72 are both inactive. Because of the similarity of the sets of conditions, only the set which results in an active state of AND 70 will be considered in detail. The AND 70 is shown to have a pair of inputs 76 and 78. Input 76 is coupled to receive the set output of a flip-flop (FF) 80 which indicates by the state of its outputs, when a net advantage time has been accrued, which wrestler accrued the net advantage time. The FF 80 shall hereinafter be referred to as the "net advantage time" FF. Input 78 is coupled to receive the set output of a FF 82 which when set indicates that the green wrestler is earning advantage time, hereinafter the "green-earning" FF. It is thus seen that AND gate 70 will be active whenever the green wrestler, both, has accrued net advantage time and is earning advantage time.

The set output of the green-earning FF 82 is also employed to set the net advantage time FF 80; setting, and resetting, of FF 80 is under the control of clock decode logic 84 and AND (or "coincidence") gates 86 and 88. As shown, the clock decode logic 84 receives as its input the output of digital clock 44 and has a pair of outputs, one of which is labeled not-equal-to-zero and the other of which is labeled equal-to-zero. The outputs correspond respectively to non-zero and zero clock decodes. Setting and resetting of the net advantage time FF 80 occurs only in response to zero clock decodes, i.e. only when the clock decode logic detects zero net advantage time to provide an enabling signal on lead 154 and condition AND gates 86 and 88 for activation. Whenever the clock decode logic detects that the clock is registering other than zero, it provides an enabling signal on lead 90 which is applied as one of the dual inputs to each of the red and green indicators 46 and 48 activation AND gates 92 and 94. The other input of each of gates 92 and 94 is one or the other of the set and reset outputs of the net advantage time FF 80. It is thus seen that the red and green indicators are both deactivated whenever the counter decode logic detects a zero net advantage time and are selectively activated in accordance with the net advantage time flip-flop state for non-zero clock decodes.

The clock control inputs not heretofore considered in depth are inputs 62, 64, and 66. Input 62 is inactive to prevent updating the clock whenever neither wrestler is earning advantage time. As can be seen, input 62 is derived by an exclusive OR gate 96 from the reset outputs of green-earning FF 82 and red-earning FF 98. If either one but not both of flip-flops 82 and 98 are reset, indicating that one of the wrestlers is earning advantage time, exclusive OR gate 96 is active to provide a signal on either of clock control increment and decrement output leads 54 and 56. The other condition for so passing the 10 hz. wavetrain is an active signal on clock control input 66, which active signal indicates that the period clock is running, i.e. that a match is in progress. Input 64 is for clearing the clock to zero preparatory to the beginning of a new match. As will become apparent upon consideration of the period timer 42, input 66 is inactive to inhibit updating of the advantage timer digital clock 44 each time the period clock is stopped, such as when a wrestler leaves or is forced off the mat. The remaining advantage timer 40 logic which has not been specifically discussed, other than that which is of identical function to logic previously discussed, is for resetting the red and green earning flip-flops. As explained, the condition of both the red and green earning flip-flops reset prevents updating of the clock; it is of course necessary to reset the flip-flops at the end of or prior to the start of a match and each time a wrestler loses a position of advantage without his opponent simultaneously acquiring such a position. And, there are other times when resetting of the flip-flops is optional, such as at the end of a period or when a match is momentarily stopped by a wrestler leaving the mat. Resetting on these latter occasions prevents inadvertent crediting of a wrestler with advantage time upon the start of a new period or upon resumption of the match stopped at a time when a wrestler lost his position of advantage. A single manual switch could be operated by a scorekeeper to effect resetting on each of the foregoing occasions, however,

both automatic and manual resetting of the flip-flops are illustrated in FIGS. 2 and 3. In FIG. 2, the implementation of the several reset alternatives is illustrated through the expedient of OR gate 100 which is shown to have a scorekeeper reset input 101 which permits a scorekeeper to reset a flip-flop anytime a wrestler loses his position of advantage, a period stop reset input 102 which automatically resets the flip-flops each time the period timer timing device is stopped, and a match reset input 103 for resetting the flip-flops, in addition to resetting all other circuits of the scoreboard which are not performing a cumulative function—the team score display is an example of a circuit which performs a cumulative function. Turning now to consideration of period timer 42, it is shown to comprise period clock 104 (a period timing device), period clock control 106, period start 108, clock pre-set 110, period stop 112, end of period indicator 114, and period clock decode 116.

Having thus described the logical implementation and principles underlying the advantage and period timers, their operation shall be briefly described by way of a hypothetical example. Assume that during a period of a wrestling match, green wrestler is the first of the wrestlers to gain a position of advantage. The scorekeeper sets the green earning FF 82 thereby activating one input to exclusive OR gate 96 while activating one input of AND gates 88 and 70. Because neither wrestler had previously accrued advantage time, the clock decode 84 zero output lead 154 will be active and thus both inputs of AND 88 will be active to set the net advantage time FF 80. With FF 80 set the second input of AND 70 is also active and AND 70 is active to activate the OR gate 74. With OR 74 active, input 60 is likewise active to place the clock control in an "increment mode" that is, to gate the timing pulses from input 58 through clock control 52 to digital clock 44 via increment lead 54. Further assume that the wrestlers leave the mat and in doing so the green wrestler loses his position of advantage. The scorekeeper operates the period timer period stop 112 which resets the green earning FF 82 by means of the signal on lead 102, and stops the period clock 104 by means of a signal passed to clock control 106 on lead 105. With FF 82 reset, the exclusive OR gate 96 again has both inputs active and is inactive to inhibit updating the digital clock by means of the signal on input 62. Upon restarting the period timer, the inactive output of exclusive OR 96 on input 62 prevents further updating of the clock. Throughout the foregoing, net advantage time FF 80 remains set, "remembering" that green wrestler has accrued a net advantage time. Assume now that red wrestler subsequently acquires a position of advantage which he holds for less than the time accrued by green wrestler following which first green and then red wrestler reacquire a position of advantage, and assume finally that the last time red wrestler is in a position of advantage he holds it for a time greater than the net advantage time of green wrestler. When red wrestler first begins to earn advantage time, the scorekeeper sets red earning FF 98 which activates exclusive OR gate 96 and activates input 107 of AND gate 72. The other input of AND 72, lead 109, remains inactive, however, because FF 80 resides in a set state. With period timer 42 providing an active signal on clock control input 66,

and with both the ANDs 70 and 72 of the increment/decrement logic 68 inactive, the similarly inactive OR 74 and clock control input 60 causes the timing pulses on input 58 to be gated to the digital clock via decrement lead 56 to periodically decrement the clock until red wrestler loses his position of advantage at which time green wrestler reacquires a position of advantage. With the resultant setting of green-earning FF 82, both it and net advantage FF 80 are set which again activates AND gate 70 to in turn activate OR 74 which causes the digital clock to again be operated in the increment mode. When red wrestler finally reacquires a position of advantage, operation is as described before for red wrestler earning advantage time until the digital clock 44 has been decremented to zero. At that time, clock decode 84 provides an equal-to-zero output on lead 154 and the AND 86 becomes active to reset net advantage FF 80. With FF 80 reset, AND 72 becomes active to activate OR gate 74 and again place the clock in the increment mode. This time, however, the clock is incremented in favor of red wrestler as indicated by red indicator 48 which is activated by AND 92 on the first update of the clock as clock decode 84 goes from a zero to a non-zero output.

A detailed logic diagram and partial schematic circuit diagram of advantage timer 40 is shown in FIG. 3. In the preferred embodiment illustrated therein, positive NAND logic is used exclusively. FIG. 3 includes logic not illustrated in FIG. 2, such as the operator actuable switches for setting and resetting the red and green earning flip-flops 82 and 98 and for clearing the digital clock. These switches are identified by reference numbers, 111, 113, 115, and 117, the red-earning set, green-earning set, red and green earning reset, and the match reset switches respectively. The switches are identical and thus only one, red-earning set switch 111, is shown in detail. Switch 111 is shown to comprise a normally open momentary action switch 118 coupled between a source of positive electrical potential (not shown) by terminal 120 to the common ends of a pair of resistors 122 and 124. The other end of resistor 122 and the base of an NPN transistor 126 and a capacitor 128 are common as are the other ends of resistor 124 and capacitor 128 and the emitter of transistor 126. With the collector of transistor 126 connected to the positive potential by terminal 120, and with the switch 118 normally open, transistor 126 is normally "off", i.e. non-conducting. When the switch 118 is momentarily closed, current flows from the source of positive potential to the network of resistors 122, 124 and capacitor 128 to store a charge in capacitor 128. The charge forward biases transistor 126 causing it to turn "on", i.e. conduct. Transistor 126 continues to conduct for as long as switch 118 is closed and for a slight period thereafter until the charge stored in capacitor 128 drains off through resistors 122 and 124 to ground. It is thus seen that the signal state on output lead 130 is normally high but switches to low when transistor 126 conducts. The output of transistor 126 is carried via lead 130 to the set input of red-earning FF 98 and to a reset input of green-earning FF 82. The switch action and the states of the signals on the output leads of each of switches 113, 115 and 117, is as described for switch 111. However, match reset switch 117 initiates an additional function, namely clearing of the advantage timer

and period timer clocks. Upon actuation of switch 117, its low output signal is coupled to the match reset circuit 119, specifically to the base of an NPN transistor 121 therein. Transistor 121 is normally conducting. Inverters 123 and 125 invert the normally low output of transistor 121 to hold high the clear inputs of counter stages 164, 166, 168 and 170. (Terminal 127 provides for a similar connection of the output of transistor 121 to the counter stages of the period timing device, not shown.) Actuation of switch 117 switches transistor 121 off to couple a low signal to the counter stage clear inputs and thereby clear the counter stages. Actuation of switch 117 also couples a signal through OR 100 to a reset input of each of flip-flops 82 and 98. The other two inputs to OR 100 which serve to reset flip-flops 82 and 98 are input 101 from the red and green reset switch 115 and input 102 from the period timer 42 period stop switch 112.

Also shown in FIG. 3 is an optional counter pre-set circuit 129 by which the advantage time clock 44 can be preset to a predetermined count for use in timing sporting events in which it is desirable to decrement a preset count to zero, e.g. basketball. The circuit consists simply of NAND 131 and inverter 133. The NAND 131 functions as an OR gate to provide an alternate path for introducing a count-up or increment signal into the fourth counter stage 170. The input terminal 135 of the circuit 129 is connected to the clear input lead 137 by lead 139 to provide an alternate source for clear signals for the first, second, and third stages 164, 166, and 168. To preset the counter fourth stage 170, and appropriate number of signal pulses are provided to terminal 135. These pulses cause the NAND 131 output to go high which high output when inverted by inverter 133 stores a count in fourth stage 170. Each pulse is also coupled to clear input lead 137 by lead 139 to clear each of stages 164, 166, and 168.

As an illustration of the action resulting from operation of a switch 111-117, assume the red and green earning flip-flops are both in the reset state. In the reset states, the FF internal NAND gate on the set side of the FF is in an active state and therefore the FF set output is a low signal; the reset output and reset side NAND gate signals are, of course, complements of their set counterparts. The set outputs of the red and green earning flip-flops are respectively connected to the reset and set input gates of the net advantage time FF 80; the reset output of both earning flip-flops each form an input of the exclusive OR 96 which for the illustrated embodiment is conveniently formed from a single NAND gate 95. Because the set side input of FF 82 and the set side input of FF 98 are each coupled as a reset side input of the other FF, both flip-flops are never simultaneously in the set state and thus the NAND gate 95 can be employed in place of an exclusive OR gate. The output of NAND 95 is tied to ground by a capacitor 97. Whenever the output of NAND gate 95 changes states, capacitor 97 delays the appearance of the change of state on lead 62 at NAND 156 and thus also at NANDs 159 and 160. Consequently, whenever an event changes the states of both leads 60 and 62, the changes do not occur simultaneously at clock control 52 to prevent erroneous outputs from NANDs 159 and 160, and hence from increment and decrement output leads 54 and 56. As previously explained,

the output of exclusive OR 96 indicates whether either wrestler is earning advantage time. The output of exclusive OR 96 is coupled by lead 62 to clock control 52 where it is applied to a NAND 156. The other inputs to NAND 156 are lead 58 (a 10 hz. wavetrain of timing pulses) and lead 66 from the period timer 42, which lead 66 provides for synchronous operation of the period timer 42 and advantage timer 40 clocks. The NAND 156 output is applied through an inverter 158 to one input of each of NANDs 159 and 160 the outputs of which are the clock control 52 output leads, increment lead 54 and decrement lead 56, respectively. Control lead 62 directly provides the other input of NAND 159 and indirectly, via the inverter 162, provides the other input of NAND 160. It can thus be seen that when either one of the earning flip-flops are set, one input to exclusive OR 96 is high and the other is low so that the high output of the NAND 95 thereof, when coupled by lead 62 to the NAND 156 of clock control 52, satisfies one of the conditions for enabling NAND 156.

The remainder of this discussion illustrating the operation of a switch shall be made with reference to the events resulting from operation of switch 111. Upon depression of momentary action switch 118 of the switch 111, the output signal on lead 130 goes from a high to a low level. This low signal at the set input 132 of FF 98 inactivates internal set NAND 134 to provide a high signal on set output lead 136 and to cross couple a high signal to the internal reset NAND 138 whereupon reset NAND 138 has both inputs high to produce a low output signal which is coupled to one input of the NAND 95 of exclusive OR 96. The NAND 95 then has only one input high to provide a high or "active" input on lead 62 to clock control 52. The other output from FF 98, set output lead 136, is one input of NAND 72 of the I/D logic 68 and one input of the reset input gate 86 of net advantage FF 80. The other input to gate 86 is the clock decode 84 zero output lead 154. With FF 98 set, one input to NAND 72 of the I/D logic 68 is active, and activation of NAND 86 and resetting of net advantage FF 80 follows upon occurrence of a zero clock decode.

The resetting of FF 80 will also activate the input 109 to NAND 72 the other input of which, 107, was activated by the setting of FF 98. The active state of NAND 72 in turn deactivates OR gate 74, shown in FIG. 3 to be implemented by means of a NAND 75, to provide a high or increment signal on lead 60. With lead 60 high, clock control 52 conditions digital clock 44 for operation in the increment mode as follows. The high signal of lead 60 is applied to one input of NAND 159 and to inverter 162. It was previously stated that input lead 62 was active, and thus NAND 156 toggles between its active and inactive states in synchronism with the timing pulse positive and negative going phases to provide a 10 hz. output. The positive going phases of the NAND 156 output activate one input of each of NANDs 159 and 160. The other input to NAND 159 is lead 60 which under the present assumed conditions is continuously active or high. Accordingly, NAND 159 is enabled and disabled by the NAND 156 output positive going and negative going phases respectively to provide timing pulses to clock 44 via increment lead 54. Conversely, the high input of lead 60 is

inverted by inverter 162 to continuously disable NAND 160 and prevent passage of timing pulses to clock 44 via decrement lead 56. From the foregoing it is thus apparent that conditioning the clock to operate in its other updating mode, the decrementing mode of operation, requires an inactive state of the NAND 75 of the I/D logic 68 to deactivate NAND 159 but to condition NAND 160 for passage of the timing pulse wavetrain on decrement output lead 56.

Considering now the sequence of events following resetting of FF 80, after flip-flop 80 is reset, NAND 92 is activated on the first update of clock 44 by a non-zero output on lead 90 from clock decode 84. With NAND 92 active, red indicator 48 is activated in the following manner. Inverter 142 provides a high output signal to the base of NPN transistor 144 which switches from a non-conducting to a conducting state. With transistor 144 conducting, current is drawn from a source of positive potential (not shown) coupled to terminal 146 through the filament of a lamp 148 to illuminate the lamp and give an indication that red wrestler has accrued a net advantage time.

Returning now to consideration of the balance of the logic illustrated in FIG. 3, clock decode 84 comprises simply a NAND gate 150 which provides the non-zero decode output signal on lead 90 and an inverter 152 which provides a zero decode output signal on lead 154.

Digital clock 44 is shown to comprise first, second, third, and fourth counter stages 164, 166, 168, and 170. The stages are connected in serial. The carry and borrow leads of stages 164, 166, and 168 are coupled to the count up (CUP) and count down (CDN) leads of stages 166, 168 and 170. For example, the first stage 164 carry and borrow leads 172 and 174 are also the CUP and CDN leads, respectively, of second stage 166. The first stage 164 is a divide by 10 counter which in response to a 10 hz. wavetrain of timing pulses at either its CUP or CDN inputs (increment lead 54 and decrement lead 56, respectively) provides a 1 hz. wavetrain of count signals on either its carry output lead 172 or its borrow output lead 174. Second stage 166 (a unit seconds counter stage) is a divide by 10 counter which converts a one count per second input of count signals from the first stage to a one count per 10 seconds output; third stage counter 168 (a tens seconds counter stage) is a divide by six counter responsive to the second stage counter to provide an output of one count per minute; and fourth stage counter 170 (a unit minutes counter stage) is a divide by 10 counter which is responsive to the third stage counter 168. Each of stages 166-170 also provide binary coded decimal outputs representative of the clock count to one of decoder drivers 176, 178, and 180. Stage 166 provides a representation of the unit-seconds digit, stage 168 a representation of the tens-seconds digit, and stage 170 a representation of the unit-minutes digit. Each of decoder drivers 176-180 is in turn coupled to a digital display 182, 184, and 186.

The principal circuits of FIG. 3 and their functions are briefly summarized below. Both the combination of switch 111 and set-reset FF register 98 and the combination of switch 113 and set-reset FF register 82 provide respective indications that the wrestler corresponding thereto is earning and not earning ad-

vantage time, each combination indicating that the corresponding wrestler is earning advantage time when the FF is set by operation of the switch and indicating that the corresponding wrestler is not earning advantage time when the FF is reset. The clock decode circuit 84, when the digital clock 44 count is equal-to-zero, provides an indication on lead 154 that neither wrestler has accrued a net advantage time, and, when the count is not-equal-to-zero, provides an indication on lead 154 that a wrestler, either, is earning or has accrued a net advantage time. The outputs of net advantage set-reset FF register 80 provide, when a net advantage time has been accrued, an indication of which wrestler accrued the net advantage time. Setting and resetting of FF 80 occurs only when clock decode 84 is indicating that neither wrestler has accrued a net advantage time and is in accordance with the indications of the switch-FF combinations. The indications provided by the switch-FF combinations and by the net advantage FF supply the increment/decrement logic 68 with the data necessary to in turn provide an indication on lead 60 that a wrestler earning advantage time has or has not accrued a net advantage time, i.e. an indication as to whether the clock should be incremented or decremented. This latter indication on lead 60 and an indication on lead 62 from the NAND 95 indicating that either one or neither of the wrestlers is earning advantage time are applied to clock control 52. Clock control 52 is coupled to receive a wavetrain of timing pulses by lead 58 and is responsive to an indication that a wrestler is earning advantage time on lead 62 to update the digital clock in either an increment or decrement mode in accordance with the indication on lead 60. One or the other of red indicator 48 and green indicator 46 are selectively activated in accordance with the state of net advantage FF 80 whenever lead 90 indicates a net advantage time has been accrued.

FIG. 4 is a detailed logic and circuit schematic drawing of the period timer 42 of FIG. 2. The period clock 104 is identical to the digital clock of the advantage timer 40 except for the interconnection of the first four stages, which stages are identified by reference numerals 188, 190, 192 and 194. The embodiment shown, is a count down only clock. Consequently, the carry and CUP leads of the stages are not interconnected as in the advantage timer. A predetermined time, in minutes, is preset into fourth stage 194 via lead 196. Only the CDN and borrow leads of successive stages are interconnected and the 10 hz. wavetrain from the period clock control 106 is applied only to the CDN input of first stage 188. A count down clock has advantages for wrestling matches having periods of different lengths; one advantage being that an alarm for signaling the end of a period can be conveniently actuated automatically. With a count down clock, the end of each period always occurs at the same point in the clock count regardless of the period length, namely, when the clock count reaches zero. The clock decode 116 is therefore simply a NAND 198 and a single-shot 200 which is activated when the zero decode output of each of the second, third and fourth stages 190-194 is a zero. Single-shot 200 is provided to limit the time of actuation of the alarm which is shown to be horn 202 the sound coil 204 of which is coupled to a source of A-C energy (not shown) applied across terminals 206 and

208 upon pull-in of relay contact 210 by flow of current through relay coil 212 in response to conduction of NPN transistor 214. The end of period circuit 114 also includes a horn disable 216 which is an optional feature provided for instances in which the horn is not to be actuated automatically such as in a tournament when several other matches are in process simultaneously with the result that an audible sound signaling the end of a match could be confusing. The horn disable illustrated is merely a current sink in the form of an NPN transistor 218 with a resistor capacitor network 220 and a toggle switch 222. When switch 222 is operated, transistor 218 conducts to sink a signal produced by single-shot 200 at the end of the match to prevent actuation of the horn. The NPN transistor 224 facilitates manual operation of the horn. Upon application of a positive potential to the terminal 226 by operation of a switch (not shown), transistor 224 will conduct to enable the horn in the same manner as just described with reference to transistor 214.

The balance of period timer 42 comprises period start switch 108, period stop switch 112, a pre-set period time switch 110, and period clock control 106. Switches 108, 110 and 112 may be identical to each other and may be identical to the switch 111 which was illustrated in detail in and described with reference to FIG. 3, consequently, none of the switches 108, 110 and 112 are shown or described in detail. Clock control 106 is shown to comprise a FF 232 the set state of which corresponds to a period in progress and the reset state of which corresponds to a period not in progress. A pair of dual input NAND gates 234 and 236 respectively have one of their inputs coupled to the reset and set outputs of FF 232. The other input of NAND 236 is coupled by lead 58 to receive the 10 hz. wavetrain of timing pulses; NAND 234 has its other input coupled to clock pre-set 110. The NAND gate 234 limits presetting of the minute digit (counter fourth stage 194) to when a period is not in progress; NAND 236 limits updating of the clock to when a period is in progress.

Clearing of the period timer 42 counter stages 188, 190, 192, and 194 is carried out in the same manner as was described with reference to the advantage timer 40 counter stages. Alternate sources of a clear signal, match reset circuit 119 (not shown) and clock pre-set circuit 110, are coupled through a NAND gate 228 to the clear inputs of the counter first, second, and third stages. The counter fourth stage is coupled through an inverter 230 by terminal 127 to only the match reset circuit 119.

It will be readily appreciated that each of a match display, a match score display and a team score display could readily be constructed using the period clock with only slight modification. Each of the second and third stages 190 and 192 would be modified to include a pre-set input like the pre-set input of the period timer fourth stages 194. The borrow and CDN inputs of the stages 190, 192 and 194 would not be interconnected and the first stage 188 could be entirely eliminated. Each stage would therefore be independent of the other stages and would be controlled by a manual switch such as the switch 111 described with reference to FIG. 3. It will be further appreciated that indicators, such as the period indicators illustrated on the

scoreboard shown in FIG. 1, could be readily provided using an arrangement such as red indicator 48 circuitry illustrated in and described with reference to FIGS. 2 and 3 with only slight, if any, modification thereof. The indicator could be controlled by any of a variety of on-off manually operated switches including a switch which latches upon actuation.

The foregoing described detailed logic arrangement of FIGS. 3 and 4 and the above referred to modifications thereof will readily permit construction of a scoreboard as illustrated in FIG. 1. Such a scoreboard is lightweight and small enough to be readily portable to permit positioning of the scoreboard adjacent the wrestling mat in full view of one watching a match. In one embodiment of a scoreboard constructed according to FIGS. 3 and 4 hereof, the NAND, flip-flop, and inverter logic were Texas Instrument (TM) integrated circuits. The two input NAND gates were integrated circuit (IC) type number 7400; the three input NAND gates, type 7410; and the inverters were type 7404. The three divide by 10 counters and the single divide by six counter were Texas Instrument IC type SN 74192 synchronous 4-bit up/down counters.

While particular embodiments of the invention have been illustrated and described, modifications thereof will occur to those skilled in the art and, therefore, the appended claims contemplate such modifications as come within the true spirit and scope of the invention.

What is claimed is:

1. A wrestling scoreboard for indicating the net advantage time accrued by one of a pair of wrestlers, comprising:

- a digital clock for displaying advantage time;
- a pair of indicators, respective ones of which correspond to one of a pair of wrestlers and indicate when activated that the wrestler corresponding thereto has accrued a net advantage time; and
- clock and indicator control means for updating the digital clock in favor of a wrestler earning advantage time to increment the clock whenever a wrestler earning advantage time has during the wrestling match accrued more advantage time and, conversely, to decrement the clock whenever the wrestler earning advantage time has accrued less advantage time than his opponent to cause the clock to display net advantage time, and for activating throughout a match the indicator which corresponds to the wrestler having accrued a net advantage time.

2. A wrestling scoreboard according to claim 1 wherein the clock and indicator control means includes:

- a first means for providing for each of the wrestlers respective indications of the wrestler earning and not earning advantage time;
- a second means for providing respective indications that neither wrestler has accrued a net advantage time, and that a wrestler, either, is earning or has accrued a net advantage time;
- a third means which, when a net advantage time has been accrued, provides an indication as to which of the wrestlers has accrued the net advantage time;
- a fourth means for providing respective indications that a wrestler earning advantage time has and has not accrued a net advantage time;

a fifth means responsive to indications of said second and third means for selectively activating said pair of indicators;

a sixth means responsive to the first means to provide respective indications that one of the wrestlers is earning advantage time and that neither of the wrestlers is earning advantage time; and

a clock control means responsive to an indication of the sixth means that a wrestler is earning advantage time to update the digital clock in either an increment or a decrement mode in accordance with the indication of the fourth means and is responsive to an indication of the sixth means that neither wrestler is earning advantage time to inhibit updating of the clock.

3. A wrestling scoreboard according to claim 2 further comprising a period timer which includes both a timing device for visually displaying the time of a wrestling match period and a means for starting and stopping the timing device and for stopping the advantage time digital clock in synchronism with stopping the period timer timing device during a period whenever said digital clock is running at the time the timing device is stopped.

4. A wrestling scoreboard according to claim 3 further comprising match reset means for resetting the advantage time digital clock to prepare the advantage timer for the beginning of a new match.

5. A wrestling scoreboard according to claim 2 wherein the digital clock comprises:

- an increment-decrement counter for producing an output set of binary-coded decimal signals representative of time, which counter is responsive to a timing pulse to update the counter output in response to an indication from said sixth means of one of the wrestlers earning advantage time and in accordance with an indication from the fourth means that a said wrestler has or has not accrued a net advantage time to increment and decrement the clock output count.

6. A wrestling scoreboard according to claim 5 wherein the increment-decrement counter comprises:

- a unit seconds counter stage, tens seconds counter stage and a unit minutes counter stage, each of which counter stages has a set of data outputs for providing a digital representation of the count of the stage and each of which counter stages has a count up input, a count down input, a carry output and a borrow output, which unit minutes stage count up and count down inputs are coupled to the tens seconds count stage carry and borrow outputs respectively and which tens seconds count stage count up and count down inputs are respectively coupled to the unit seconds stage counter carry and borrow outputs; and,

means for providing count signals to either the unit seconds stage counter count up or count down inputs according to said fourth means.

7. A wrestling scoreboard according to claim 2 wherein:

- the first means comprises an operator actuable switch and a set-reset register for each wrestler, a said switch when actuated producing an output signal which is stored in a said register and which is representative that the wrestler corresponding thereto is earning advantage time, which registers

have their set inputs cross coupled to the reset input of the other register so that only one of the registers is in a set state at any given time;

the second means comprises a clock decode circuit for decoding the digital clock to provide an indication that a wrestler is earning or has accrued a net advantage time for a clock decode not-equal-to-zero and to provide an indication that neither wrestler has accrued a net advantage time for a clock decode equal to zero;

the third means comprises a net advantage time register which in response to an indication from the first means of a clock decode equal-to-zero, either, resides in a set state for an output from the first means representative that one of the first means registers is in a set state, or resides in a reset state for a first means output representative that the other first means register is in a set state;

the fourth means comprises a pair of dual input coincidence gates and an OR gate, each of which coincidence gates has one input coupled to an output of the net advantage time register and its other input coupled to the set output of one of the first means registers, and both of which coincidence gates have their outputs connected to the OR gate inputs, whereby, both, when neither wrestler is earning advantage time and when one wrestler both is earning but has not accrued a net advantage time, the coincidence gates and the OR gate each reside in a first state, but when one of the wrestlers, both, is earning and has accrued a net advantage time, one of the coincidence gates resides in a second state and causes the OR gate to reside in a second state;

the fifth means comprises a pair of dual input coincidence gates each of which has one input which is coupled to the clock decode means and which input is in an active state when the clock decode is not equal to zero, one of which coincidence gates has its other input connected to the reset output of the net advantage time register, and the other of which coincidence gates has its other input connected to the set output of the net advantage time register whereby when the clock decode is not equal to zero one or the other of the coincidence gates is in an active state in accordance with the state of the net advantage time register to activate the indicator associated with the active coincidence gate; and

the sixth means comprises an OR gate connected to like outputs of the first means registers to provide an output indicative that a wrestler is earning advantage time when the states of said like outputs are not the same and for providing an indication that neither of the wrestlers is earning advantage time when the state of said like outputs are the same.

8. A wrestling scoreboard according to claim 7 wherein the clock control means comprises:

means adapted to receive a wavetrain of timing pulses and, in response to an indication from the sixth means of a wrestler earning advantage time, selectively passes said timing pulses on either an increment or a decrement output lead in accordance with an indication from the fourth means that the

wrestler earning advantage time has or has not accrued a net advantage time; and wherein the digital clock comprises:

an increment-decrement counter for producing an output set of binary-coded-decimal signals representative of advantage time in response to count signals, which counter has a count up input and a count down input coupled to receive timing pulses from the clock control increment and decrement output leads respectively as count signals.

9. A wrestling scoreboard according to claim 8 wherein the digital clock comprises:

a unit seconds counter stage, a tens seconds counter stage and a unit minutes counter stage, each of which counter stages has a set of data outputs for providing a digital representation of the count of the stage and each of which counter stages has a count up input, a count down input, a carry output and a borrow output, which unit minutes stage count up and count down inputs are coupled to the tens seconds count stage carry and borrow outputs respectively and which tens seconds count stage count up and count down inputs are respectively coupled to the unit seconds stage counter carry and borrow outputs; and, wherein the clock control means comprises:

an input gate, which input gate is a coincidence gate having one input coupled to receive a wavetrain of timing pulses and having another input coupled to said sixth means whereby said input gate passes timing pulses on its output in response to an indication from the sixth means of a wrestler earning advantage time; and

a pair of output gates the respective outputs of which are the clock control increment and decrement output leads, which output gates are each dual input coincidence gates, which output gates each have one input coupled to the output of said input gate and the other of its inputs coupled to the fourth means, and which other inputs are respectively active in response to an indication from the fourth means that a wrestler has and to an indication that neither wrestler has accrued a net advantage time.

10. A wrestling scoreboard according to claim 9 further comprising:

a digital match score display, a digital match display, and a digital team score display, each of which displays include a counter stage for each digit of the display; and,

wherein the match reset means includes means for clearing each advantage time register, each advantage time clock counter stage, and each period timer timing device counter stage, and includes means for clearing each match score display.

11. A wrestling scoreboard according to claim 10 further comprising a pre-set circuit for presetting the advantage time clock to a predetermined count.

12. A wrestling scoreboard according to claim 11 wherein the pre-set circuit comprises means for coupling a count up signal to the unit minutes counter stage and a clear signal to the unit and tens seconds stages.

13. A method of visually indicating which of two wrestlers has accrued a net advantage time comprising:

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providing a digital clock for displaying net advantage time;
 providing visual indicator means for indicating which of the wrestlers has accrued a net advantage time displayed on the digital clock;
 updating the digital clock in favor of a wrestler earning advantage time by incrementing the clock whenever the wrestler earning advantage time has

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during a match accrued more advantage time than his opponent and, conversely, by decrementing the digital clock whenever the wrestler earning advantage time has accrued less advantage time than his opponent; and
 controlling the indicator means to indicate which wrestler has accrued a net advantage time.

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