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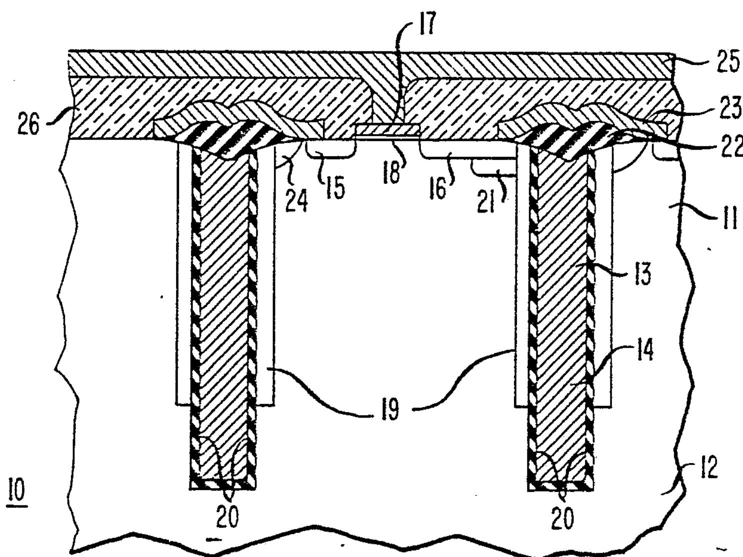
(54) Title: SILICON INTEGRATED CIRCUITS

(57) Abstract

A semiconductor integrated circuit such as a dynamic RAM is formed in mesas (11) formed by grooves (13) in the surface of a semiconductor body. Capacitors are formed between conductive layers (19) on the mesa sidewalls and a conductive filling (14) in the grooves. The filling may be of polycrystalline semiconductor and is separated from the semiconductor body by a layer of dielectric material (20). Since the capacitors extend into the semiconductor body their lateral extent for a given effective plate area is reduced. In the RAM example each mesa constitutes a cell and each access transistor (15, 16, 17, 18) is formed in the top surface of the respective mesa. A similar arrangement, with the grooves filled with polycrystalline semiconductor preferably of high resistivity, can be used to obtain lateral isolation between mesas avoiding the thermal mismatch problems associated with dielectric-filled grooves.



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SILICON INTEGRATED CIRCUITS

Background of the Invention

This invention relates to silicon devices and
5 more particularly to silicon integrated circuits. Typical of such circuits are dynamic random access memories of the kind which utilize an array of memory cells, each of which includes an access or gating transistor for controlling the charging and discharging of a series-connected storage
10 capacitor.

It will be convenient to describe the invention with particular reference to such a dynamic RAM, although the invention in its broader aspects is not limited to such devices.

15 In memory technology, the emphasis is on increasing the number of memory cells that can be included on a single chip. To this end, it is important to minimize the surface area required of a memory cell since the surface area available on the chip for the memory array
20 currently is a limiting factor in the total number of cells that can be included in one chip. Presently the preferred cell from the standpoint of minimum area is the one-transistor, one-capacitor cell. In such a cell, the capacitor normally has been a surface device and its
25 capacitance is determined by the amount of surface area it is permitted to occupy. A characteristic of dynamic RAMs of this type is that the amount of signal charge that can be stored and later read out is a function of the capacitance of the storage capacitor, and accordingly the
30 larger the capacitance the more easily is the signal detected. Additionally, for a high signal-to-noise ratio it is also important that the storage capacitance be large compared to the parasitic capacitance of the sense lines. For these reasons, it is generally advantageous to have as
35 large a storage capacitance as size considerations permit.

To increase the storage capacitance, there have been proposed in the past memory cells in which the storage capacitor is buried under an access transistor of the V-MOS type to facilitate interconnection, but these cells have proven difficult to fabricate reliably in the densities needed to be competitive with available technology.

Summary of the Invention

According to the first of the present inventions there is provided a semiconductor integrated circuit comprising a semiconductor body having a major surface with grooves therein which define a plurality of mesas, each of the said mesas having at least one circuit component formed therein and a conductive layer in the side wall thereof, the grooves being filled with a conductive material which is separated from the body by a layer of dielectric material. With this invention a capacitance is formed between the conductive layer in the sidewall of each mesa and the conductive material filling the grooves. By thus making capacitors which extend into the semiconductor body the lateral area occupied by the capacitors for a given effective plate area is reduced.

According to the second of the present inventions there is provided a semiconductor integrated circuit comprising a semiconductor body having a major surface with grooves therein which define a plurality of mesas, each of the said mesas having at least one circuit component formed therein, the grooves being filled with a polycrystalline form of the semiconductor which constitutes the body. The polycrystalline semiconductor may be of high resistivity or separated from the body by a layer of insulating material or both to provide a high degree of lateral isolation of the mesas without the problems due to thermal mismatch in known integrated circuits in which grooves separating mesas are filled with dielectric material.

Brief Description of the Drawing

FIG. 1 is a schematic circuit of a conventional two-by-two array of memory cells useful in the description

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of the invention;

FIG. 2 is a schematic cross-sectional view of a portion of memory cell array in accordance with one embodiment of the invention;

5 FIG. 3 is a schematic perspective view of a portion of the embodiment of FIG. 2;

FIGS. 4 through 13 show various stages in an illustrative process for fabricating a memory cell array of the kind shown in FIG. 2; and

10 FIG. 14 is a schematic cross-sectional view of a portion of a chip useful for incorporating a plurality of bipolar circuits in accordance with another embodiment of the invention.

It will not be convenient for the drawing to be 15 to scale because of the small dimensions involved in some of the elements.

Detailed Description

In FIG. 1 there is shown schematically a memory of the kind to which the invention is applicable. It 20 comprises simply a two-dimensional matrix of four cells of which 1A and 1B form the two access transistors of one row, 2A and 2B the transistors of another, and 1A and 2A form one column and 1B and 2B form the other. Although the roles will reverse during operating, it will be convenient 25 to refer to the transistor electrodes connected to the bit lines as the sources. Accordingly, the sources of 1A and 2A are connected to a common bit or sense line 3A, and the sources of 1B and 2B to a common bit or sense line 3B. The gates of 1A and 1B are coupled to a common word line 4A, 30 and the gates of 2A and 2B to a common word line 4B. Serially connected between the drains of the access transistors, 1A, 1B, 2A and 2B and a point of reference potential, shown as ground, are the storage capacitors, 5, 6, 7, and 8, respectively. A parasitic capacitance C_S is 35 shown associated with each bit line. Normally the memory would include a much larger number of cells.

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Advantageously, in a memory of this kind, for a large signal it is important to have a large value of storage capacitance. For a good signal-to-noise ratio it is important that the storage capacitance be large compared
5 to the parasitic capacitance C_S. The operation of a memory of this kind is well known.

FIGS. 2 and 3 show a portion of the memory cell array 10 at a stage almost ready for packaging. It comprises a monocrystalline p-type silicon chip whose top
10 surface is grooved to provide a two-dimensional array in rows and columns of individual mesas 11, typically rectangular in cross-section, sharing a common support portion 12.

It is to be understood that as used herein the
15 term "silicon chip" includes both a thick monocrystalline silicon wafer which is self-supporting, and an epitaxial silicon layer grown either on a suitable conductive base which may be silicon or on a suitable insulating base which may be sapphire.

20 Each mesa houses an individual cell comprising its own access N-MOS transistor and storage capacitor. The individual mesas are separated by the grooves 13 which are filled with conductive polycrystalline silicon 14 to maintain an essentially planar top surface to facilitate
25 the desired interconnection of the cells by patterned metallization of the top surface. Each access transistor comprises a source and a drain formed by spaced localized n-type surface regions 15 and 16, respectively, and a gate electrode 17 spaced from the silicon surface by the gate
30 insulator 18, typically of silicon dioxide. Each storage capacitor comprises one plate formed by an n-type diffused layer 19 which preferably extends in a closed path completely around the sidewall of the groove and the other plate formed by the polycrystalline silicon filling 14 of
35 its surrounding groove. The p-n junction formed between the surface layer and the bulk of the mesa isolates the layer from the bulk. In some instances it may prove

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desirable to maintain the bulk at a fixed negative potential. A dielectric layer 20, typically of silicon dioxide, which coats the groove and provides d-c isolation between the filling 14 and the monocrystalline silicon of 5 the mesa, serves as the capacitor dielectric. As best seen in FIG. 3, the various polycrystalline silicon fillings are all interconnected and these are maintained at a common reference potential, typically ground. This ground connection advantageously is made outside of the memory 10 area at the periphery of the chip and need not be made to individual fillings. To ensure isolation between the storage capacitors, the n-type layers 19 do not extend the full depth of the grooves so that each is limited to a single mesa. Advantageously in each mesa, a highly doped 15 n-type region 21 is included to provide a low resistance connection between the drain region 16 and the storage electrode plate region 19. Additionally, a chanstop 24, which is a more heavily doped p-type zone, is included at the source end of the mesa.

20 Each filled groove includes thereover a relatively thick dielectric layer 22, typically of silicon dioxide. Over these layers run the bit lines 23 which make low resistance connection to the source region 15, and which run the length of the array, normal to the plane of 25 FIG. 2 as seen in FIG. 3 interconnecting all the sources of the access transistors in a common column. These bit lines are advantageously of polycrystalline silicon treated to be highly conductive. This treatment comprises high doping, and optionally also overlaying a metal layer, as for 30 example, of tantalum or titanium, and sintering to form a silicide.

Also overlaying the top surface of the chip will be the word lines 25 running parallel to the plane of the paper in FIG. 2 as seen in FIG. 3. These word lines 35 typically comprise an aluminum layer, and cross over the bit lines, electrically isolated therefrom by a dielectric layer 26, typically phosphosilicate glass, which is

appropriately apertured to permit an individual word line to make connection to the gate electrode of each of the access transistors in a common row, as is well known in the art.

5 With a memory cell of the kind described, the size of the storage capacitance will be dependent on the properties of the capacitor dielectric and the surface area of the capacitor plates. These can be adjusted to provide the desired value of capacitance with little effect on the 10 area of the top surface of the chip. Moreover, because the bit line which is used as the sense line runs over the insulating layer on the top of the grooves, its parasitic capacitance may be kept low, which is desirable for a high signal-to-noise ratio.

15 This design also permits a large value of storage capacitance because of the relatively large area of the capacitor, which area is the product of the circumference of the mesa and the height of the n-type layers 19. This distance can be readily increased if desired without 20 increasing the surface area required of an individual cell by increasing the depth of the grooves.

For forming an array of memory cells of the kind shown in FIGS. 1 and 2, illustratively there is first prepared a slice of monocrystalline silicon in which many 25 chips, each housing the desired array of memory cells, are to be formed simultaneously. The slice may be either uniformly of relatively high p-type resistivity or else have a support portion of relatively low resistivity on which has been grown an epitaxial layer of relatively high 30 resistivity within which the access transistor is to be formed. In either case the slice is provided with a surface portion at least several microns thick in which the predominant significant impurity has a concentration of, for example, between 10^{15} and 5×10^{15} acceptor atoms per 35 cubic centimeter. There is then formed over this surface portion a layer of silicon dioxide illustratively about 300 Angstroms thick. This is best done by heating the slice,

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after suitable cleaning, in an oxidizing atmosphere in known fashion. This oxide layer is then covered in turn with a silicon nitride layer of about 1200 Angstroms thick. Techniques for the deposition of a suitable layer are well
5 known. The dual SiO_2-Si_3N_4 layer is intended to serve, after patterning, as a mask for forming the desired grooves in the various silicon chips to be formed from the slice.

Techniques for patterning such a dual layer are
10 well known. Typically, a photoresist is deposited over the layer and photolithographic techniques are used to form a desired pattern in the photoresist. Selective etchants are thereafter used to remove in turn the silicon nitride and the silicon dioxide to arrive at the stage depicted in
15 FIG. 4. At this point the silicon slice 40 has its top surface covered with a layer 41 of silicon dioxide and a layer 42 of silicon nitride, which are patterned in two dimensions to provide openings down to the silicon surface. The pattern is such as to leave masked regions forming a
20 two-dimensional array corresponding to that desired for the cell array.

The masked silicon slice is then treated to form grooves 44, as seen in FIG. 5, in the region where the bare silicon has been exposed, leaving a two-dimensional array
25 of mesas 45. To conserve space it is advantageous that the grooves be narrow with essentially straight vertical walls, although in some instances some slight taper may be desirable to facilitate further processing, such as the doping of the sidewalls of the mesa and the filling of the
30 grooves. Reactive ion anisotropic etching is presently a known technique for forming grooves of the kind desired. For a typical design using two micron design rules, the grooves may be about three microns deep and two microns wide, and the mesas formed may be rectangular in cross
35 section, about seventeen microns by seven microns. The longer dimension would accommodate the length of the access transistor being shown in the plane of the drawing. The

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sidewalls of the mesas are then doped to form the heavily doped n-type regions which serve as one plate of the storage capacitor in each mesa. Advantageously this is done by first implanting arsenic ions on the vertical side
5 walls of the grooves and then heating to diffuse the arsenic ions deeper into the mesas away from the sidewalls. Alternatively, solid state-vapor diffusion alone may be used. In either case, the dual SiO_2-Si_3N_4 layer may continue to serve as the mask for localizing the
10 introduction of the donor atoms to the walls of the grooves. In a typical design, there are formed layers about several tenths of a micron thick with an average doping of about 10^{19} arsenic atoms per cubic centimeter. In FIG. 6 there is shown the resultant with n-type
15 layers 46 coating the walls of the grooves.

The slice is then subjected to a treatment that will eliminate that portion of the layer 46 that covers the bottoms of the grooves and thereby confine each layer 46 to a single mesa. This most conveniently is done by deepening
20 the grooves another micron or two without disturbing significantly the doped layers on the sidewalls. Reactive ion anisotropic etching again can be used to this end. FIG. 7 shows the grooves deepened below the n-type layers 46.

25 Then as seen in FIG. 8, there is formed a dielectric layer 47 over the walls of the groove to serve as the storage capacitor dielectric. This may be done conveniently by heating the slice in an oxidizing atmospheric fashion for a time and at a temperature
30 sufficient to form an oxide layer of about 500 Angstroms on the exposed walls of the mesas.

Next, as seen in FIG. 9, the grooves are filled with polycrystalline silicon 48 to a level to restore essentially the planarity of the top surface of the slice.
35 Various techniques are available for this purpose, particularly since the semiconductive properties of the silicon are not important. Known chemical vapor deposition

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techniques should be particularly advantageous. For use as a capacitor plate, it is desirable that this silicon be conductive, and so it should be appropriately doped. This can readily be done by including an appropriate impurity in
5 the vapor. Moreover, other conductors would be suitable for this fill although the silicon is preferred to minimize thermal mismatch problems that might strain the monocrystalline silicon mesas undesirably.

It can be appreciated that the fillings will all
10 be interconnected so that they can all be maintained at a uniform potential simply by connections at the edges of the chip.

It then usually will be necessary to remove any polycrystalline silicon that has deposited over the silicon
15 nitride on the top of the mesas. A wet etchant suitable for silicon, such as potassium hydroxide, should be adequate for this purpose. Some etching of the polycrystalline filling is tolerable, as depicted in FIG. 9.

20 It will usually be desirable to include a channel stop to minimize inadvertent inversion of the surface layer of the chip underlying the region of the bit line conductor near its connection to the source region of the transistor. To this end, it is desirable to form a boron-rich p+type
25 region localized at the edge of the top surface of the mesa opposite the edge where the transistor drain is connected to the n+diffused layer forming one of the capacitor plates.

Advantageously, this is done by masking the
30 surface to expose only one edge of the top surface of the mesa, and etching away the exposed portion of the silicon nitride-silicon dioxide dual layer, thereby to bare this edge of the top surface of the mesa, as is seen in FIG. 10.

Boron ions are then implanted selectively into
35 this bared edge portion to form a p-type localized surface zone 49 as seen in FIG. 10. The doping in this region advantageously is lower than the doping in layer 46 and is

typically about 3 x 10^{16} impurities per cubic centimeter.

The slice is then subjected to another oxidizing treatment to form a relatively thick dielectric layer over the chanstop regions and over the top of the polycrystalline filled grooves over which are to be deposited the bit or sense lines. This layer serves to electrically isolate these lines from the underlying polycrystalline silicon fill which is all to be maintained at the constant reference potential, such as ground. Typically, heating in an oxidizing atmosphere can be used to convert the polycrystalline silicon at the top of the grooves and the exposed chanstop region of the monocrystalline silicon to silicon dioxide to form the dielectric layer 50, typically between one and two microns thick, shown in FIG. 11.

Then there is preferably removed, in known fashion, the remainder of the silicon nitride layer 42 and the silicon dioxide layer 41 overlying the top of the mesa.

It is then advantageous to form at the top surface of each mesa a heavily doped n-type localized zone which will be useful in facilitating low resistance connection between the drain of the access transistor and the mesa wall layer which serves as one plate of the storage capacitor.

To this end, as seen in FIG. 12, there is then formed in each mesa at one edge a heavily doped localized n-type portion 51 which overlaps the n-type wall layer 46 and will help interconnect the drain of the access transistor to this layer. Typically, these portions are formed by the known combination of silicon oxide masking and vapor-solid diffusion techniques.

The mesa surface is now stripped clean and the surface prepared for the formation of the access transistor therein in conventional fashion.

Accordingly, after such surface preparation, the transistor gate oxide is grown over the mesa, typically about 500 Angstroms thick. This is followed by the

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deposition of a polycrystalline silicon layer over the surface of the chip which is patterned to provide both a plurality of bit lines, each of which overlies a grooved region and runs normal to the plane of the drawing, and a
5 plurality of discrete gate electrode portions, one for each mesa, localized over the surface region which is to serve as the channel of the corresponding access transistor.

In FIG. 13, there is shown the bit lines 52, the gate electrodes 53, and the gate oxide 54.

10 Then with the polysilicon gate electrode 53 and the polysilicon bit line 52 serving as masks, the surface of the slice is subjected to ion implantation and diffusion drive-in, in known fashion, to form in each mesa the n-type source and drain zones of the access transistor. As seen
15 in FIG. 13, the various elements are positioned such that the implanted source region 55 extends to connect to the bit line 52 and the implanted drain region 56 overlaps the previously formed zone 51. Typically, the lengths of the source, channel and drain are each between one and two
20 microns.

Then as seen in FIGS. 2 and 3, the slice is then coated with a phosphosilicate glass. There remains the need to provide the plurality of word lines, and to this end contact windows are opened selectively in the glass at
25 regions overlying the gate electrodes. Techniques are well known for this purpose and typically involve photolithography for masking the glass except where the openings are to be made and reactive ion etching for opening holes at unmasked portions of the glass.

30 This is followed by deposition of a metal layer over the chip suitable for providing the word lines. This layer is then appropriately patterned in known fashion to provide the plurality of word lines, each word line making low resistance connection selectively to the gate
35 electrodes of all the access transistors in a common row as is usual. Typically, the metal layer may be of aluminum and there is included a sintering step to better fuse the

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aluminum layer to the polycrystalline silicon forming the gate electrode. The resultant is shown in FIG. 2 in which the glass layer 26 is shown apertured to permit the word line conductor 25 to contact the gate electrodes 17.

5 It is to be appreciated that typically each memory chip includes, in addition to the array of memory cells, various auxiliary circuits for writing into and reading out of individual cells and such circuits would be fabricated in the chip. Additionally, in high capacity 10 memories, it might prove desirable to provide redundancy to permit the electrical substitution of unsatisfactory cells with satisfactory cells. Provision would normally be made for such additional circuitry in usual fashion.

Moreover, in usual fashion, after the slice 15 processing has been completed, the slice would be cut up in individual chips for testing and packaging in the usual fashion.

It is to be appreciated that considerable variation from the specific process described is feasible 20 in making a memory cell in accordance with the invention.

It should also be appreciated that the specific embodiment described is merely illustrative of the general principles of the invention. If it were desired to use P-channel access transistors, it would be necessary to 25 reverse the conductivity-types of the various regions where the type is important. Moreover, it may be feasible to provide a topology for individual cells that would permit sharing of connections, for example, the sources of a pair of transistors in adjacent rows may be made to share a 30 common bit line connection.

It should also be evident that other types of access transistors, such as bipolar forms, could be employed, if this were found desirable, after appropriate change in the interconnections. It will be advantageous 35 that such access transistors include a pair of terminals which may be termed the conduction terminals corresponding functionally most nearly to the source and drain and a

control terminal corresponding to the gate.

Additionally, it should be recognized that the basic principles of the embodiment described might find utility in any circuit where there is desired, in a single
5 chip, a large array of capacitors without sacrificing large amounts of chip surface area. Such circuits might include other forms of memories or other forms of signal processing circuits.

Additionally, in a broader aspect, the invention
10 provides an alternative to the partially dielectrically isolated silicon integrated circuits now known in the art in which a monocrystalline silicon chip is grooved to form a plurality of mesas and the grooves are thereafter filled with silicon dioxide to establish planarity. Technology of
15 this kind has variously been described as ISOPLANAR and OXIL technology. With such devices, it has sometimes proven difficult to refill the grooves with oxide without affecting deleteriously the electrical properties of the monocrystalline mesas because of the difference in thermal
20 mismatch between the silicon and the silicon dioxide. To mitigate the mismatch problem, in accordance with the broader aspect of the invention, nonconductive polycrystalline silicon is used to fill the grooves either partially or completely.

25 FIG. 14 shows an integrated circuit chip useful in this way. It includes a silicon chip 60 which is provided with a plurality of grooves 61 to define a plurality of mesas 62. The chip includes a bulk portion 63 of p-type conductivity and a surface portion 64 of n-type
30 conductivity. The grooves typically extend beyond portion 64 into the bulk 63 whereby the portion 64 of each mesa is effectively electrically isolated from similar portions 64 of all other mesas, particularly if a reverse bias is maintained on the p-n junctions between the
35 portions 64 and the bulk 63. Since each mesa is isolated, each can support its own circuit elements, which may be any of the known forms, including either bipolar or MOS

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transistors.

Moreover, the grooves 61 ordinarily will be filled with doped polycrystalline silicon as in the prior embodiment, in which case it will normally be advantageous
5 to provide a layer of silicon dioxide in the grooves, as before, to isolate the fill from the individual mesas. In this case the fill can be maintained at some reference voltage useful in the circuit.

Alternatively, the fill can be of undoped
10 polycrystalline silicon to be of high resistivity. In this case, if the resistivity is sufficiently high, there may be eliminated the need for the silicon dioxide layer in the grooves to provide electrical isolation. In this case, there may be doped selectively localized regions of the
15 fill to serve as localized resistors for use in combination with circuit elements in the mesas. Alternatively thin conductive films may be deposited over the fill to serve as resistors.

Similarly, undoped polycrystalline silicon may be
20 used to provide isolation between the two different types of transistors in circuits using complementary pairs of transistors.

Moreover, in some instances after the polycrystalline silicon is used to fill the grooves between
25 mesas, there results a corrugated top surface which cannot readily be made planar by simple etching. In such instances, it may prove useful to deposit over the polysilicon a sacrificial layer of a material which can be etched substantially at the same rate as the polysilicon by
30 some convenient etching technique. The sacrificial layer is deposited to a thickness to provide a composite layer of polysilicon and the material which has a substantially planar layer, and then subjected to the etching treatment to reduce uniformly the thickness of the dual layer until
35 there results substantially a planar surface only of the polysilicon.

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Claims

1. A semiconductor integrated circuit comprising a semiconductor body (11, 12) having a major surface with grooves (13) therein which define a plurality of mesas (11), each of the said mesas having at least one circuit component (15, 16, 17, 18) formed therein

CHARACTERIZED IN THAT

each of the mesas has a conductive layer (19) in the side wall thereof, the grooves (13) being filled with a conductive material (14) which is separated from the body (11, 12) by a layer (20) of dielectric material.

2. An integrated circuit as claimed in claim 1 wherein the conductive material (14) is a polycrystalline form of the semiconductor which constitutes the body (11, 12).

3. An integrated circuit as claimed in claim 1 or claim 2 wherein the conductive layer (19) in the side wall of each mesa (11) is a layer of opposite conductivity type from the bulk of the mesa.

4. An integrated circuit as claimed in any of the preceding claims wherein the semiconductor is silicon.

5. A semiconductor memory comprising an integrated circuit as claimed in any of the preceding claims wherein each of the mesas (11) constitutes a cell (1A) of the memory and the capacitance between the conductive layer (19) in the sidewall of each mesa and the conductive material (14) constitutes a storage capacitor (6) for the respective cell.

6. A semiconductor integrated circuit comprising a semiconductor body (60) having a major surface with grooves (61) therein which define a pluarlity of mesas (62), each of the said mesas having at least one circuit component formed therein,

CHARACTERIZED IN THAT

the grooves (61) are filled with a polycrystalline form of the semiconductor which constitutes the body (60).

7. An integrated circuit as claimed in claim 6 wherein the polycrystalline semiconductor is separated from the body (60) by a layer of insulating material (66).

8. An integrated circuit as claimed in claim 6
5 or claim 7 wherein the polycrystalline semiconductor is of high resistivity compared with the bulk of the mesas (62).

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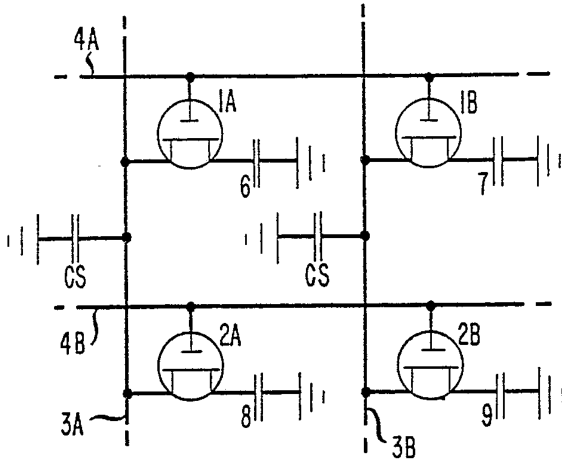

FIG. 1

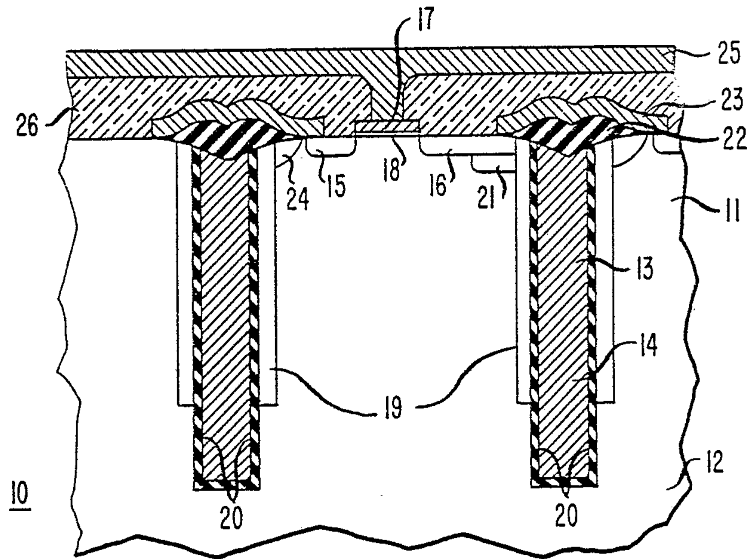

FIG. 2

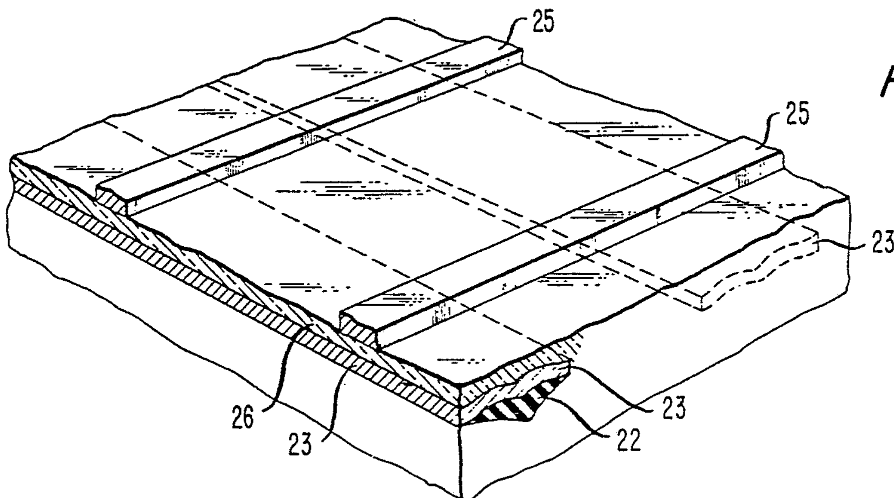

FIG. 3

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FIG. 4

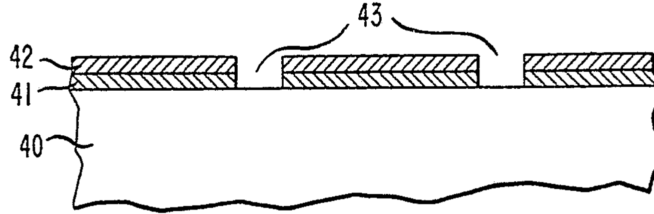


FIG. 5

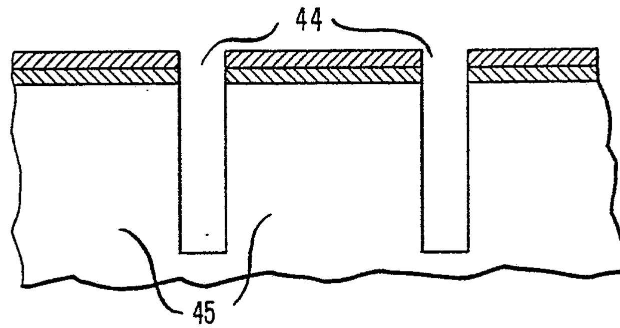


FIG. 6

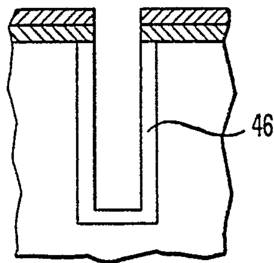


FIG. 7

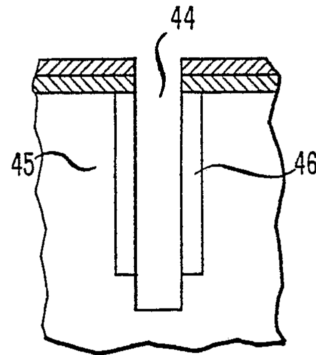


FIG. 8

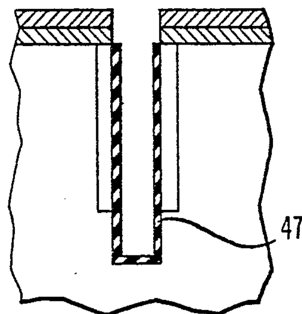
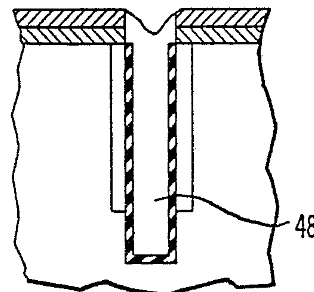


FIG. 9



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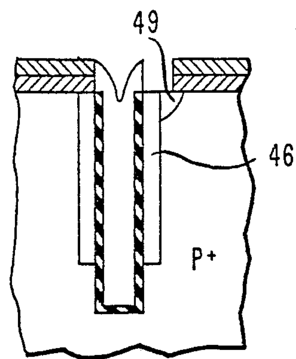

FIG. 10

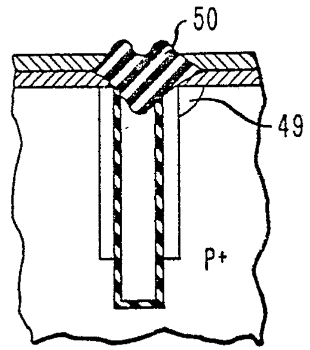

FIG. 11

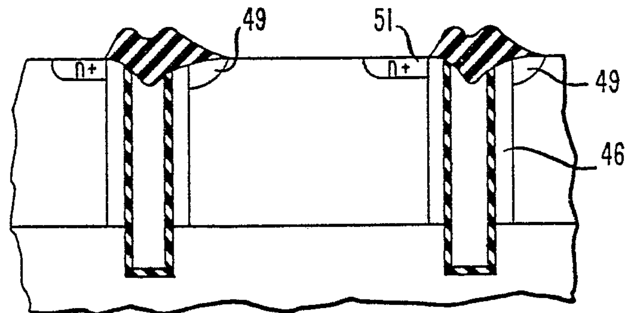

FIG. 12

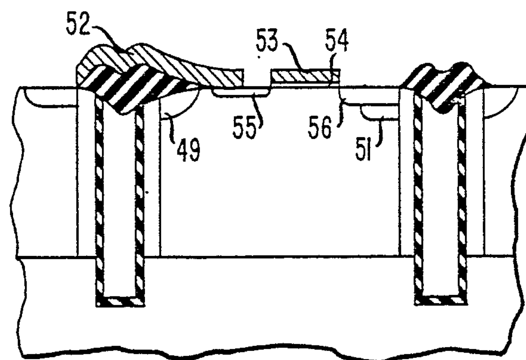

FIG. 13

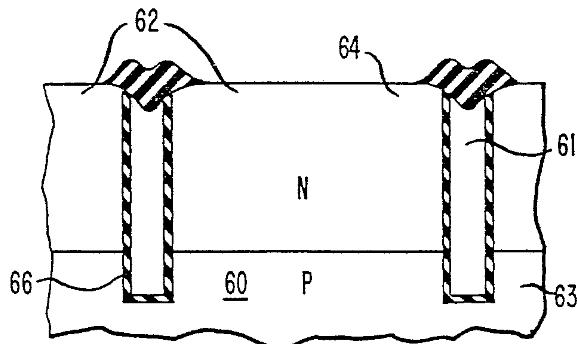

FIG. 14

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INTERNATIONAL SEARCH REPORT

International Application No PCT/US81/00495

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int Cl[3] H01L 27/04, 27/12, 29/04,
U.S.Cl 357/49, 50, 55, 59

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	397/49, 50, 55, 59

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 4,048,649, PUBLISHED 13 SEPTEMBER, 1977	ALL
A,P	US, A, 4,222,062, PUBLISHED 9 SEPTEMBER, 1980	ALL
A,P	US, A, 4,222,063, PUBLISHED 9 SEPTEMBER, 1980	ALL
A	US, A, 4,140,558, PUBLISHED 20 FEBRUARY, 1979	ALL
A	US, A, 4,009,484, PUBLISHED 22 FEBRUARY, 1977	ALL
A,E	US, A, 4,272,776, PUBLISHED 9 JUNE, 1981	ALL
A,P	US, A, 4,229,474, PUBLISHED 21 OCTOBER, 1981	ALL

* Special categories of cited documents: [15]

"A" document defining the general state of the art
"E" earlier document but published on or after the international filing date
"L" document cited for special reason other than those referred to in the other categories
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but on or after the priority date claimed
"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention
"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
29 July 1981	04 AUG 1981
International Searching Authority [1]	**Signature of Authorized Officer** [20]
ISA/US	M. Edlow

Form PCT/ISA/210 (second sheet) (October 1977)