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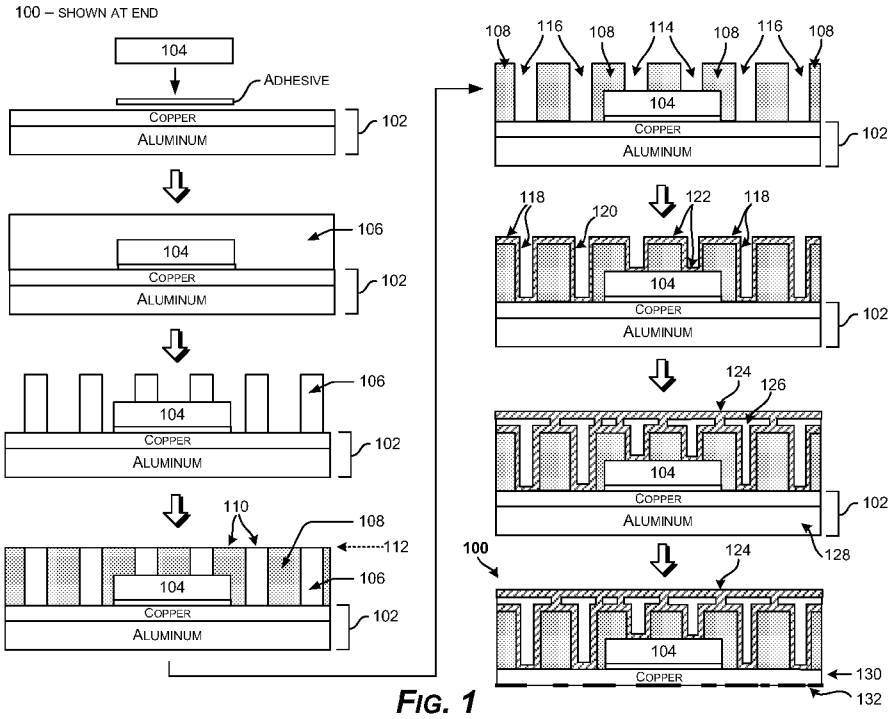

FIG. 1

(57) Abstract: Fan-out wafer level packages with resist vias are provided. In an implementation, an example wafer level process or panel fabrication process includes adhering a die to a carrier, applying a temporary resist layer over the die and the carrier, developing the resist layer to form channels or spaces, filling the channels or the spaces with a molding material, removing the remaining resist to create vias in the molding material, and metalizing the vias in the molding material to provide conductive vias for the microelectronics package. The methods automatically create good via and pad alignment. In another implementation, an example process includes adhering a die to a carrier, applying a permanent resist layer over the die and the carrier, developing the resist layer to form vias in the resist layer, and metalizing the vias in the remaining resist of the permanent resist layer to provide conductive vias for the microelectronics package. Assemblies may be constructed with the semiconductor dies face-up or face-down. One or more redistribution layers (RDLs) may be

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FAN-OUT WAFER LEVEL PACKAGE WITH RESIST VIAS

RELATED APPLICATIONS

[0001] This patent application claims the benefit of priority to U.S. Provisional Patent Application No. 62/484,974 to Haba et al., filed April 13, 2017 and incorporated by reference herein in its entirety.

BACKGROUND

[0002] In conventional wafer-level packages, input-output terminals are located over the chip surface area, limiting the number of possible input-output connections. Fan-out wafer level packages (FOWLP) conventionally have a smaller package footprint with greater input-output connections, compared to standard wafer-level packages (WLPs), thereby providing a higher integration level and also a higher number of external electrical contacts.

[0003] Conventional fan-out wafer level packages embed each individual die in a low cost epoxy mold compound (EMC) with space allotted between each die for additional input-output points. Redistribution layers (RDLs) are then formed to "fan out" the input-output connections using physical vapor deposition (PVD) seeding, electroplating, and patterning to reroute the input-output connections on the die to the periphery of the epoxy mold compound.

[0004] These conventional fan-out wafer level packages require a bumped die (e.g., solder balls), and package-on-package vias that are drilled, plated, etched, or preformed. The fan-out packages demand good alignment between die pads and vias due to die shift, and achieving good alignment can add to the cost.

SUMMARY

[0005] Fan-out wafer level packages with resist vias are provided. In an implementation, an example wafer level process or panel fabrication process includes adhering a die to a carrier, applying a temporary resist layer over the die and the carrier, developing the resist layer to form channels or spaces, filling the channels or the spaces with a molding material, removing the remaining resist to create vias in the molding material, and metalizing the vias in the molding material to provide conductive vias for the microelectronics package. The methods automatically create good via and pad alignment. In another implementation, an example process includes adhering a die to a carrier, applying a permanent resist layer over the die and the carrier, developing the resist layer to form vias in the resist layer, and metalizing the vias in the remaining resist of the permanent resist layer to provide conductive vias for the microelectronics package. Assemblies may be constructed with the semiconductor dies face-up or face-down. One or more redistribution layers (RDLs) may be built on one or both sides of an assembly with resist vias.

[0006] This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Certain embodiments of the disclosure will hereafter be described with reference to the accompanying drawings, wherein like reference numerals denote like elements. It should be understood, however, that the accompanying figures illustrate the various implementations described herein and are not meant to limit the scope of various technologies described herein.

[0008] Fig. 1 is a diagram of an example process for making vias in an example wafer level package using a temporary resist, such as a photoimagable resist, to shape a molding.

[0009] Fig. 2 is a diagram of an example process for making vias in an example wafer level package using a permanent resist for the vias.

[0010] Fig. 3 is a diagram of an example microelectronics package, showing selection of an adhesive thickness and density to balance dielectric filler properties in the microelectronics package.

[0011] Fig. 4 is a diagram of an example process for making vias in an example microelectronics package with dies face-up, using temporary resist.

[0012] Fig. 5 is a diagram showing different example techniques for metalizing or filling the resist vias.

[0013] Fig. 6 is a diagram of various example options and features for a fan-out wafer level package created by the example processes described herein.

[0014] Fig. 7 is a diagram of an example process for making vias in an example microelectronics package with dies face-up, using permanent resist.

[0015] Fig. 8 is a diagram of an example process for making vias in an example microelectronics package with dies face-down, using temporary resist.

[0016] Fig. 9 is a diagram of an example process for making vias in an example microelectronics package with dies face-down, using permanent resist.

[0017] Fig. 10 is a flow diagram of an example method of making an electronics package with temporary resist used to shape molding, and the molding used to form permanent vias in the package.

[0018] Fig. 11 is a flow diagram of an example method of making a microelectronics package with permanent resist used for vias in the microelectronics package.

DESCRIPTION

[0019] This disclosure describes example fan-out wafer level packages (FOWLP) with resist vias. An example process uses a layer of resist, such as photo-resist, to create contact vias and package-on-package (POP) vias simultaneously, integrating bumping the die at the same time as POP vias, or eliminating bumping altogether, while improving alignment and minimizing cost.

[0020] The example process can be used for wafer level packages, but can also be used as a large panel process.

[0021] In an implementation, after a die is bonded to a carrier, a temporary layer of resist is applied and patterned to provide a template for mold material. The mold material is added, molded around the temporary resist. The resist is then removed leaving via channels in the mold material, and the surface of the mold material is metalized to directly form contact vias, package-on-package vias, and die pads, all in the same process step. These vias can be smooth in contrast with lased vias. Metalization of the vias can be accomplished by plating both the POP vias and the pad vias simultaneously and conformly. Thus, the contact vias and the package-on-package vias are made together. It may take only one lithography pass to expose the package-on-package (POP) vias and die pad vias, thereby providing great registration.

[0022] In another implementation, after a die is bonded to a carrier, a permanent layer of resist is applied and patterned, and then the surface of the patterned resist itself is metalized to form contact vias, package-on-package vias, and die pads, all in the same processing step. In this implementation, permanent resist is used instead of the mold material.

[0023] The example process can be used with the die facing up or the die facing down on carrier.

[0024] An example carrier for these example processes may have two layers, including support layer and a conductor layer, such as copper. The die can be attached to the copper side of the carrier, and then the support layer removed later after the resist process and metalization steps described above have been achieved. The remaining copper layer can become a redistribution layer (RDL) that is already attached and perfectly aligned after patterning. For example, an aluminum/copper substrate (for example, Al/Cu in thicknesses of 150 μm/18 μm, respectively) can be used as the carrier, with the aluminum being dissolved at the end to leave the remaining copper layer as a RDL back layer, without extra cost or effort. Part of the carrier can remain and stays a RDL layer.

[0025] In an implementation, the die is permanently bonded to the carrier from the outset, eliminating the need for handling carriers that require temporary adhesives and that require release of the die from the carrier at some point. The die can be placed and cured, and thereby secured in place to the carrier, which eliminates the possibility of unwanted movement during molding.

[0026] Adhesives for the example package-on-package processes can be selected to have properties, such as a selected density, that provide a balanced package or a package-on-package assembly that has homogeneous density and balance. In an implementation, a balanced structure can be achieved when the adhesive is made thick and physical properties of the adhesive are chosen to balance the top side, for example.

[0027] An example process can eliminate the need for bumping the die, while providing excellent alignment of vias and die pads, and while also minimizing cost. In some cases, there is no need for bumping the die (usually 40-50 μm Cu bumping), yet the mold material still covers the die for reliability.

[0028] The procedures introduced above can also provide a very thin fan-out wafer level package (FOWLP).

[0029] In an implementation, the example processes provide coplanar aspects of a top surface that eliminate the need to polish the top, in some circumstances.

Example Processes and Structures

[0030] Fig. 1 shows an example wafer level package 100 with one or more fan-out conductor layers 124 during an example process of assembly. The illustration is diagrammatic, components are not shown in real size or in relative scale to each other, but are stylized for the sake of description. In a beginning step, a carrier 102 is provided that may consist of a metal or metals, such as copper bonded to aluminum, or may consist of another rigid material. The aluminum, for example, may provide a support layer of the carrier 102, while the copper may provide a conductive layer of the carrier 102. A die 104 is permanently adhered to the carrier 102. The die 104 may be attached to the carrier 102 as a single raw die, as a packaged die, as stacked dies, as side-by-side dies, or as a die with a redistribution layer (RDL). Temporary resist 106, such as a photoimagable resist 106, is applied over the die 104 and over the carrier 102, and the temporary resist 106 is developed, for example, by photolithography. Molding material 108 is applied over the top of the package. The top surface 110, including the top surface of the molding material 108 and the top

surface of the temporary photoresist 106 may be planarized 112. The temporary photoresist 106 is then removed, leaving vias 114 over the die 104 and vias 116 through the molding material 108, suitable for providing package-on-package (POP) through-vias. This patterned molding material 108 is metalized 118 to form conductive vias 120 and pads 122. One or more RDL layers 124 may be formed on top, with a dielectric 126 or other filler in the interstices. A support layer of the carrier 102, such as an aluminum layer 128, may be removed, and when used with the carrier 102, a copper layer 130 of the carrier 102 may remain as a back RDL layer 132, for example.

[0031] Fig. 2 shows an example wafer level package 200 with one or more fan-out conductor layers in an example process of assembly. In a beginning step, a carrier 102 is provided, which may consist of a metal or metals, such as copper bonded to aluminum, or may consist of another rigid material. The aluminum, for example, may provide a support layer of the carrier 102 while the copper may provide a conductive layer of the carrier 102. A die 104 is permanently adhered to the carrier 102. The die 104 may be attached to the carrier 102 as a single die, or as a packaged die, stacked dies, side-by-side dies, or as a die with a redistribution layer (RDL) already attached. Permanent resist 202, such as photoimagable resist 202 is applied over the die 104 and over the carrier 102. The permanent resist 202 is developed by photolithography, for example, leaving contact vias 204 over the conductive pads of the die 104 and also vertical vias 206 through the permanent resist material 202. Alternatively, vias 204 & 206 may be drilled or otherwise formed or placed in the permanent resist 202 instead of, or in addition to, developing the resist 202 to form the vias 204 & 206. The vertical vias 206 are suitable for use as package-on-package (POP) through-vias. In contrast to the implementation of Fig. 1 described above, in the implementation of Fig. 2, the

photoresist material 202 remains permanently in place, and takes the place of the molding material 108 in the implementation of Fig. 1. This developed resist 106 is then metalized 208 to form conductive vias 210 & 212. One or more RDL layers 214 may be formed on top, with a dielectric 216 or other filler in the interstices. A support layer 218 of the carrier 102 may be removed, and when used with the carrier 102, a copper layer 220 of the carrier 102 may remain as basis for a backside RDL layer 222.

[0032] Fig. 3 shows an example wafer level package 300 in which the die 104 is attached to the carrier 102 with an adhesive 302. The support layer 218 of the carrier has been removed. Fig. 3 shows the location of the adhesive 302 binding the die 104 to the remaining conductive layer 220 of the carrier 102, and also shows a dielectric 304 or other filler in the spaces above the die 104. The adhesive 302, and the dielectric 304 as an example filler, may be selected for similarity of physical properties, such as density, to balance the package or assembly, or may be selected to have complementary physical properties. This allows the adhesive 302 and/or the dielectric filler 304 to determine the deportment of the package 300, in light of the physical properties of the resist 106 or the molding 108 (not shown) that remains permanently in the package 300 as walls of the various vias formed. The thickness and density of the adhesive 302 binding the die 104 to the carrier 102 may be selected to balance or compensate for the thickness and density of the dielectric filler 304, or to balance or compensate for the combination of resist 106 and dielectric filler 304, or the combination of molding material 108 (not shown) and dielectric filler 304. In general, the physical properties of the materials above the die 104 and the materials to be used below the die 104 may be selected to balance each other.

[0033] Fig. 4 shows an example assembly process 400 of manufacturing a fan-out wafer level package 402 (shown at last step in Fig. 4), with the die 104 face-up (pads 412 face-up), and a temporary resist 106 used in the manufacture. Fabrication of an example package 402 begins with attaching a die 104 to a metal sheet or an RDL on a carrier 404. The die 104 may be a single die, or may be a packaged die, stacked dies, side-by-side dies, with pads 412 face up. At 406, temporary resist 106, such as a photoimagable resist 106, is applied over the die 104 and over the carrier 404. At 408, the temporary resist is developed 409, for example, by photolithography. At 410, this technique automatically establishes alignment between die pads 412 and (future) conductive posts 414 that will be materialized later in the process 400 in place of the temporary resist 106. At 416, molding material 108 is applied into the top surface of the package, including the top surface of the molding material 108 and the top surface of the temporary photoresist 106. The top surface may be planarized 112. At 418, the temporary photoresist 106 is then stripped or otherwise removed leaving patterned molding material 108 that has vias 114 over the die 104 and its pads 412 suitable for being metalized and bumped later, at a higher level, at the same time as package-on-package bumping, and that has longer vertical vias 116 through the molding material 108, suitable for package-on-package (POP) through-vias that can be bumped at the same time as the vias 114 over the die 104. At 420, this patterned molding material 108 is plated or metalized with a conductor 118 to form conductive vias 120 and pads. At 422, the conductor 118 that has been plated, deposited, or otherwise metalized over the molding material 108 can be patterned 424 into circuits and/or RDLs. One or more additional RDL layers 124 may be formed on top for providing fan-out conductive traces, with dielectric 126 or other filler occupying voids

and supporting the RDLs 124. A support component of the carrier 404 may be removed, leaving a conductive layer 426. At 428, one or more backside RDL layers 132 may also be added.

[0034] Fig. 5 shows various techniques of filling vias 114 & 116. Vias 114 & 116 may be formed in process 400 of Fig. 4, for example, which leaves patterned molding material 108 in place after temporary photoresist 106 is removed. A first process 500 completely fills vias 114 and vias 116 with metal 502, through seeding, plating, deposition, or other metalization techniques. One or more RDL layers 124 may be formed on the top surface of the package after the vias 114 & 116 are filled with metal 502. Dielectric material 126 or other nonconductive fillers may be used over pads, around posts, and under one or more RDLs 124 built up on top of the package.

[0035] A second process 504 plates or deposits a metal layer 506 within the vias 114 & 116. The metal layer 506 is thinner than the complete metalization 502 deposited in process 500 above. Top surfaces of the deposited metal layer 506 may optionally be etched into a patterned metal layer 508 or RDL. Then, one or more additional RDL layers 124 may be built-up on the top surface of the package after the vias 114 & 116 are lined or filled with metal. A dielectric 126 or other filler may be used for space-filling above the patterned 508 or unpatterned metal layer 506 and for supporting the one or more RDLs 124, when present.

[0036] A third process 510 deposits or plates a thicker metal layer 512 into the vias 114 & 116 in the patterned molding material 108. The thicker metal layer 512 may fill some vias 114 while completely leaving some empty space 514 in longer vertical vias 116. The thicker metal layer 512 may be patterned 516, and one or more RDL layers 124 built-up above the patterned thick metal layer 516 with a dielectric 126 or

other nonconductive filler occupying the previously empty spaces 514 in the vias 116 and supporting the one or more RDL layers 124.

[0037] Fig. 6 summarizes some of the features available as options for example fan-out wafer level packages (FOWLPs) that can be created by the processes described herein. First, at 600, the microelectronic packages may have vias in a layer of molding 108 after temporary resist 106 is removed, or may have vias in a permanent layer of resist 202, with no extra molding necessary. The microelectronic packages may be manufactured in a wafer level process with fan-out traces, or may be manufactured in a panel fabricating process 602. Dies 104 may be placed either face-up or face-down 604 on a carrier 102. For reliability, the package may use copper-bumped dies 104 and may have a thick dielectric 126 added 606. Vias 114 & 116 may also be drilled, then plated, or preformed and plated, and formed in other ways 608 besides etching resist. A molding material 108 may be used for the molding steps, and in an implementation 610, the molding material may be a laminated dielectric 126. A first RDL 124 may be built-up before or after a molding step 612. Second and subsequent RDLs 132 may be added as needed.

[0038] Fig. 7 shows an example assembly process 700 of manufacturing a fan-out wafer level package, with the die 104 face-up, and permanent resist 202 used in the manufacture. Fabrication of an example package 702 (shown in last step) begins with attaching a die 104 face-up to a metal sheet or an RDL on a carrier 704. The die 104 may be a single die, or may be a packaged die, stacked dies, side-by-side dies, or as a die with one or more redistribution layers (RDLs). At 706, permanent resist 202, such as a photoimagable resist 202, is applied over the die 104 and over the carrier 704. At 708, the permanent resist 202 is developed 709, for example, by

photolithography, to form vias 114 over the die 104 and vertical vias 116 through the permanent resist 202 where there is no die 104. At 710, the developed permanent resist 202 is removed leaving open vias 114 over the die 104 and longer open vertical vias 116 through the molding material 108, suitable for becoming package-on-package (POP) through-vias. The vias 114 over the die can become conductive posts later in the process. At 712, the patterned permanent resist 202 is plated or metalized 714 to form conductive vias 114 & 116, and in an implementation, an RDL layer. At 716, one or more additional RDL layers 718 & 720 may be formed on top for providing fan-out conductive traces or for adding subsequent RDLs, with dielectric 126 or other filler occupying voids and supporting the RDLs 720. A support component of the carrier 704 may be removed, leaving a conductive layer 722. At 724, one or more backside RDL layers 132 may also be added.

[0039] Fig. 8 shows an example assembly process 800 of manufacturing a fan-out wafer level package with the die 104 face-down, and temporary resist 106 used in the manufacture. Fabrication of an example package 802 or 802' (shown at final step in Fig. 8) begins with attaching a die 104 face-down to a metal sheet or an RDL on a carrier 804. Face- down means that one-sided electrical contacts of the die 104 face the carrier 804 when the die 104 is adhered to the carrier 804. The die 104 may be a single die, or may be a packaged die, stacked dies, side-by-side dies, or as a die with one or more redistribution layers (RDLs). At 806, temporary resist 106, such as a photoimagable resist 106, is applied over the die 104 and over the carrier 804. At 808, the temporary resist 106 is developed 810, for example, by photolithography. At 812, the developed resist 810 is removed, leaving undeveloped temporary resist 106 in place. At 814, a molding material 108 is applied over the die 104 and the carrier 102

surfaces that are still exposed from the top. The undeveloped temporary resist 106 forms or shapes the molding material 108, with the space occupied by the temporary resist 106 becoming the vias 116 when the temporary resist 106 is removed. At 816, the top surface of the package 802 may be lapped or planarized. The remaining temporary photoresist 106 is then stripped or otherwise removed leaving patterned molding material 108 with vertical vias 116 formed through the molding material 108 by the removed temporary resist 106, suitable for providing package-on-package (POP) through-vias. At 818, the patterned molding material 108 is plated or metalized 118 to form conductive vias 120 and pads. The top metalization layer may be patterned into circuits or an RDL, and one or more RDL layers 124 may be formed on top for providing fan-out conductive traces, with dielectric 126 or other nonconductive filler occupying voids and supporting the one or more RDLs 124. At 822, a support component of the carrier 804 may be removed, leaving a metal layer 824 of the carrier 804, or the carrier 804 is removed entirely and the bottom of the assembly can be etched and metalized 824 for forming circuits coupled to the down-facing die pads 412. At 826, one or more backside RDL layers 132 may also be added, coupled in electrical contact with the conductive die pads 412. The top RDL(s) 124 may be formed closely on top of the back face 828 of the die 104 as in package 802, or on a thicker layer of the intervening molding material 108 placed at step 814, as in package 802'.

[0040] Fig. 9 shows an example assembly process 900 of manufacturing a fan-out wafer level package 902 or 902' (shown at final step in Fig. 9) with the die 104 face-down, and permanent resist 202 used in the manufacture. Fabrication of an example package 902 or 902' begins with attaching a die 104 face-down to a metal

sheet or an RDL on a carrier 904. The die 104 may be a single die, or may be a packaged die, stacked dies, side-by-side dies, or as a die with one or more redistribution layers (RDLs). At 906, permanent resist 202, such as a photoimagable resist 202, is applied over the die 104 and over the carrier 904. At 908, the permanent resist 202 is developed, by photolithography for example, resulting in areas of developed resist 910. At 912, the top of the package may be lapped or planarized 112. At 914, the developed resist 910 is removed, leaving open vertical vias 116. At 916, the open vertical vias 116 are metalized 918 by deposition, plating, or other techniques, and an RDL 920 may be formed on top. At 922, one or more additional RDL layers 124 may be formed on top for providing fan-out conductive traces, with dielectric 126 or other filler occupying voids and supporting the RDLs 124. At least a supporting layer of the carrier 904 is also removed, leaving a metal layer 924 or allowing closer access to the conductive die pads 412. At 926, one or more backside RDLs 132 may be built in conductive contact with the electrical contacts 412 of the die 104. The top RDL(s) 124 may be formed closely on top of the back face 928 of the die 104 as shown in package 902, or on an intervening layer of the resist material 202, when a thicker layer of the resist material 202 is maintained between steps 910-912, as shown in package 902'.

Example Methods

[0041] Fig. 10 shows an example method 1000 of making an electronics package with temporary resist used to form permanent vias in the package. Operations of the example method 1000 are shown as individual blocks.

[0042] At block 1002, a die is adhered to a carrier.

[0043] At block 1004, a resist layer is applied over the die and carrier.

[0044] At block 1006, the resist is developed and the developed resist is removed, creating channels or spaces in the remaining resist.

[0045] At block 1008, the channels or spaces in the remaining resist are filled with a molding material.

[0046] At block 1010, the remaining resist is removed, creating vias in the molding material.

[0047] At block 1012, the vias are metalized to provide conductive vias in the package.

[0048] Fig. 11 shows an example method 1100 of making a microelectronics package with permanent resist used to form conductive vias in the microelectronics package. Operations of the example method 1100 are shown as individual blocks.

[0049] At block 1102, a die is adhered to a carrier.

[0050] At block 1104, a layer of resist is applied over the die and the carrier.

[0051] At block 1106, the layer of resist is developed to form vias in the layer of resist.

[0052] At block 1108, the vias in the layer of resist are metalized to provide conductive vias for the microelectronics package.

[0053] In the above specification and appended claims: the terms “connect,” “connection,” “connected,” “in connection with,” and “connecting,” are used to mean “in direct connection with” or “in connection with, via one or more elements.” The

terms “couple,” “coupling,” “coupled,” “coupled together,” and “coupled with,” are used to mean “directly coupled together” or “coupled together via one or more elements.”

[0054] While the present disclosure has been disclosed with respect to a limited number of embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations possible given the description. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the disclosure.

CLAIMS

1. A method, comprising:

adhering a die to a carrier for making a microelectronics package;

applying a resist layer to the die and the carrier;

forming a space in the resist layer;

using the space to make a via for the microelectronics package; and

metalizing the via to provide a conductive pathway for the microelectronics package.

2. The method of claim 1, further comprising:

developing the resist layer to directly form vias in the resist layer; and

metalizing the vias in the resist layer to provide conductive pathways for the microelecronics package.

3. The method of claim 2, wherein the resist layer comprises a photoimagable resist.

4. The method of claim 2, further comprising drilling or forming one or more holes in the resist layer to form at least one of the vias.

5. The method of claim 2, further comprising:

forming contact vias and vertical package-on-package (POP) vias in the resist layer; and

plating or depositing a metal in the contact vias and the vertical package-on-package (POP) vias simultaneously and conformly.

6. The method of claim 1, further comprising using a temporary resist layer to make vias in a molding material of the microelectronics package.

7. The method of claim 6, further comprising:

developing the temporary resist layer to form channels or spaces in the temporary resist layer;

filling the channels or the spaces with a molding material;

removing a remaining resist material of the temporary resist layer to create vias in the molding material; and

metalizing the vias in the molding material to provide conductive pathways for the microelectronics package.

8. The method of claim 6, wherein metalizing the vias further comprises lining at least some of the vias with metal and filling a remaining space in the vias with a dielectric material or a nonconducting filler material.

9. The method of claim 1, further comprising forming one or more redistribution layers on a top of the microelectronics package, at least one of the redistribution layers coupled to the conductive pathway.

10. The method of claim 1, wherein a conductive part of the carrier is patterned to becomes a redistribution layer (RDL) coupled to the conductive pathway.

11. The method of claim 10, further comprising removing a supportive component of the carrier and forming one or more redistribution layers (RDLs) on a bottom of the microelectronics package.

12. The method of claim 1, wherein the die is adhered face-up on the carrier.

13. The method of claim 1, wherein the die is adhered face-down on the carrier.

14. The method of claim 1, wherein the carrier comprises a layer of aluminum or a support material, and a layer of copper releasably attached to the aluminum or the support material.

15. An apparatus, comprising:

a carrier, a substrate, or a panel of a microelectronics package;

vias in a layer of resist or in a molding material on the carrier, substrate or panel; and

a metal in the vias for providing conductive pathways for the microelectronics package.

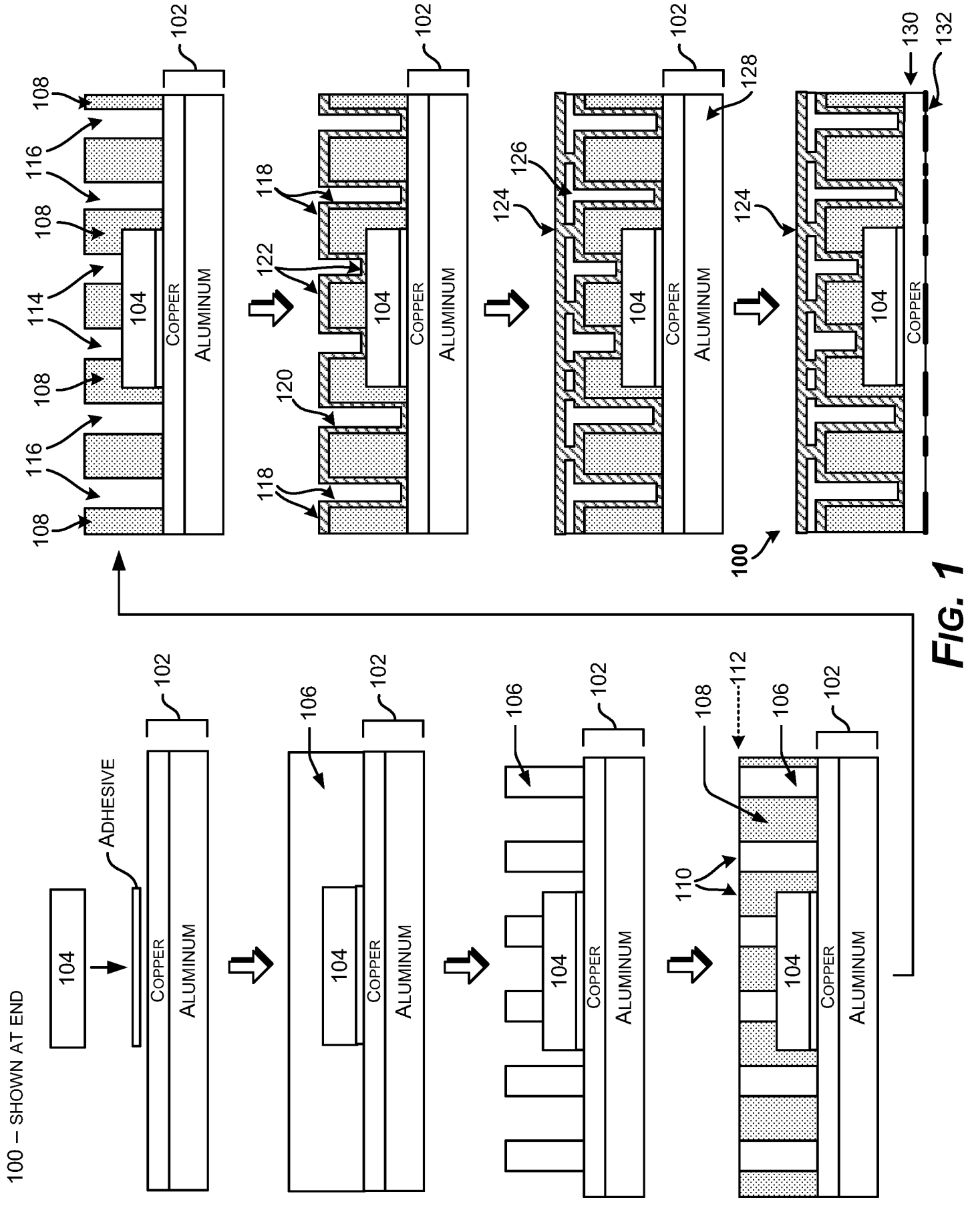
16. The apparatus of claim 15, wherein the layer of resist comprises a photoimagable material.

17. The apparatus of claim 15, wherein the layer of resist comprises a mold for the vias in the molding material.

18. The apparatus of claim 15, where the layer of resist comprises a mold for the vias, wherein the vias are in the layer of resist.

19. The apparatus of claim 15, further comprising a semiconductor die adhered to the carrier, substrate, or panel, wherein a thickness and density of an adhesive adhering the semiconductor die to the carrier, substrate, or panel balances physical properties of a dielectric or a filler material in the microelectronics package.

20. The apparatus of claim 15, further comprising one or more redistribution layers (RDLs) on a top or a bottom of the microelectronics package coupled to one or more of the conductive pathways of the microelectronics package.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ADHESIVE
COPPER
ALUMINUM
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106
108
110
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114
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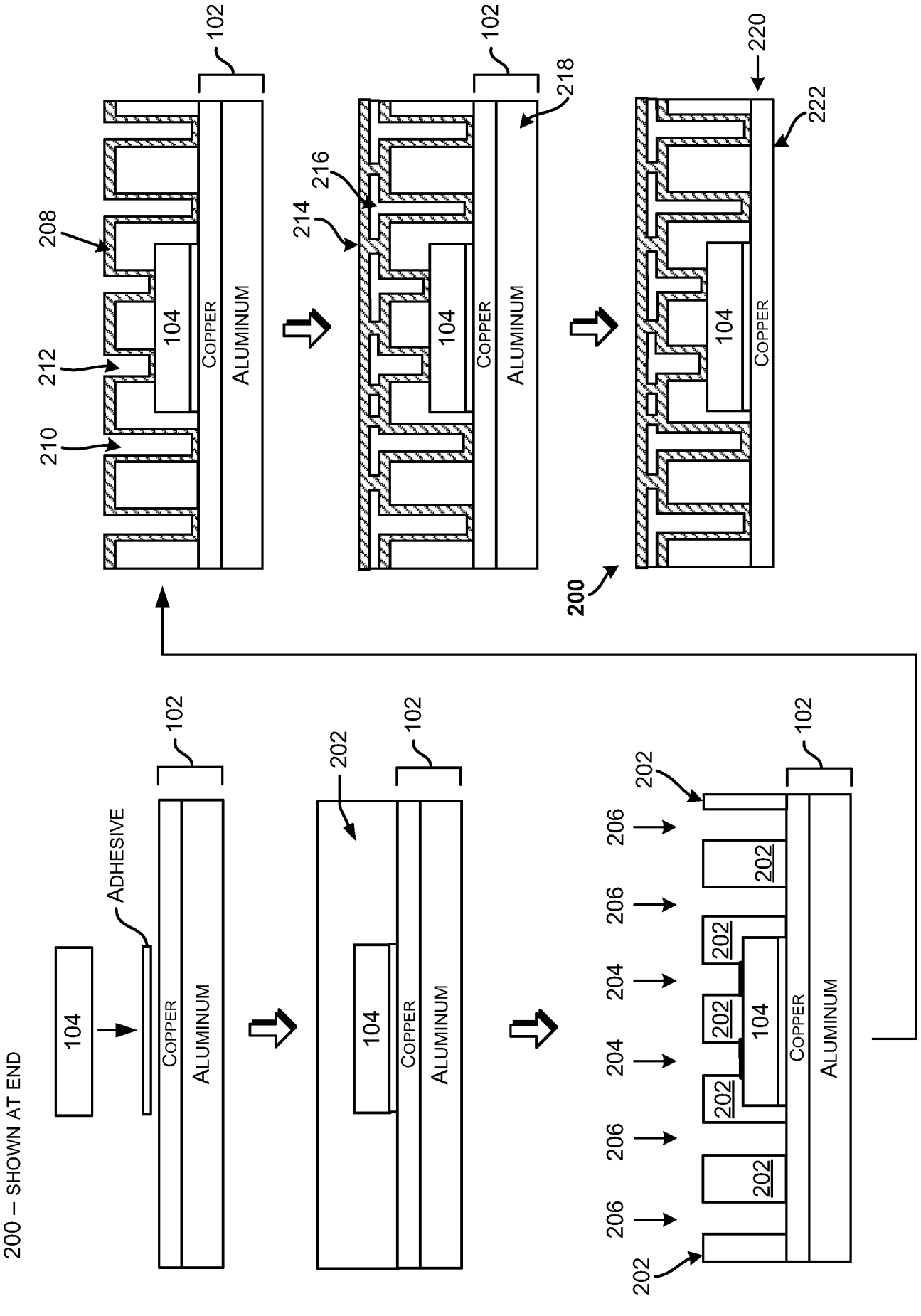
128
130
132

FIG. 1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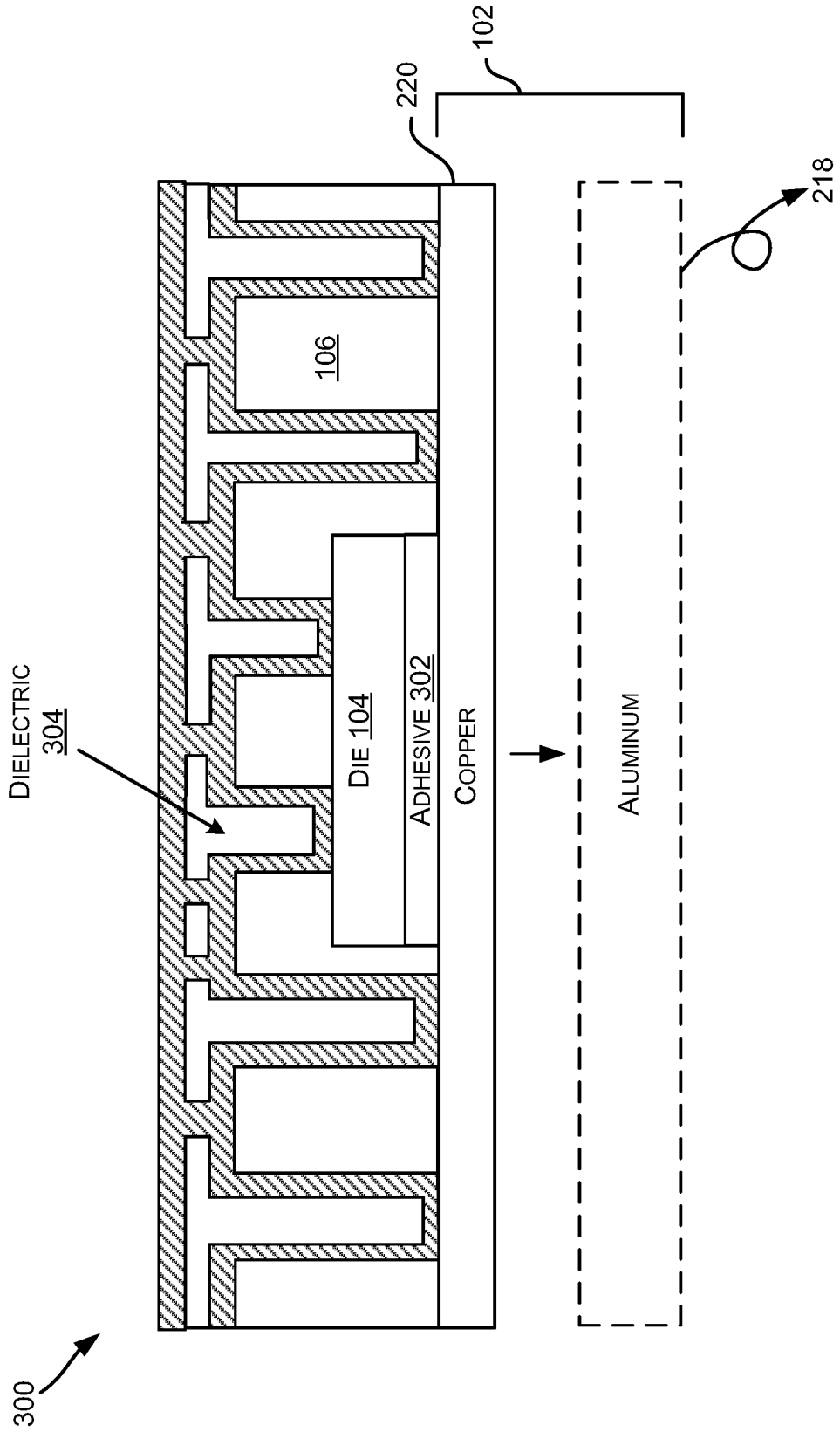
222
200

FIG. 2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DIE 104
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COPPER
ALUMINUM
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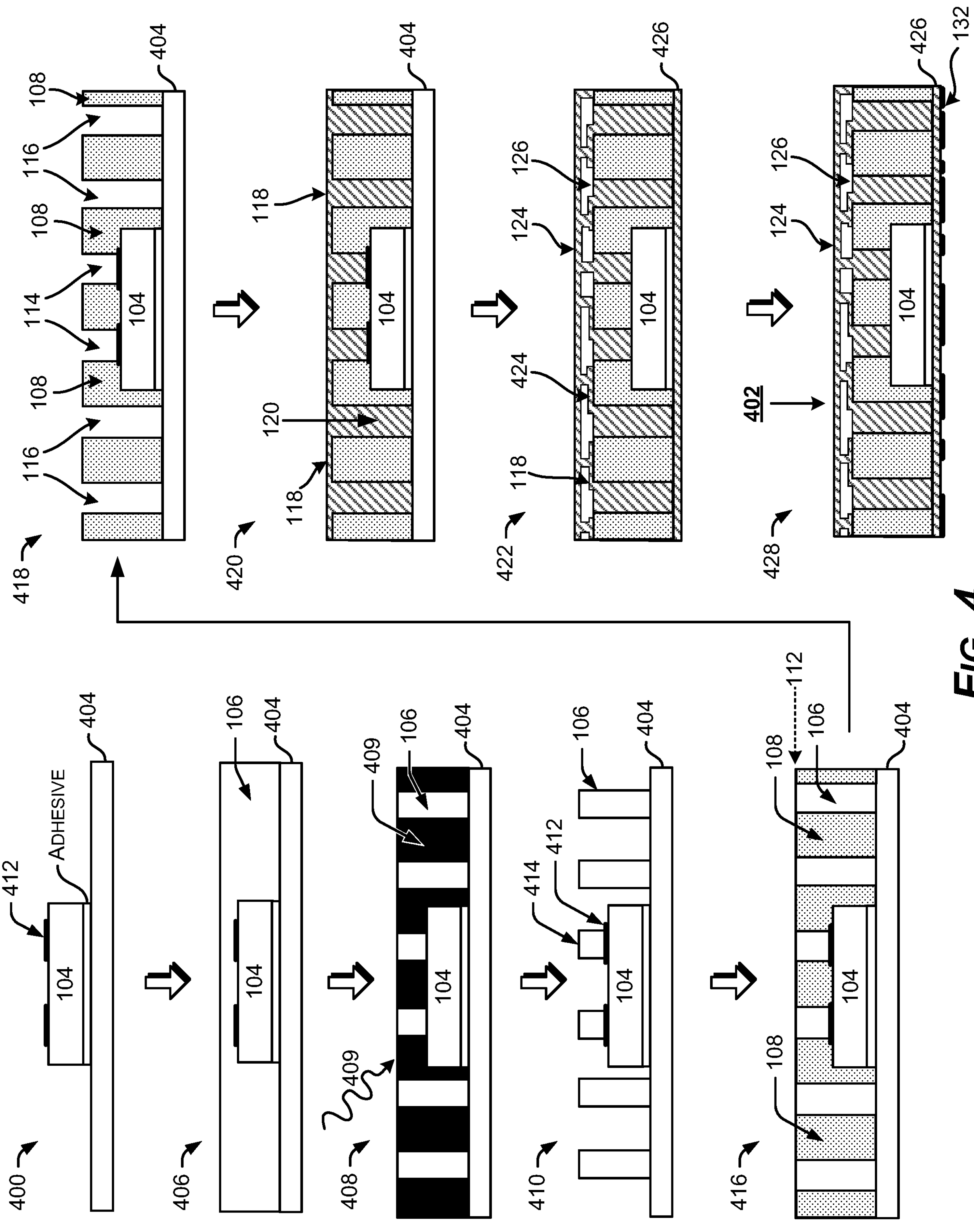
FIG. 3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124
126
424
428
402
132

FIG. 4

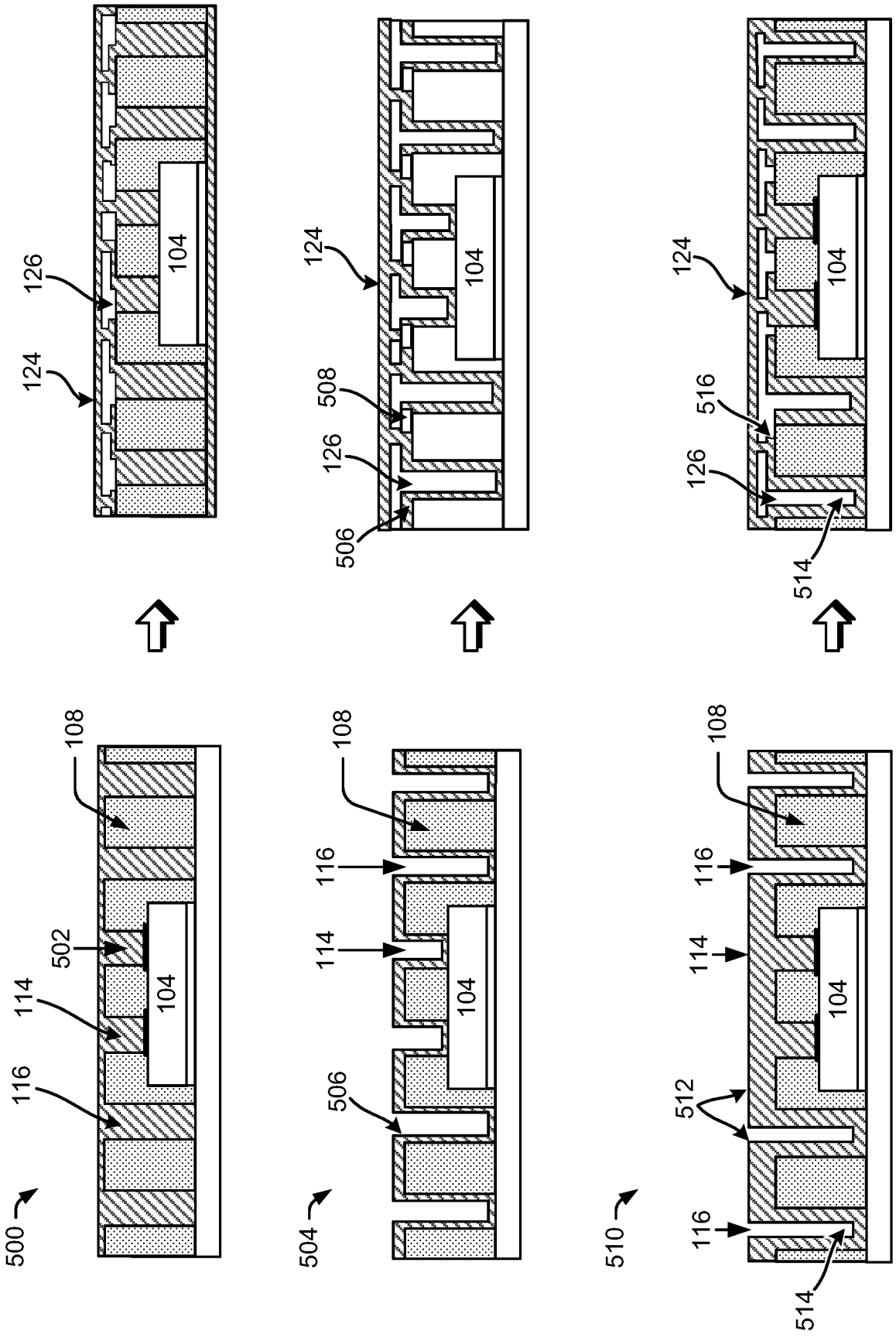


FIG. 5

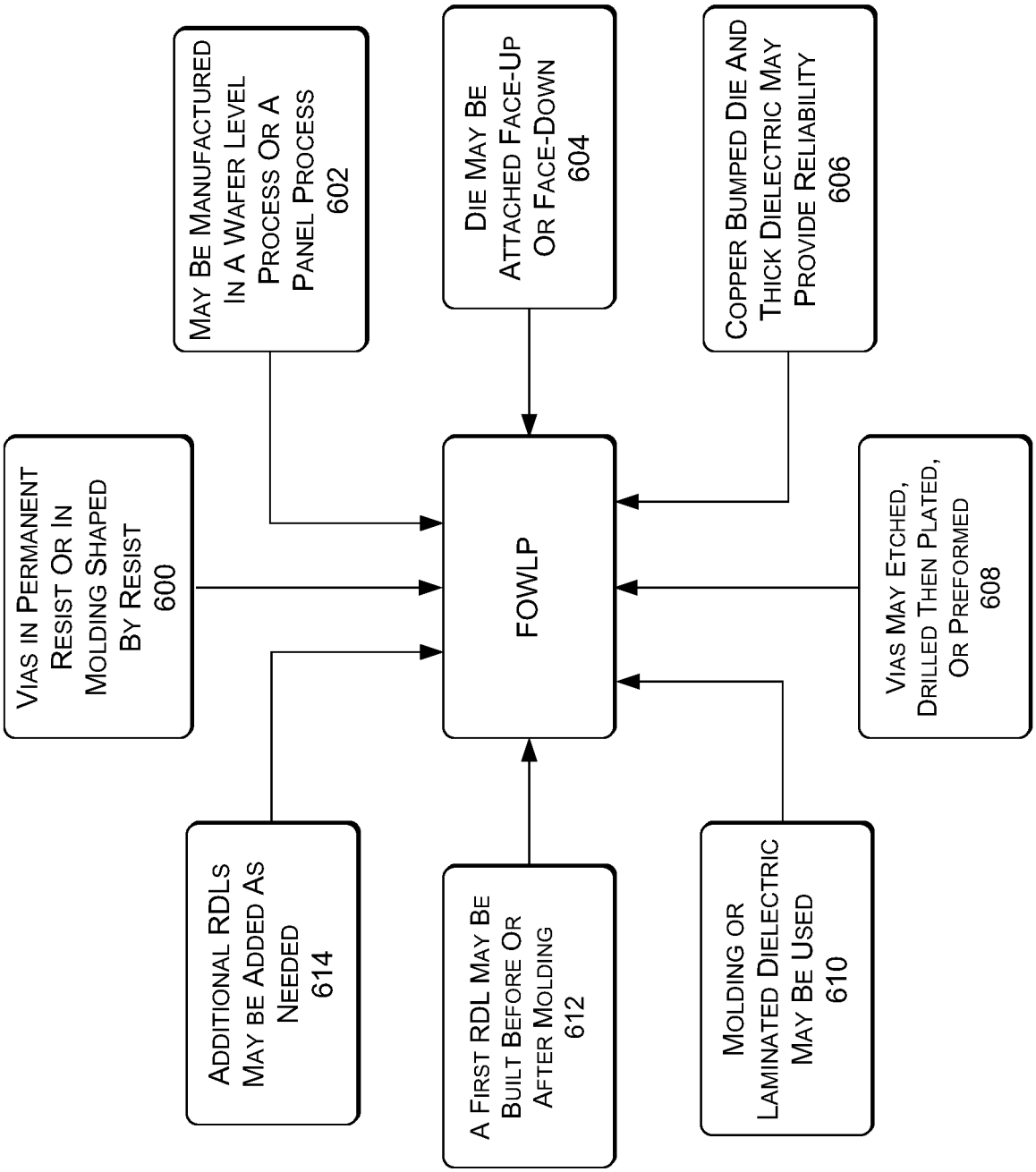
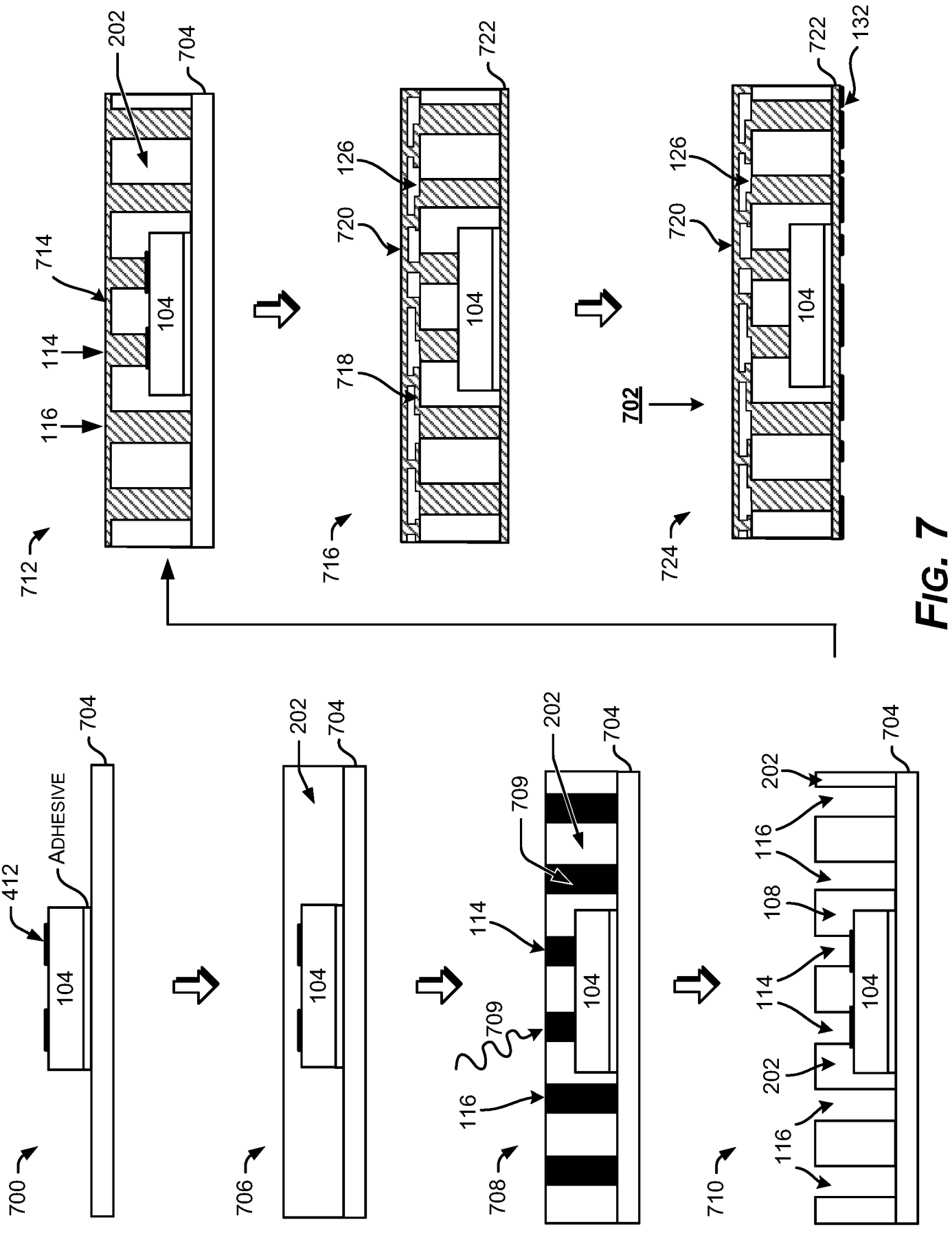

FOWLP
VIAS IN PERMANENT RESIST OR IN MOLDING SHAPED BY RESIST 600
MAY BE MANUFACTURED IN A WAFER LEVEL PROCESS OR A PANEL PROCESS 602
DIE MAY BE ATTACHED FACE-UP OR FACE-DOWN 604
COPPER BUMPED DIE AND THICK DIELECTRIC MAY PROVIDE RELIABILITY 606
VIAS MAY ETCHED, DRILLED THEN PLATED, OR PREFORMED 608
MOLDING OR LAMINATED DIELECTRIC MAY BE USED 610
A FIRST RDL MAY BE BUILT BEFORE OR AFTER MOLDING 612
ADDITIONAL RDLS MAY BE ADDED AS NEEDED 614

FIG. 6

6/11


700
412
ADHESIVE
704
104
706
202
704
104
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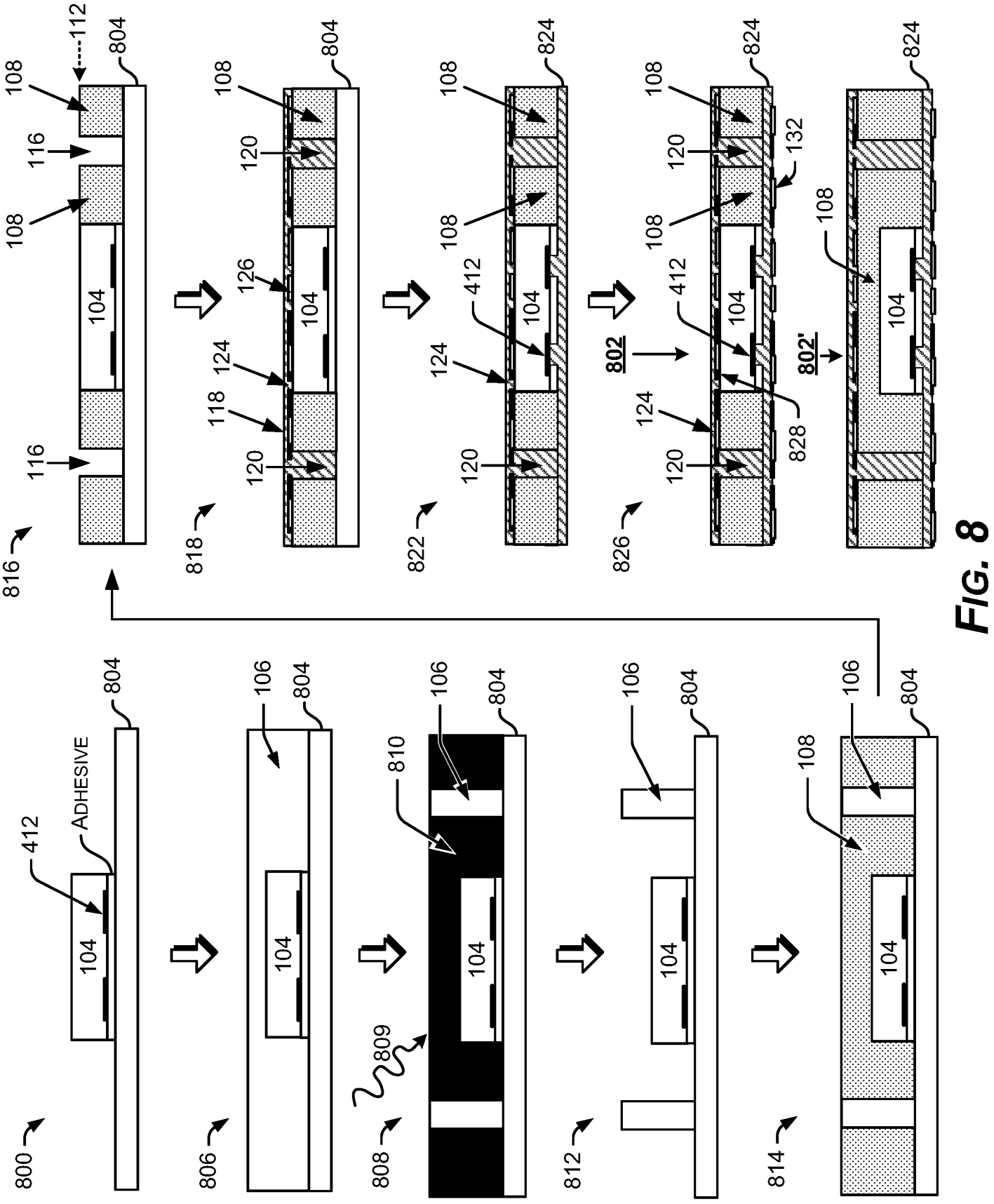
202
704
114
104
709
116
710
704
202
116
108
114
104
202
116
712
202
704
714
114
116
104
716
722
126
720
104
718
724
722
132
126
720
104
702

FIG. 7


800
806
808
812
814
816
818
822
826
104
106
108
112
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120
124
126
132
412
ADHESIVE
804
809
810
824
802
802'
828

FIG. 8

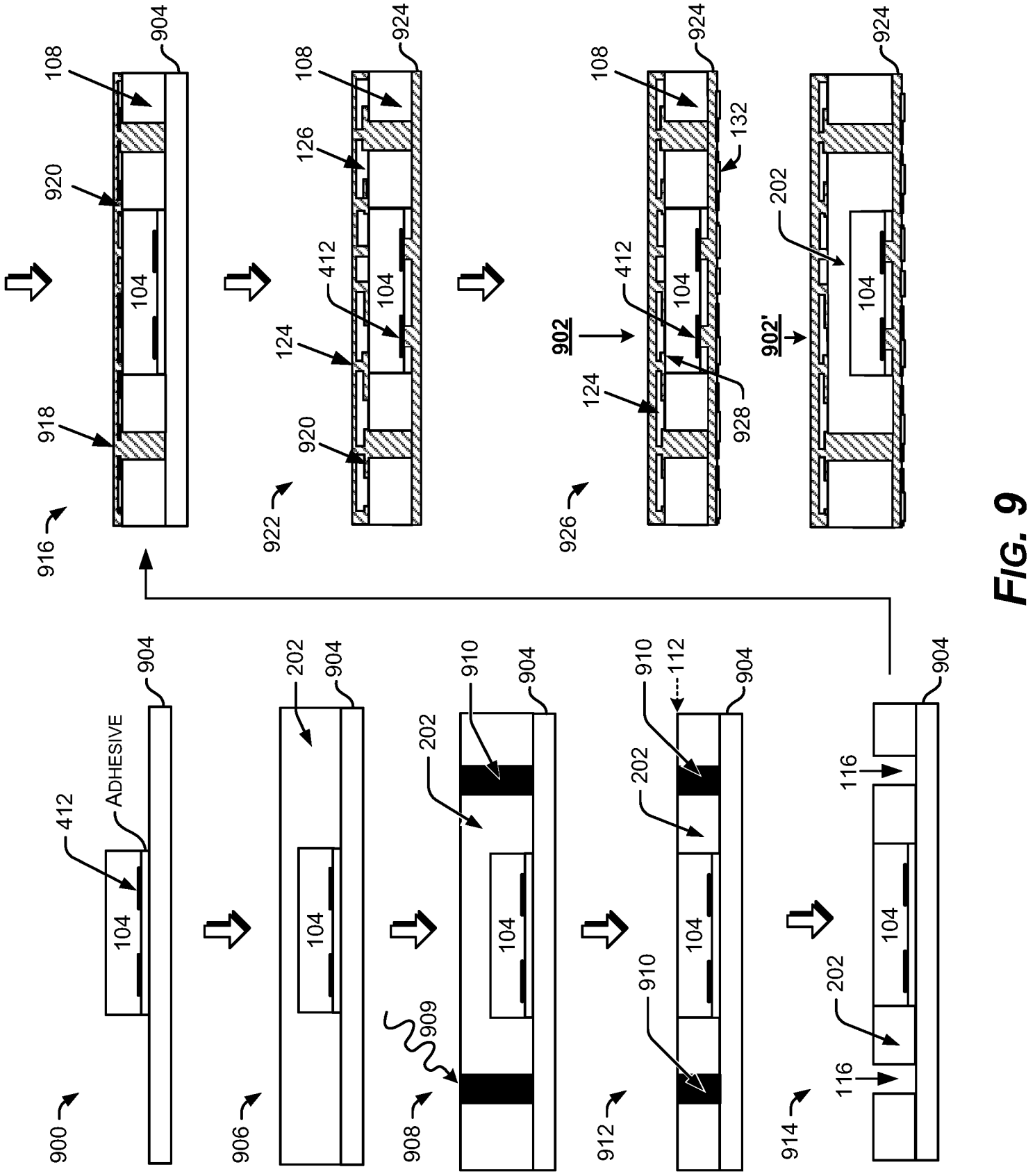
900
906
908
912
914
916
922
926
902
902'
ADHESIVE
104
108
112
116
124
126
132
202
412
904
909
910
918
920
924
928

FIG. 9

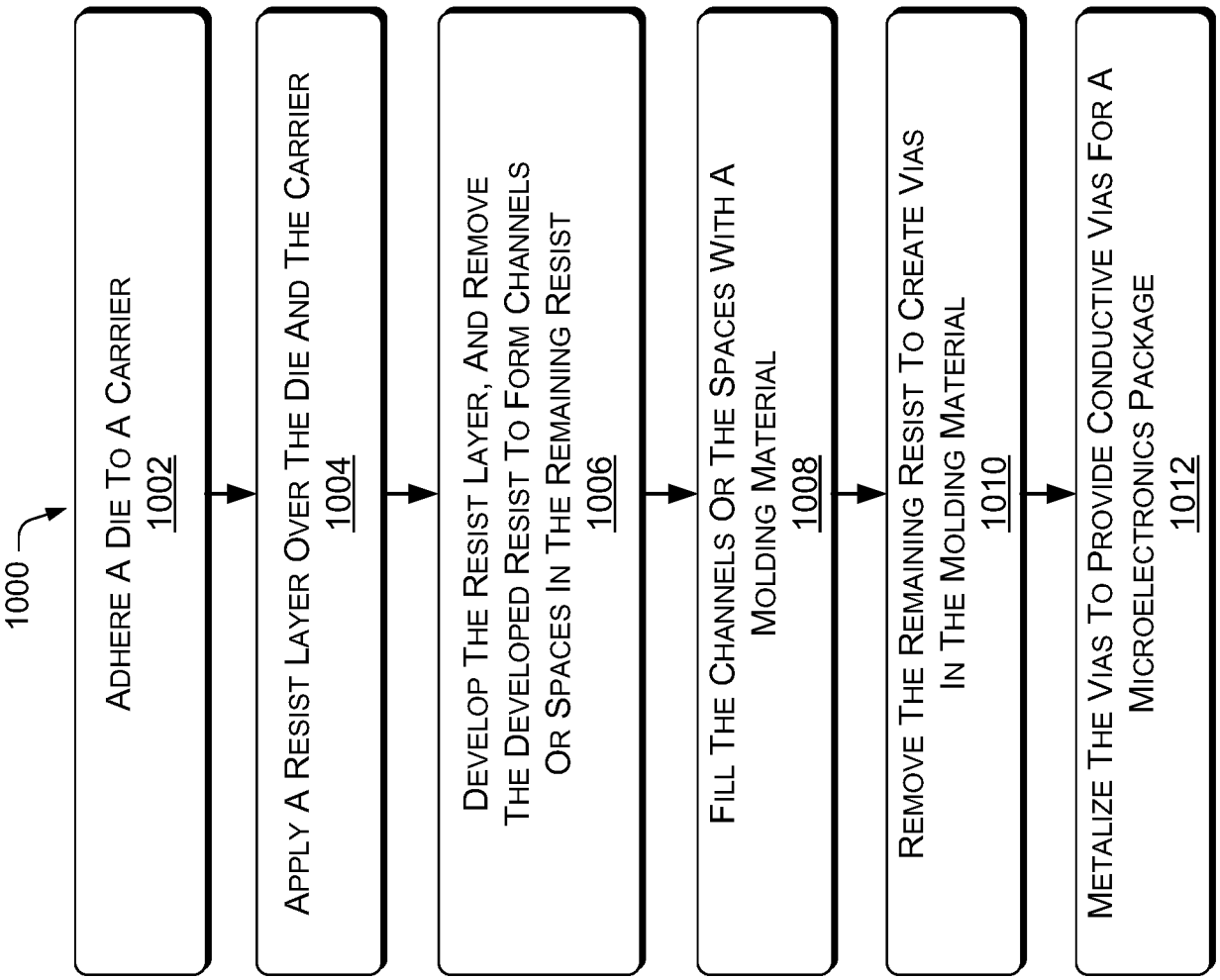
1000
Adhere A Die To A Carrier
1002
Apply A Resist Layer Over The Die And The Carrier
1004
Develop The Resist Layer, And Remove The Developed Resist To Form Channels Or Spaces In The Remaining Resist
1006
Fill The Channels Or The Spaces With A Molding Material
1008
Remove The Remaining Resist To Create Vias In The Molding Material
1010
Metalize The Vias To Provide Conductive Vias For A Microelectronics Package
1012

FIG. 10

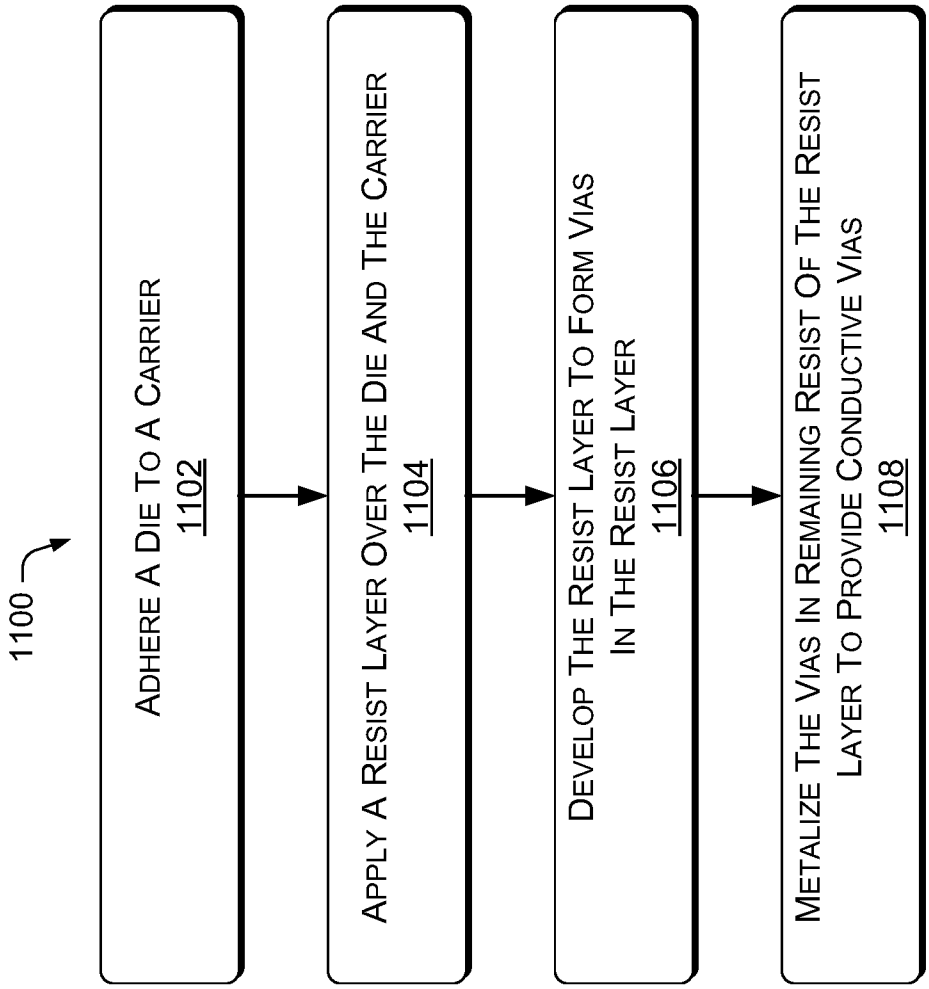
1100
ADHERE A DIE TO A CARRIER
1102
APPLY A RESIST LAYER OVER THE DIE AND THE CARRIER
1104
DEVELOP THE RESIST LAYER TO FORM VIAS IN THE RESIST LAYER
1106
METALIZE THE VIAS IN REMAINING RESIST OF THE RESIST LAYER TO PROVIDE CONDUCTIVE VIAS
1108

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/027112

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/00(2006.01)i, H01L 23/538(2006.01)i, H01L 23/498(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/00; H01L 21/68; H01L 21/027; H01L 23/48; H01L 23/544; H01L 23/12; H05K 3/00; H01L 23/49; H01L 25/07; H01L 25/18; H01L 23/538; H01L 23/498

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: carrier, die, resist, vias, metal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2011-0114165 A (AMKOR TECHNOLOGY KOREA, INC.) 19 October 2011 See paragraphs 31-45 and figures 1a-2	1-20
Y	KR 10-2015-0144305 A (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 24 December 2015 See paragraphs 12-33 and figures 1a-3a.	1-20
Y	JP 2014-533892 A (JIANGSU CHANGJIANG ELECTRONIC TECHNOLOGY CO., LTD.) 15 December 2014 See paragraphs 15-27 and figures 1-9.	11,14
A	US 2011-0252637 A1 (KIMITAKA ENDO et al.) 20 October 2011 See claims 1-8 and figures 1(A)-7(A).	1-20
A	KR 10-2011-0076606 A (HANA MICRON INC.) 06 July 2011 See claims 1-5 and figures 1-5.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 July 2018 (27.07.2018)	**27 July 2018 (27.07.2018)**

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Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/027112

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JP 2014-533892 A	15/12/2014	CN 102376672 A	14/03/2012
		CN 102376672 B	29/10/2014
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		WO 2006-039633 A3	24/08/2006
KR 10-2011-0076606 A	06/07/2011	KR 10-1059629 B1	25/08/2011