United States Patent

Dlugos et al.

[15] **3,692,988**

[45] **Sept. 19, 1972**

[54] **PARCEL POSTAGE METERING SYSTEM**

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[22] Filed: **Jan. 18, 1971**

[21] Appl. No.: **107,223**

[52] **U.S. Cl.**.....**235/151.33,** 177/25

[51] **Int. Cl.**.....**G06f 15/20,** G01g 19/413

[58] **Field of Search** .....235/151.33, 177; 177/25, 58, 177/61, DIG. 1, DIG. 3; 340/146.2, 173 LM

[56] **References Cited**

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Primary Examiner—Eugene G. Botz
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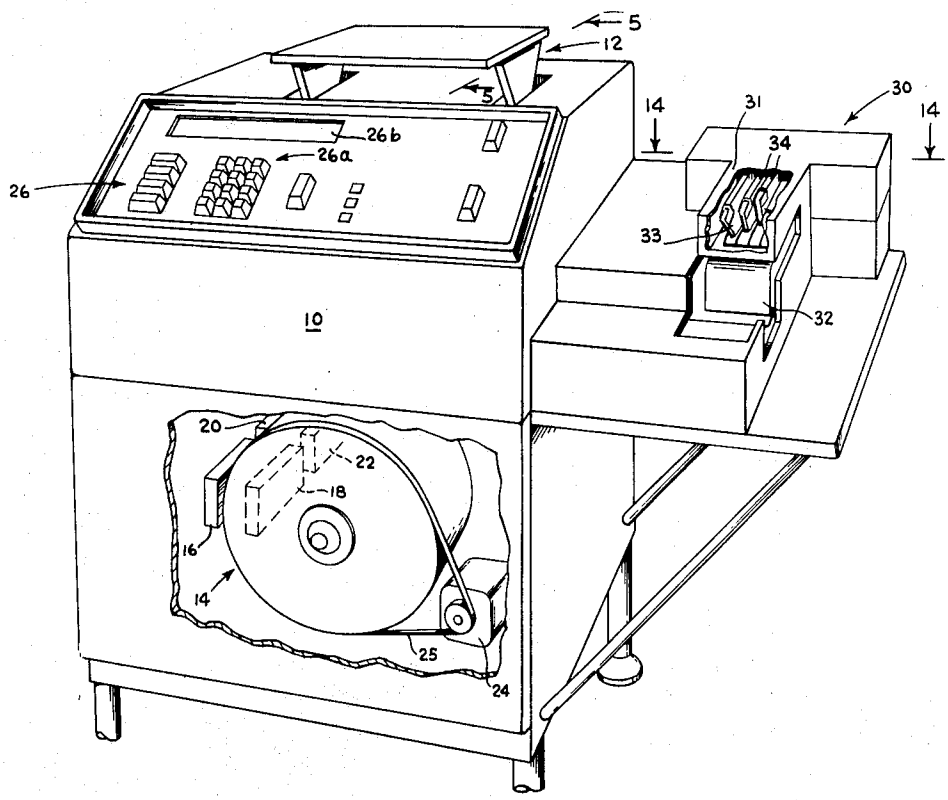
Attorney—William D. Soltow, Jr., Albert W. Scribner, Martin D. Wittstein and Louis A. Tirelli

[57] **ABSTRACT**

A parcel postage metering system comprises a scale for providing a parcel weight reading which is used in conjunction with the parcel destination (postal zone) to enter a postage memory and obtain the appropriate postage. The thus obtained postage controls apparatus for setting a postage meter to issue a stamp imprinted with the appropriate parcel postage. A zip code to zone conversion memory is incorporated to provide the appropriate zone entry into the postage rate memory, given the zip code of the parcel destination.

23 Claims, 20 Drawing Figures



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SHEET 01 OF 14

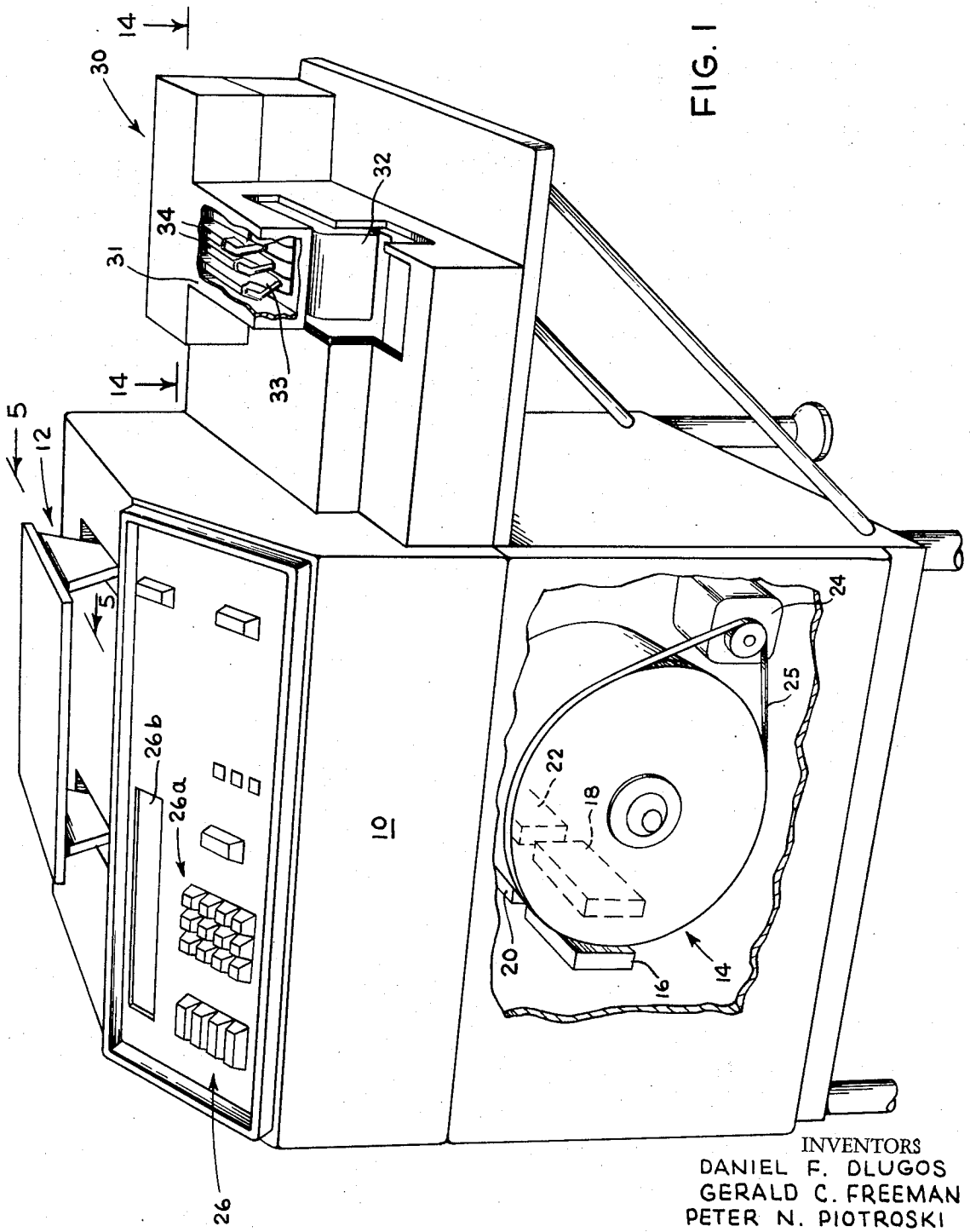

FIG. 1

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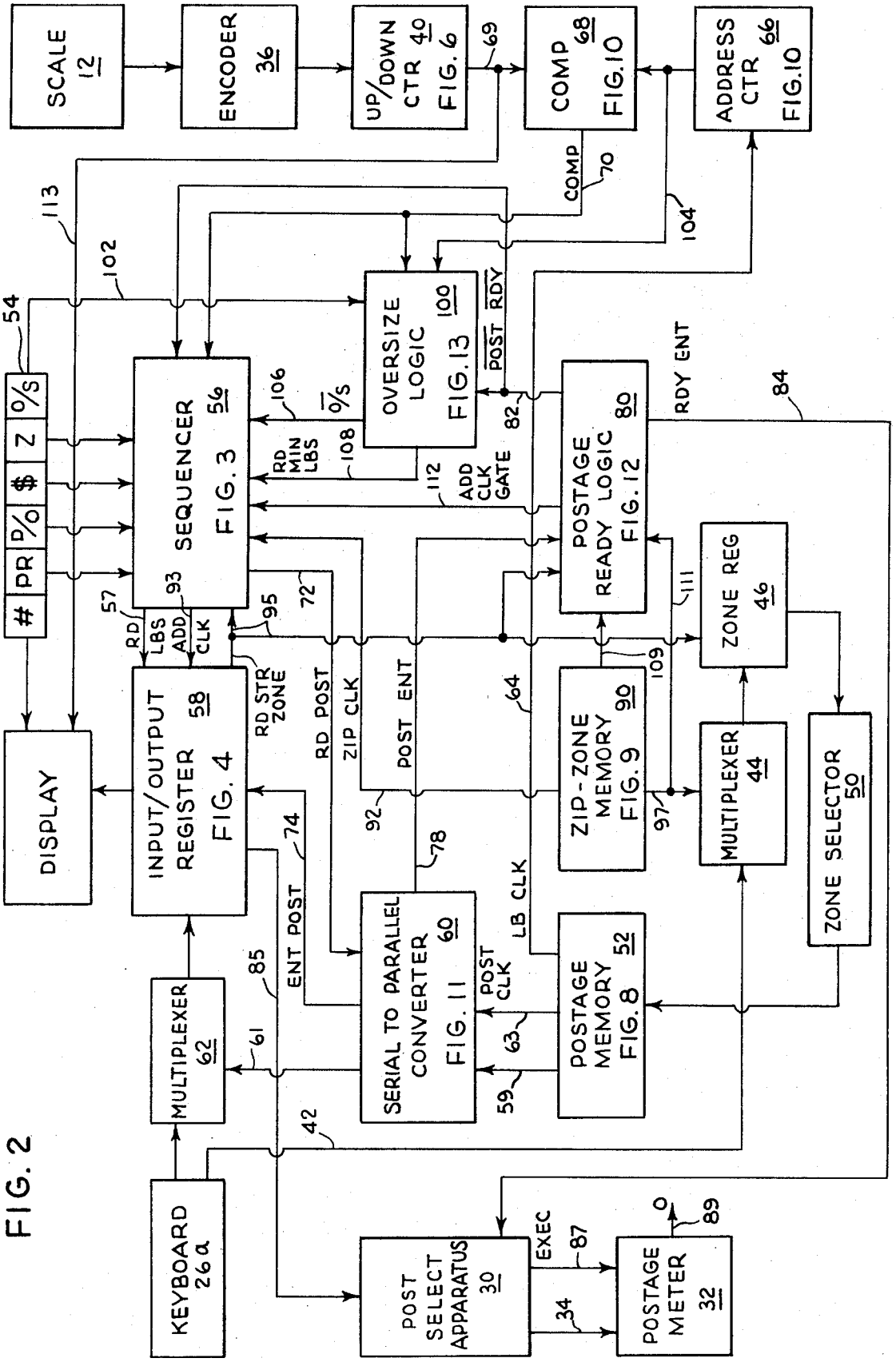

SCALE 12
ENCODER 36
UP/DOWN CTR 40 FIG. 6
COMP 68 FIG. 10
ADDRESS CTR 66 FIG. 10
COMP
70
69
104
113
102
54
OVERSIZE LOGIC 100 FIG. 13
POST RDY
82
RDY ENT
84
SEQUENCER FIG. 3 56
106
108
112
RD MIN LBS
ADD CLK GATE
POSTAGE READY LOGIC FIG. 12 80
ZONE REG 46
111
109
PR P/O $ Z O/S
57
RD
LBS
ADD
CLK
93
95
72
INPUT/OUTPUT REGISTER FIG. 4 58
RD STR ZONE
RD POST
ZIP CLK
POST ENT
64
ZIP-ZONE MEMORY FIG. 9 90
MULTIPLEXER 44
ZONE SELECTOR 50
DISPLAY
92
78
97
74
ENT POST
LB CLK
SERIAL TO PARALLEL CONVERTER FIG. 11 60
POST CLK
POSTAGE MEMORY FIG. 8 52
MULTIPLEXER 62
85
61
63
59
42
KEYBOARD 26a
POST SELECT APPARATUS 30
EXEC
87
34
POSTAGE METER 32
0
89

FIG. 2

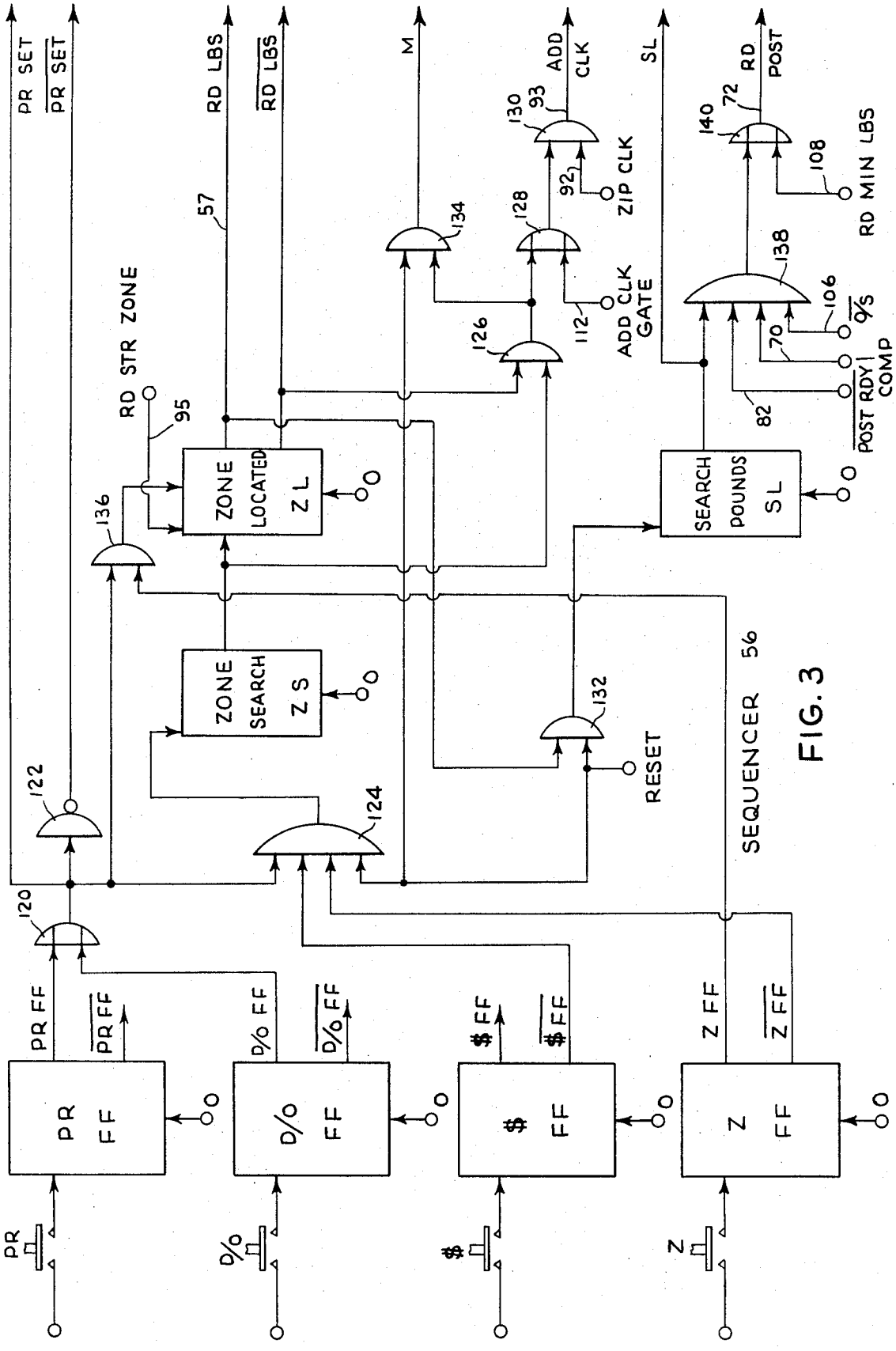

PR SET
PR SET
RD LBS
RD LBS
M
ADD CLK
SL
RD POST
57
130
93
140
72
92
ZIP CLK
108
RD MIN LBS
RD STR ZONE
95
128
134
138
ADD CLK GATE
112
106
%S
126
70
POST RDY / COMP
82
136
ZONE LOCATED Z L
SEARCH POUNDS S L
ZONE SEARCH Z S
122
124
132
RESET
SEQUENCER 56
120
PR FF
PR FF
D/% FF
D/% FF
FF
FF
Z FF
Z FF
PR FF
D/% FF
FF
Z FF
PR
D/%
#
Z

FIG. 3

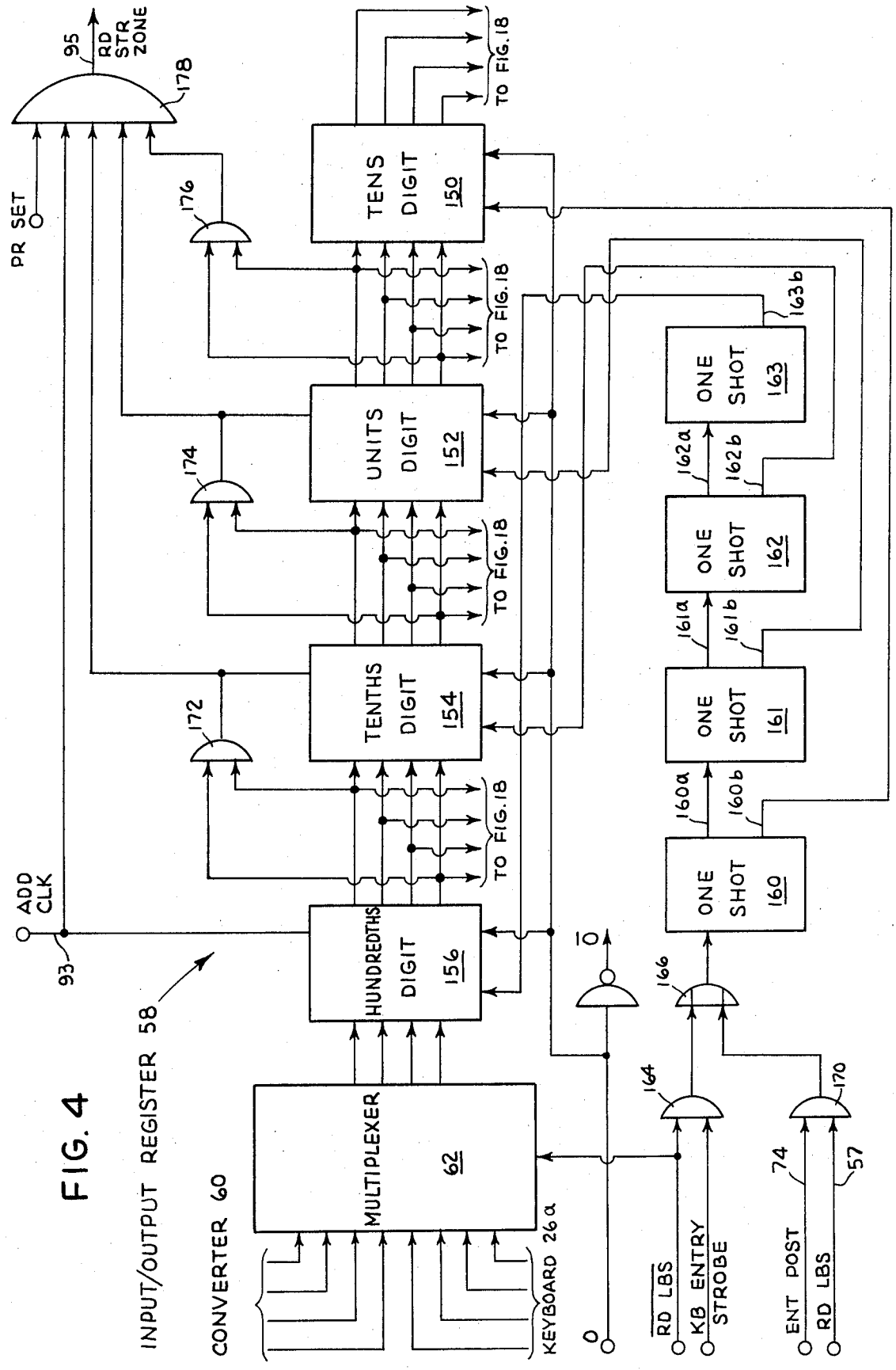

95
RD STR ZONE
178
PR SET
176
TENS DIGIT 150
TO FIG. 18
174
UNITS DIGIT 152
TO FIG. 18
172
TENTHS DIGIT 154
TO FIG. 18
ADD CLK
93
HUNDREDTHS DIGIT 156
TO FIG. 18
INPUT/OUTPUT REGISTER 58
CONVERTER 60
MULTIPLEXER 62
KEYBOARD 26a
ONE SHOT 160
160a
160b
ONE SHOT 161
161a
161b
ONE SHOT 162
162a
162b
ONE SHOT 163
163b
166
164
170
RD LBS
KB ENTRY STROBE
ENT POST
RD LBS
74
57

FIG. 4

FIG. 5

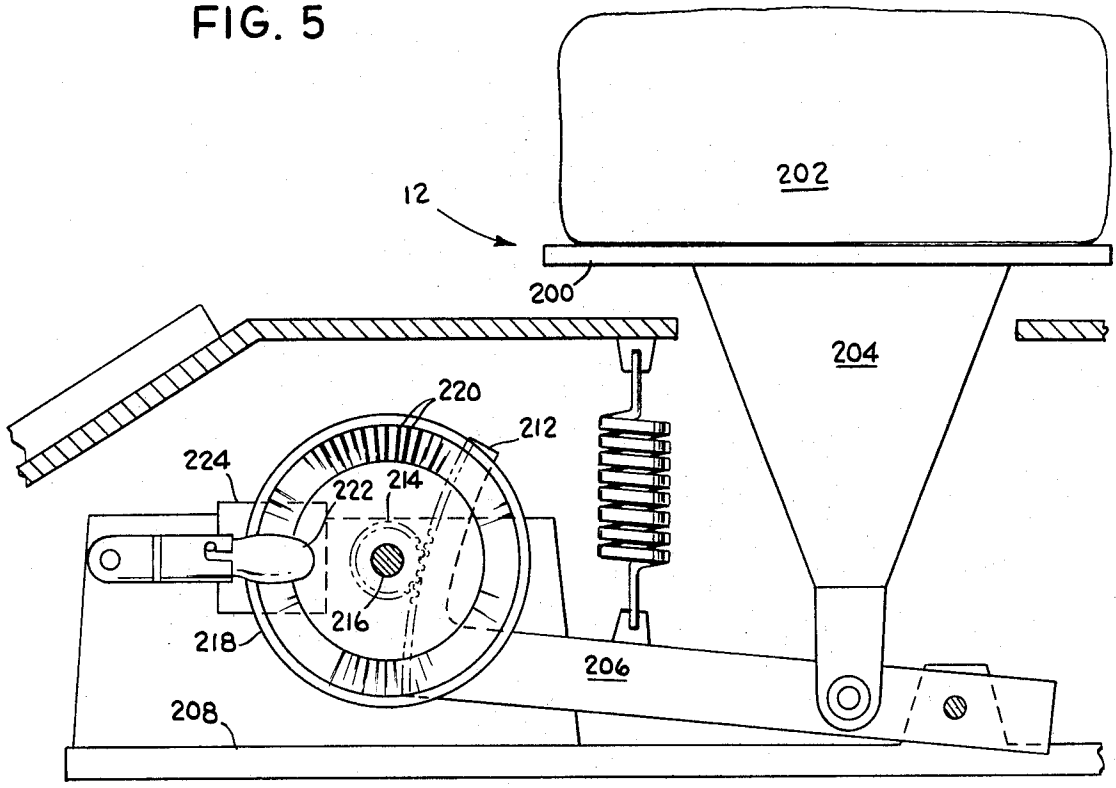

202
12
200
204
220
212
224
222
214
216
218
206
208

FIG. 20

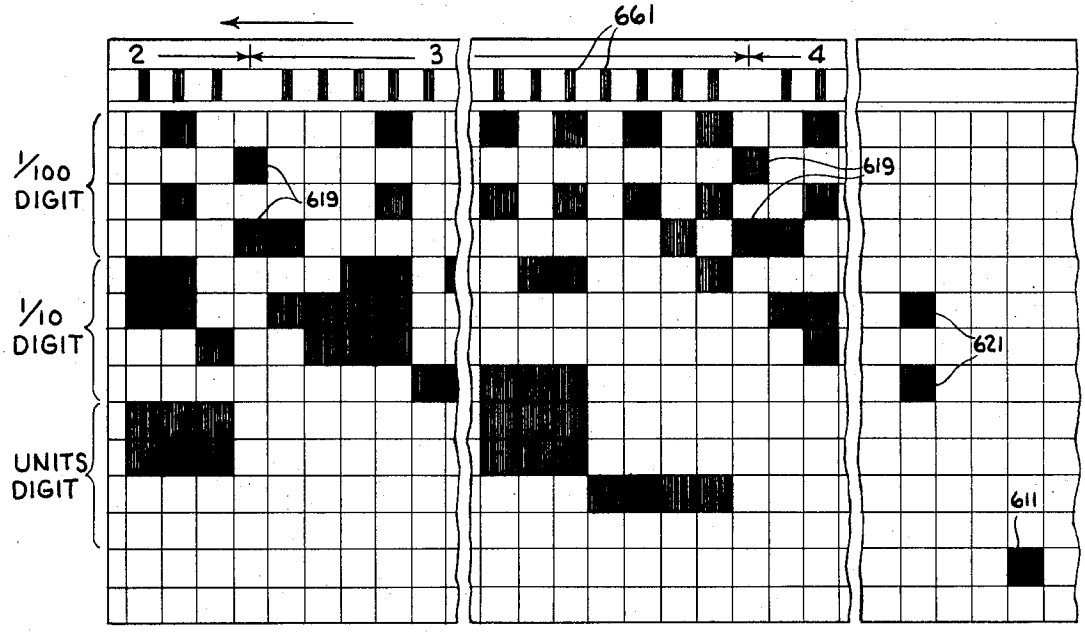

661
2
3
4
1/100 DIGIT
1/10 DIGIT
UNITS DIGIT
619
619
621
611

FIG. 6

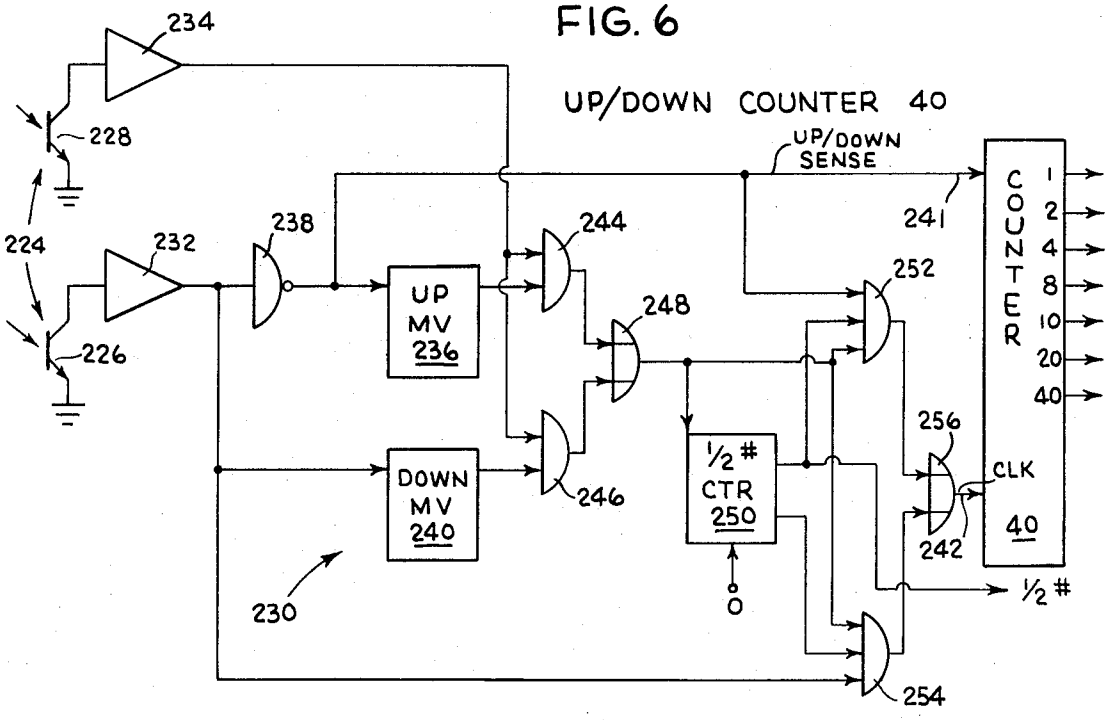

UP/DOWN COUNTER 40
234
228
224
232
226
238
UP MV 236
DOWN MV 240
230
244
246
248
252
254
256
242
½ # CTR 250
0
UP/DOWN SENSE
241
COUNTER
1
2
4
8
10
20
40
CLK
40
½ #

FIG. 7

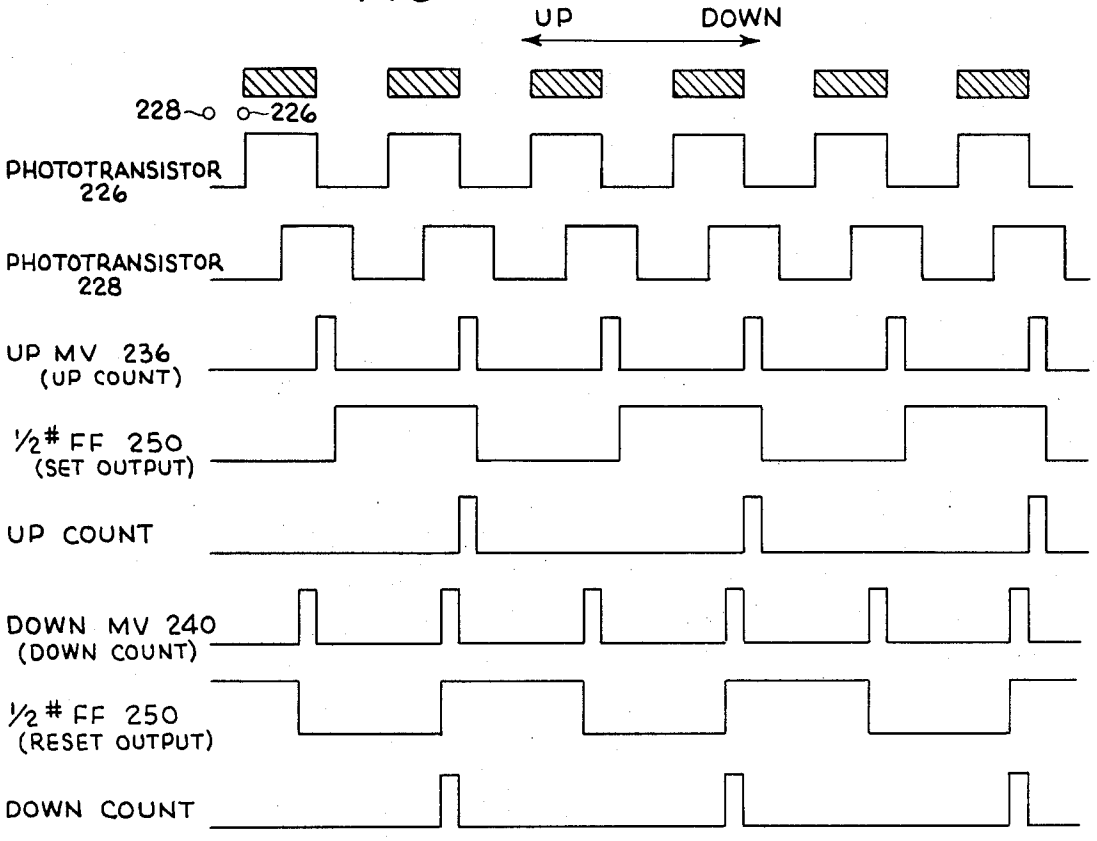

UP
DOWN
228
226
PHOTOTRANSISTOR 226
PHOTOTRANSISTOR 228
UP MV 236 (UP COUNT)
½# FF 250 (SET OUTPUT)
UP COUNT
DOWN MV 240 (DOWN COUNT)
½# FF 250 (RESET OUTPUT)
DOWN COUNT

FIG. 8

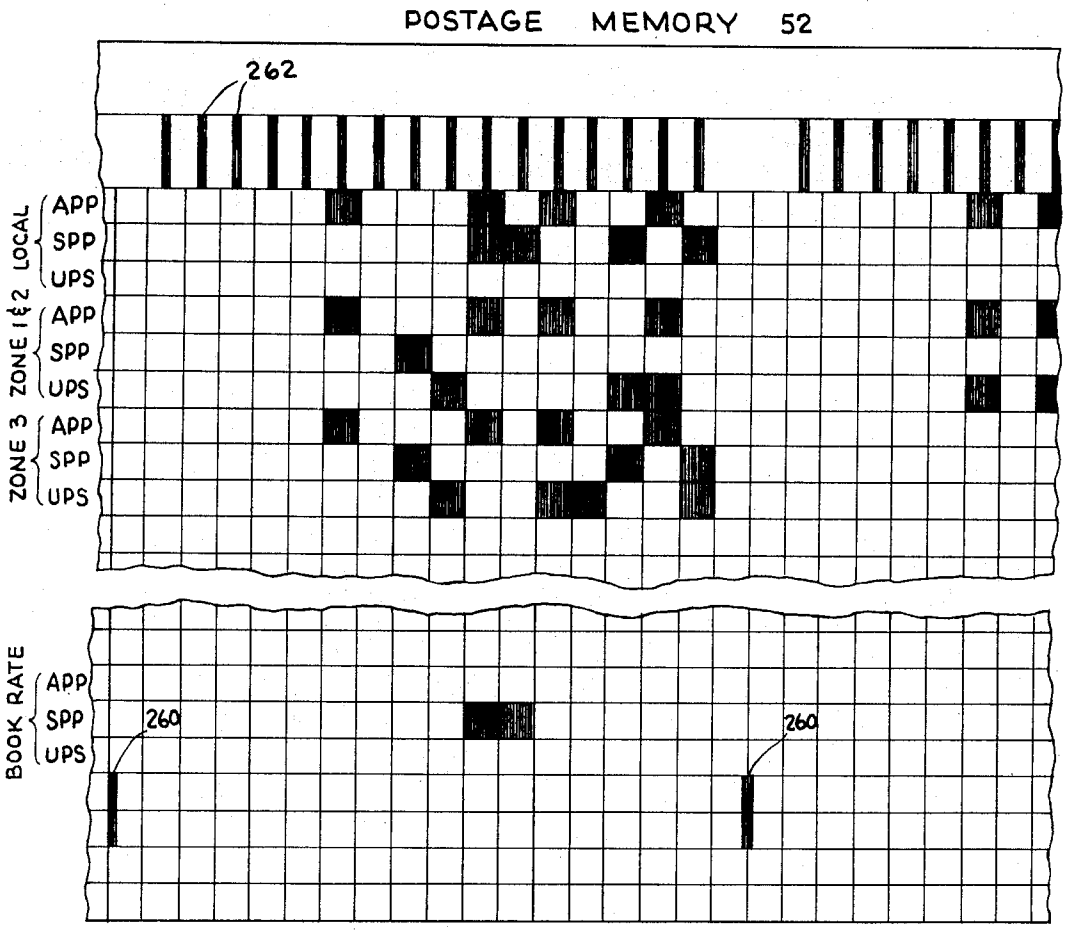

POSTAGE MEMORY 52
262
LOCAL
APP
SPP
UPS
ZONE 1 & 2
APP
SPP
UPS
ZONE 3
APP
SPP
UPS
BOOK RATE
APP
SPP
UPS
260
260

FIG. 9

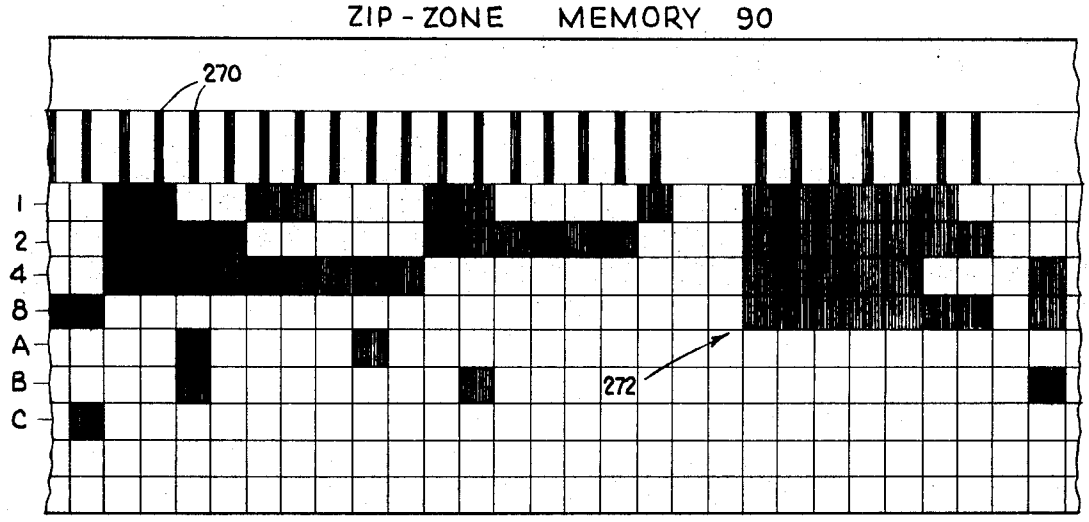

ZIP - ZONE MEMORY 90
270
1
2
4
8
A
B
C
272

FIG. 10

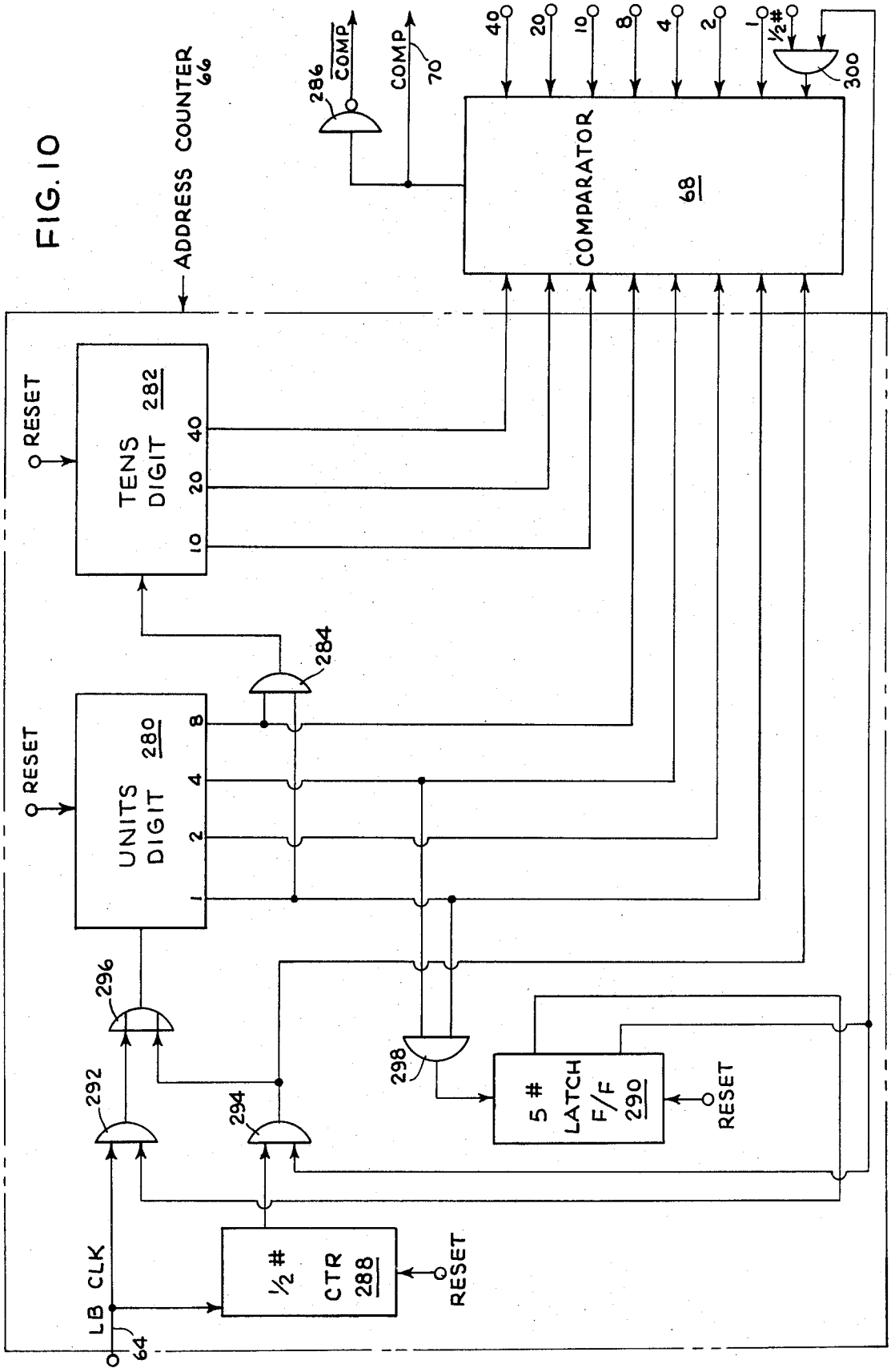
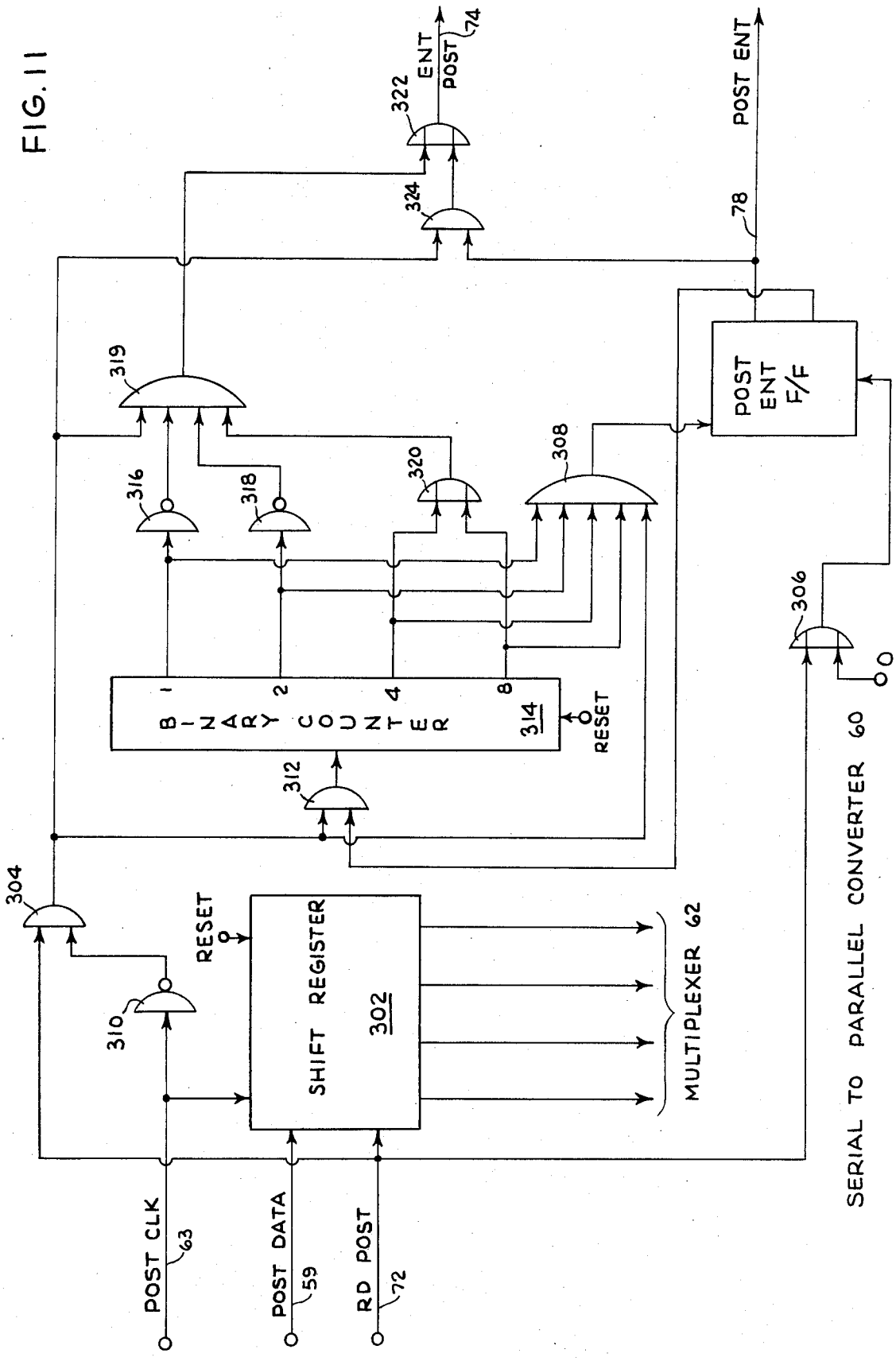

ADDRESS COUNTER 66
286
COMP
COMP
70
40
20
10
8
4
2
1
½#
300
COMPARATOR 68
RESET
TENS DIGIT 282
40
20
10
284
RESET
UNITS DIGIT 280
8
4
2
1
296
298
292
294
5 # LATCH F/F 290
RESET
LB CLK
64
½ # CTR 288
RESET

FIG. 11


322
POST ENT
74
324
78
POST ENT
319
POST ENT F/F
316
318
320
308
306
1
2
4
8
BINARY COUNTER
314
RESET
312
304
RESET
SHIFT REGISTER
302
310
MULTIPLEXER 62
SERIAL TO PARALLEL CONVERTER 60
POST CLK
63
POST DATA
59
RD POST
72

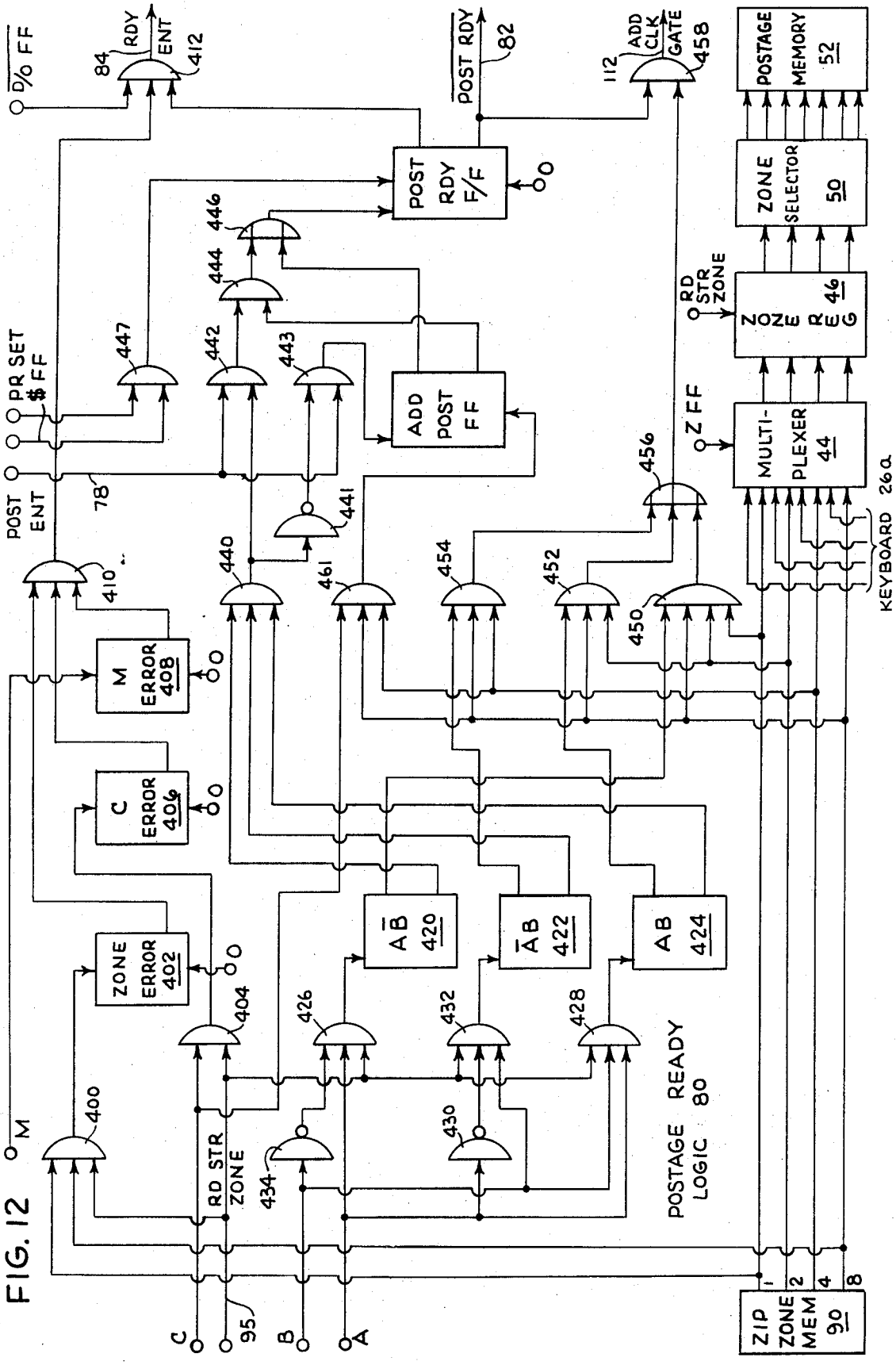

D/O FF
84
RDY ENT
412
POST RDY
82
112
ADD CLK GATE
458
POSTAGE MEMORY 52
POST RDY F/F
ZONE SELECTOR 50
446
444
447
442
443
RD STR ZONE
ZONE REG 46
PR SET $ FF
ADD POST FF
MULTI-PLEXER 44
Z FF
456
POST ENT
78
441
410
440
461
454
452
450
KEYBOARD 26a
M ERROR 408
C ERROR 406
ZONE ERROR 402
404
426
432
428
AB̄ 420
ĀB 422
AB 424
400
M
RD STR ZONE
434
430
POSTAGE READY LOGIC 80
C
95
B
A
ZIP ZONE MEM 90
1
2
4
8

FIG. 12

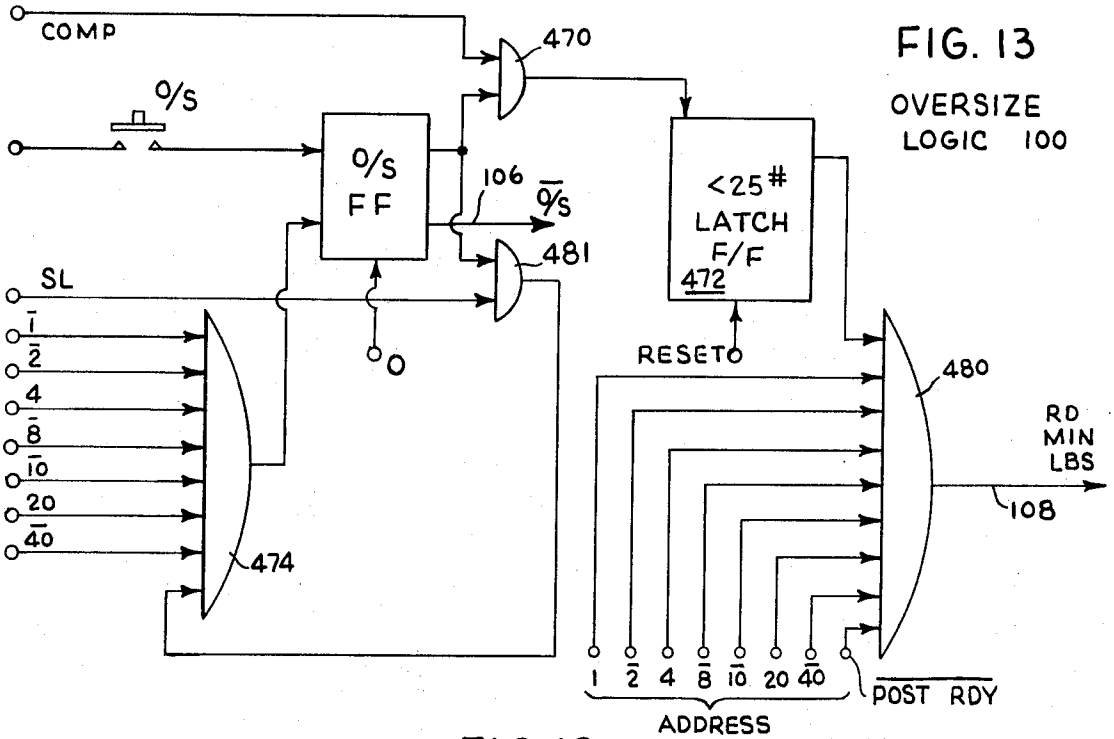
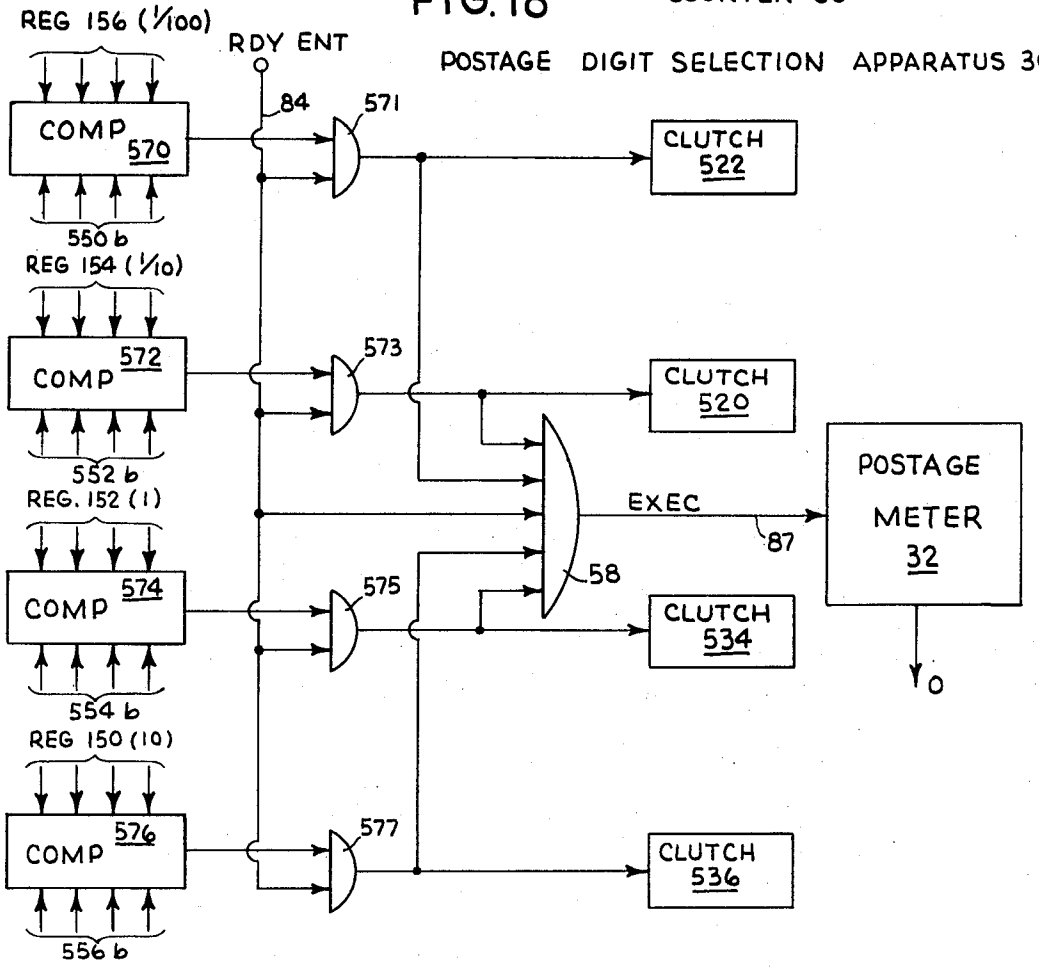


FIG. 13
OVERSIZE LOGIC 100

FIG. 18
POSTAGE DIGIT SELECTION APPARATUS 30



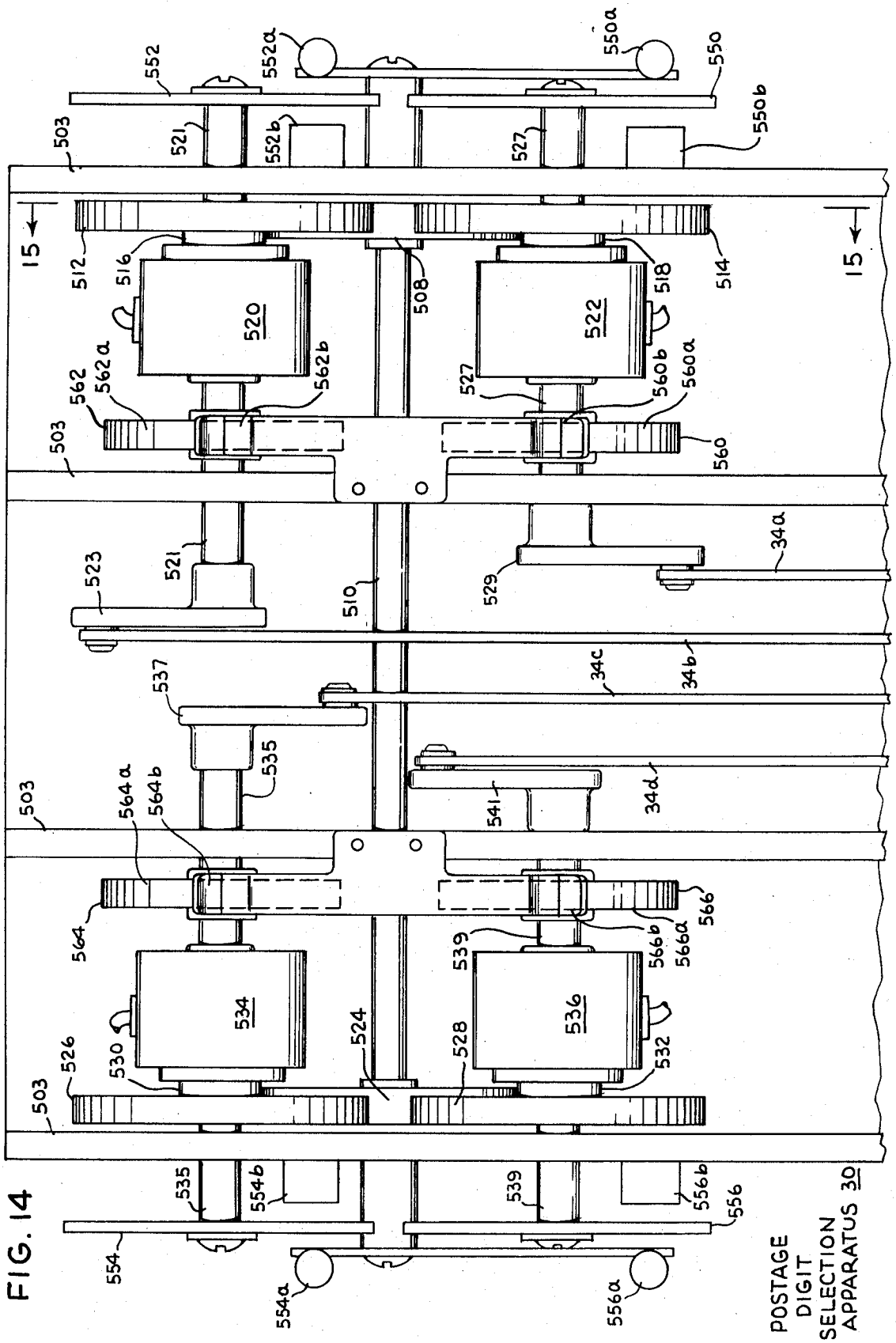

552
552a
550a
550
550b
503
521
552b
527
15
512
516
520
508
522
518
514
562
562a
562b
560b
560a
560
523
510
529
34a
537
34c
34b
535
564a
564b
541
34d
564
566
566b
566a
539
534
536
524
528
532
526
530
554
554a
556a
POSTAGE
DIGIT
SELECTION
APPARATUS 30

FIG. 14

FIG. 15

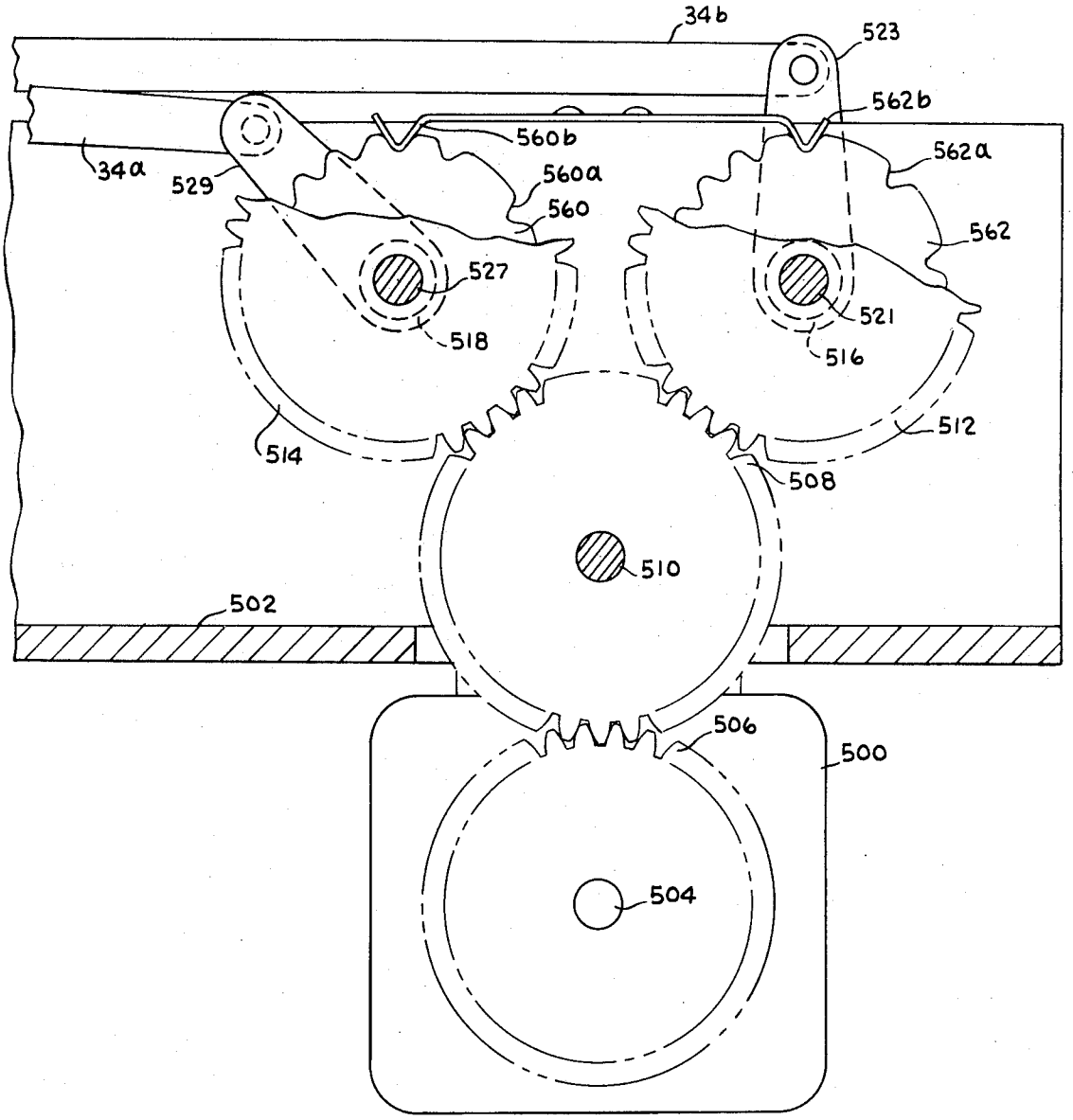


FIG. 16

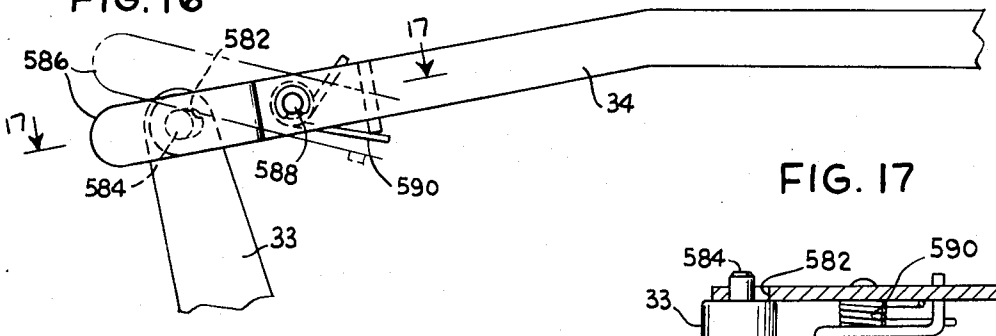
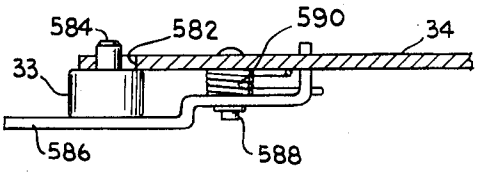


FIG. 17



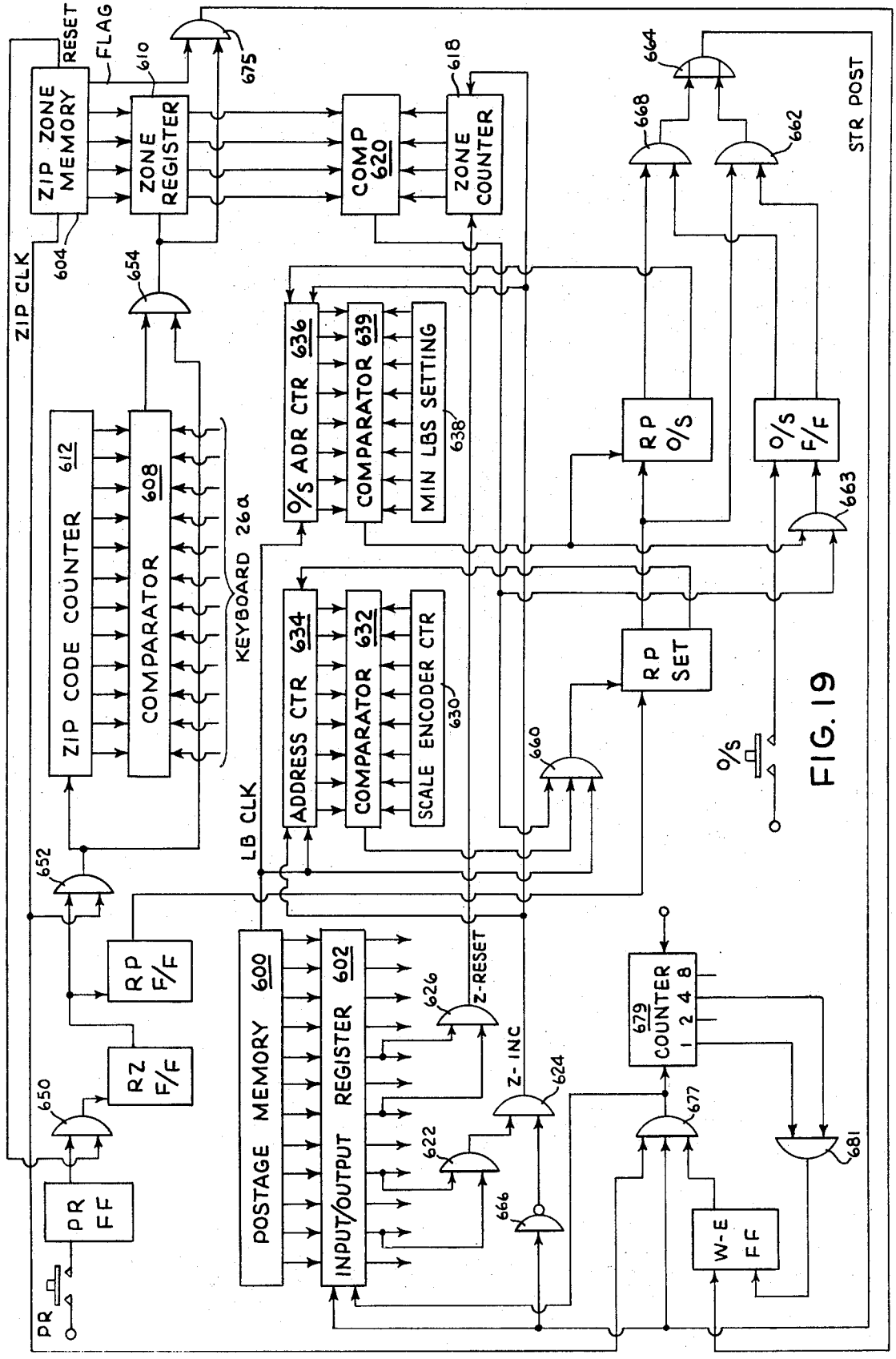

ZIP ZONE MEMORY
RESET
FLAG
610
675
ZONE REGISTER
COMP 620
618
ZONE COUNTER
664
668
662
STR POST
ZIP CLK
604
654
% ADR CTR 636
COMPARATOR 639
MIN LBS SETTING
638
RP %S
% F/F
663
ZIP CODE COUNTER 612
COMPARATOR 608
KEYBOARD 26a
ADDRESS CTR 634
COMPARATOR 632
SCALE ENCODER CTR
630
RP SET
660
%S
LB CLK
652
RP F/F
RZ F/F
650
PR F/F
PR
POSTAGE MEMORY 600
INPUT/OUTPUT REGISTER 602
626
Z-RESET
Z-INC
624
622
666
679 COUNTER 1 2 4 8
677
681
W-E F/F

FIG. 19

PARCEL POSTAGE METERING SYSTEM

BACKGROUND OF THE INVENTION

There have been a number of proposals for parcel postage systems to be used in the processing of parcels for mailing or shipping. A comprehensive or universal system must be sufficiently flexible to handle a number of variables which are involved in mailing or shipping parcels. The weight of each parcel must be determined with reasonable accuracy and speed. The distances between the original and the various parcel destinations must be determined in order to identify the appropriate postal zone for each parcel. Then, the postage applicable to each parcel must be determined on the basis of its weight and destination or postal zone. Having determined the applicable postage, a postage meter or the like is ten set up and controlled to issue a stamp imprinted with that postage; the stamp being adhered to the parcel.

There are other factors or variables which a truly universal system should be equipped to handle. For example, the United States Post Office offers various classes of parcel post service, such as surface parcel post and air parcel post, each with different postage rate schedules based according to weight and postal zone. Also, there is United Parcel Service which offers parcel shipping services. It would thus be desirable to have a system which can be selectively controlled to compute postage or shipping charges for each of these different services.

In addition. there are factors such as insurance, special handling, special delivery, etc., which are often times desired and preferably should be capable of system implementation. Also, the special situation involving the computation of postage or shipping charges for oversize parcels should be considered in the design of a universally flexible parcel postage system.

When dealing with United Parcel Service, there are special shipping situations which require an additional charge, such as when shipping from west to east. Moreover, United Parcel Service (UPS) does not have authorized land routes between a number of geographical locations and must resort to so-called "drop shipping," which presents a special shipping charge situation. In some areas UPS has different rate schedules for intrastate and interstate shipments. All of these various situations should be accounted for.

Heretofore, some of the proposed parcel postage computing systems have been essentially "special purpose" and thus inflexible machines adapted to handle only a single class of postage service. Attempts to provide "general purpose" machines have resulted in extreme complexity; such systems being unwieldy from both the operator standpoint and the servicing standpoint.

From a practical standpoint, such systems cannot operate without human intervention. At the very least, an operator must be on hand to determine the postal zone of each parcel destination. This determination must then be introduced into the system as an operator input. Other operator inputs manifesting selections of service, class of service, insurance, etc., are called for if the system is to be applicable to diverse mailings. An oversize parcel situation must also be entered into the system by the operator if the correct postage is to be computed. Thus, operational simplicity is a most important consideration in the design of a truly flexible parcel postage system if the use of highly skilled and thus highly paid operating personnel is to be avoided.

It is accordingly an object of the present invention to provide an improved system for automatically determining parcel postage or shipping charges for various selected types and classes of postal services.

An additional object is to provide a system of the above character which is capable of rapidly processing a large number of parcels pursuant to automatically determining the postage of each and controlling a postage meter accordingly.

Still another object is to provide a system of the above character which is selectively controllable to accommodate special situations requiring additional postage or shipping charges, such as oversize parcels, insurance, special handling, etc.

An additional object is to provide a system of the above character which is adapted to automatically determine the postal zone from the zip code of the parcel destination address.

Another object is to provide apparatus for mechanically positioning the postage digit selectors of a postage meter in accordance with the postage determined by the system.

A further object is to provide a system of the above character which is reliable, accurate, and readily operated by relatively unskilled personnel.

Other objects of the invention will in part be obvious and in part appear hereinafter.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a system for weighing a parcel to be mailed or shipped and automatically determining the postage or shipping charges therefor. Having done this, the system automatically controls a printing device, such as a postage meter, to issue a stamp imprinted with the appropriate postage or shipping charge to be applied to the parcel. The consecutively executed functions of weighing, postage determination, and stamp issuance are performed rapidly, accurately and reliably without operator intervention except to identify the parcel destination and for special circumstances.

More specifically, the present invention provides a scale for weighing successive parcels. The weight of each parcel is translated into encoded weight data, which is stored in a register. The operator enters the geographical zone to which the parcel is destined, i.e., the mailing or shipping distance. This zone entry and the stored weight data are used to enter a postage memory which stores the postage or shipping charges for the various combinations of parcel weight and mailing distance (zone). The appropriate postage is read from the postage memory and stored in a register where it is used to condition a postage meter or the equivalent to print out the appropriate postage, typically on a stamp to be adhered to the parcel.

In many instances, the operator is not given the parcel destination zone but rather the postal zip code of the parcel destination address. As an important feature of the invention, the system includes a zip-to-zone memory which is adapted to convert a zip code entry by the operator to the appropriate zone for entry into the postage memory.

The system of the present invention is also adapted to compute the proper postage or shipping charge applicable to oversize parcels. When the operator determines that a parcel is oversized, he initiates an oversize designation input which automatically conditions the system to determine if the oversize parcel weight is less or greater than an established minimum weight and determine the postage accordingly.

The system includes apparatus for interfacing the postage register, which is the system output register, with a conventional postage meter. Separate position encoders translate the digit positions of the various postage digit selector arms of the postage meter into coded digits which are compared with the corresponding postage digits stored in the postage register, as read from the postage memory. The postage digit selector arms are separately driven through their various digit positions, and as each assumes the digit positions corresponding to the associated digits in the postage register, they are decoupled from their respective drives. When all have been positioned to set up a digit by digit comparison with the postage held in the postage register, the postage meter is triggered to issue a postage imprinted stamp.

The invention accordingly comprises the features of construction, combinations of elements, and arrangement of parts which will be exemplified in the constructions hereinafter set forth, and the scope of the invention will be indicated in the claims.

DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. 1 is a perspective view of a parcel postage metering system constructed in accordance with the invention;

FIG. 2 is an overall functional block diagram of the parcel postage metering system of FIG. 1;

FIG. 3 is a detailed logic block diagram of the sequencer of FIG. 2;

FIG. 4 is a detailed logic block diagram of the input/output register of FIG. 2;

FIG. 5 is a sectional view taken along line 5—5 of FIG. 1 to show the scale and encoder of FIG. 2;

FIG. 6 is a detailed logic block diagram of the up/down counter of FIG. 2;

FIG. 7 is a timing diagram illustrating the operation of the up/down counter of FIG. 6;

FIG. 8 is a plan view of a portion of a pounds to postage conversion table as stored in the postage memory of FIG. 2;

FIG. 9 is a plan view of a portion of a zip code to postal zone conversion table as stored in the zip-zone memory of FIG. 2;

FIG. 10 is a logic block diagram of the address counter and comparator of FIG. 2;

FIG. 11 is a detailed block diagram of the serial to parallel converter of FIG. 2;

FIG. 12 is a detailed logic block diagram of the postage ready logic of FIG. 2;

FIG. 13 is a detailed logic block diagram of the oversize logic of FIG. 2;

FIG. 14 is a sectional view taken along line 14—14 of FIG. 1;

FIG. 15 is a sectional view taken along line 15—15 of FIG. 14;

FIG. 16 is a side elevational view of one end portion of one of the links interconnecting the postage digit selection apparatus of FIG. 14 and the postage meter of FIG. 1;

FIG. 17 is a sectional view taken along line 17—17 of FIG. 16;

FIG. 18 is a detailed logic block diagram of the postage data handling portion of the postage digit selection apparatus;

FIG. 19 is a overall functional block diagram of an alternative embodiment of the console portion of the postage metering system of FIG. 1; and

FIG. 20 is a plan view of a portion of a pounds to postage conversion table as stored in the postage memory of FIG. 19.

Like reference notations refer to corresponding parts throughout several views of the drawings.

DETAILED DESCRIPTION

Referring now to the drawings, and first to FIG. 1, the parcel postage system of the present invention includes a console, generally indicated at 10, which contains, among other things, electronic circuitry for processing weight and postage data. Parcel weight data is obtained from a scale, generally indicated at 12, incorporated in console 10, while postage data is primarily obtained from a memory drum, generally indicated at 14 and also accommodated within the console. As will be seen, memory drum 14 has two separate memory banks; one storing a postage rate schedule and the other storing a zip code to postal zone conversion table. The data stored on memory drum 14 is optically encoded as opaque and transparent binary bits which are sensed by optical readout stations. As seen in FIG. 1, a light emitter 16 shines light through the postage rate memory bank peripheral portion of the memory drum 14 to a receiver 18, consisting of an array of suitable photosensors such as phototransistors. Similarly, the zip to zone memory bank peripheral portion of the memory drum is read out using a light emitter 20 and a receiver 22. Memory drum 14 is rotated by a motor 24 and an interconnecting belt drive 25.

It will readily occur to those in the art that other forms of data memories may be employed in the system of the present invention. For example, the postage and zone data may be optically encoded on one or more transparent discs. Moreover, suitable data memories may be provided in the form of magnetically encoded discs and drums, or even magnetic core matrices, although it is preferred to use a cyclical memory wherein the data is revolved passed readout stations, thus simplifying accessing from a component standpoint.

The console 10 also includes a control panel, generally indicated at 26 in FIG. 1, which contains a plurality of mode keys selectively depressed by an operator to initiate various system operating modes to be described. The control panel also includes numerical entry keys accommodating the manual input of data pursuant to the invention. Space is also provided in the control panel 26 to accommodate a display panel 26*b* where data is displayed; such data being system derived postage and weight data, as well as data entered from the control panel 26.

The console **10** is electrically linked to electromechanical postage selection apparatus, generally indicated at **30**. The selection apparatus, as will be seen, is mechanically linked to a postage meter **32** of known construction, such as a Pitney-Bowes 5300 Series Postage Meter. Parcel postage data derived at the console on the basis of the parcel weight is fed to the selection apparatus **30**, which operates to mechanically position the various postage digit selector arms, jointly indicated at **33** in FIG. **1**, by way of interconnecting links, jointly indicated at **34**, so as to set up the postage meter **32** for the proper postage. The postage meter is then signaled to issue a stamp printed with the value of the postage received from console **10**.

At this point, it should be pointed out that the system of the present invention is applicable to United States Post Office parcel post service and United Parcel Service (UPS). As is well known, a parcel can be sent either by parcel post (PP) or UPS. Thus, when reference is made to determining the applicable postage, this is intended to mean either the postage charged by the Post Office or the shipping charges applicable to the parcel if sent by UPS. Each service has its own rate schedule determined on the basis of the parcel weight, and, generally speaking, the distance the parcel is to be sent, and, in fact, the present invention contemplates storing both rate schedules on memory drum **14**.

In practice, parcels would be separated into groups depending upon whether they are to be sent by PP or UPS. One group of parcels, for example, those to be sent by Parcel Post would be successively weighed on a scale **12** to obtain the parcel postage stamps from postage meter **32**; the postage values being automatically deducted from a prepaid postage amount entered by postal officials. The parcel postage meter **32** would then be removed; the cover **31** being opened and the links **34** readily disconnected from the postage digit selector arms **33**. A UPS meter is substituted, and the console **10** is conditioned to determine the shipping charges for the parcels to be sent by UPS.

Alternatively, separate selection apparatus **30** and mechanically interlinked meters **32** can be provided for each service. They would be separately electrically linked to the console and would be individually selected from the control panel **26** by the operator according to which service is to be employed, either PP or UPS, for each parcel being weighed on scale **12**.

Overall System Block Diagram

The basic operation of the system of FIG. **1** will be more readily understood from the system block diagram seen in FIG. **2**. With the exception the postage meter **32** and the electromechanical selection apparatus **30**, all of the components seen in FIG. **8** are functionally and physically located within console **10**. When a parcel is placed on scale **12**, its mechanical response is coupled to a scale encoder **36** adapted to convert the parcel weight into a proportional number of pulses which are accumulated in a counter **40**. As will be seen, counter **40** is an up/down pulse counter, enabling it to accurately follow the scale response as it oscillates about and ultimately settles down to a final weight reading.

The operator, upon reading the parcel address destination, determines the appropriate postal zone on the basis of the distance between his geographical location and the parcel destination. The operator enters the postal zone by depression of the appropriate key of a numerical entry keyboard **26***a* included in control panel **26** (FIG. **1**). This zone entry is supplied by connection **42** and a multiplexer or switch **44** to a zone register **46**. Prior to the entry of a zone from numerical entry keyboard **26***a*, the operator presses a mode key Z included in a mode key group **54**, which has as one of its functions the conditioning of multiplexer **44** to route the keyboard zone entry through to zone register **46**. The zone digit entry held in zone register **46** conditions a zone selector **50** to effect appropriate zone entry into the postage memory **52** which, as previously noted, comprises one of the memory banks carried by memory drum **14** (FIG. **1**). In physical terms, zone entry into the postage memory **52** is effective by selecting one of a plurality of phototransistors, or the equivalent, included in the receiver array **18** generally illustrated in FIG. **1**. As will be subsequently described, the postage memory **52** includes a series of side by side zone channels in which postage data is serially recorded by parcel weight. Thus, the zone selector **50** effects selection of the appropriate phototransistor of the receiver array **18** which is aligned with the channel of the postage memory **52** assigned to the particular zone entered into the zone register **46** from the keyboard **26***a*.

The next operator function, and in most situations the only remaining operator function required for each parcel, is to depress a postage request key PR included in mode key group **54** in control panel **26**. This generates an input over lead **55** to a sequencer **56** which operates to organize the system operating functions pursuant to determining the applicable parcel postage.

Since the appropriate zone has already been entered into zone register **46**, thereby accessing postage memory **52** for all postage data, regardless of parcel weight, for that particular zone, the sequencer **56** generates a signal RD LBS over lead **57** to an input/output register **58**. This signal conditions register **58** for acceptance of the appropriate postage data read from the postage memory **52** over connection **59** to a serial to parallel converter **60** and thence over connection **61** and multiplexer **62** to the input/output register. As will be described, the postage data is stored and read out from postage memory in serial binary coded decimal, while the input/output register **58** is designed to accept the postage data in serial digit, parallel bit fashion. Thus, the serial to parallel converter **60** is necessary to accept the digit bits serially from postage memory **52** and successively pass the bits of each postage digit in parallel to the input/output register **58**. The memory **52** also includes a postage clock bit channel which is read out to provide postage clock pulses POST CLK over lead **63** to converter **60** for synchronizing the serial to parallel conversion.

Having accessed the postage memory **52** for the appropriate zone, it now remains to further access the postage memory for the appropriate parcel weight, held in up/down counter **40**, in order to obtain the applicable postage for entry into input/output register **58**. To this end, the postage memory is provided with a pound clock pulse channel in which are recorded a series of pound clock bits located in predetermined relation to the stored postage data. These pound clock pul-

ses LB CLK, read out during each revolution of the drum memory **14** (FIG. **1**), are applied over lead **64** to an address counter **66**. The pound clock pulse count accumulating in address counter **66** is continuously compared in a comparator **68** with the parcel weight stored in the up/down counter **40** supplied over connection **69**. When a comparison is reached between the pulse counts in address counter **66** and up/down counter **40**, comparator **68** generates a compare signal COMP over lead **70** to the sequencer **56**. Due to the arrangement of the postage data in postage memory **52**, the generation of compare signal COMP signals that the postage data applicable to the parcel weight registered in the up/down counter **40** is about to be read out to the serial to parallel converter **60**. The sequencer circuit **56**, in response to the compare signal COMP generates a read postage command signal RD POST over lead **72** to the serial to parallel converter **60**. This signal conditions the converter **60** to perform the serial to parallel bit conversion on a digit by digit basis for the next four postage digits read from the postage memory **52**. The four bits of each postage digit are assembled and then transferred in parallel, digit by digit, to the input/output register **58**. Each postage digit is shifted into the input/output register in response to an enter postage signal ENT POST generated over lead **74**.

When the last of the four postage digits, in the illustrated embodiment of the invention, has been assembled in parallel bit fashion and shifted into the input/output register **58**, the serial to parallel converter **60** generates a postage entered signal POST ENT over line **78** to a postage ready logic circuit **80**. Prior to receipt of this signal the postage ready logic circuit **80** provides a postage not ready signal $\overline{\text{POST RDY}}$ over lead **82** to the sequencer **56** effective to enable the various sequence control functions of the sequencer. When the postage not ready signal $\overline{\text{POST RDY}}$ goes false in response to receipt of the postage entered signal POST ENT, signifying that the postage has been fully entered into the input/output register **58**, the sequencer **56** is effectively disabled.

Assuming that no additional postage over and above the postage value held in the input/output register is applicable to the particular parcel on scale **12**, the postage ready circuit **80** generates a ready enter signal RDY ENT which is supplied over lead **84** to the electromechanical postage selection apparatus **30**. This apparatus then looks at the postage digits registered in the input/output register **58** communicated over connection **85** and operates to mechanically position the postage digit selector arms **33** of postage meter **32** accordingly via the interconnecting links, diagrammatically indicated at **34** in FIG. **2**. After all the postage levers have been approximately positioned by the selection apparatus **30**, an execute signal EXEC issues over lead **87**, signaling the postage meter to execute a print cycle and issue an appropriately imprinted postage stamp which may then be applied to the parcel. After the postage meter **32** has issued the stamp, it issues a cycle complete signal **0** which is fed back over lead **89** to the console for the purpose of resetting the console components preparatory for the next parcel.

In some of the cases, it is contemplated that the operator will not be supplied with the postal zone or the parcel destination, but will be able to readily obtain the zip code of the parcel destination typically recorded on the parcel address. In these cases, the operator enters the first three digits of the zip code into the input/output register **58** via numerical keyboard **26***a* and multiplexer **62**. It is only when key Z is depressed preparatory to a direct zone entry, that the keyboard is connected by multiplexer **44** to the zone register **46**.

With the entry of a zip code into the input/output register and the depression of the postage request key PR, the sequencer **56** initiates a zone search through a zip to zone memory **90**, included as the other memory bank carried by memory drum **14** (FIG. **1**). As will be seen, the zip-zone memory **90** includes a zip clock bit channel, with each zip clock bit storage position aligned with a binary coded decimal zone storage position. As will become apparent, the zip-zone memory is specially encoded on the basis of the geographical location of each particular system installation, since the applicable postal zone in each case is determined by the distance to the parcel destination. These zip clock bits are read as zip clock pulses ZIP CLK from the zip-zone memory **90** during each memory drum revolution and are fed over lead **92** to sequencer **56** during a zone search. These zip clock pulses are gated through as add clock pulses ADD CLK over lead **93** to the input/output register **58**.

As will be seen, the input/output register is adapted not only as a binary coded decimal (BCD) digit shift register, but also as a BCD counter. Thus, each zip clock pulse ZIP CLK gated through as an add clock pulse ADD CLK to the input/output register increments the zip code number registered therein by one. The input/output register is incremented until it overflows, i.e., goes from 999 to 000. When overflow occurs, the input/output register **58** generates a read store zone signal RD STR ZONE on output lead **95** to zone register **46**. The zone register responds by accepting and holding the zone number coincidentally read from the zip-zone memory **90** and supplied over connection **97** and multiplexer **44**.

From this general description, it is seen that by serially arranging the zone data in the zip-zone memory **90** in accordance with the distance between the various zip code designated geographical locations and the system installation location, where the zone data is located in the memory by counting up to the compliment of the zip code held in the input/output register, the appropriate zone can be entered into the zone register **46** from the zip-zone memory **90**, thereby effecting a zip to zone conversion.

The read store zone signal RD STR ZONE on output lead **95** is also supplied to the sequencer **56** to indicate that the appropriate zone has been located and entered into the zone register **46** and that a search of the postage memory **52** for the applicable postage may now be performed in the manner previously generally described.

Occasionally, the system of the present invention may be called upon to determine the postage applicable to an oversize package. Under both the PP and UPS rate schedules, the postage applicable to an oversized package is determined as follows. If the oversize package is less than an established minimum weight, 25 pounds for UPS and 10 pounds for PP, the applicable postage is determined on the basis of the established

minimum weight. However, if the oversize parcel weights more than the established minimum weight, the applicable postage is determined by its actual weight.

Still referring to FIG. 2, when the operator determines that a parcel placed on scale 12 is oversized, an oversize key O/S is depressed, conditioning an oversize logic circuit 100 over lead 102. During the searching of the postage memory 52 for the applicable postage, the accumulating count of the pound clock pulses LB CLK read from the postage memory 52 into the address counter 66 is applied over connection 104 to the oversize logic circuit 100, as well as the comparator 68. The oversize logic circuit also receives the compare output COMP from comparator 68. As will be seen, the count content of the address counter 66 is continuously decoded to detect when it is incremented to the established minimum pound value. Until this minimum pound value is reached in the search of the postage memory 52, the oversize logic circuit 100 supplies a signal $\overline{O/S}$ over lead 106 to the sequencer 56, in effect telling the sequencer to disregard the compare signal COMP issuing from the comparator 68 over lead 70, which would occur if the oversized package weighs less than the established minimum. In this case, when the address counter increments to the established minimum weight value, the oversize logic circuit 100 supplies a read minimum pounds signal RD MIN LBS over lead 108 to the sequencer 56, which responds by issuing the read postage signal RD POST over lead 72 to the serial to parallel converter 60. The postage applicable to the established minimum weight is thus entered into the input/output register.

On the other hand, if the established minimum weight value is achieved in the address counter 66 before a compare signal COMP issues from comparator 68, the oversize logic circuit 100 is converted to its inoperative state as though it had not been conditioned in the first instance by oversize key O/S. The disabling effect of the signal $\overline{O/S}$ is removed, and the sequencer awaits the receipt of the compare signal COMP from comparator 68 pursuant to retrieval from the postage memory 52 of the postage value based on the actual weight of the oversized parcel.

In certain situations dealing with the UPS system, a nominal additional postage charge is required in shipping parcels between certain locations. These special situations can be conveniently handled in accordance with the present invention by providing recorded flag bits in the zip-zone memory 90 which are read out as flag pulses into the postage ready logic 80 over lead 109 under the control of the read store zone signal RD STR ZONE at the same time that the zone is read into the zone register 46. After the postage applicable to the parcel weight has been located in the postage memory 52 and entered into the input/output register 58, the postage ready logic 80 determines whether it received on or more flag pulses over lead 109 from the zip-zone memory 90 at the time the proper zone was located and entered into the zone register 46. If flag pulses had been received, the postage ready logic circuit 80 is conditioned to accept over connection 111 from the zip-zone memory 90 uniquely coded bits in effect designating the amount of additional postage to be added to the postage already registed in the input/output register 58. The postage ready logic circuit 80 generates an add clock gate pulse ADD CLK GATE over lead 112 to the sequencer 56 effective to gate through to the input/output register a predetermined number of zip clock pulses ZIP CLK as add clock pulses ADD CLK to the input/output register 58. The input/output register is thus incremented accordingly so as to register the original postage plus the additional postage.

The various entries into the input/output register 58, such as zip code numbers and postage are displayed at the display panel 26*b*. In addition, a key # in group 54 may be depressed to condition the display panel to display the parcel weight in the up/down counter 40 communicated over connection 113.

Sequencer

The sequencer 56 of FIG. 2, as seen in detail in FIG. 3, operates to initate various system operating modes and insures that the various operating steps involved in each mode are performed in the appropriate sequence. Specifically, the sequencer 56 is conditioned by various mode keys of the group 54 to initiate a particular operating mode. As seen in FIG. 3, the postage request key PR, postage display/only key D/O, additional postage key $ and the zone entry key Z, upon depression, provide separate inputs directly to the sequencer 56. The oversize key O/S of the group 54, as seen in FIG. 2, applies its input to the oversize logic 100 which, in turn, provides signal $\overline{O/S}$ to the sequencer. The mode of function keys PR, D/O, $ and Z, upon depression are effective to set respective flip-flops PREF, D/OFF, $FF and ZFF. These flip-flops serve as latches for their respective keys, and thus a key need only be momentarily depressed to register the fact that a particular operating mode has been called for. These flip-flops are set by depressions of their respective keys and are reset by the cycle complete signal O issued by the postage meter 32.

Depression of the postage request key PR initiates the system operation culminating in the issuance of a postage imprinted stamp by postage meter 32 applicable to the parcel placed on scale 12. Postage display only key D/O initiates essentially the same operation as the postage request key PR, except that the applicable postage is merely displayed at the display panel 115 (FIG. 2). Thus, the postage display only function is largely a test function performed to check the operating accuracy of the system The additional postage key $ is employed in the situation where additional postage, over the above the postage applicable to the parcel weight, is to be applied to a parcel. Thus, key $ is depressed prior to the entry of numerical postage data from keyboard 26*a* into the input/output register 58 to cover the cost of, for example, insurance, special handling, etc. Upon depression of postage request key PR, the postage selection apparatus 30 is immediately actuated by the signal RDY ENT to set up the postage meter 32 to the addition postage value in register 58 and issue an additional postage imprinted stamp.

The zone entry key Z is depressed preparatory to the entry of the zone of the parcel destination directly from the keyboard 26*a* into the zone register 46 (FIG. 2). As will be seen, the system is normally conditioned to accept the parcel destination keyboard entry into the input/output register in the form of a zip code number. The system then proceeds to search the zip-zone

memory **90** for the postal zone corresponding to the zip code entry; the located postal zone then being entered into the zone register **46**, as previously generally described. Thus, depression of the zone key Z in effect causes the system to skip the zone search operation, since the appropriate zone has already been entered into the zone register **46** directly from the keyboard **26***a*.

The set outputs of the postage request flip-flop PRFF and the postage display only flip-flop D/OFF are gated together in an OR gate **120** to provide a common output, identified as PR SET and, through inverter **122**, the complement $\overline{\text{PR SET}}$. As will be seen, these signals are used as controls elsewhere in the system. The output PR SET is applied as one input to an AND gate **124**. The remaining inputs to this gate are the reset output $\overline{\$FF}$ of the additional postage flip-flop $FF and the reset output $\overline{ZFF}$ of the zone entry flip-flop ZFF. The last remaining input to AND gate **124** is a reset pulse read from the zip-zone memory **90** at the beginning of each revolution of the memory drum **14** (FIG. 1). This reset pulse issues at the beginning of each revolution of the zip to zone conversion table stored in the memory **90** passed its readout station. Actually, this reset pulse is common to both the zip-zone memory and the postage memory **52**, and, in the latter case, signals the start of each revolution of the pounds to postage conversion table stored in the postage memory passed its readout station.

Assuming either the postage request key PR or the postage display only key D/O is depressed and the additional postage key $ and the zone entry key Z are not depressed, the output of AND gate **124** goes to a logical ONE upon the receipt of the next occurring reset pulse. Upon the termination of the reset pulse, the gate output goes to a logical ZERO, which is effective to trigger a zone search flip-flop ZS from its reset state to its set state. The set output of the flip-flop is connected to the set input of a zone located flip-flop ZL and also is in an AND gate **126** with the reset output $\overline{\text{RD LBS}}$ of a zone located flip-flop ZL. While the zone search flip-flop is set and until the zone located flip-flop is set, AND gate **126** provides a logical ONE output which is passed through an OR gate **128** to enable an AND gate **130**. The other input to AND gate **130** consists of zip clock pulses ZIP CLK read from the zip-zone memory **90**, which feed through this gate, while enabled, as add clock pulses ADD CLK on lead **93** to the input/output register **58**. The input/output register, as will be seen, functions both as a binary coded decimal BCD shift register and a BCD counter. These add clock pulses serve to increment the zip code number entered in register **58** from keyboard **26***a* prior to depression of either the postage request key PR or the postage display only key D/O.

The arrangement of the zone data stored in the zip-zone memory **90** is such that when the number of zip clock pulses read from the stored zip-zone conversion table after the occurrence of a reset pulse equals the complement of the zip code number held in the input/output register **58**, the zone applicable to the zip code number entered from keyboard **26***a* has arrived at the readout station. When the input/output counter has been incremented to the complement of the zip code number previously entered therein, it spills over or is zeroed, and this event is decoded to provide the read store zone signal RD STR ZONE. This signal is returned to the sequencer **56** over lead **95** to trigger the zone located flip-flop ZL to its set state, signifying that the zone applicable to the zip code entered into input/output register **58** has been located in the zip-zone memory **90**. AND gate **130** is disabled via AND gate **126**, thereby terminating the application of add clock pulses ADD CLK to the input/output register.

If, upon the occurrence of the next reset pulse after the zone search flip-flop ZS have been set, the zone located flip/flop ZL has not been set by a read store zone signal, the output of AND gate **126** remains a logical ONE, enabling the passage of this next occurring reset pulse through AND gate **134** as an error signal M.

As will be seen, the postage ready logic **80** supplies an enabling input ADD CLK GATE through OR gate **128** to AND gate **130**, thus enabling the application of a selected number of additional add clock pulses ADD CLK to the input/output register to increment a postage value previously entered therein from postage memory **52**.

Assuming that the appropriate zone has been located in the zip-zone memory **90**, AND gate **132** is enabled from the set output RD LBS of flip-flop ZL, and upon the next occurring reset pulse a search pounds flip-flop SL is triggered to its set condition. This has the controlling effect of initiating a search of the postage memory **52** (FIG. 2). As previously noted, each reset pulse read from the zip-zone memory **90** is also common to the postage memory **52**, and thus signals the arrival of the start of the stored pounds to postage conversion table at its readout station. The logical ONE set output of the search pounds flip-flop, indicated as SL, enables an AND gate **138**, whose other inputs are $\overline{\text{POST RDY}}$ from the postage ready logic **80**, COMP from the comparator circuit **68**, and $\overline{\text{O/S}}$ from the oversize logic **100**. Assuming that the postage has not been located in the postage memory and entered into the input/output register ($\overline{\text{POST RDY}}$ a logical ONE) and the parcel is not oversized ($\overline{\text{O/S}}$ a logical ONE), AND gate **138** passes the compare signal COMP through to the output of an OR gate **140** and a read postage command signal RD POST, which is fed over lead **72** to the serial to parallel converter **60**. This signal announces the arrival of the applicable postage in the pounds to postage conversion table at the readout station, and conditions the converter **60** to effect the requisite serial to parallel digit bit conversion and the transfer of the postage digits serially into the input/output register via the multiplexer **61** (FIG. 2).

As will be seen from the details of the oversize logic circuit **100** to be described, if the package is oversized and the operator signals this fact by depression of the oversize key O/S, AND gate **138** is disabled by the signal $\overline{\text{O/S}}$, and the read postage command signal RD POST is derived from the read minimum pounds signal RD MIN LBS supplied from the oversize logic circuit over lead **108**.

Still referring to FIG. 3, if the zone is to be entered into the zone register **46** directly from the keyboard **26***a*, key Z is depressed to set flip-flop ZFF. The appropriate zone number is then entered into the zone register. The set output of flip-flop ZFF enables an AND gate **136**, and, upon depression of postage request key

PR (or key D/O), the zone located flip-flop is forced to its set state just as though the zone had been located from the zip-zone memory. The next reset pulse sets the search pounds flip-flop SL to enable a search of the postage memory **52**.

As shown in FIG. **3**, the various flip-flops in the sequencer **56** all receive the cycle complete signal O from the postage meter **32** as a forced reset input, insuring that they are all reset preparatory for the system operating cycle.

Input/Output Register

The input/output register **58**, as seen in detail in FIG. **4**, may be considered as comprising four digit registers, namely, a tens digit register **150**, a units digit register **152**, a tenths digit register **154** and a hundredths digit register **156**. Each digit register consists of four bit stages, enabling it to store a decimal digit in binary coded decimal format. The input/output register **58** is loaded from the left via multiplexer **62** from either the postage memory **52** and converter **60** or the numerical keyboard **26***a* (FIG. **2**). The digits, parallel by bit, enter serially and are shifted through the digit registers to their ultimate register positions under the control of a series of one shot multivibrators **160–163**. During digit entry from the keyboard **26***a*, the system has to be conditioned to search the postage memory **52**, since the zone located flip-flop ZL in the sequencer (FIG. **3**) is still in its reset state. Its reset output $\overline{\text{RD LBS}}$, a logical ONE, is applied to the multiplexer **62**, conditioning it to connect the input/output register to the numerical keyboard **26**a. The output $\overline{\text{RD LBS}}$ also conditions an AND gate **164** to pass a keyboard entry strobe pulse, which accompanies each keyboard digit entry, to the first one shot multivibrator **160** via an OR gate **166**. The one shot multivibrator **160** is triggered to execute a pulse cycle. The multivibrator output pulse appears both on its set output lead **160***a* and, in complemented form, on its reset output lead **160***b*. The leading edge of the output pulse of multivibrator **160** on lead **160***b*, in effect, clears the tens digit register **150** by accepting the contents of the units register **152**, while the trailing edge on lead **160***a* triggers the next one shot multivibrator **161** into a pulse cycle. The leading edge of its output pulse on reset output lead **161***b* is used to condition the units digit register **152** to accept the contents of the tenths digit register **154**. The trailing edge of the pulse output of one shot multivibrator **161**, appearing on its set output lead **161***a*, triggers one shot multivibrator **162** into a pulse cycle. The reset output of this multivibrator, on lead **162***b*, conditions the tenths digit register **154** to accept the content of the hundredths digit register **156**, while the trailing edge of its output pulse on lead **162***a* triggers the last one shot multivibrator **163**. The leading edge of the output pulse of this multivibrator on lead **163***b*, is applied to the hundredths digit register **156** to accept the digit entry in parallel bit, binary coded decimal form from the keyboard **26***a* via multiplexer **62**.

It is thus seen that in response to each keyboard entry strobe pulse, the one short multivibrators **160–163** fire in succession to effect the shifting of the digits content of the input/output register **58** to the right one digit position. As will be seen, a zip code entry from the numerical keyboard **26***a* requires only the first three digits of the zip code of the parcel destination. Thus, a zip code entry encompasses three digit entries, each entry accompanied by a keyboard entry strobe pulse, and the zip code, once entered into the input/output register **58**, is held in the first three digit registers **152**, **154** and **156**.

During the time that the system is to read a postage value from the postage memory **52** via serial to parallel converter **60**, the zone located flip-flop ZL in the sequencer **56** (FIG. **3**) is set, and its set output RD LBS, a logical ONE, enables an AND gate **170** in FIG. **4** to pass enter postage strobe pulses ENT POST from the serial to parallel converter **60** through to one short multivibrator **160** via OR gate **166**. The reset output $\overline{\text{RD LBS}}$ from the zone located flip-flop ZL, being a logical ZERO, conditions the multiplexer **62** to accept postage digit entries from the postage memory **52** by way of a serial to parallel converter, rather than keyboard **26***a*. The postage digits, in parallel bit, binary coded decimal form, are shifted into the input/output register most significant digit first in the same manner as described for digit entries from the numerical keyboard **26***a*.

During a zone search, as previously described in connection with the sequencer of FIG. **3**, add clock pulses ADD CLK are gated over lead **93** to the input/output register. As seen in FIG. **4**, these clock pulses are applied to increment the hundredths digit register **156**, which contains the least significant digit of the zip code entry. Each add clock pulse increments the hundredths digit register one count. The outputs of the one and eight bit stages of the hundredths digit register **156** are gated in an AND gate **172** to generate carry pulses for incrementing the tenths digit register **154**. Similarly, the outputs of the one and eight bit stages of the tenths digit register are gated together in an AND gate **174** to generate carry pulses for the units digit register **152**. These outputs of the one and eight bit stages of the units digit register are gated together in an AND gate **176** to generate a carry pulse which is gated in an AND gate **178** with the carry pulse outputs from gates **172** and **174**, the add clock pulses arriving over lead **93**, and the output PR SET from sequencer **56** (FIG. **3**).

From this detailed description, it is seen that a zip code entry in the hundredths, tenths and units digit registers of the input/output register is incremented by the add clock pulses to 999. Upon the next add clock pulse, simultaneous carry pulses will be applied to AND gate **178** from AND gates **172**, **174** and **176**. This signifies that the input/output register has overflowed, i.e., counted to the complement of the zip code number originally entered therein, and the read store zone signal RD STR ZONE issues on lead **95** at the output of AND gate **178** for transmittal to the sequencer **56**, the zone register **46** and the postage ready logic **80**, all as seen generally in FIG. **2**.

Scale And Weight Encoder

The scale unit **12**, as seen in FIG. **5**, includes a platform **200** on which a parcel **202** is placed to be weighted. The platform **200** is mounted by a pair of laterally spaced supports **204** pivotally linked at their lower ends to a lever **206**, which, in turn, is pivotally mounted by a base **208**. It is thus seen that upon placement of parcel **202** on the scale platform **200**, the parcel weight forces the scale platform **200** downward, causing a counterclockwise pivotal movement of lever **206** against the restraining force of a spring **210** through an angle proportional to the parcel weight.

The free end of lever **206** carries a rack gear sector **212** which engages a pinion **214** keyed on a shaft **216** which also mounts an encoder disc **218**. By virtue of this construction, it is seen that the pivotal movement of lever **206** in response to the parcel weight is translated into a proportional increment of angular rotation of the encoder disc **218**. The encoder disc carries a series of opaque bars **220** which, upon rotation of the encoder disc, cause interruptions of a light beam between a source **222** and a receiver **224**. Thus, the increment of rotation of the encoder disc **218** in response to the parcel weight is translated into a proportionate number of electrical pulses at the receiver **224**.

Up/Down Scale Counter

The up/down counter **40** of FIG. **2** is seen in detail in FIG. **6**. The receiver **224** noted in FIG. **5**, comprises a pair of phototransistors **226** and **228**. The use of two photosensors in the receiver **224** is for the purpose of conditioning steering logic circuitry, generally indicated at **230**, pursuant to controlling the up/down counter **40** to count either up or down in response to movement therepassed of the bars **220** on encoder disc **218**. As seen in FIG. **7**, the phototransistors **226** and **228** of receiver **224** are positioned such that the response of the former to the bars **220** leads that of the latter for counting up in pounds, and vice versa for counting down in pounds. Thus, in FIG. **7**, the encoder disc may be assumed to be moving to the left during countup and to the right during countdown. The phototransistors **226** and **228** are spaced apart by a distance equal to approximately one-half the width of a single opaque bar **220** on encoder disc **218**. When the bars **220** are moving to the left passed the phototransistors, phototransistor **226** sees a dark to light transition while the phototransistor **228** is obscured by a bar. As will be seen, each time this occurs, a countup pulse is generated. On the other hand, a countdown pulse is generated when the phototransistor **226** sees a light to dark transition while the phototransistor **226** sees a light to dark transition while the phototransistor **228** is obscured by a bar **220** of the encoder disc **218**. As was previously noted, the up/down capability of counter **40** is necessary to resolve any bounce of the scale platform **200** into an accurate registration of the weight of parcel **202**.

Returning to FIG. **6**, the emitter of phototransistor **226** is grounded, while its collector is connected to the input of an amplifier **232**. Similarly, phototransistor **228** has its emitter grounded and its collector connected to the input of an amplifier **234**. For purposes of the present description, it will be assumed that when the phototransistors are illuminated, they apply a logical ZERO input to their respective amplifiers, and when they are not illuminated, they develop logical ONE inputs.

The output of amplifier **232** is connected through an inverter **238** to the triggering input of an up multivibrator **236** and directly to the triggering input of a down multivibrator **240**. The output of inverter **238** is also connected to the up/down sense input **241** of counter **40**. It will be further seen that the counter will count up in response to clock pulses received at its clock input **242** as long as its sense input is a logical ONE, and will count down in response to those clock pulses received while its sense input is a logical ZERO.

Up multivibrator **236** is triggered in response to each logical ZERO to ONE transition, which through inverter **238** corresponds to each dark to light transition sensed by phototransistor **226**. Since down multivibrator **240** is connected directly to the output of amplifier **232**, it is triggered in response to each light to dark transition sensed by phototransistor **226**. The pulse outputs of the up and down multivibrators are separately gated in AND gates **244** and **246**, respectively. These AND gates are enabled only during the time that the output from amplifier **234** is a logical ONE, which corresponds to the times that phototransistor **228** is obscured by bars **220**. The output of AND gates **244** and **246** are connected as separate inputs to an OR gate **248**, whose output is connected to the toggling input of a flip-flop **250** which, in the present application, serves as a half-pound counter since the encoder disc **218** is assumed to be graduated in half-pound increments. The set output of flip-flop **250** is gated with the output of OR gate **248** and the output of inverter **238** in an AND gate **252**. The reset output of flip-flop **250** is gated with the output of OR gate **248** and the output of amplifier **232** in an AND gate **254**. The outputs of gates **252** and **254** are gated together in an OR gate **256**, whose output is connected to the clock input **242** of counter **40**.

The operation of the steering logic **230** of FIG. **6** will now be described in conjunction with the timing diagram of FIG. **7**. Assuming that the counter **40** is counting up from 0 pounds, the first dark to light transition sensed by phototransistor **226** triggers up multivibrator **236**. Its pulse output is passed by AND gate **244** since it is enabled by the logical ONE output from amplifier **234** due to the fact that phototransistor **228** senses no light. Flip-flop **250** is triggered on the trailing edge of the up multivibrator pulse from its original reset condition to its set condition. Counter **40** is not however pulsed on its clock input **242** from gate **252** since the up multivibrator pulse terminates as flip-flop **250** is set and gate **254** is disabled by the now prevailing logical ZERO output from amplifier **232**. In response to the next dark to light transition the up multivibrator generates another pulse and flip-flop **250** is reset by its trailing edge. However during the interval of this pulse, AND gate **254** is enabled since flip-flop **250** is still set and the output of inverter **238** is a ONE. Thus, this up multivibrator output pulse passes through gates **252** and **256** to the clock input of counter **40**. Since the sense input **241** receives a ONE from inverter **238**, counter **40** is incremented.

It is thus seen that with alternate dark to light transitions sensed by phototransistor **226**, counter **40** is incremented to progressively register the angular displacement of the encoder disc **218** in response to the parcel weight.

If at any time, the encoder disc **218** rotates in the opposite or downward direction, down multivibrator **240** will be triggered by light to dark transitions sensed by phototransistor **226** during the time that phototransistor **228** senses no light. AND gate **246** is thus enabled to pass a pulse to reverse the state of flip-flop **250** on its trailing edge. Assuming that the flip-flop **250** has previously been triggered to its reset state at the conclusion of an up clock pulse to counter **40**, the first increment of reverse or downward movement of

half-pound counter **288** to its set state. At this time, AND gate **292** is disabled from the 5 pound latch **290**, and the units digit stage is not incremented. With the next occurring pound clock pulse LB CLK, the half-pound counter is triggered to its reset state, producing a logical ONE to ZERO transition at its set output which passes through AND gate **294** and OR gate **296** to increment the units digit stage **280** of the address counter **66**. It is thus seen that the address counter **66** is incremented with every other pound clock pulse LB CLK read from postage memory **52**.

The one and four bit outputs of the units digit stage **280** are gated together in an AND gate **298**, such that when the units digit stage has been incremented to a 5 pound count, the 5 pound latch **290** is forced to its set state, thereby enabling AND gate **292** and disabling AND gate **294**. Thereafter, each pound clock pulses passes through AND gate **292** to increment the units digit stage **280** of the address counter **66**.

Prior to achieving a 5 pound count in the address counter **66**, the content of the half-pound counter **288**, appearing at the output of AND gate **294**, is compared with the output of the half-pound counter **250** of the up/down counter **40** (FIG. **6**). Thus, the output of AND gate **294** is applied to comparator **66** for comparison with the output of an AND gate **300** which receives as inputs the set output of half-pound counter **250** and the reset output of the 5 pound latch **290** of FIG. **10**. It is thus seen that prior to the achievement of a 5 pound count in the address counter **66** the comparator **68** compares the content of the address counter and the up/down counter by half-pound increments. Above 5 pounds, both AND gates **294** and **300** are disabled by the 5 pound latch **290**, and thus the content of the half-pound counters **250** and **288** are effectively ignored by comparator **68**.

Serial to Parallel Converter

The serial to parallel converter **60**, seen in FIG. **2**, is shown in detail in FIG. **11**. The operation of the serial to parallel converter begins with the read postage command signal RD POST supplied over lead **72** from the output of OR gate **140** in the sequencer **56** (FIG. **3**). It will be recalled that the read postage command signal, except for oversized parcel situations, is derived from the comparison signal COMP issuing from comparator **68**. As the read postage command signal goes to a logical ONE, a four bit shift register **302** is enabled to shift in the four bits of a postage digit read serially from the postage memory **52** over line **59**. The read postage command signal RD POST is also supplied as one input to an AND gate **304** and as one input to an OR gate **306**, whose output is connected to the forced reset input of a postage enter flip-flop POST ENT. The cycle complete signal O is supplied to the other input of OR gate **306**, thus assuring that the postage enter flip-flop POST ENT is reset preparatory to the receipt of postage data by converter **60**. As will be seen, the postage enter flip-flop is triggered to its set condition from the output of AND gate **308** to generate a postage enter signal POST ENT signifying that the last postage digit has been entered into the input/output register **58** from converter **60**.

The postage clock pulses POST CLK read from postage memory **52** over lead **63** are used to shift the postage digit bits into shift register **302** and are also inverted in an inverter **310** for application to the other input of AND gate **304**. The output of AND gate **304** is applied to one input of an AND gate **312** which is enabled from the reset output of the postage enter flip-flop POST ENT. Thus, as long as this flip-flop is in its reset state, AND gate **312** passes clocking pulses from the output of AND gate **304** to increment a four bit binary counter **314**. The one and two bit stages of binary counter **314** are inverted in inverters **316** and **318**, whose outputs are connected as separate inputs to an AND gate **319**, together with the output of AND gate **304**. The fourth input to AND gate **316** originates from an OR gate **320** whose inputs come from the four and eight bit stages of the binary counter **314**.

It is seen that gate **319**, as controlled by inverters **316**, **318** and OR gate **320**, provides an output pulse when the count of the binary counter **314** reaches four, eight and 12. This pulse output is supplied through an OR gate **322** as the enter postage shift or strobe pulse ENT POST to the input/output register **58**, causing the first three digits of the postage data to be successively shifted into the input/output register from the shift register **302** of the serial to parallel converter. When the binary counter **314** reaches a count of 16, AND gate **308** is fully enabled to trigger the postage enter flip-flop POST ENT to its set position. The set output of this flip-flop enables an AND gate **324**, whose other input is obtained from AND gate **304**. The output of gate **324** is connected as the other input to OR gate **322**, such that the last enter postage shift pulse ENT POST effecting the shift in of the last postage digit comes from gate **324**, rather than gate **319**.

The purpose of gating the complement of the postage clock pulses POST CLK with the read postage command signal RD POST in AND gate **304** is to derive a train of clock pulses for clocking binary counter **314** which is effectively shifted ahead in time relative to the postage clock pulse train. In this way, the binary counter is incremented one count just prior to the shifting of the corresponding postage digit bit into shift register **302**.

Specifically, when the read postage command signal RD POST appears, line **72** goes from a logical ZERO to a logical ONE, and the output of AND gate **304** goes to a ONE. When the first postage clock pulse POST CLK appears, the output of AND gate **304** goes to a logical ZERO and this ONE to ZERO transition passes through AND gate **312** to increment the binary counter **314**. As each postage clock pulse terminates, the shift register **302** is shifted to accept the postage digit bit being read from the postage memory **52**. On the leading edge of the fourth postage clock pulse, the binary counter **314** is incremented to four, and the fourth bit of the first postage digit is shifted into the shift register **302** on the termination of the fourth postage clock pulse. At this point, the output of the AND gate **304** goes to a logical ONE, which passes through AND gate **317** as the enter postage shift pulse ENT POST to the input/output register **58**. This shift pulse terminates with the leading edge of the fifth postage clock pulse, which is also effective through AND gate **312** to increment the binary counter to five. When the binary counter reaches the counts of eight and 12, the same operation occurs to shift the second or third postage digits into the input/output register.

the encoder disc 218 triggers the down multivibrator and its output pulse is passed by gate 254 before flip-flop 250 is set. This pulse is effective to decrement counter 40 since its up/down sense input 241 is now a logical ZERO as seen in FIG. 7.

Postage and Zip-Zone Memories

The postage memory 52, actually a read-only memory, stores a pounds to postage conversion table, which may take the form of a film strip secured on the periphery of the memory drum 14 (FIG. 1). It will be appreciated that, in the event of a postage rate change, a film strip bearing the new rate table may be readily substituted. A typical arrangement of the postage data for a portion of the conversion chart of postage memory 52 is shown in FIG. 8. The postage memory includes a series of opaque pound bars, of which two are shown in FIG. 8 at 260. These pound bars are read out as pound clock pulses LB CLK, which are accumulated in the address counter 56, as generally described in connection with FIG. 2. The postage data is stored in a series of channels according to postal zone and carrier service. For example, each postal zone may be allotted three separate channels of postage data according to the carrier desired. Thus, one channel of each zone is devoted to the postage for air parcel post (APP), a second for surface parcel post (SPP) and the third for United Parcel Service (UPS). The postage data is stored in binary coded decimal form, most significant digit and most significant bit first. It it is assumed that the left pound bar 260 shown in FIG. 8 corresponds to the 9 pound clock pulse and the one to the right the 10 pound clock pulse, the postage data stored therebetween is applicable to a parcel weighing 9, but less than 10, pounds. Each block of postage data is accompanied by a series of 16 postage clock bits 262 which are read out as postage clock pulses POST CLK to the serial to parallel converter 60 (FIG. 2) to synchronize the handling of the serially read four bits of each postage digit for parallel bit transmission of successive postage digits to the input/output register 58.

It is apparent from FIG. 8, that when the appropriate postal zone has been determined and entered into the zone register 46 (FIG. 8), and the desired carrier APP, SPP or UPS has been selected by the operator, the postage memory readout station is conditioned to serially read out the postage data in only one of the various postage data channels in the postage memory 52.

The zip-zone memory 90, seen in FIG. 9, is also a read-only memory storing an optically encoded zip code to postal zone conversion table carried as a film strip on the periphery of the memory drum 14 (FIG. 1). The array of opaque timing bits 270 are read out to provide the zip clock pulses ZIP CLK which are applied, as previously discussed, as add clock pulses ADD to the input/output register 58, pursuant to counting to the complement of the zip code number entered therein. Aligned with each bar 270 are four bit positions for storing the appropriate zone number in binary coded decimal; the bits being read out in parallel.

The zip-zone memory also includes three additional channels A, B and C which contain flag bits for designating special situations, as will be described in connection with the postage ready logic circuitry 80, generally disclosed in FIG. 2 and detailed in FIG. 12. Any flag bits aligned with the appropriate zone are read out with the zone number in response to the read store zone signal RD STR ZONE and used in conjunction with add-on control data, generally indicated at 272 and stored at the end of the zip to zone conversion table. As will be seen, this add-on data, together with any flag bits read from channels A, B and C is utilized by the postage ready logic 80 to augment the postage data read from the postage memory 52 into the input/output register 58.

Address Counter and Comparator

The address counter 56 of FIG. 2 is shown in detail in FIG. 10 and operates to count the pound clock pulses LB CLK read from the postage memory 52 starting from the beginning of the pound to postage conversion table stored therein. The units digits of the pounds address are accumulated in binary coded decimal form in a units digit stage 280 of the address counter 66. The one and eight bit outputs of the units digit stage 280 are gated together in an AND gate 284 to provide carry pulses which are accumulated in a tens digit stage 282 of the address counter 66. The content of the address counter 66 is continuously compared in comparator 68 with the parcel weight held in the up/down counter 40 (FIGS. 2 and 6). When the address counter 66 has been incremented to a pound count comparable to that held in the up/down counter 40, comparator 66 generates the output COMP on lead 70 and its complement $\overline{\text{COMP}}$ through inverter 286.

As was previously noted, the pound encoder 218 of FIG. 6 is graduated in half-pound increments, thus the up/down counter 40 counts in half-pound increments by virtue of flip-flop 250 in FIG. 6. Since the rate schedule for APP is based on half-pound increments for parcel weights up to 5 pounds and pound increments above 5 pounds, the address counter 66 must be initially adapted to interpret the pound clock pulses LB CLK as half-pound increments up to 5 pounds and pound increments thereafter. To this end, the control logic for the address counter 66 includes two flip-flops 288 and 290, the former serving as a half-pound counter for the pound clock pulses LB CLK and the latter as a 5 pound latch for disabling the half-pound counter when the address counter 66 has been incremented to 5 pounds.

Specifically, as seen in FIG. 10, the pound clock pulses LB CLK from the postage memory 52 arriving over lead 64 are applied to one input of an AND gate 292 and also to the triggering input of the half-pound counter 288. The set output of the half-pound counter is connected as one input to an AND gate 294, whose output is gated with the output of AND gate 292 in an OR gate 296. The output of this OR gate is connected to the clock input of the units digit stage 280 of the address counter 66.

The other input to AND gate 292 is obtained from the set output of the 5 pound latch 290, while the other input to AND gate 294 is obtained from the reset output of the 5 pound latch. Initially, the 5 pound latch is reset by the reset pulse issuing at the beginning of each revolution of the pounds to postage conversion table passed its readout station. Thus, AND gate 292 is disabled, while AND gate 294 is enabled. Similarly, the half-pound counter 288 is also initially in its reset state. The first pound clock pulse LB CLK read from the postage memory 52 after each reset pulse triggers the

When the binary counter **314** goes from a count of 15 to 16 on the leading edge of the 16th postage clock pulse, the output of AND gate **308** goes from ONE to ZERO, triggering postage enter flip-flop POST ENT to its one state. On the trailing edge of the sixteenth postage clock pulse, the last postage digit is shifted into the shift register **302** and the output of AND gate **304** goes to a ONE, which passes through AND gate **324** and OR gate **322** as the fourth enter postage shift pulse ENT POST. This shift pulse terminates as the read postage command signal RD POST goes to ZERO, which occurs when the address counter **66** is incremented and the comparator **68** senses that there is no longer a comparison between the address counter **66** and the up/down counter **40**. Shift register **302** is disabled, as is the binary counter **314** by the reset output of the postage enter flip-flop POST ENT.

Postage Ready Logic

The postage ready logic **80** of FIG. **2**, seen in detail in FIG. **12**, generally handles special situations which affect the postage data entered into the input/output register **58**. In addition, the postage ready logic handles various error situations identified by a flag bit stored in the channel C of the zip-zone memory (FIG. **9**). Ultimately, the postage ready logic is responsible for generating the ready enter signal RDY ENT over lead **84** enabling the postage digit selection apparatus **30** to initiate the setting up of the postage meter **32** to the postage value registered in the input/output register **58**.

Referring to FIG. **12**, the four zone data bits in channels **1**, **2**, **4** and **8** of the zip-zone memory **90** (FIG. **9**) in parallel to multiplexer **44** for entry into the zone register **46** upon issuance of the read store zone command signal RD STR ZONE from the input/output register **58**. If the zone is to be entered from the numerical keyboard **26***a*, depression of the key Z sets flip-flop ZFF in the sequencer **56** (FIG. **3**), and the set output ZFF conditions multiplexer **44** to connect the zone register **46** to the numerical keyboard **26***a* for direct zone entry.

In certain situations, there may not be an appropriate zone conversion for a zip code entered into the input/output register **58**. To handle these situations, the zone number which would be read out in response to the read store zone command signal RD STR ZONE is coded as a decimal nine. Since the postage rate schedules under the parcel post and the United Parcel Service systems only contemplates eight postal zones, a nine readout may be used to identify a zone error. Thus, channels **1** and **8** of the zip-zone memory are applied to an AND gate **400**, together with the read store zone signal RD STR ZONE. If, when the read store zone signal issues, the number 9, in binary coded decimal, is read from the zip-zone memory, AND gate **400** is enabled to set a zone error flip-flop **402**. The set output of this flip-flop may be used to initiate energization of a suitable error light at the control panel **26**.

In certain situations, particularly with respect to the UPS system, United Parcel Service does not have authorized land routes between the mailing site and certain parcel destinations. For these situations, UPS resorts to so-called "drop shipping," requiring special shipping charges which the present system is not equipped to handle. However, it is necessary to identify these special situations, and the present system is equipped to do so. To this end, a flag bit is encoded in channel C in the zip-zone memory (FIG. **9**) aligned with storage locations of those zones for which "drop shipping" must be employed. The coincidence of a readout of a flag bit from channel C and the issuance of a read store zone signal is detected by AND gate **404**, whose output is connected to set a flip-flop **406** to register the occurrence of a C error. The set output of this flip-flop may be used to initiate energization of an appropriate error light to notify the operator that, for example, a "drop shipping" situation has arisen.

Returning briefly to the sequencer of FIG. **3**, it will be recalled that error signal M issues from AND gate **134** if the system fails to locate a zone on the basis of a zip code entry into the input/output register **58**. Returning to FIG. **12**, this error signal M is applied to set an M error flip-flop **408**. It will be noted that the reset outputs of flip-flops **402**, **406** and **408** are gated together in an AND gate **410**, whose output is connected as one input to an AND gate **412** from which the ready enter signal RDY ENT issues. As a consequence, if an error situation is detected, AND gate **412** is disabled to inhibit the ready enter signal and thus prevent the postage digit selection apparatus **30** from setting the postage meter **32** to any postage value registered in input/output register **58**. In addition, if the postage value in the input/output register is to be displayed only, the display only key D/O (FIG. **3**) is depressed to set the display only flip-flop D/OFF, and its reset output $\overline{\text{D/OFF}}$ disables AND gate **412** to inhibit the ready enter signal.

Flag bits encoded in the channels A and B of the zip-zone memory **90** and read out during the occurrence of a read store zone signal RD STR ZONE are used in conjunction with the add-on postage control data **272** (FIG. **9**) stored at the end of the zip-zone conversion table stored in the zip-zone memory. As seen in FIG. **12**, the readout of flag bits stored in channels A and B are used to set one of three flip-flops **420**, **422** and **424**. Specifically, the readout of channel A is applied to AND gates **426** and **428**, and, through an inverter **430**, to AND gate **432**. The readout of channel B is applied to AND gate **428**, AND gate **432**, and through an inverter **434**, to AND gate **426**. The read store signal RD STR ZONE is applied as a third input to each of these gates. If a flag bit is read from channel A when the read store zone signal issues, an output issues from AND gate **426** to set the flip-flop **420**, labeled AB. If a flag bit is read from channel B when the read store zone command signal issues, the resulting output from AND gate **432** sets flip-flop **422**, labeled $\overline{\text{AB}}$. If a flag bit is read from both channels A and B when the read store zone signal issues, AND gate **428** provides an output to set flip-flop **424**, labeled AB.

Assuming that no additional postage function is to be executed, and thus neither of the flip-flops **420**, **422** and **424** is set, their reset outputs, all logical ONES, enable an AND gate **440**, whose output enables an AND gate **422**. Thus, AND gate **442** is conditioned to pass the postage entered signal POST ENT generated by the postage entered flip-flop in the serial to parallel converter **60** (FIG. **11**) through to one input of a normally enabled AND gate **444**. It will be recalled that the postage entered signal POST ENT issues as the last postage digit is shifted into the input/output register **58**.

The AND gate **444** is normally enabled from the reset output of an add postage flip-flop ADD POST, and thus the postage entered signal is passed through to OR gate **446** to set a postage ready flip-flop POST RDY. Assuming no error and that the postage is not merely to be displayed, the logical ONE at the set output of the postage ready flip-flop is passed through AND gate **412** as the ready enter signal RDY ENT for transmission over lead **84** to the postage digit selection apparatus **30** (FIG. **2**).

On the other hand, if one of the flip-flops **420**, **422** and **426** has been set during the issuance of the read store zone signal RD STR ZONE, the output of AND gate **440** is a logical ZERO, which is inverted by an inverter **441** to a ONE to enable an AND gate **443**. Thus, the postage entered signal POST ENT passes through AND gate **443** to set add postage flip-flop ADD POST. Since AND gate **442** is disabled from the output of AND gate **440**, the postage entered signal is inhibited from setting the postage ready flip-flop POST RDY.

Still referring to FIG. **12**, the set output of the AB flip-flop **420** is connected to an AND gate **450** together with the readout of channels **1**, **2** and **8** of the zip-zone memory. The set output of $\overline{AB}$ flip-flop **424** is gated in AND gate **452** with the readout of channels **2** and **8** of the zip-zone memory, while the set output of AB flip-flop **422** is gated in AND gate **454** with the readout of channels **4** and **8**. The outputs of AND gates **450**, **452** and **454** are gated together in an OR gate **456**, whose output is gated with the reset output $\overline{\text{POST RDY}}$ of the postage ready flip-flop in an AND gate **456** to provide an add clock gate signal ADD CLK GATE. It will be recalled that the add clock gate signal is used in the sequencer **56** of FIG. **3** to enable AND gate **130** to pass zip clock pulses ZIP CLK as add clock pulses ADD CLK over lead **93** to input/output register **58**.

Referring to FIG. **9**, the add-on postage control data **272**, stored at the end of the zip to code conversion table in zip-zone memory is selectively encoded in channels **1**, **2**, **4** and **8** to gate a selective number of zip clock pulses ZIP CLK through gate **130** in the sequencer **56** to increment the postage value in the input/output register. For example, under the UPS rate schedule, shipping from west to east requires a flat 5 cent charge in addition to the charge applicable to the parcel weight. If it is assumed that this situation is identified by encoding a flag bit in channel B opposite the various zone which would require a west to east shipment, when the read store zone signal RD STR ZONE issues to read out one of those zones, a flag bit would also be read from channel B to set the $\overline{AB}$ flip-flop **422**. The set output of the AB flip-flop enables AND gate **454**. When the add-on postage data block **272** revolves around to the readout station, it is seen that the first five bit positions in both channels **4** and **8** are opaque and thus ONES. Thus, AND gate **454** is enabled for these first five bit positions, and its logical ONE output passes through OR gate **456**, AND gate **458**, and OR gate **128** in the sequencer (FIG. **3**) to enable AND gate **130** to pass five zip clock, pulses ZIP CLK as add clock pulses ADD CLK to the input/output register **58**. It is thus seen that the postage value held in the input/output register **58** is incremented by five cents.

Similarly, if flag bits are read out from both channels A and B at the time of the read store zone signal, the AB flip-flop **424** is set. This qualifies AND gate **452** for seven zip clock pulses, which are gated through AND gate **130** in the sequencer to increment the postage value in the input/output register by 7 cents. Finally, if a flag bit is read from channel A at the time of the read store zone signal, $\overline{AB}$ flip-flop **420** is set to enable AND gate **450**, and the postage value in the input/output register is incremented by 6 cents.

The conclusion of the add-on postage data block **272** is marked by logical ONE bits encoded in the **4**, **8** and C channels of the zip-zone memory **90**, as seen in FIG. **9**. The coincidence of these bits detected in an AND gate **461**, and the resulting gate output forces the add postage flip-flop ADD POST back to its reset condition. The resulting logical ONE to ZERO transition on its set output sets the postage ready flip-flop POST RDY. The set output of this flip-flop goes to a logical ONE, which passes through AND gate **412** as the ready enter signal RDY ENT to the postage digit selection apparatus **30** of FIG. **2**.

When it is desired to add additional postage from the control panel to cover insurance, special handling, etc., the key $ is depressed, followed by entry of the additional charge into the input/output register **58** via numerical keyboard **26***a*. The set output $FF of flip-flop $FF in sequencer **56** enables an AND gate **447** in the postage ready logic **80**. Then, when the postage request key PR is depressed, the output of AND gate **447** goes to a ONE, forcing the postage ready flip-flop POST RDY to its set state. This results in the immediate generation of the RDY ENT signal at the output of AND gate **412**, and the postage digit selection apparatus **30** proceeds to set up the postage meter to issue a second stamp imprinted with the additional postage as entered from the control panel.

Oversize Logic

The oversize logic **100** of FIG. **2** is shown in detail in FIG. **13**. In the event of an oversized parcel, the operator presses the oversize key O/S to set oversize flip-flop O/SFF, as previously described. The reset output $\overline{O/S}$ of this flip-flop to used to disable AND gate **138** in the sequencer **56** (FIG. **3**) to inhibit derivation of the read postage command signal RD POST at the output of OR gate **140** from the comparator output signal COMP, applied as one of the other inputs to AND gate **138**. The set output of the oversize flip-flop O/SFF is gated in an AND gate **470** with the COMP signal from comparator **68** (FIGS. **2** and **10**). If the comparator output signal goes to a logical ONE during the time that the oversize flip-flop O/SFF is set, an output issues from AND gate **470** to set a flip-flop **472**. An AND gate **474** decodes the outputs of the address counter **66** (FIG. **10**) and resets the oversize flip-flop O/SFF when the count in the address counter reaches 24. It is thus seen that for an oversized package situation, the oversize flip-flop is initially set, and if the compare signal COMP comes up before the address counter increments to 24, the latch flip-flop **472** is set to store the fact that the oversized package weighs less than the established minimum weight, in this case 25 pounds. The set output of the flip-flop **472** qualifies an AND gate **480** which is connected to also decode the outputs of the address counter when it is incremented to 25 pounds. The remaining input to AND gate **480** is the reset output of the postage ready flip-flop $\overline{\text{POST RDY}}$. The set output

SL of the search pounds flip-flop SL in the sequencer **56** (FIG. 3) is gated with the set output of the oversize flip-flop in an AND gate **481** to provide a qualifying input to AND gate **474** during the search pounds mode.

From the above description, it is seen that if the oversized package weighs less than 25 pounds, flip-flop **472** is set, and, when the address counter **66** increments to 25 pounds, the read minimum pounds command signal RD MIN LBS issues from AND gate **480**. This signal is supplied over lead **108** to OR gate **140** in the sequencer **56** of FIG. **3** to derive the read postage command signal RD POST, applied over lead **72** to the serial to parallel converter **60** (FIG. **11**). If, on the other hand, the oversized package weighs 24 pounds or more, the oversize flip-flop O/SFF is reset from the output of AND gate **474** to remove the disabling input $\overline{O/S}$ from AND gate **138** in the sequencer **56**. Stated another way, the reset output $\overline{O/S}$ of the oversize flip-flop goes to a logical ONE to enable AND gate **138** in the sequencer. AND gate **480** was not qualified to generate the read minimum pounds signal RD MIN LBS since flip-flop **472** had not been set. As a consequence, the read postage command signal RD POST is derived from the compare signal COMP, which in this event occurs when the address counter has been incremented to the actual weight of the oversize package, as would be the case if the oversized parcel key O/S had not been depressed in the first place.

Postage Selection Apparatus

The electromechanical postage digit selection apparatus **30**, seen generally in FIGS. **1** and **2**, is shown in detail in **14** through **18**. It will be recalled from the general description of FIGS. **1** and **2** that the postage digit selection apparatus is mechanically interconnected to the settable postage digit arms **33** of postage meter **32** by links **34** and operates to position the postage digit arms to the corresponding postage digit values registered in the input/output register **58**.

Referring first to FIG. **15**, the postage digit selection apparatus **30** includes a motor **500** supported by a frame casting **502**. The output shaft **504** of motor **500** carries a gear **506** which meshes with a gear **508** keyed on an elongated jack shaft **510**, best seen in FIG. **14**. Jack shaft gear **508** engages gears **512** and **514** respectively mounted on the input shafts **516** and **518** of clutches **520** and **522**. The other end of jack shaft **510** carries a gear **524** which engages a pair of gears **526** and **528** respectively mounted on the input shafts **530** and **532** of clutches **534** and **536**.

Output shaft **527** of clutch **522** extends coaxially through input shaft **518**, which is in the form of a sleeve, and beyond both sides of the clutch body and carries at one end a crank **529**. This crank is pivotally connected to one end of link **34*a***, which is pivotally connected at its other end to the hundredths digit selector arm **33** of the postage meter **32**. Similarly, the output shaft **521** of clutch **520** carries at one end a crank **523** which is pivotally connected to one end of link **34*b***. The other end of link **34*b*** is pivotally connected to the tenths digit selector arm **33** of the postage meter **32**. One end of output shaft **535** of clutch **534** carries a crank **537**, which is pivotally connected to one end of the units digit selection link **34*c***, while one end of output shaft **539** of clutch **536** carries a crank **541** pivotally connected to the one end of the tens digit selection link **34*d***.

It will be appreciated that the various clutch output shafts and jack shaft **510** are journalled by laterally spaced vertical extensions **503** of the frame casting **502**.

Still referring to FIG. **14**, the other end of output shaft **527** of clutch **522** is adapted to mount an encoder disc **550** rotating with the output shaft in a plane between a light source **550*a*** and a receiver **550*b***. Disc **550** is encoded in binary coded decimals with the numbers 0 through 9 around its periphery and is angularly oriented on output shaft **527** so as to provide a digital readout of the digit positions of the hundredths postage digit selector arm **33**, as positioned by crank **529** and link **34*a***. Similarly, output shaft **521** mounts an encoder disc **552** which is read out by a light source **552*a*** and receiver **552*b*** to provide a digital readout of the digit positions of the tenths postage digit selector arm, as positioned by crank **523** and interconnecting link **34*b***. In the same manner, encode discs **554** and **556** provide digital readouts of the digit positions of the units and tens postage digit selector arms of the postage meter **32**.

Each of the clutch output shafts carries a detent disc which serves to ultimately angularly orient the clutch output shafts to the various postage digit positions. In practice, these detent discs serve as course positioning means for the postage digit selector arms **33** of the postage meter; the internal detent mechanism of the postage meter serving as the final, precise digit positioning means for the various postage digit selector arms. Thus, as seen in FIGS. **14** and **15**, output shaft **527** carries a detent disc **560** which is formed with an annular array of detents **560*a***, as best seen in FIG. **15**. The detents **560*a*** are engaged by a pawl **560*b*** to ultimately angularly orient the crank **529** and link **334*a*** for the various hundredths postage digit positions. Similarly, output shaft **521** carries a detent disc **562** formed having an array of detents **562*a*** which are engaged by pawl **562*b*** to ultimately orient crank **523** and link **34*b*** for the various tenths postage digit positions. In the same manner, putput shafts **535** and **541** carry detent discs **564** and **566**, respectively, which are engaged by pawls **564*b*** and **566*b*** to ultimately orient their associated cranks and links for the various units and tens postage digit positions.

The operation of the postage selection apparatus **30** can best be appreciated from a description of FIG. **18**. As long as the system is turned on, motor **500** of the postage selection apparatus **30** (FIG. **15**) is energized to supply continuous drive to the input shafts of the various clutches of FIG. **14**. The various clutches are initially conditioned such that their input shafts are drivingly coupled to their output shafts, and the various cranks are continuously rotated. The links **34** interconnecting the cranks and the postage digit selector arms **33** cause the selection arms to continuously move back and forth through their various postage digit positions. As seen in FIG. **18**, the digital readout of the positions of the hundredths postage digit selector arm is supplied to a comparator **570** for comparison with the content of the hundredths digit register **156** of the input/output register **58** (FIG. **4**). Similarly, the digital readout of the positions of the tenths digit selector arm is applied to comparator **572** for comparison with the content of the tenths digit register **154** of input/output register **58**. The digital readout of the positions of the units postage

digit selector arm is fed to comparator **574** for comparison with the content of the units digit register **152** of the input/output register while the digital readout of the tens postage digit selector arm digit positions is compared with the content of the tens digit register **150** of the input/output register in a comparator **576**.

The outputs of these comparators are supplied as one input to separate AND gates **571, 573, 575** and **577**. The other input to each of these AND gates is the ready enter signal RDY ENT, which issues from the postage ready logic **80** (FIG. **12**) when it is determined that the postage value stored in the input/output register is the final value to be issued by the postage meter **32**.

As the postage digit selection arms **33** are moved to the postage digit positions called for by the corresponding postage digits held in the input/output register, AND gates **571, 573, 575** and **577** supply outputs to the various clutches effective to disengage their input shafts from their output shafts. Thus, as the hundredths postage digit selector arm moves to the digit position corresponding to the hundredths postage digit stored in the hundredths digit register **156** of the input/output register **58**, comparator **570** generates an output which passes through AND gate **571** to disengage clutch **522**. Output shaft **527** is decoupled from input shaft **518** of clutch **522**, and crank **529** and link **34***a* are ultimately positioned by pawl **560***b* acting on detent disc **560**. However, the ultimate and precise positioning of the hundredths postage digit selector arm is achieved by the internal detent mechanism of the postage meter **32**. The tenths, units and tens postage digit selector arms **33** of the postage meter **32** are ultimately positioned in accordance with the digit contents of the tenths, units and tens postage digits stored in the input/output register **58** in the same manner. It will be noted that the positions of the postage digit selector arms are carried out concurrently and independently of each other, thus permitting rapid postage setting of the postage meter **32**.

When all of the postage digit selector arms **33** have been positioned, AND gate **580** is enabled to pass an execut signal EXEC over lead **87** (see also FIG. **2**), commanding the postage meter to execute a print cycle and issue a stamp with the postage value held in the input/output register imprinted therein. At the conclusion of the postage meter operating cycle, the cycle complete signal O issues to be fed back to the console to clear the various flip-flops, registers and counters preparatory for the next system operation.

As seen in FIGS. **16** and **17**, the forward end of each link **34** is formed having an elongated slot **582** which accommodates a laterally extending pin **584** carried at the upper end of each postage digit selector arm **33**. A latch **586** pivotally mounted on a pin **588**, carried adjacent the forward end of each link **34**, engages the side of the postage digit selector arm **33** opposite pin **584** so as to maintain the pin captive in slot **582**. By virtue of this arrangement, there is provided a lost motion connection between the links **34** and their associated postage digit selector arms **33**, thereby enabling the internal detent mechanism of the postage meter to take over from the final positioning of the postage digit selector arms from the various detent discs **560, 562, 564** and **566** of the postage digit selection apparatus **30**.

Arm **586** at the forward end of each link **34** is biased downwardly into engaging relation with the postage digit selector arm **33** by a spring **590**. The arm **586** is readily pivoted upwardly, as indicated in phantom in FIG. **16** to facilitate disconnection of the links from their associated postage digit selector arms **33**, thus freeing the upper portion of the postage meter **32** for removal from its base when it becomes necessary to obtain additional prepaid postage at a local post office.

Parallel Postage Data System

A modification of the console **10** shown in the functional block diagram of FIG. **2** is disclosed in FIG. **19**. The major distinction between the two consoles is that, in the former the data is stored in the postage memory in serial binary coded decimal, whereas in the latter, now to be described, the data is stored and read out in parallel from the postage memory. The layout of the pounds to postage conversion table stored in the postage memory **600** is generally shown in FIG. **20**. Basically, the postage data for each zone is stored in separate blocks on the basis of pounds. It will be recalled from FIG. **8**, that in the console design of FIG. **2**, the postage data for a particular zone is stored serially in a single channel. To provide for separate services, such as parcel post (PP) and UPS, separate pounds to postage conversion charts would be stored at different locations on the memory drum **14**, rather than integrated into a single chart, as illustrated in FIG. **8**.

It is appreciated that by virtue of the layout of the postage data illustrated in FIG. **20**, all bits making up the digits of the postage values are successively read out in parallel into the input/output register, thus eliminating the need for a serial to parallel converter. The console of FIG. **19** is disclosed as a three bank system (3 postage digits) for purposes of simplicity, rather than a four bank system, as has been described. Thus, as illustrated in FIG. **19**, the readout of postage memory **600** is applied in parallel to the respective digit registers of an input/output register **602**.

The zip to zone conversion table stored in the zip-zone memory **604** of the console of FIG. **19** is similar to that shown in FIG. **9**, except that location of the appropriate zone number is based on counting zip clock pulses up to the zip code number entered from the keyboard **26***a* rather than the complement thereof. Thus, as seen in FIG. **19**, the first three digits of the zip code number are entered via the numerical keyboard **26***a*. However, instead of entering the zip code number into the input/output register, the keys of the keyboard **26***a* are self-latching, such that they remain depressed to develop a sustaining digital output in binary coded decimal for application to a comparator **608**. The zip code numbers are read from the zip-zone memory **604** in parallel into a zone register **610**. The zip clock pulses ZIP CLK are read from the zip-zone memory **604**, beginning from a reset pulse (indicated at **611** in FIG. **20**) issuing in advance of the beginning of the readout of the zip to zone conversion table, and are accumulated in a counter **612**. When the counter **612** is incremented to the zip code number registered by keyboard **26***a*, comparator **608***a* generates an output which causes the zone register **610** to accept and hold the zone number then being read from the zip-zone memory **604**.

As in the console of FIG. 2, the zone register 610 of FIG. 19 may be adapted to accept zone entry from the zip-zone memory 604 or directly from the numerical keyboard 26*a* by using a multiplexer (not shown).

Having loaded the zone register 610 with the applicable postal zone, the console must now locate the block of postage data in the postage memory 600 applicable to that zone. To this end, a zone counter 618 is incremented as each zone block of postage data comes up for readout. When the zone counter has been incremented to the zone number held in the zone register 610, comparator 620 provides a compare output indicative of the fact that the postage data applicable to the appropriate postal zone is arriving at the readout station. To increment the zone counter 618, a decimal 10 is encoded in the least significant postal digit location in advance of each zone postage data block, as indicated at 619 in FIG. 20. A decimal 10 digit is used since this number is not a valid postage digit value.

Thus, as seen in FIG. 19, as the least significant digit is read out from the postage memory 600 into the input/output register 602, the two and eight bits thereof are decoded in an AND gate 622 to provide for a decimal 10 digit a zone increment pulse Z-INC, which is gated through AND gate 624 to increment the zone counter 618. To reset the zone counter 618 at the end of each pounds to postage conversion table (e.g., one of PP and one for UPS) stored in the postage memory 600, a decimal 10 is encoded in the tenths digit position as indicated at 621 in FIG. 20, which, when read out into the input/output register, is detected by AND gate 626 to develop a zone reset pulse Z-RESET to reset the zone counter 618 to 0.

The scale, scale encoder and up/down counter, commonly indicated at 630 in FIG. 19, may be constructed in the manner previously described for the console of FIG. 2. The weight registered in the up/down counter is continuously compared in a comparator 632 with the accumulating pound clock pulses LB CLK read from the postage memory into an address counter 634. A compare output from comparator 632 is used to condition the input/output register 602 to hold the postage data applicable to the parcel weight, as read from postage memory 600. Unlike the console of FIG. 2, the console of FIG. 19 employs a separate address counter 636 to handle oversized parcel situations. A logic network 638 is set up to generate the decimal digits of the appropriate minimum pounds limit for an oversized package depending on the carrier desired; the minimum pounds value being compared with the accumulating pound clock pulses LB CLK in the oversize address register 636 in a comparator 639 to generate a compare output which is used to condition the input/output register 602 to hold the postage data applicable to the minimum weight, as read from the postage memory 600.

The remaining components of the console disclosed in FIG. 19 will be considered during the following description of its operation.

After a parcel has been placed on the scale and its weight has been registered in the up/down register 630, the postage request key PR is depressed to set the postage request flip-flop PRFF. The set output of this flip-flop enables an AND gate 650 to pass the next reset pulse readout from the zip-zone memory 604, which is effective to set a read zone flip-flop RZ. As previously noted, the reset pulse is read from the zip-zone memory just prior to the arrival of the beginning of the stored zip to zone conversion table at ita readout station. The set output of the read zone flip-flop RZ enables an AND gate 652 to pass zip clock pulses ZIP CLK, read from the zip-zone memory, through to increment counter 612. The counter begins counting up to the zip code number previously entered via the numerical keyboard 26*a*. Upon comparison, comparator 608 generates an output, enabling AND gate 654 to pass the next occurring zip clock pulse through to zone register 610, which is thereby conditioned to hold the zone number last read from the zip-zone memory 604.

Having obtained the appropriate zone number based on the zip code entered via keyboard 26*a*, the next occurring reset pulse from the zip-zone memory passes through AND gate 650 to trigger the read zone flip-flop RZ to its reset stage. Its set output goes from ONE to ZERO, causing a read postage flip-flop RP to the triggered from its reset condition to its set condition. The set output of the read postage flip-flop RP is connected to the set enabling input of a read postage set flip-flop RP SET. As in the case of the console of FIG. 2, the cycle complete signal O is transmitted back from the postage meter 32 at the conclusion of the last cycle zeroes the various flip-flops preparatory for the next system operating cycle.

As previously described, zone counter 618 is reset from the output of AND gate 626 and is incremented from the output of AND gate 624. In addition, address counters 634 and 636 are reset by each Z-INC pulse issuing from AND gate 624. When the zone counter is incremented to the zone number held in zone register 610, comparator 620 issues an output to qualify one input of an AND gate 660. The input/output register 602 now is receiving from postage memory 600 postage data applicable to the appropriate zone. The pound clock pulse train, indicated at 661 in FIG. 20, associated with the zone postage data block is accumulated in address counter 634 for comparison with the parcel weight held in the up/down counter 630. When the contents of the two counters compare, comparator 632 issues an output to AND gate 660, enabling this gate to pass the next occurring pound clock pulse, which is effective to trigger the flip-flop RP SET to its set condition. The reset output of this flip-flop goes to a logical ZERO to disable address counter 634, and it retains the pound count which compared with the parcel weight held in the up/down counter 630. The ZERO to ONE transition at the set output of flip-flop RP SET passes through AND gate 662 and OR gate 664 as a store postage command signal STR POST to the input/output register 602, conditioning it to retain the postage digits just read from the postage memory 600. These postage digits represent the postage value applicable to the parcel weight and the postal zone of its destination. When the store postage signal STR POST assumes a logical ONE, it is inverted in an inverter 666 to disable AND gate 624 and inhibit further Z-INC pulses. The postage retained in input/output register 602 is then applied to the postage digit selection apparatus 30 pursuant to positioning the postage digit selector arms of the postage meter to the appropriate digit positions and the initiation of a postage meter cycle to issue an appropriately imprinted stamp.

In the event of an oversized parcel situation, oversize key O/S is depressed to set oversize flip-flop O/SFF. It will be noted that the reset output of oversize flip-flop O/SFF is now a logical ZERO, disabling AND gate **662**. The set output of this flip-flop enables AND gate **668**, whose other input comes from the set output of a read postage oversize flip-flop RPO/S. The reset output of this flip-flop, when a logical ONE, enables the oversize address counter **636** to accumulate pound clock pulses LB CLK read from the postage memory **600**.

If the actual weight of the oversized package is less than the minimum weight established by the minimum pound setting logic **638**, a compare output will first issue from comparator **632**. The read postage set flip-flop RP SET is set, but the ZERO to ONE transition at set output is blocked by the now disabled AND gate **662**. When the minimum weight count is accumulated in the oversize address counter **636**, comparator **639** provides an output which sets the read postage oversize flip-flop RPO/S. Since AND gate **668** is enabled from the set output of the oversize flip-flop O/SFF, the ZERO to ONE transition on the set output of flip-flop of RPO/S passes through, as the store postage command signal STR POST to the input/output register **602**. This register then retains the postage applicable to the minimum pounds limit established by the logic **638** as read from postage memory **600**.

On the other hand, if the oversized parcel weights more than the minimum pounds setting, a comparison output first issues from comparator **639**. Flip-flop RPO/S is not set since it is effectively disabled by the logical ZERO on the set output of the read postage set flip-flop RP SET. The output of comparator **639** is however effective to reset oversize flip-flop O/SFF through AND gate **663** when reading the appropriate zone data block, thus enabling AND gate **662** to pass the store postage command signal STR POST when the read postage set flip-flop RP SET is set from the output of AND gate **660**.

The system of FIG. **19** is also adapted to increment the postage value retained in the input/output register **602** in response to the STR POST signal by a pre-set amount, such as 5 cents, as required under the UPS system for shipments west to east. A west to east shipping situation is identified by flag bits stored in the zip-zone memory **604** in alignment with the various stored zones which call for a west to east shipment. When zone register **610** is conditioned from the output of AND gate **654** to retain the appropriate zone read from the zip-zone memory **604**, the output of this gate also enables an AND gate **675** to pass a flag bit, if read from the zip-zone memory **604**, to set a west to east flip-flop W-E. The set output of this flip-flop goes to a ONE to enable AND gate **677**. The other inputs to AND gate **677** are zip clock pulses ZIP CLK and the store postage command signal STR POST. The output of this AND gate is applied to the increment input of the input/output register **602** and to the clock input of a counter **679**. The one and four bit outputs of counter **679** are gated together in AND gate **681** to generate a reset pulse for flip-flop W-E when the counter is incremented to five by the zip clock pulses passed through AND gate **677**.

It is seen that the number of zip clock pulses incremented in the counter **679** are also effective to increment the postage value held in the input/output register **602**. Thus, when the store postage command signal STR POST issues from OR gate **664** to, in effect, latch up the input/output register **602** with the postage value read from the postage memory applicable to the parcel weight, this signal also enables AND gate **677**. If the west to east flip-flop W-E had been set from the output of AND gate **675**, clock pulses pass through AND gate **677** to increment both the input/output register and counter **679**. When the counter is incremented to five, or any other desired pre-set number, the output of AND gate **681** resets the west to east flip-flop, thereby disabling AND gate **677**. The postage originally held in the input/output register **602** has thus been incremented by 5 cents.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in the above constructions without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

Having described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A postage metering system comprising, in combination:

A. a scale for weighing a parcel;

B. an encoder providing an electrical readout of the weight reading of said scale;

C. a weight register electrically connected to said encoder for registering said electrical readout;

D. a cyclical postage memory storing a weight to postage conversion table, said table including

1. a channel storing a series of weight clock pulses, each pulse representing an increment of parcel weight, and

2. recorded postage data physically arranged by parcel weight and postal zones;

E. a cyclical zip-zone memory storing a zip code to postal zone conversion table, said table including

1. a channel storing a series of zip clock pulses, each pulse representing a different zip code number, and

2. stored postal zone data physically associated with each zip clock pulse to provide the postal zone number conversion for the zip code number represented thereby;

F. a zone register adapted to hold a postal zone number and adapted to access said postage memory for the postage assigned thereto;

G. entry means for entering a zip code number;

H. zone search means initiated upon a postage request to accumulate said zip clock pulses read from said zip-zone memory from the beginning of a memory cycle and thereby locate the stored postal zone number conversion for the entered zip code number, said located postal zone number conversion being entered into said zone register;

I. an output register;

J. postage memory address means initiated upon entry of a postal zone number in said zone register, said means including

1. an address counter for accumulating weight clock pulses read from said postage memory from the beginning of a memory cycle, and

2. a comparator for comparing the contents of said weight register and said address counter and providing a weight compare signal locating in said postage memory the postage data applicable to the parcel weight registered in said weight register; said located postage data being entered in said output register;

K. a postage meter; and

L. means for setting said postage meter to the postage digits of the postage data in said output register and initiating a meter operating cycle.

2. The postage metering system defined in claim 1, wherein said electrical readout of said encoder is in the form of a series of pulses proportional in number to the weight reading of said scale, said weight register is in the form of an up/down pulse counter connected to accumulate said pulses.

3. The postage metering system defined in claim 2, wherein said encoder is adapted to provide distinctively different pulse outputs depending upon the direction of response of said scale, and said weight register includes steering logic circuitry adapted to interpret said encoder pulse outputs and control said up/down counter to be incremented and decremented in accordance with the scale response direction.

4. The system defined in claim 1, wherein said entry means includes a numerical keyboard for entering zip code and postal zone numbers, and means for selectively conditioning said zone register to accept a postal zone number entry directly from said keyboard and thereupon to immediately initiate said postage memory address means without initiating said zone search means.

5. The system defined in claim 1, wherein said output register is adapted to hold a zip code number entered by said entry means and is further adapted as a pulse counter for accumulating said zip clock pulses read from said zip-zone memory, said zone search means including first gating means operating to pass said zip clock pulses to said output counter to increment said output register and second gating means for detecting when said output register is zeroed to develop a store zone signal conditioning said zone register to accept and hold the postal zone member conversion for said zip code entry, as read from said zip-zone memory.

6. The system defined in claim 1, wherein said entry means comprises a numerical keyboard for generating a zip code number entry, and said zone search means includes a counter for accumulating said zip clock pulses and a comparator for generating a store zone signal conditioning said zone register to accept and hold the postal zone number conversion for the entered zip code number, as read from said zip-zone memory, when said counter has been incremented to the entered zip code number.

7. The system defined in claim 1, wherein said postage data is stored in said postage memory in serial binary coded decimal, said system further includes a serial to parallel converter operating to arrange the bits of each postage data digit read serially from said postage memory for parallel transmission, digit by digit, to said output register.

8. The system defined in claim 7, wherein said postage memory stores a series of postage clock pulses which are read out to synchronize the operation of said serial to parallel converter.

9. The system defined in claim 1, wherein said postage of said weight to postage conversion table is grouped in successive postal zone data blocks, each said block including postage for a particular postal zone and arranged relative to said weight clock pulses by parcel weight, and said system further includes a zone counter adapted to be incremented as each said zone data block comes up for readout during each cycle of said postage memory and a comparator adapted to provide a zone compare signal when said zone counter has been incremented to the postal zone number held in said zone register, said zone compare signal serving to access said postage memory for the postage data assigned to the postal zone number held in said zone register.

10. The system defined in claim 9, wherein said postage memory address means further includes gating means connected to detect a coincidence of said zone compare signal and said weight compare signal for developing a store postage command signal conditioning said output register to hold the applicable postage, as read from said postage memory.

11. The system defined in claim 1, which further includes oversize logic circuitry adapted to be triggered to an activated condition for an oversized parcel situation, said circuitry including first gating means for inhibiting said weight compare signal as long as said circuitry is in its activated condition, means connected to said postage memory address means for generating a read minimum weight signal locating in said postage memory for entry into said output register the postage applicable to an oversized parcel weighing less than an established minimum weight, and second gating means responsive to said weight compare signal and said read minimum weight signal for de-activating said oversize logic circuitry when an oversized parcel weighs more than the established minimum weight.

12. The system defined in claim 1, which further includes a display panel electrically connected to display the numerical content of said output register.

13. The system defined in claim 1, which further includes add-on postage logic circuitry conditioned by flag bits stored in said zip-zone memory and read therefrom in conjunction with the readout of the postal zone number conversion into said zone register, said add-on postage logic including means for incrementing the applicable parcel postage entered in said output register from said postage memory to a selected increased value.

14. The system defined in claim 13, wherein said add-on postage logic circuitry includes gating means adapted to pass a predetermined number of said zip clock pulses read from said zip-zone memory to increment the applicable postage in said output register entered from said postage memory.

15. The system defined in claim 14, wherein said add-on postage logic circuitry includes gating means controlled by a pulse counter counting said zip clock pulses up to said predetermined number.

16. The system defined in claim 14, wherein said zip-zone memory stores add-on postage control data at the end of said zip code to postal zone conversion table, said add-on postage logic circuitry includes means responsive to the readout of said add-on postage control data for controlling said gating means to pass a predetermined number of said zip clock pulses to increment the postage held in said output register.

17. The system defined in claim 1, wherein said entry means includes a keyboard for entering postage directly into said output register, and said system further includes means initiating operation of said postage meter setting means upon keyboard entry of postage into said output register.

18. The system defined in claim 1, wherein said postage meter setting means includes:

1. units digit, tenths digit and hundredths digit clutches, each having input and output shafts;
2. a motor continuously drivingly rotating said clutch input shafts;
3. links interconnecting the respective output shafts of said clutches to the units, tenths, and hundredths postage digit selector arms of the postage meter, whereby to reciprocate the various postage digit selector arms through their various digit positions so long as their respective clutches are engaged;
4. separate means coupled to each said clutch output shaft for providing digital readouts of the digit positions of the associated postage meter digit selector arms as they are moved through their various digit positions; and
5. separate comparator means for continuously comparing the digital readouts of the postage digit positions of the various postage digit selector arms with the corresponding postage digit held in the output register, and, as comparisons are achieved, signalling the appropriate clutches to disengage their input shafts from their output shafts, whereby to stop the various postage digit selector arms at the postage digit position called for by the corresponding postage digits held in the output register.

19. The system defined in claim 18 wherein said postage meter setting means further includes gating means electrically connected to each said comparator means for signalling the postage meter to execute a print cycle upon disengagement of all of said clutches.

20. A parcel postage metering system comprising, in combination:

A. a scale for weighing a parcel and providing a digital readout of its weight;
B. a weight register for storing said digital weight readout;
C. a read-only memory containing zone address data for separately locating a plurality of stored weight-to-postage conversion tables, each said conversion table containing weight address data for separately locating associated postage data;
D. a zone register for storing the postal zone number of the parcel destination;
E. memory address means responsive to the contents of said weight and zone registers and the readouts of said zone and weight address data from said memory for generating a first control signal locating the postage data applicable to the parcel;
F. oversized parcel logic circuitry including
   1. means responsive to said weight address data read from said memory for generating a second control signal locating the postage data applicable to the minimum weight for an oversized parcel, and
   2. gating means activated for an oversized parcel situation and connected to receive said first and second control signals, said gating means operating to generate a store postage signal in response to said first control signal when the parcel weight exceeds the minimum weight and in response to said second control signal when the parcel weight is less than the minimum weight; and
G. an output register conditioned by said store postage signal to accept and hold the postage data located by the one of said first and second control signals to which said store postage signal is responsive.

21. The parcel postage metering system defined in claim 20, wherein:

1. said weight address data consists of a series of recorded weight clock pulses, each representing an increment of parcel weight;
2. said postage data consists of discrete, recorded postage values serially arranged according to parcel weight as represented by the accumulating counts of said weight clock pulses read out from the beginning of said conversion tables during a cycle of said memory,
3. said address means includes a counter for accumulating said weight clock pulses read from said memory from the beginning of each said conversion table, and a comparator for continuously comparing the count in said counter with the contents of said weight register and generating said first control signal when the comparison is detected, and
4. said oversized parcel logic circuitry includes means for registering weight data representing the minimum weight for an oversized parcel, a counter for accumulating said weight clock pulses read from said memory from the beginning of each said conversion table, and a comparator for comparing the count in said counter and the minimum weight data in said registering means and generating said second control signal when a coincidence is sensed.

22. The parcel postage metering system defined in claim 20 which further includes a postage meter and postage digit selection apparatus operating to physically position the various postage digit selector arms of said meter in accordance with the digits of the postage data held in said output register.

23. The system defined in claim 22, wherein said postage digit selection apparatus includes:

1. units digit, tenths digit and hundredths digit clutchees, each having input and output shafts;
2. a motor continuously drivingly rotating said clutch input shafts;
3. links interconnecting the respective output shafts of said clutches to the units, tenths, and hundredths postage digit selector arms of the postage meter, whereby to reciprocate the various postage digit selector arms through their various digit positions so long as their respective clutches are engaged;
4. separate means coupled to each said clutch output shaft for providing digital readouts of the digit positions of the associated postage meter digit selector arms as they are moved through their various digit positions; and

5. separate comparator means for continuously comparing the digital readouts of the postage digit poistions of the various postage digit selector arms with the corresponding postage digit held in the output register, and, as comparisons are achieved, signalling the appropriate clutches to disengage their input shafts from their output shafts, whereby to stop the various postage digit selector arms at the postage digit position called for by the corresponding postage digits held in the output register.

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